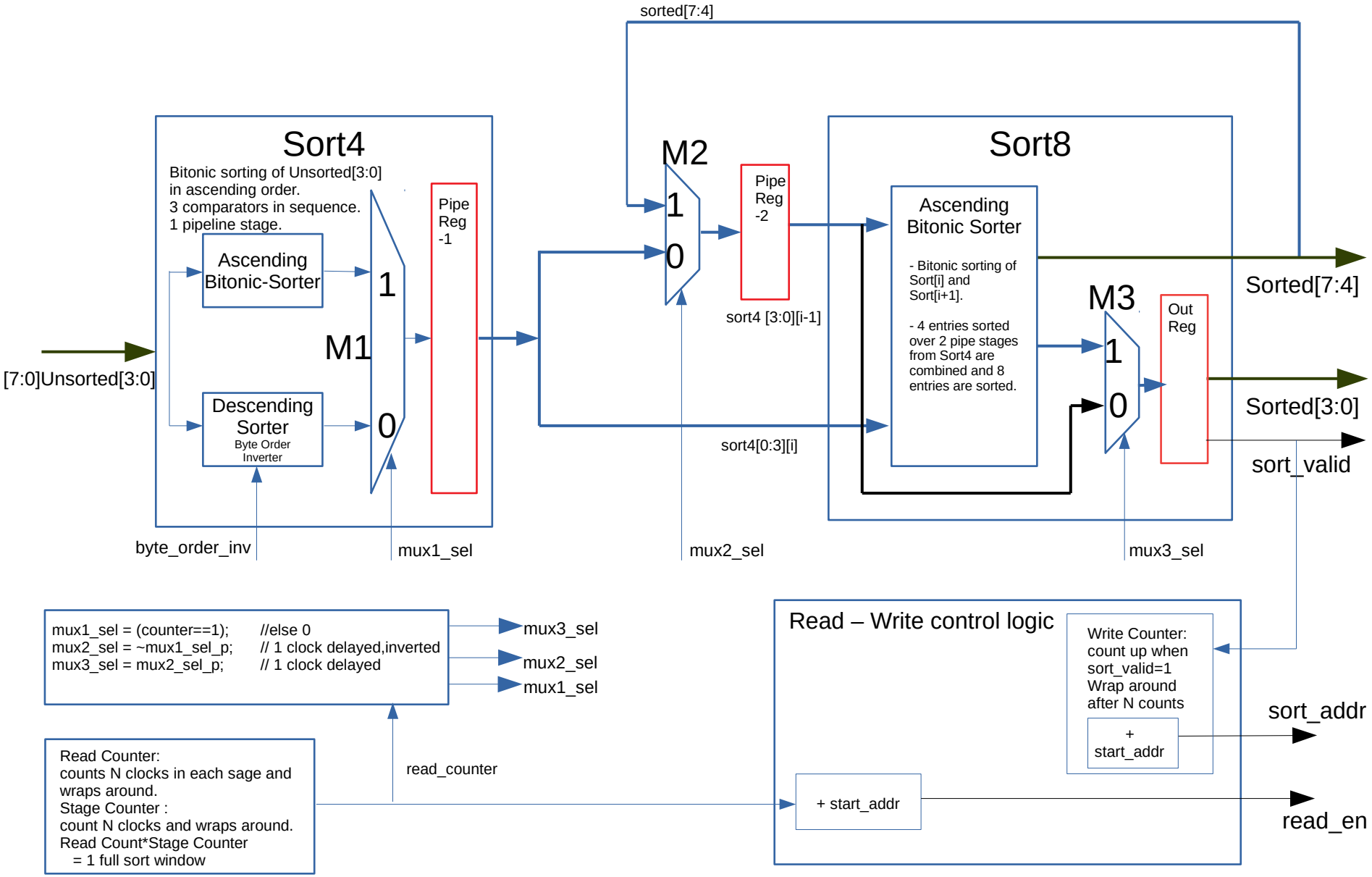
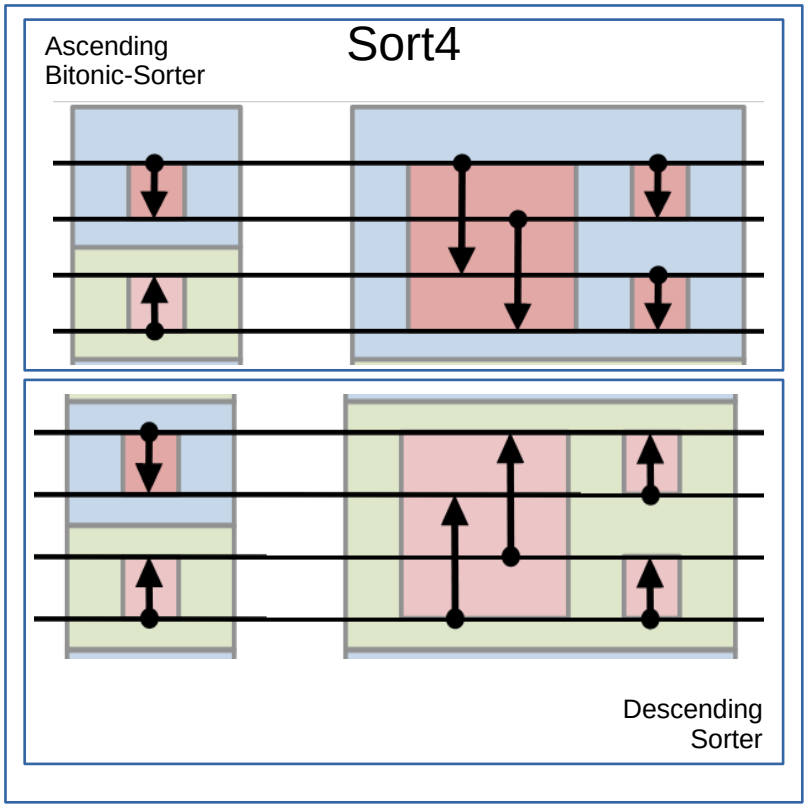
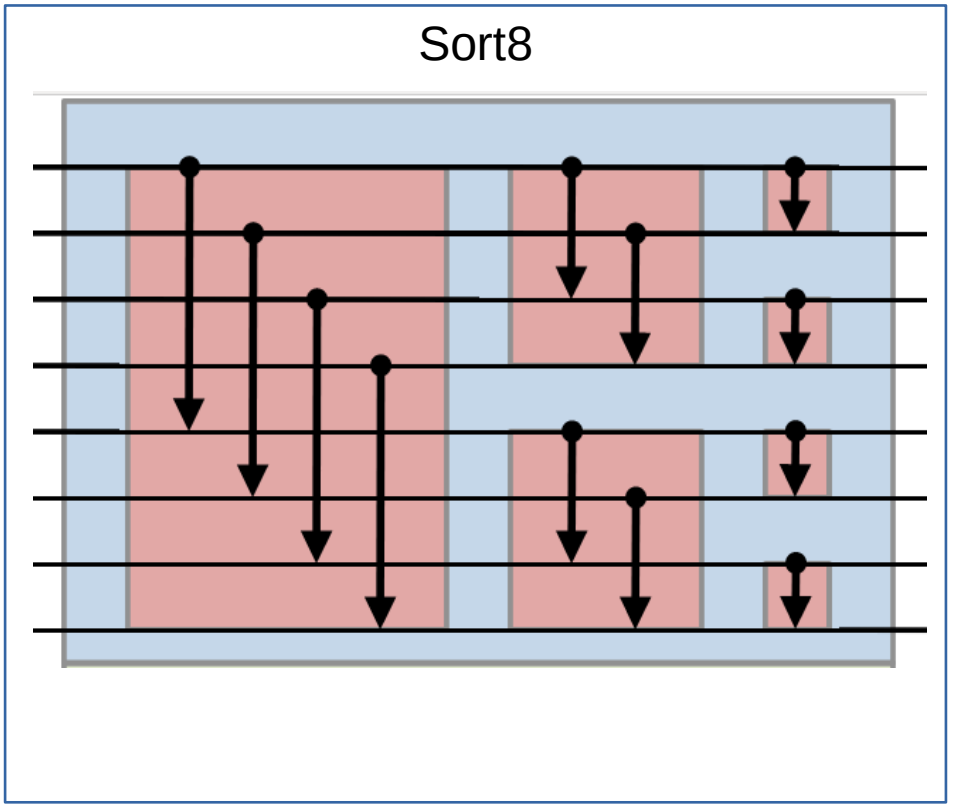

sorted[7:4]
Sort4
Bitonic sorting of Unsorted[3:0]
in ascending order.
3 comparators in sequence.
1 pipeline stage.
Ascending
Bitonic-Sorter
Descending
Sorter
Byte Order
Inverter
M1
1
0
Pipe
Reg
-1
[7:0]Unsorted[3:0]
byte_order_inv
mux1_sel
M2
1
0
Pipe
Reg
-2
sort4 [3:0][i-1]
sort4[0:3][i]
mux2_sel
Sort8
Ascending
Bitonic Sorter
- Bitonic sorting of Sort[i] and Sort[i+1].
- 4 entries sorted over 2 pipe stages from Sort4 are combined and 8 entries are sorted.
M3
1
0
Out
Reg
mux3_sel
Sorted[7:4]
Sorted[3:0]
sort_valid
mux1_sel = (counter==1); //else 0
mux2_sel = ~mux1_sel_p; // 1 clock delayed,inverted
mux3_sel = mux2_sel_p; // 1 clock delayed
mux3_sel
mux2_sel
mux1_sel
Read Counter:
counts N clocks in each sage and
wraps around.
Stage Counter :
count N clocks and wraps around.
Read Count*Stage Counter
= 1 full sort window
read_counter
Read – Write control logic
Write Counter:
count up when
sort_valid=1
Wrap around
after N counts
+
start_addr
sort_addr
+ start_addr
read_en

Bitonic sorting of Unsorted[3:0] in ascending order.
3 comparators in sequence.
1 pipeline stage.



- Bitonic sorting of Sort[i] and Sort[i+1].
- 4 entries sorted over 2 pipe stages from Sort4 are combined and 8 entries are sorted.



Reference:
https://upload.wikimedia.org/wikipedia/commons/b/bd/BitonicSort1.svg