# Synchronous FIFO

wr_clk

wr_rstb

rd_clk

rd_rstb

write_en

wr_data

## Write Control

Wr Ptr Incr

Full Logic

full

## SRAM

### Write
data_out
cs_b
data_in
addr
wr_en_b

### Read
data_in
cs_b
data_out
wr_en_b
addr

## Read Control & Pre-Fetch

cs_b
pre_read_data
pre_fetch

Rd Ptr Incr

Empty Logic

rd_data

read_en

empty

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## Read Control & Pre-Fetch

Rd Ptr Incr

Pre-Fetc Empty

Pre-Fetch Control FSM

pre-fetch read_en

pre-fetch-ready

read_data

rd_empty

Pre Fetch Read Buff (PRB)

rd_data

Pre-Fetch States:
Empty      : FIFO and PRB empty
    FIFO is empty and there is no read request, so no pre-fetch

PreFetch  : FIFO not empty, PRB empty
    FIFO is not empty, pre-fetch buffer contains first read data

Flow        : FIFO and PRB not empty
    Continuous read and pre-fetch state

Flush       : FIFO emtpy, PRB not empty
    FIFO is empty, PRB contains the last read data