# CHAPTER – 6
# INSTRUMENTATION AND CONTROL APPLICATIONS OF OTRA

The content and results of the following papers have been reported in this chapter.

1. Rajeshwari Pandey, Neeta Pandey, Sajal K. Paul, "**Electronically Tunable Transimpedance Instrumentation Amplifier based on OTRA**," Journal of Engineering, Volume 2013, Article ID 648540, 5 pages, doi.org/10.1155/2013/648540.

2. Rajeshwari Pandey, Saurabh Chitransi, Neeta Pandey, Chandra Shekhar. **"Single OTRA based PD Controllers,"** International Journal of Engineering Science and Technology, vol. 4 no.4, pp.1426-1437, 2012.

## 6.1 INTRODUCTION

Electronic instrumentation serves to amplify, shape and convert an analog signal into a form suitable for measurement, recording and/ or for further processing [94]. In instrumentation system quite often the analog signal is derived from a transducer which converts the physical quantity to be measured into an electrical signal either voltage or current [94]. In some cases this processed signal can be used as a part of automatic feedback control system to control the system parameters and thus improving system performance.

This chapter deals with the instrumentation and control applications of OTRA and describes the design of an OTRA based transimpedance instrumentation amplifier (TIA) followed by classical analog controllers namely proportional (P), proportional-derivative (PD), proportional integral (PI) and proportional derivative and integral (PID). A brief review of ava33ilable work on TIA and analog controllers has also been included.

## 6.2 INSTRUMENTATION AMPLIFIER

Instrumentation amplifier (IA) is an essential part of electronic instrumentation system which faithfully amplifies low level differential output of the transducer in the presence of high common mode noise. The gain of an amplifier is defined as ratio of output and input parameters. The choice between voltage and current as two possible input and output signals leads to four type of amplifiers namely the voltage controlled voltage source (VCVS) or voltage amplifier, the current controlled current source (CCCS) or current amplifier, the voltage controlled current source (VCCS) or transadmittance amplifier, the current controlled voltage source (CCVS) or transimpedance amplifier. VCVS and VCCS are suitable for amplification of signals from voltage-source transducers whereas for amplification of signals from current-source transducers CCCS and CCVS would be a better choice wherein the current input can be directly processed without conversion to voltage signal.

A review of earlier work suggests that a number of IAs have been proposed in literature [95] – [99], which are suitable for amplification of signals from voltage-source transducers and produce voltage output. The conventional operational amplifier based IA [95], [96] aren't capable of operating at higher frequencies because of slew rate and fixed

gain-bandwidth-product limitations [3]. The configurations proposed in [97] – [99] use the second-generation current conveyor (CCII). An op-amp based TIA is presented in [100] and is designed, for a specific low frequency application in a gamma-ray dosimeter. It consists of two current to voltage converters followed by an amplifier and uses three opamps and nine resistors. An extensive literature review reveals that no OTRA based IA has been proposed in open literature.

## 6.3 PROPOSED TRANSIMPEDANCE INSTRUMENTATION AMPLIFIER

OTRA is the most suitable analog building block for transimpedance type signal processing due to its very nature of current input and voltage output. The proposed OTRA based TIA circuit is shown in Fig. 6.1. It consists of two input buffers and a subtractor designed using three OTRAs and five resistors.

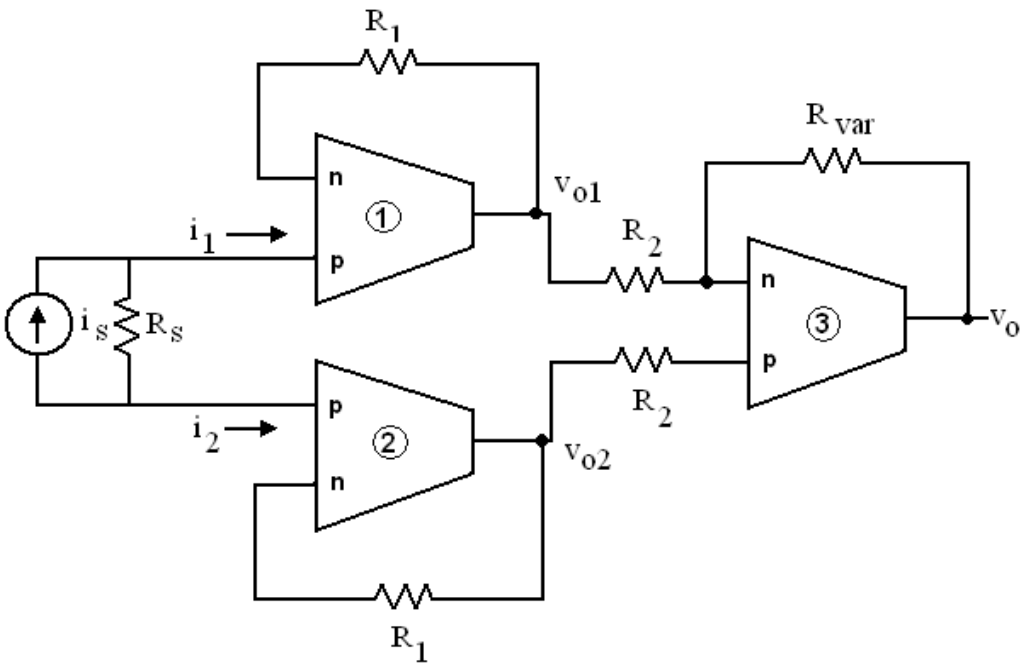



Fig. 6.1 The proposed TIA

The differential current signal from the current source/transducer is represented as $i_s$ and can be written as

$$i_s = ( i_1 - i_2) \tag{6.1}$$

The voltages $v_{o1}$ and $v_{o2}$ in Fig. 6.1 can be expressed as

$$v_{o1} = i_1 R_1 \tag{6.2}$$

$$v_{o2} = i_2 R_1 \tag{6.3}$$

The differential transimpedance gain ($A_d$) for the amplifier can be computed as

$$A_d = \frac{v_0}{i_1 - i_2} = \frac{-R_{var}\, R_1}{R_2} \tag{6.4}$$

It can be seen from (6.4) that $A_d$ can be adjusted by varying resistance $R_{var}$.

### 6.3.1 Nonideality Analysis

Taking into account the nonideality of OTRA as explained in section 2.8, the output voltages at different nodes of TIA can be expressed as

$$V_{o1}\big|_n = \frac{i_1 R_1}{1 + sC_{P1}R_1} \tag{6.5}$$

$$V_{o2}\big|_n = \frac{i_2 R_1}{1 + sC_{P2}R_1} \tag{6.6}$$

$$V_o\big|_n = \frac{-R_1 R_{var}}{R_2(1 + sC_{P3}R_{var})}\left(\frac{i_1}{(1 + sC_{P1}R_1)} - \frac{i_2}{(1 + sC_{P2}R_1)}\right) \tag{6.7}$$

where $C_{pi}$ is the parasitic capacitance of $i^{th}$ OTRA. Considering $C_{p1} = C_{p2} = C_{p3} = C_p$, the $A_d$ given by (6.4) modifies to

$$A_d\big|_n = \frac{v_0}{i_1 - i_2} = \frac{-R_{var}\, R_1}{R_2}\, \varepsilon_{uc}(s) \tag{6.8}$$

Where

$$\varepsilon_{uc}(s) = \frac{1}{(1 + sC_P R_1)(1 + sC_P R_{var})} \tag{6.9}$$

is uncompensated error function.

It is to be noticed from (6.8) that the gain $A_d$ can be adjusted by $R_{var}$ $R_1$/ $R_2$ and the bandwidth (BW) is controlled by $\varepsilon_{uc}(s)$ . Thus the gain of the amplifier remains same as ideal one and can be adjusted by varying $R_{var}$ without affecting the BW as $C_p$ is a small value. From (6.7) by using $i_1 = i_2 = i_c$, the transimpedance common mode gain ($A_c$) can be computed as

$$A_c = \frac{v_0}{i_c} = \frac{-R_1 R_{var}}{R_2(1+sC_{P3}R_{var})}\left(\frac{1}{(1+sC_{P1}R_1)} - \frac{1}{(1+sC_{P2}R_1)}\right) \tag{6.10}$$

For perfectly symmetric circuits having $C_{p1} = C_{p2} = C_{p3} = C_p$, the output common mode voltage will be zero. This property of common mode voltage cancellation is known as common-mode rejection. The extent to which a common mode signal is rejected by an IA is measured by the performance parameter common mode rejection ratio (CMRR) defined as the ratio of differential gain to common mode gain. For the proposed TIA CMRR can be computed as

$$CMRR = \frac{A_d}{A_c} = \frac{2+s(C_{p1}+C_{p2})R_1}{s(C_{P2}-C_{p1})R_1} \tag{6.11}$$

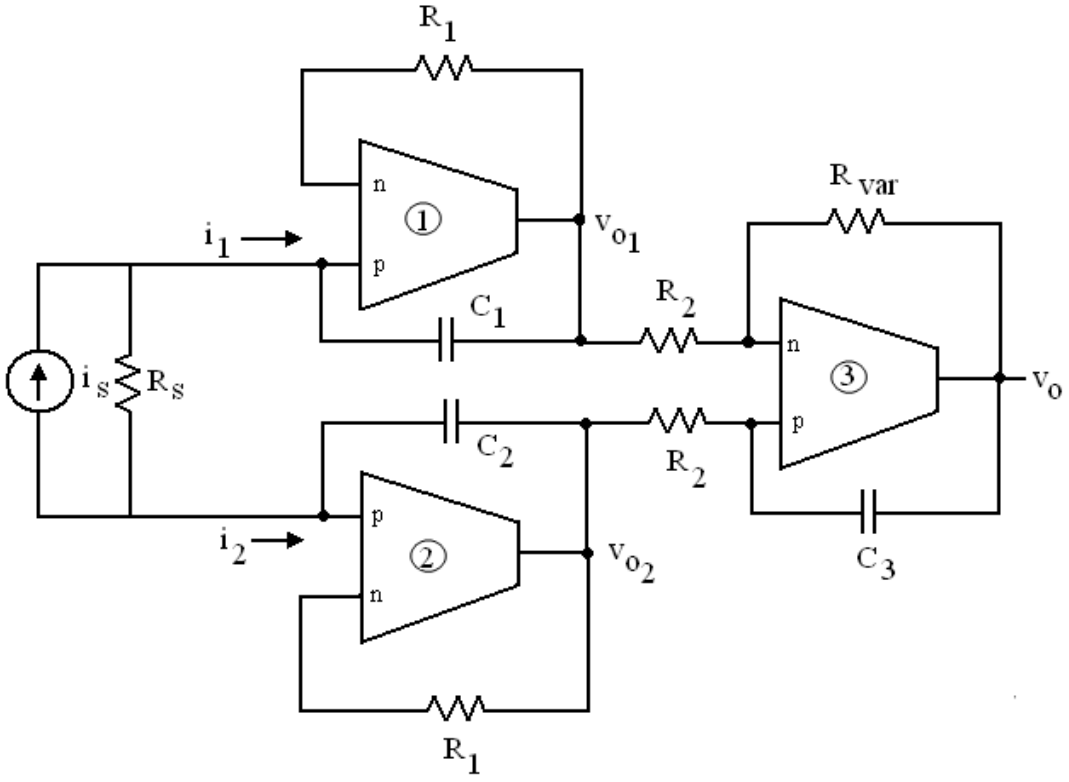



Fig. 6.2 TIA with high frequency compensation.

For high-frequency applications, compensation methods must be employed to account for the error $\varepsilon_{uc}(s)$ introduced in (6.4) and given by (6.9). High frequency passive compensated topology of the TIA is shown in Fig. 6.2. Routine analysis of Fig. 6.2 results in

$$A_d = \frac{v_0}{i_1 - i_2} = \frac{-R_{var}\, R_1}{R_2}\, \varepsilon_c(s) \tag{6.12}$$

where $\varepsilon_c(s)$ is compensated error function and is given by

$$\varepsilon_c(s) = \frac{1}{(1+R_1 s(C_P - C_1))(1+R_{var} s(C_P - C_3))} \tag{6.13}$$

By taking $C_1 = C_2 = C_3 = C_p$, $\varepsilon_c(s)$ reduces to 1, which makes (6.12) same as (6.4). The effect of single pole model of $R_m$ can thus be eliminated.

## 6.3.2 MOS – C Realization

Using the method of active implementation of passive resistors as explained in section 2.8, the proposed configuration is made fully integrated. The MOS based implementation of the proposed TIA is shown in Fig. 6.3 wherein $R_1$, $R_2$ and $R_{var}$ are

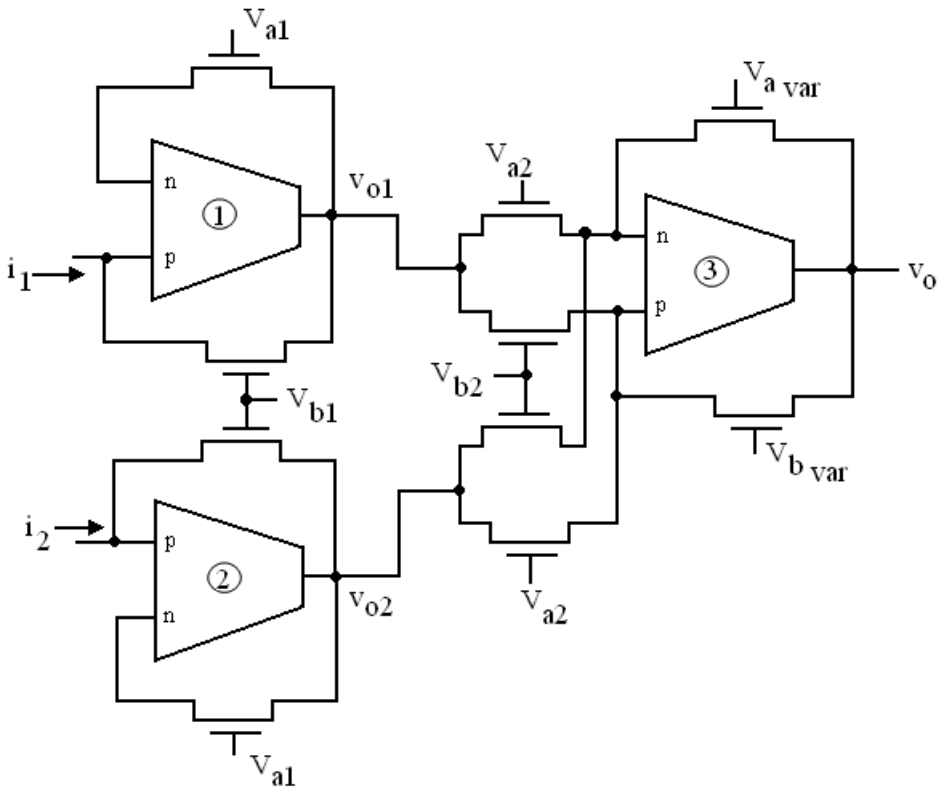
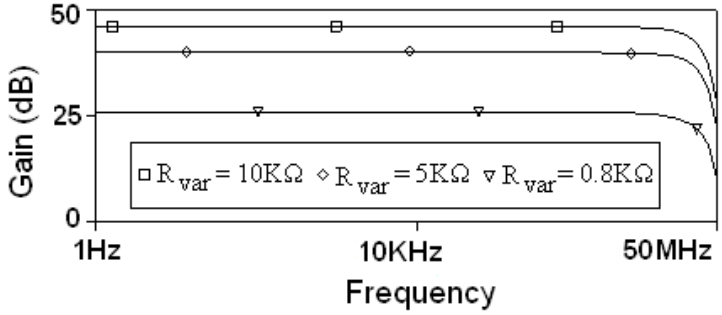



Fig. 6.3 MOS based implementation of the proposed TIA.

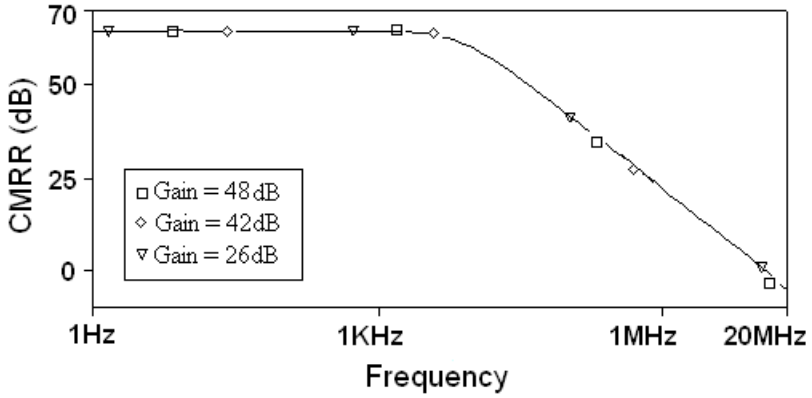
implemented using MOS transistors operating in linear region. The resistance value may be adjusted by appropriate choice of gate voltages. This not only makes the circuit suitable for integration but also makes the TIA gain electronically tunable.

### 6.3.3 Simulation and Experimental Results

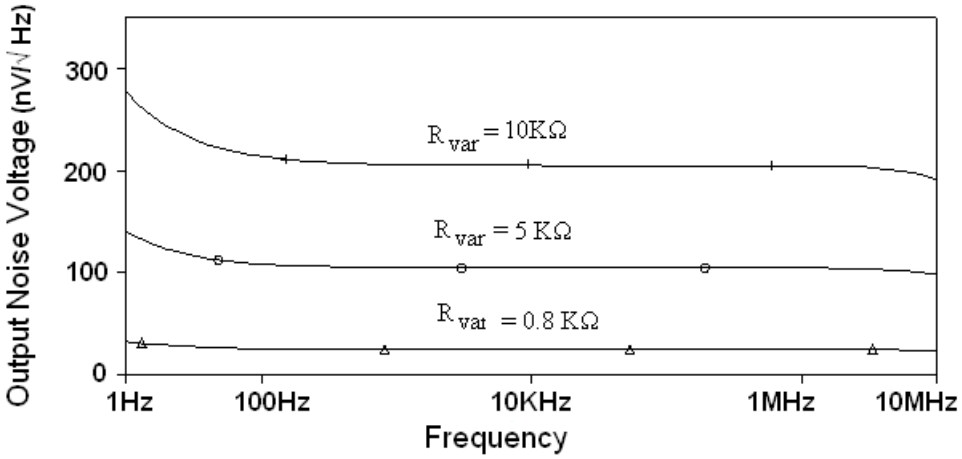
The performance of the proposed TIA is verified through SPICE simulation using CMOS implementation of the OTRA discussed in section 2.5. The frequency response of the proposed amplifier is shown in Fig. 6.4 (a). The input differential current was chosen as 5 mA. The component values are taken as $R_1 = 5$ KΩ and $R_2 = 1$ KΩ. The $R_{var}$ is assigned values as 0.8 KΩ, 5 KΩ and 10 KΩ for which the differential gains obtained were 26 dB, 42 dB and 48 dB respectively. The 3 dB frequency of the amplifier is 10 MHz for all the three cases confirming that the bandwidth of the amplifier is independent of gain. Total power consumption of the proposed TIA is simulated to be 4.93 mW. Figure 6.4 (b) shows the CMRR responses of the circuit for differential gains of 26 dB, 42 dB, and 48 dB. It is observed that the proposed TIA exhibits a CMRR magnitude of 64.5 dB and bandwidth of 10 KHz, which is independent of gain. The simulation results of the noise performance analysis of the proposed TIA for different values of $R_{var}$ are depicted in Fig. 6.4 (c). It may be noticed from the Fig. 6.4 (c) that the noise level being low would result in high signal-to-noise ratio of the TIA. A hardware prototype of the proposed TIA is also designed to test its functionality experimentally. The OTRA is realized using commercial IC AD 844AN as explained in section 2.4.1. Supply voltages used are ± 5 V. The experimental and simulated frequency response for the TIA, for $R_1$ = 5 KΩ, $R_2 = 1$ KΩ and $R_{var}$ = 10 KΩ, are shown in Fig. 6.5(a) and CMRR response is shown in Fig. 6.5 (b). The slight variations in experimental and simulated results may be attributed to component tolerances. Observed outputs showing the performance of the proposed TIA at 70 KHz and 2 MHz for $R_1 = 5$ KΩ, $R_2 = 1$ KΩ and $R_{var}$ = 10 KΩ are given in Fig. 6.5(c) and (d) respectively.




(a)




(b)




(c)

Fig. 6.4 Simulation results of the proposed TIA. (a) Frequency response. (b) CMRR response. (c) Output noise spectral density.

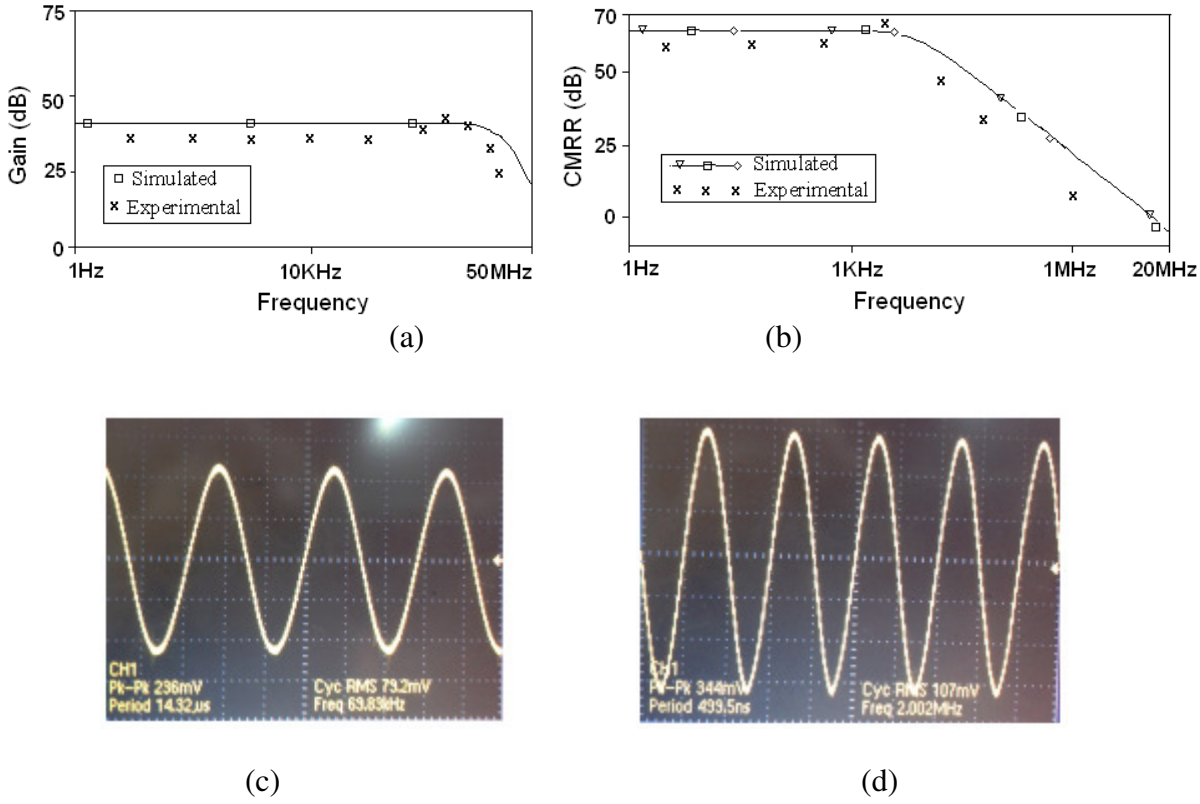



Fig. 6.5 Experimental results of the proposed TIA.(a) Frequency Response for $R_{var}$=10 Ω. (b) CMRR Response. (c) Output for 70 KHz input. (d) Output for 2 MHz input.

## 6.4 CONTROLLERS

A controller monitors and modifies the operational conditions of a given dynamical system. These operational conditions are referred to as measured output variables and can be modified by adjusting certain input variables. The controller calculates the difference between a measured output variable and a desired set point as an error value and attempts to minimize the error by adjusting the process control inputs. In general, controllers can be classified as (i) conventional (ii) non conventional controllers. For conventional controllers apriori knowledge of the mathematical model of the process to be controlled is required in order to design a controller whereas for unconventional controllers this information is generally not required. Proportional (P), proportional-derivative (PD), proportional-integrator (PI) and proportional derivative and integral (PID) controllers, are few typical examples of conventional controllers and neuro, fuzzy controllers are representatives of the unconventional class. The controllers based on proportional-

integral-derivative (PID) algorithm are most popularly used in the process industries. These are used to control various processes satisfactorily with proper tuning of controller parameters. In a PID controller as shown in Fig. 6.6 the proportional, integral and the derivative of the error signal E(s) are summed up to calculate the output actuating signal U(s) of the controller.

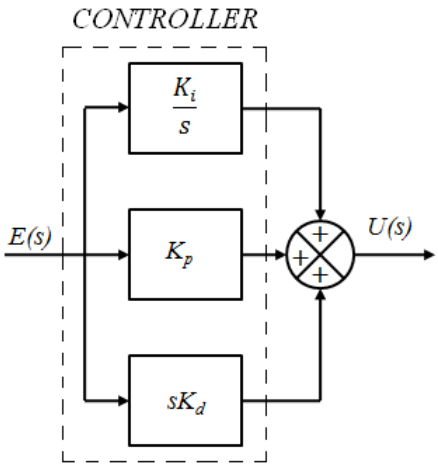



Fig. 6.6 PID controller.

Thus the transfer function $G_{PID}(s)$ of the PID controller can be written as

$$G_{PID}(s) = \frac{U(s)}{E(s)} = K_p + \frac{K_i}{s} + K_d\, s \tag{6.14}$$

where $K_p$, $K_i$ and $K_d$ are the proportional, integral and derivative constants, respectively. A second order unity feedback control system using PID controller is shown in Fig. 6.7. If in Fig. 6.6 only proportional action is considered, then it becomes a proportional controller where actuating signal depends on the instantaneous value of the control error.

The transfer function of proportional controller can be represented as

$$G_P(s) = \frac{U(s)}{E(s)} = K_p \tag{6.15}$$

The closed loop transfer function of the control system with P controller can be expressed as

$$T_P(s) = \frac{K_p\omega_n^2}{s^2+2\xi\omega_n s+K_p\omega_n^2} \tag{6.16}$$

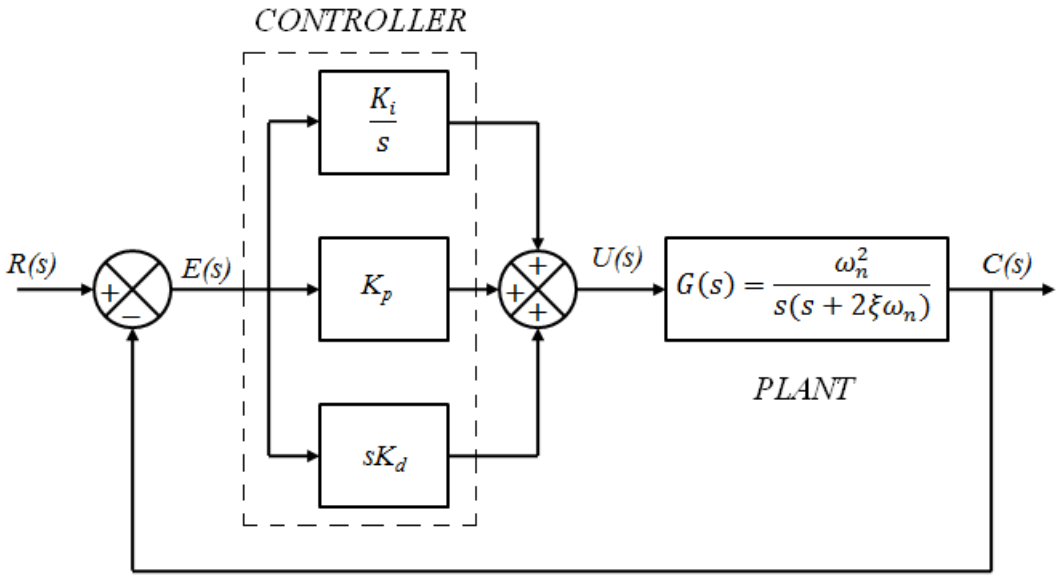



Fig. 6.7 Block diagram of a control system with PID controller.

The standard characteristic polynomial, D(s), of second order system [101] is given by

$$D(s) = s^2 + 2\xi\omega_n s + \omega_n^2 \tag{6.17}$$

where $\omega_n$ is natural frequency of oscillations and $\xi$ represents the damping factor. On comparing the denominator of (6.16) with (6.17) it is observed that by using P controller in feedback, natural frequency increases and damping ratio decreases by a factor $\sqrt{K_p}$, which results in reduction of peak time, rise time and steady state error. However, the maximum peak overshoot increases for P controller.

From the controller block of Fig. 6.6 if only proportional and integral actions are considered into account the resulting controller is known as PI controller. The transfer function $G_{PI}(s)$, of the PI controller so obtained can be given by

$$G_{PI}(s) = K_p + \frac{K_i}{s} \tag{6.18}$$

and the transfer function of the closed loop system can be computed as

$$T_{PI}(s) = \frac{(K_i + sK_p)\omega_n^2}{s^3 + 2\xi\omega_n s^2 + (K_i + sK_p)\omega_n^2} \tag{6.19}$$

PI controller increases the order of the system. It improves steady state response by reducing the steady state error however it has a negative effect on speed of the response and overall stability of the system.

A PD controller can be derived from the generalized controller block of Fig. 6.6 if proportional and derivative actions only are taken into consideration thus the actuating signal U(s) is sum of proportional to the error signal E(s) and its rate of change. Transfer function of a PD Controller $G_{PD}(s)$, can be expressed as

$$G_{PD}(s) = K_p + K_d\, s \tag{6.20}$$

The transfer function of second order unity feedback control system using PD controller can be computed to be

$$T_{PD}(s) = \frac{(K_p+sK_d)\omega_n^2}{s^2+(2\xi\omega_n+K_d\omega_n^2)s+K_p\omega_n^2} \tag{6.21}$$

Considering $K_p = 1$, and comparing denominator of (6.21) with (6.17), it can be noticed that natural frequency, does not change while damping ratio increases. This results in reduction of the peak overshoot, rise time, peak time and settling time; however it does not affect the steady state error.

From the discussion so far it can be concluded that in a given system the proportional action improves the rise time of the system, the integral action improves the steady-state error whereas the derivative action improves the degree of stability. So, none alone is capable of achieving the complete improvement in system performance [101]. This leads to the motivation of using a PID controller so that the system performance can be optimized.

Classical analog controllers [102] − [104] are generally designed using operational amplifiers. However the op-amp based circuits, being voltage mode, have their own limitations of constant gain bandwidth product and low slew rate. It is well known that inherent wide bandwidth which is almost independent of closed loop gain, greater linearity, and large dynamic range; are the key performance features of current mode technique [3]. Therefore the current mode building blocks would be good alternative of op-amp for designing the analog controllers. Literature survey on PID controllers reveals that number of current mode building blocks such as OTA [105], CDBA [106] and

CCII [107] – [109] have been used to implement analog controllers. However no OTRA based controllers are available in open literature.

## 6.5 PROPOSED CONTROLLER CIRCUITS

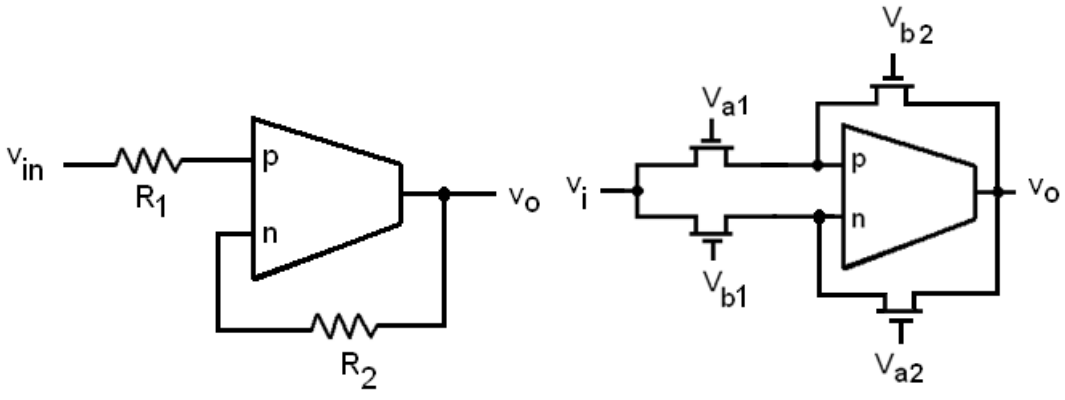
In this section, OTRA based realization of the classical controllers discussed in section 6.4, namely P, PI, PD and PID has been proposed. The proposed circuits can be made fully integrated by implementing the resistors using MOS transistors operating in non-saturation region. This also facilitates electronic tuning of the controller parameters. Finally influence of controllers on performance of a second order system is also evaluated.

### 6.5.1 P Controller

The proposed P controller is shown in the Fig. 6.8(a). The circuit is basically a voltage controlled voltage source [36] and its transfer function can be expressed as

$$G_P(s) = \frac{V_o(s)}{V_i(s)} = \frac{R_2}{R_1} \tag{6.22}$$

Equation (6.22) represents the controller parameter $K_p$ which can be tuned by changing either $R_1$ or $R_2$, or both. Electronic tuning of $K_p$ can be achieved by implementing the resistors $R_1$ and $R_2$ using MOS transistors operating in non-saturation region, and then controlling their gate bias as shown in Fig. 6.8(b).



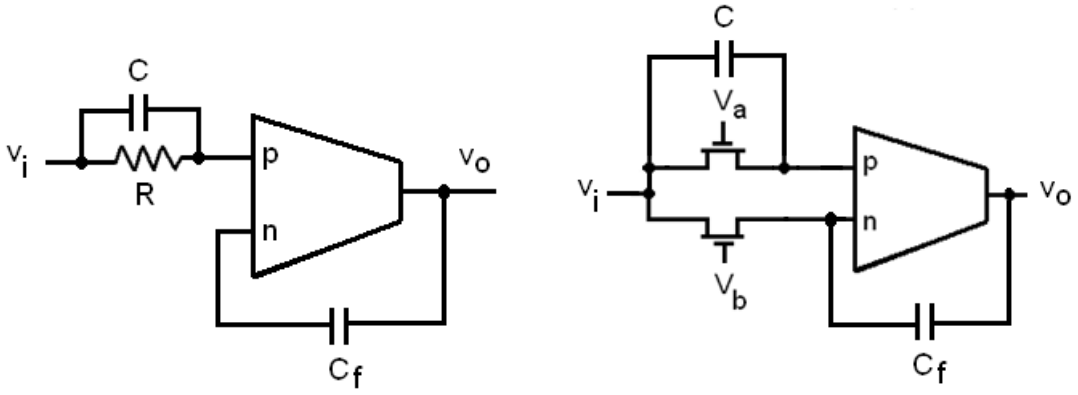

(a) (b)

Fig. 6.8 (a) OTRA based P Controller. (b) MOS– C implemented P Controller.

### 6.5.2 PI Controller

The OTRA based proposed PI controller is shown in Fig. 6.9(a) and its MOS-C implementation is shown in Fig. 6.9(b). Using routine analysis of this controller the voltage transfer function can be computed as

$$G_{PI}(s) = \frac{V_o}{V_i} = \frac{C}{C_f} + \frac{1}{sC_fR} \tag{6.23}$$




(a) (b)

Fig. 6.9 (a) OTRA based PI Controller. (b) MOS− C implemented PI Controller.

From (6.23) the controller parameters can be expressed as

$$K_p = \frac{C}{C_f},\ K_i = \frac{1}{C_fR} \tag{6.24}$$

It is clear from (6.24) that $K_p$ value can be adjusted independent of $K_i$ by varying C, and $K_i$ can be independently controlled by varying R.

### 6.5.3 PD Controller

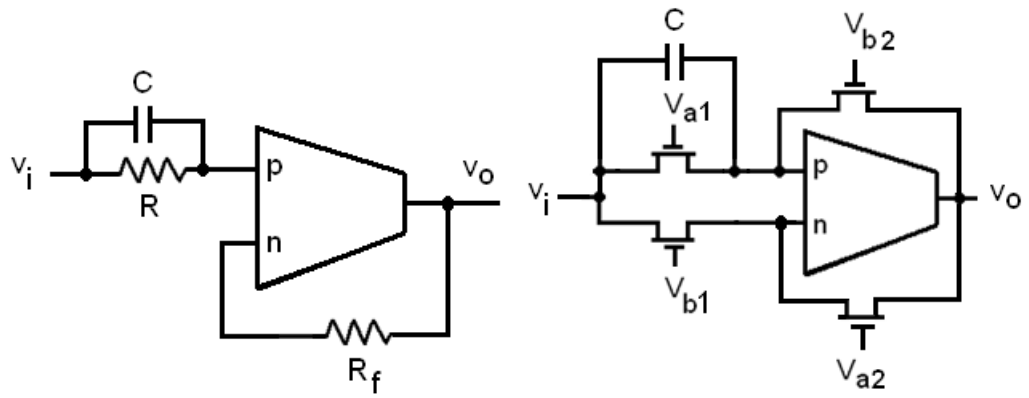
Figure 6.10 shows the proposed PD controller circuit and the transfer function of this controller can be obtained as

$$G_{PD}(s) = \frac{V_o}{V_i} = \frac{R_f}{R} + sCR_f \tag{6.25}$$

Equation (6.25) results in

$$K_p = \frac{R_f}{R},\ K_d = CR_f \tag{6.26}$$

From (6.26) it is clear that by varying R, $K_p$ value can be adjusted independent of $K_d$ and by simultaneous variation of $R_f$ and R, $K_d$ can be independently controlled. In MOS–C implemented structure, as shown in Fig. 6.10 (b), the controller parameters can be electronically tuned through appropriate choice of gate voltages of the transistors used for implementing the resistive elements.




(a) (b)

Fig. 6.10 (a) Proposed PD Controller. (b) MOS− C implemented PD Controller.

## 6.5.4 PID Controller

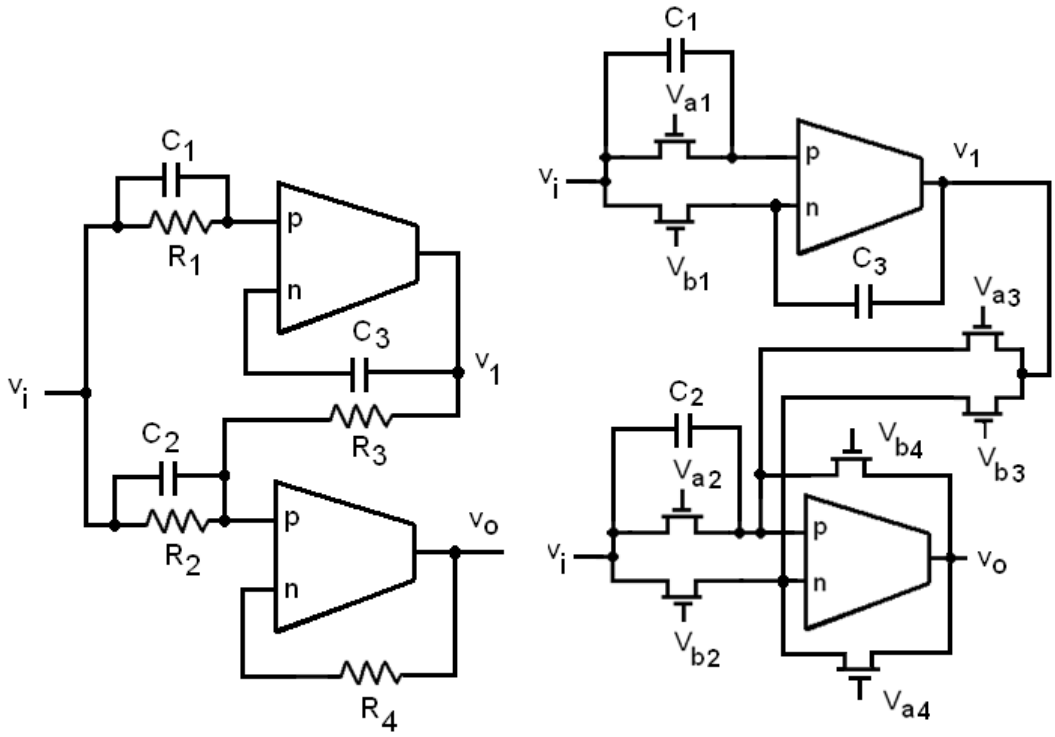
The proposed PID-Controller can be derived by combining the proposed PI and PD controllers and is shown in Fig. 6.11. The routine analysis of this circuit gives the transfer function of the controller as

$$G_{PID}(s) = \frac{V_o}{V_i} = \left(\frac{R_4}{R_2} + \frac{R_4}{R_3}\frac{C_1}{C_3}\right) + \frac{R_4}{sC_3R_1R_3} + sC_2R_4 \qquad (6.27)$$

From (6.27) the controller parameters can be identified as

$$K_p = \frac{R_4C_1}{R_3C_3} + \frac{R_4}{R_2}\ , K_i = \frac{R_4}{R_1R_3C_3} \quad \text{and} \quad K_d = C_2R_4 \qquad (6.28)$$

It is clear from (6.28) that $K_p$ value can be adjusted independently by varying $R_2$, independent tuning of $K_i$ is possible through $R_1$ variation whereas $K_d$ can be controlled independently by simultaneous variation of $R_2$ , $R_3$ and $R_4$.




(a) (b)

Fig. 6.11 (a) OTRA based PID Controller. (b) MOS− C implemented PID Controller.

## 6.6 NONIDEALITY ANALYSIS

The behaviour of the OTRA based circuits may deviate from the ideal one in practice. This section examines the effect of nonideality of OTRA as discussed in section 2.3, on proposed controllers and suggests the compensation so as to make them suitable for high frequency applications.

### 6.6.1 Nonideality analysis of P controller

Considering the effect of nonideality of OTRA, the controller transfer function given by (6.22) modifies to

$$G_P\big|_n(s) = \frac{R_2}{R_1} \quad \varepsilon_{uc}(s) \tag{6.29}$$

where $\varepsilon_{uc}(s) = \frac{1}{(1+sC_pR_2)}$ is uncompensated error function.

The error $\varepsilon_{uc}(s)$, so introduced must be accounted for; therefore compensation must be employed for high-frequency applications. Considering the circuit of Fig. 6.12 the transfer function can be written as

$$G_P\big|_{n\_c}(s) = \frac{R_2}{R_1}\,\varepsilon_c(s) \tag{6.30}$$

where $\varepsilon_c(s) = \frac{1}{1+R_2(sC_p-Y)}$ is compensated error function.

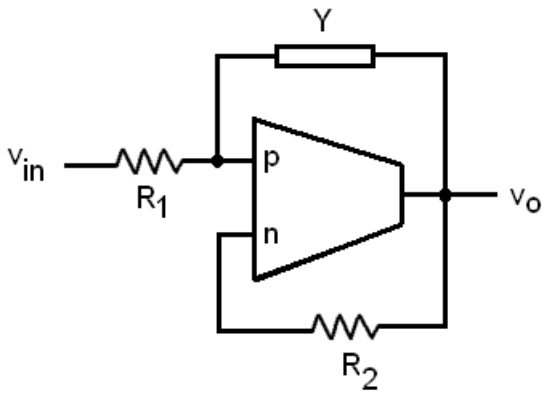



Fig. 6.12 Compensated P controller.

By choosing Y = $sC_p$, $\varepsilon_c(s)$ reduces to its ideal value of unity thereby making (6.29) same as (6.22). Thus, passive compensation of the P controller can be achieved by using a single capacitor connected between the output and the non-inverting terminal of the OTRA.

## 6.6.2 Nonideality Analysis of PI Controller

The PI controller transfer function in presence of nonidealities given by (6.23) modifies to

$$G_{PI}\big|_n(s) = \left(\frac{1}{s(C_f+C_p)R} + \frac{C}{(C_f+C_p)}\right) \tag{6.31}$$

By pre-adjusting the value of capacitors $C_f$, the effect of $C_p$ can be eliminated and self compensation can be achieved.

## 6.6.3 Nonideality Analysis of PD Controller

Due to the nonideality effect of OTRA the transfer function of PD controller changes and

can be expressed as

$$G_{PD}\big|_{n}(s) = \frac{R_f}{R(1+sC_pR_f)} + \frac{sCR_f}{1+sC_pR_f} \tag{6.32}$$

For high-frequency applications, compensation methods must be employed to account for the error introduced in (6.24). Considering the circuit shown in Fig. 6.13, (6.32) modifies to

$$G_{PD}\big|_{n\_c}(s) = \frac{R_f}{R(1+R_f(sC_p-sY))} + \frac{sCR_f}{1+R_f(sC_p-sY)} \tag{6.33}$$

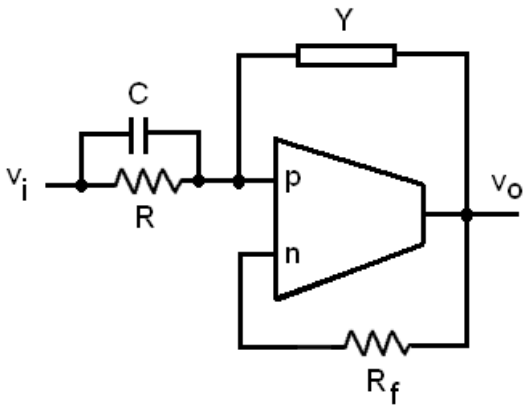



Fig. 6.13 Compensated PD Controller.

By taking Y = $sC_p$, (6.33) reduces to (6.24). So the error can be eliminated by connecting a single capacitor between the non inverting terminal and the output as shown in Fig. 6.13, and the passive compensation can be achieved.

## 6.6.4 Nonideality Analysis of PID Controller

The modified transfer function of the PID controller, due to nonideality of OTRA can be computed as

$$G_{PID}\big|_{n}(s) = \left(\frac{R_4C_1}{R_3\,(C_3+C_{p1})(1+sC_{p2}R_4)} + \frac{R_4}{R_2(1+sC_{p2}R_4)}\right) + \left(\frac{R_4}{R_1R_3\,s(C_3+C_{p1})(1+sC_{p2}R_4)}\right) + \left(\frac{sC_2R_4}{(1+sC_{p2}R_4)}\right) \tag{6.34}$$

Passive compensation method is employed to account for the error introduced in (6.27). The effect of $C_{p1}$ can be eliminated by pre-adjusting the value of capacitors $C_3$ and thus achieving self compensation. The $sC_{p2}$ term appearing in parallel to $R_4$ will result in introduction of a parasitic pole having radian frequency as $\omega = 1/R_4C_{p2}$. The effect of $C_{p2}$ can be eliminated by connecting a single admittance Y between the noninverting and the output terminals as shown in Fig. 6.14.

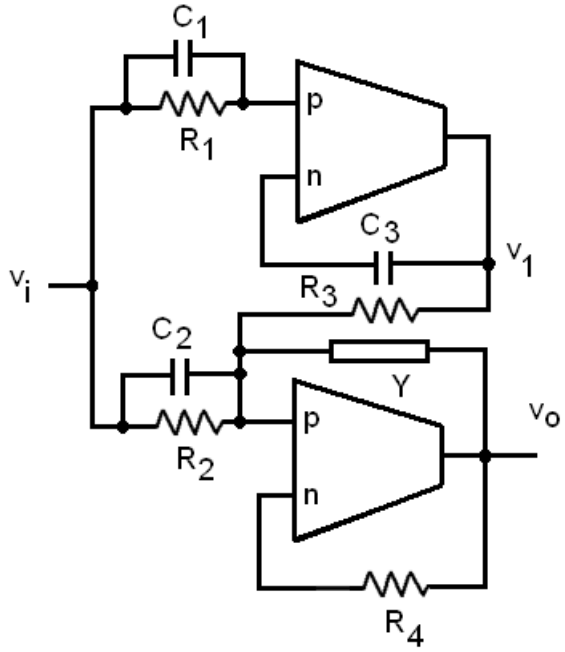



Fig. 6.14 Compensated PID Controller.

Considering the circuit of Fig. 6.14., (6.34) modifies to

$$G_{PID}\big|_{n\_c}(s) = \left(\frac{R_4C_1}{R_3\,C_3\left(1+s(C_{p2}-Y)R_4\right)} + \frac{R_4}{R_2\left(1+s(C_{p2}-Y)R_4\right)}\right)$$

$$+\left(\frac{R_4}{R_1R_3\,sC_3(1+s(C_{p2}-Y)R_4)}\right) + \left(\frac{sC_2R_4}{R_2(1+s(C_{p2}-Y)R_4)}\right) \qquad (6.35)$$

By taking $Y = sC_{p2}$, (6.35) reduces to (6.27) thus eliminating the effect of $C_{p2}$ and hence achieving the passive compensation.

## 6.7 SIMULATION RESULTS

The functionality of all the proposed controller circuits is verified through SPICE simulations using circuit schematic of Fig. 2.9 for OTRA realization.

### 6.7.1 P Controller

For the simulation of proposed P controller (Fig. 6.8), the passive component values are chosen as $R_1$ = 10 KΩ and $R_2$ = 20 KΩ. An aspect ratio of W/L = 0.18µm/0.54µm is used for both the transistors used for implementing passive resistor $R_1$ whereas for those used to implement $R_2$ the aspect ratio is chosen to be 0.18µm/1.08µm. Gate voltages are set as $V_{a1} = V_{a2}$ = 1.2 V, $V_{b1}$ = 0.59 V and $V_{b2}$ = 0.64 V which result in resistance values as $R_1 \approx$ 10 KΩ and $R_2 \approx$ 20 KΩ. These passive component values result in controller parameter value $K_P$ = 2. For time domain analysis, a 3 mV, 2.5 MHz sinusoidal input voltage is applied. The ideal and simulated frequency responses of the P controller are depicted in Fig. 6.15 and the time domain responses are shown in Fig. 6.16. Figure 6.17 shows the transfer curve of P controller for different values of $K_P$ for which $R_1$ is kept constant at 10 KΩ and $R_2$ is varied. In MOS implemented circuit value of $R_2$ is changed by modifying gate voltage $V_{b2}$ while keeping $V_{a2}$ constant. The gate voltage $V_{a2}$ is assigned a value of 1.2 V and $V_{b2}$ is placed at 0.64 V, 0.89 V, and 0.99 V resulting in $R_2$ values of 20 KΩ, 30 KΩ and 40 KΩ respectively. This shows the electronic tunability feature of the proposed controller.

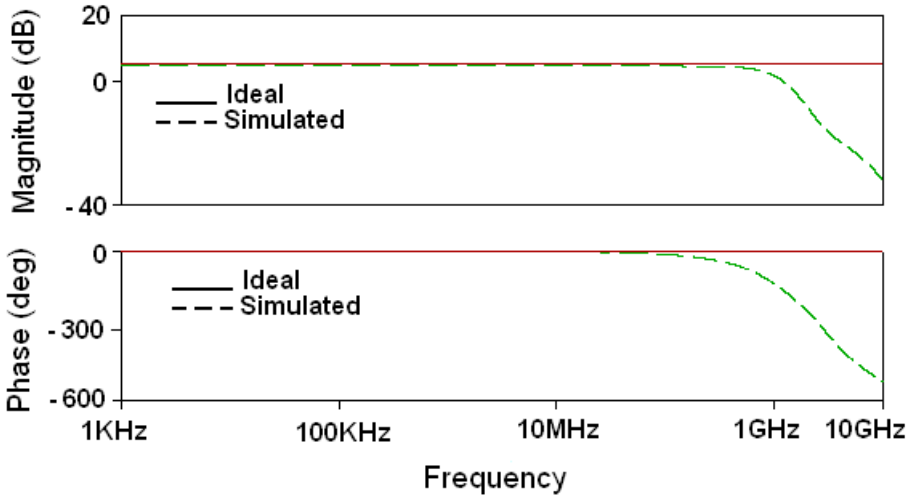



Fig. 6.15 Frequency response of P controller.

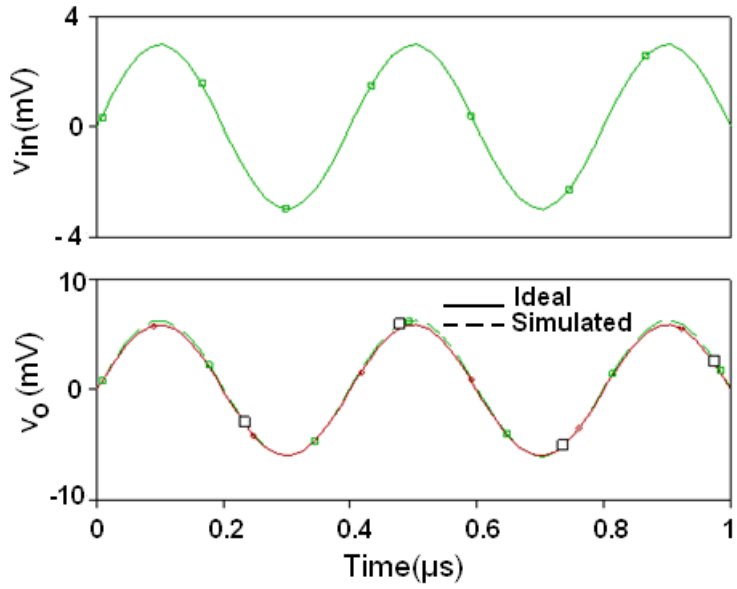



Fig. 6.16 Transient response of the P controller.

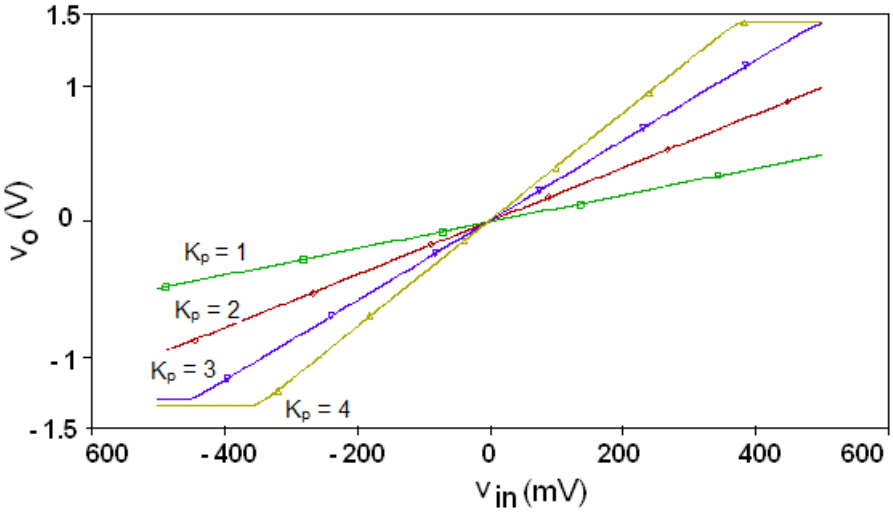



Fig. 6.17 Transfer curve of P controller.

## 6.7.2 PI Controller

For the simulation of proposed PI controller (Fig. 6.9) the passive component values are chosen as $R_1$ = 50 KΩ, $C_1$ = 4 pF and $C_f$ = 2 pF. An aspect ratio of W/L = 0.18µm/1.08µm is used and gate voltages are set as $V_{a1}$ = 1 V and $V_{b1}$ = 0.5 V for the transistors used to implement resistor $R_1$ which result in resistance value as $R_1 \approx$ 50 KΩ. Using the passive component values the controller parameters are computed to as $K_p$ = 2 and $K_i = 10^7\ s^{-1}$. For time domain analysis, a 3 mV step input voltage with

20 ns rise time is applied. The ideal and simulated frequency responses of the PI controller are depicted in Fig. 6.18 and the time domain responses for the controller are shown in Fig. 6.19.

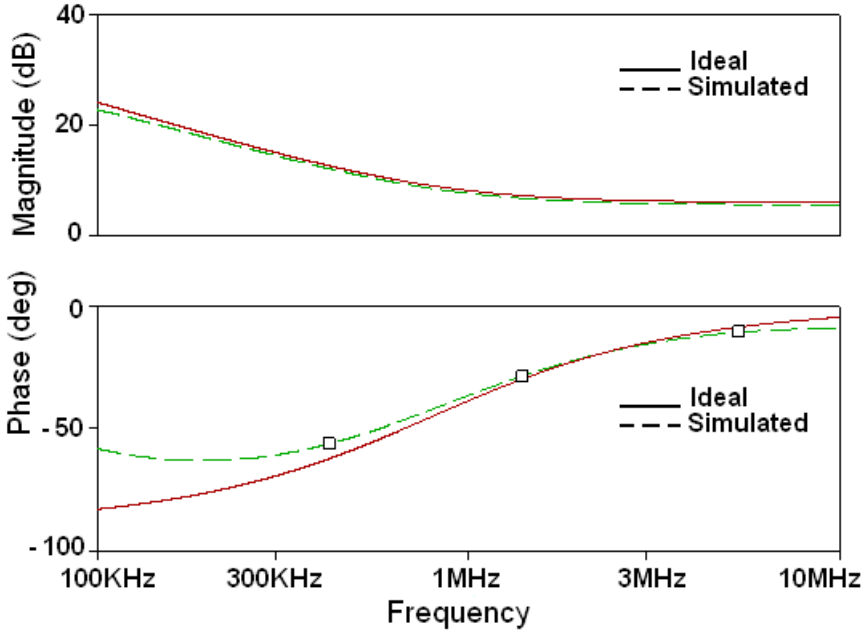



Fig. 6.18 Frequency response of the PI Controller.

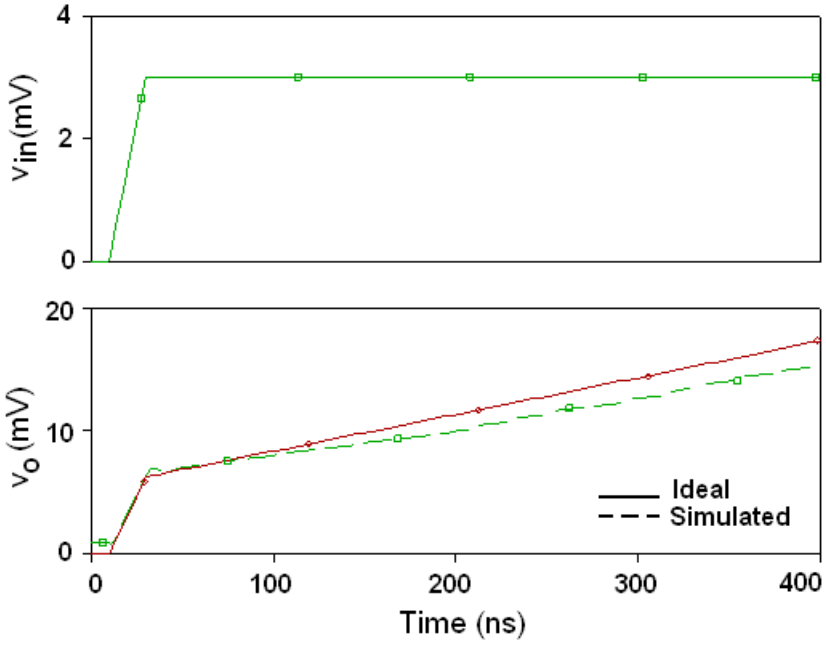



Fig. 6.19 Transient response of the PI Controller.

### 6.7.3 PD Controller

The passive component values for proposed PD controller are chosen as R = 10 KΩ, $R_f$ = 20 KΩ and C = 20 pF. For MOS-C implemented controller an aspect ratio of W/L = 0.18µm/0.54µm is chosen for the transistors used for implementing R whereas W/L = 0.18µm/1.08µm is used for the transistors which realize $R_f$. Gate voltages are set as $V_{a1} = V_{a2} = 1.2$ V, $V_{b1} = 0.59$ V and $V_{b2} = 0.64$ V which result in resistance values as R ≈ 10 KΩ and $R_f$ ≈ 20 KΩ.The controller parameters are computed to be $K_p = 2$ and $K_d = 0.4$ µs. For transient analysis of PD controller, a 3 mV peak triangular input voltage is applied. The ideal and simulated frequency responses of the PD controller are shown in Fig. 6.20 whereas in Fig. 6.21 the transient responses are shown. Both ideal and simulated results are found in close agreement.

### 6.7.4 PID Controller

For the proposed PID controller shown in Fig. 6.11, the values of passive element are chosen as $R_1 = R_2 = R_3 = R_4 = 50$ KΩ, $C_1 = C_3 = 10$ pF and $C_2 = 0.05$ pF. For time domain analysis, a 3 mV step signal with 10 ns rise time is applied. For MOS-C implemented PID controller shown in Fig. 6.14(b) an equal aspect ratio of W/L= 0.18µm/1.8µm, is chosen for all the transistors used for implementing the resistances.

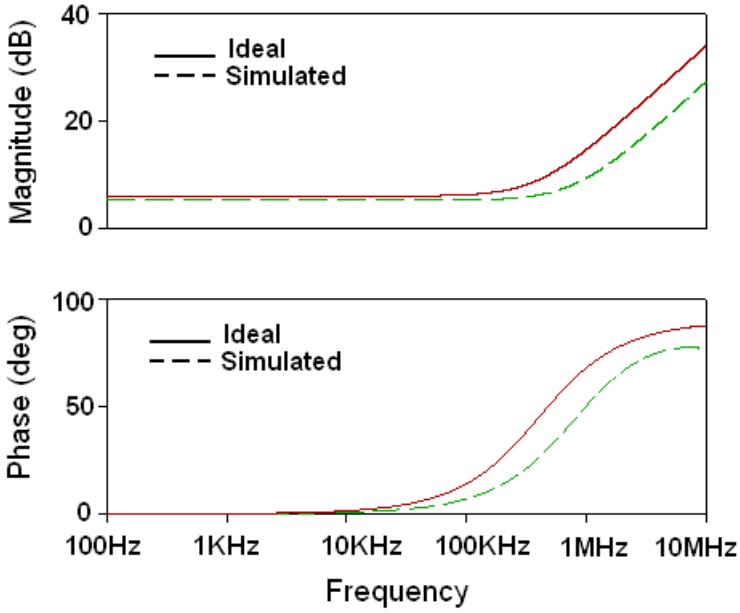



Fig. 6.20 Frequency response of the PD Controller.

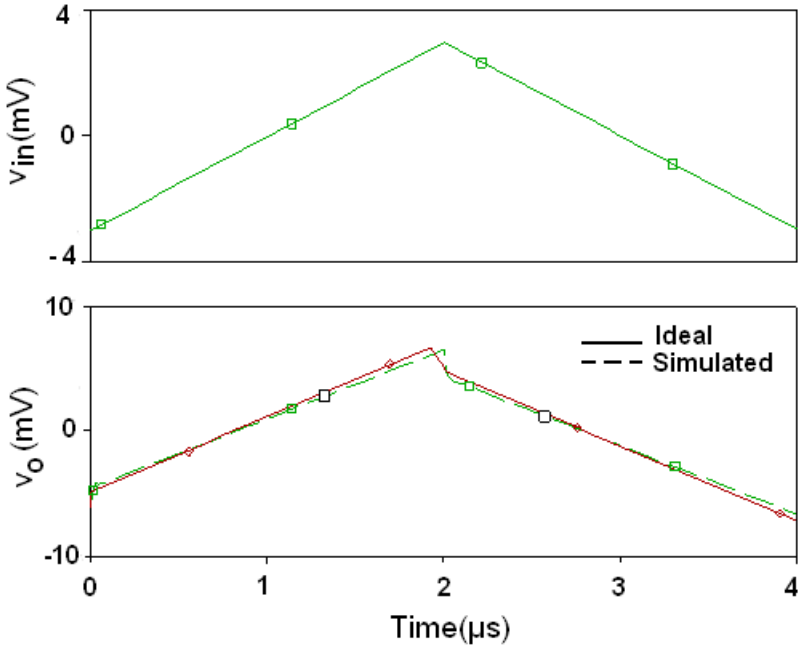



Fig. 6.21 Transient response of the PD Controller.

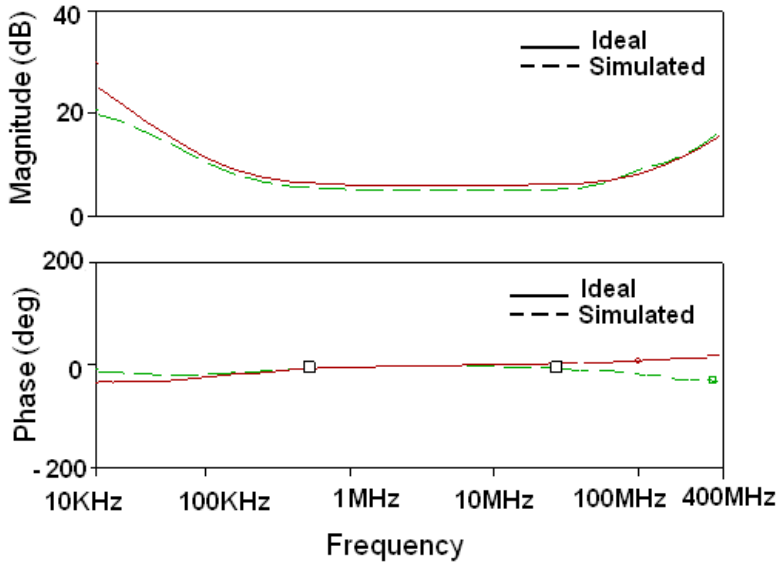



Fig. 6.22 Frequency response of the PID Controller.

Gate voltages are set as $V_{a1}= V_{a2} = V_{a3} = V_{a4} = 1$ V and $V_{b1}= V_{b2} = V_{b3} = V_{b4} = 0.5$ V which result in resistance values as $R_1 = R_2 = R_3 = R_4 \approx 50$ KΩ and the chosen value of capacitances are $C_1 = C_3 = 10$ pF and $C_2 = 0.05$ pF. Using these passive component values various controller parameters can be computed as $K_p = 2$, $K_i = \frac{R_4}{R_1 R_3 C_3} = 2 \times 10^6\ s^{-1}$ and $K_d = C_2R_4 = 2.5$ ns. Figure 6.22 represents the ideal and simulated frequency responses of PID controller and the transient responses are shown

in Fig. 6.23.

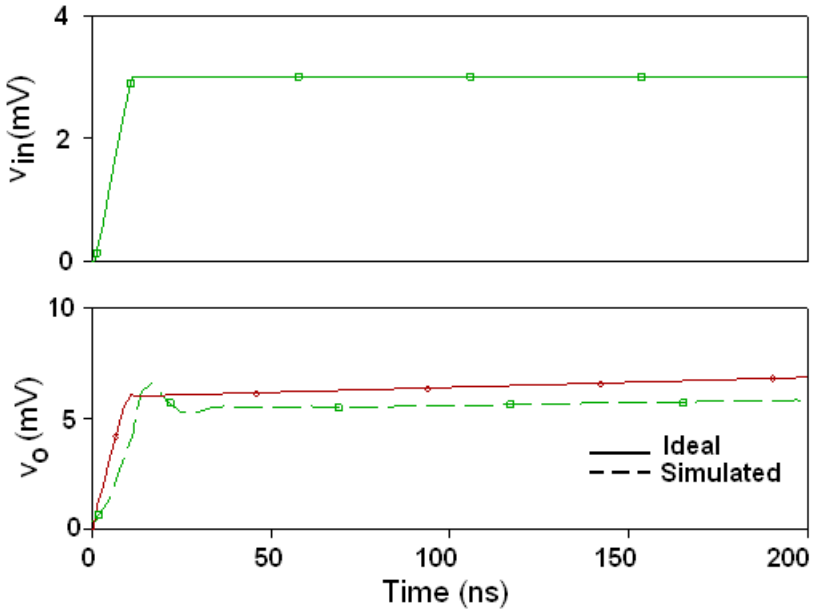



Fig. 6.23 Transient response of the PID Controller.

## 6.8 PERFORMANCE EVALUATION OF THE PROPOSED CONTROLLERS

To evaluate the performance of various controllers their effect on a second order plant is analyzed by forming a closed loop system as shown in Fig. 6.24. An LPF [44] as shown in Fig. 6.25 is used as a second order system. The LPF circuit can also be made electronically tunable by implementing all the related resistors using MOS transistors operating in linear region. The transfer function of the LPF using equal component design with $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C$ can be derived as

$$\frac{V_0(s)}{V_i(s)} = \frac{\frac{1}{R^2C^2}}{s^2+2\frac{s}{CR}+\frac{1}{R^2C^2}} \tag{6.36}$$

The LPF of Fig. 6.25 can be characterized by

$$\omega_n = \frac{1}{RC} \ , \xi = 1 \tag{6.37}$$

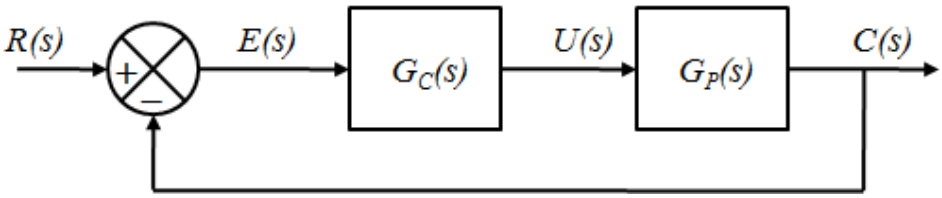



Fig. 6.24 Closed loop control system.

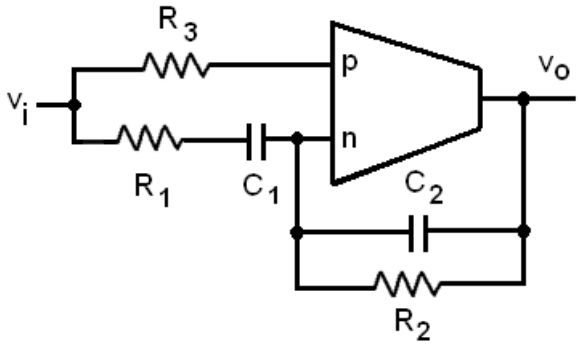



Fig. 6.25 The second order low pass filter.

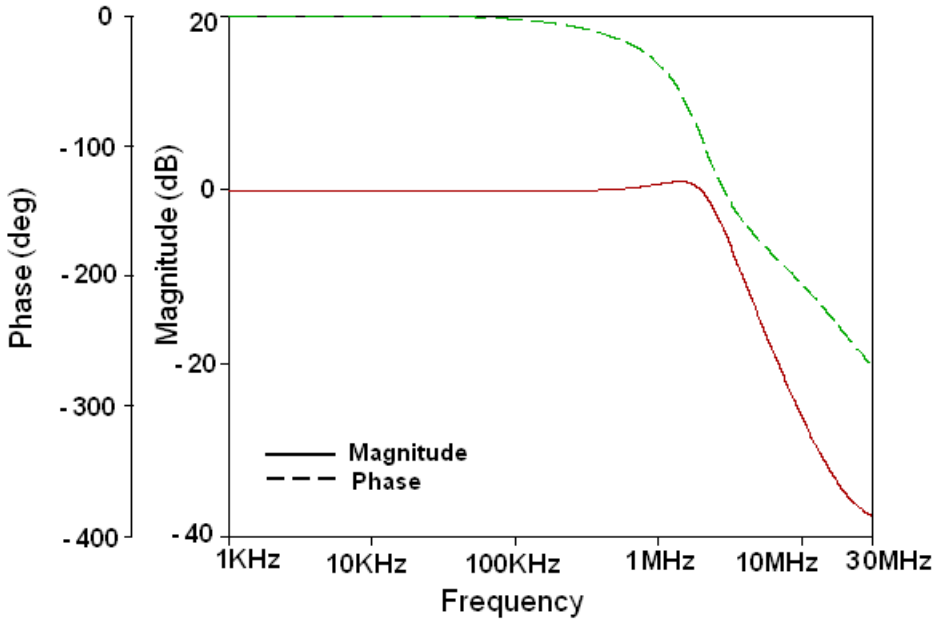



Fig. 6.26 Frequency response of the second order LPF.

First the step response of the open loop second order system is studied and then the effect of various proposed controllers is observed by realizing a closed loop system. The LPF is designed for $\omega_n$ = 3.98 MHz and $\xi$ = 1.0 for which capacitance values are chosen as

$C_1 = C_2 = 20$ pF and the resistance value is computed as $R_1 = R_2 = R_3 = 2$ KΩ. The frequency response of the LPF is shown in Fig. 6.26. For time domain analysis a step signal of 50 mV is applied and the simulated response is shown in Fig. 6.27.

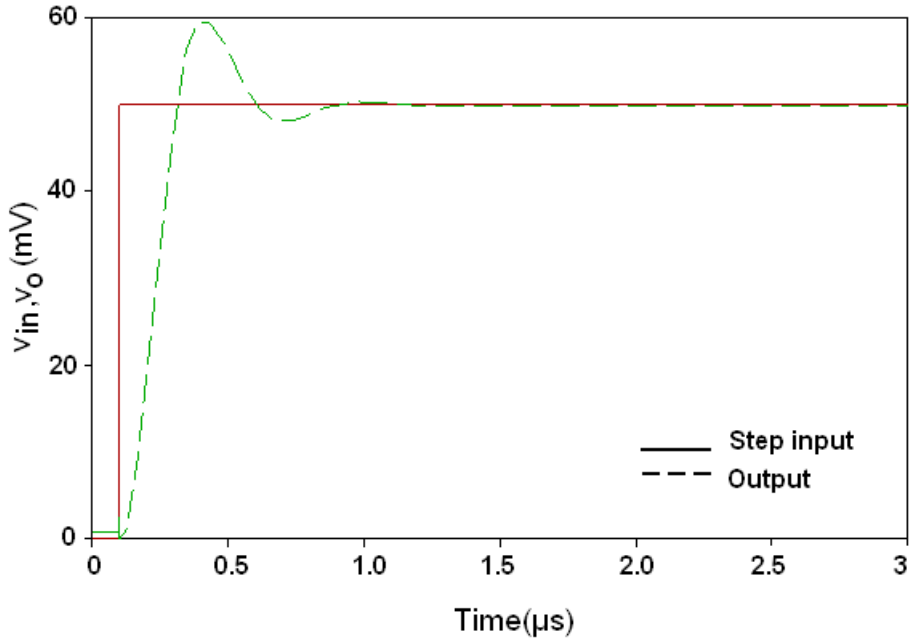
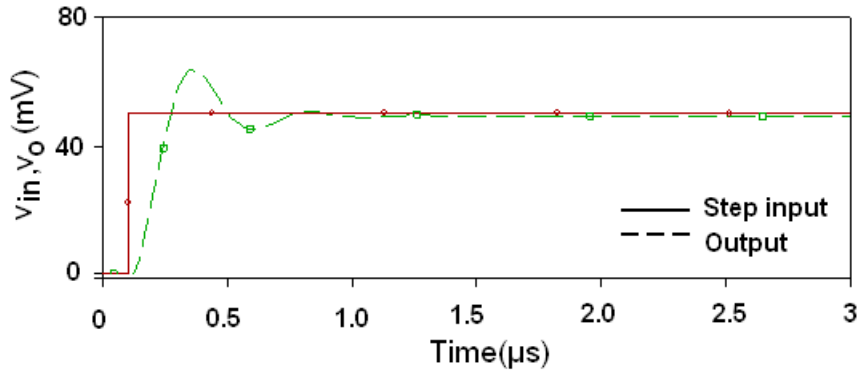
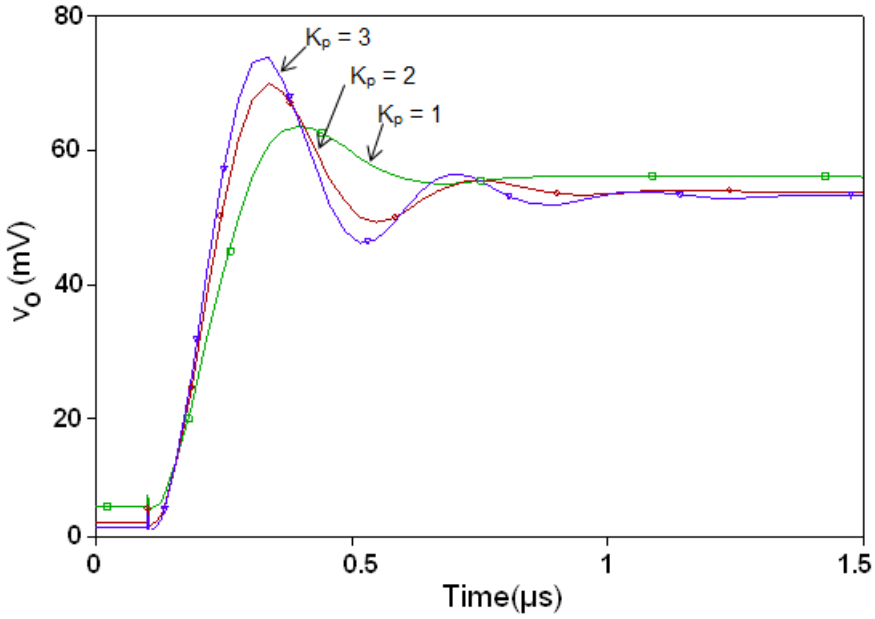



Fig. 6.27 Step Response of the LPF.

To compare the performance of the second order system with and without P-controller, step responses of the system for a 50 mV step input are recorded while choosing $K_P = 2$. Step response of the closed loop system is shown in Fig. 6.28 (a) whereas the effect of varying $K_p$ on closed loop second order system response ,with $K_p$ = 1, 2 and 3 respectively, has been shown in Fig. 6.28 (b). These values of $K_p$ are achieved by keeping $R_1 = 10$ KΩ, while changing $R_2$ from 10 KΩ to 30 KΩ in steps of 10 KΩ. In MOS-C implemented controller $R_2$ is varied by assigning different gate voltage to the transistors used to realize this resistor. It is observed from Fig. 6.28 (b) that the rise time reduces with increasing magnitude of $K_p$ however, the peak overshoot increases. For fair comparison the performance parameters such as overshoot, peak output, rise time and settling time are measured and recorded in Table 6.1 and it was observed that the system performance improves with P controller in terms of rise time; however, the peak overshoot percentage and settling time are increased.




(a)




(b)

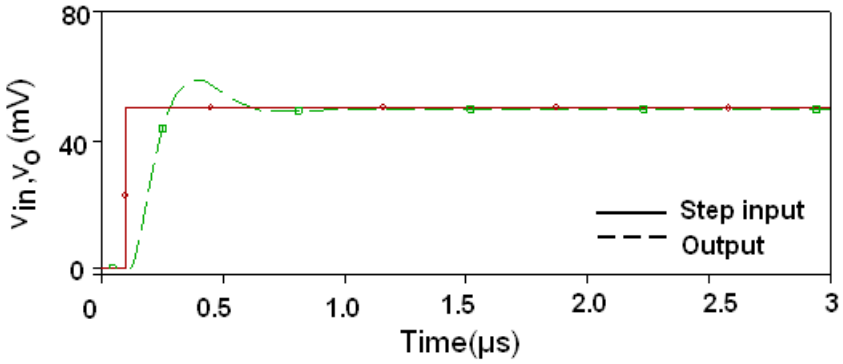
Fig. 6.28 (a) Step Response of second order closed loop system with P controller.

(b) Step response with variable $K_p$.

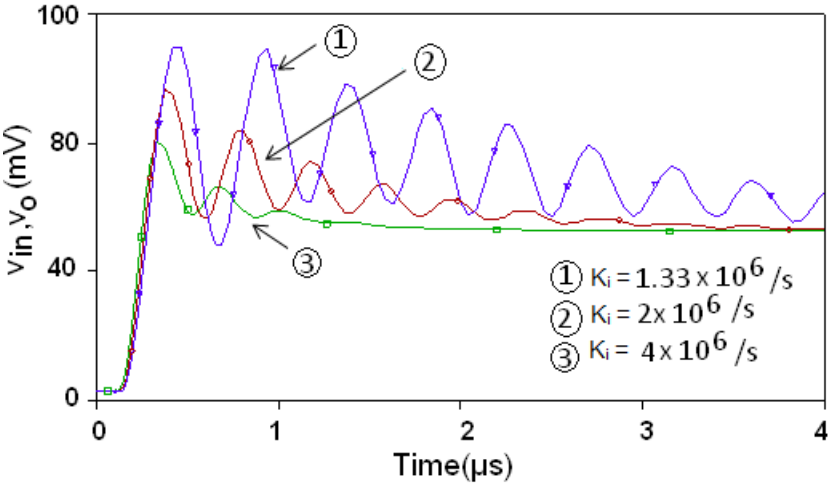
Table 6.1: Performance Comparison of closed loop system with and without P controller.

| Parameter | Without P-Controller | With P-Controller |
|---|---|---|
| Overshoot | 19.56 % | 30.14 % |
| Peak output | 58.26 mV | 62.64 mV |
| Rise time | 140.43 ns | 108.75 ns |
| Settling time | 303.12 ns | 675.11 ns |

The step response of closed loop system with PI controller is shown in Fig. 6.29 (a) having $K_p = 2$ and $K_i = 10^7 s^{-1}$ and Fig. 6.29 (b) shows step response for varying values of $K_i$ while keeping $K_p = 2$ constant. The performance parameters for PI controller are recorded in Table 6.2 which indicates that PI controller influences mainly the settling time as compared to all other parameter.




(a)




(b)

Fig. 6.29 (a) Step response of closed loop system with PI controller. (b) Step response with variable $K_i$ keeping $K_p$ constant.

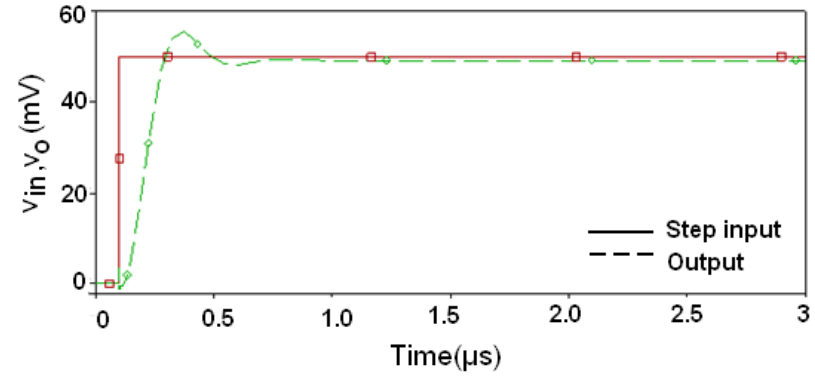
The closed loop step response with PD controller is depicted in Fig. 6.30(a) with $K_p = 2$ and $K_d = 0.4$ μs and in Fig. 6.30(b) step response for varying values of $K_d$ while keeping $K_p = 2$ constant, is shown. Table 6.3 lists the performance parameters for PD controller and there form it can be observed that the PD controller improves all the parameter, prominently overshoot and very small improvement in settling time is observed.

Table 6.2: Performance Comparison of closed loop system with and without PI controller.

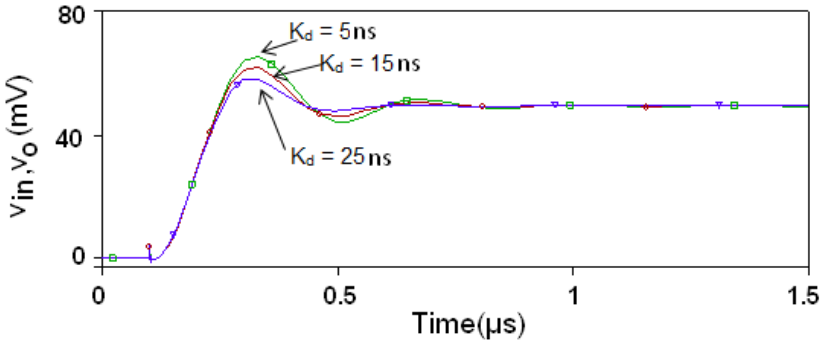
| Parameter | Without PI Controller | With PI Controller |
|---|---|---|
| Overshoot | 19.56 % | 18.76 % |
| Peak output | 58.26 mV | 57.83 mV |
| Rise time | 140.43 ns | 112.28 ns |
| Settling time | 303.12 ns | 266.11 ns |

Table 6.3: Performance Comparison of closed loop system with and without PD controller.

| Parameter | Without PD Controller | With PD Controller |
|---|---|---|
| Overshoot | 19.56 % | 12.89 % |
| Peak output | 58.26 mV | 56.53 mV |
| Rise time | 140.43 ns | 124.27 ns |
| Settling time | 303.12 ns | 278.97 ns |




(a)




(b)

Fig. 6.30 (a) Step Response of second order closed loop system with PD controller. (b) Step response with variable $K_d$ keeping $K_p$ constant.

Step response of the closed loop system with PID controller for a 50 mV step signal having $K_p = 2$, $K_i = 2 \times 10^6\ s^{-1}$ and $K_d = 2.5$ ns is shown in Fig. 6.31. The performance parameters are recorded in Table 6.4 which clearly shows a notable improvement in all the system performance parameters.

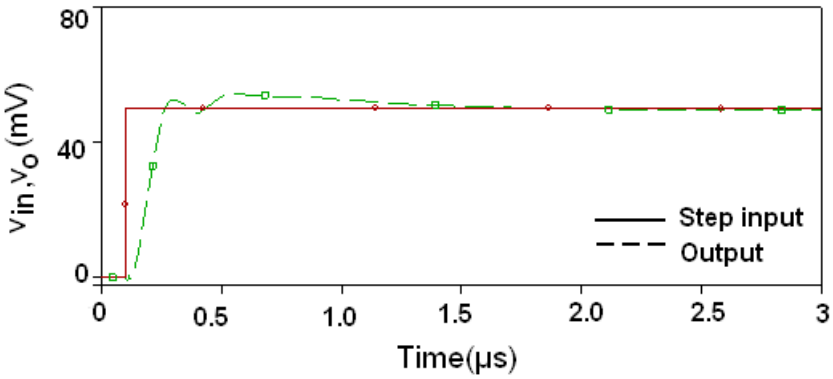



Fig. 6.31 Step Response of closed loop second order system with PID controller.

Table 6.4: Performance Comparison of closed loop system with and without PID controller.

| Parameter | Without PID Controller | With PID Controller |
|---|---|---|
| Overshoot | 19.56 % | 8.16 % |
| Peak output | 58.26 mV | 52.59 mV |
| Rise time | 140.43 ns | 99.75 ns |
| Settling time | 303.12 ns | 252.27 ns |

## 6.9 PERFORMANCE COMPARISON OF THE CONTROLLERS

In Table 6.5 performance parameters of all the four types controllers studied so far are summarized. This table clearly indicates the PD controller prominently improves the overshoot whereas PI controller influences mainly the settling time as compared to all other parameter. PID includes best features of all individual controllers and results in improvement of all the performance measure parameters as is also verified through step response for a 50 mV step signal shown in Fig. 6.31.

Table 6.5: Performance Comparison of closed loop system with and without controllers

| Parameter | Open loop LPF | With P Controller | With PD Controller | With PI Controller | With PID Controller |
|---|---|---|---|---|---|
| Overshoot | 19.56 % | 30.14 % | 12.89 % | 18.76 % | 8.16 % |
| Peak output | 58.26 mV | 62.64 mV | 56.53 mV | 57.83 mV | 52.59 mV |
| Rise time | 140.43 ns | 108.75 ns | 124.27 ns | 112.28 ns | 99.75 ns |
| Settling time | 303.12 ns | 675.11 ns | 278.97 ns | 266.11 ns | 252.27 ns |

## 6.10 CONCLUDING REMARKS

This chapter describes OTRA based circuits suitable for instrumentation and control application. TIA, suitable for amplification of signals from current-source transducers, is proposed first. The proposed amplifier provides high gain for a wide range of frequencies, having a 3dB bandwidth independent of its gain. The gain of the proposed amplifier is electronically tuned by implementing the passive resistor using MOS transistor which also makes circuit MOS-C implementable. The proposed circuit can easily be compensated for parasitics. The proposed circuit, to the best knowledge of author, is the only TIA which uses current mode techniques, though an opamp based TIA is proposed in [100] which uses three opamps and nine resistors; quite a large number as compared to proposed TIA.

The design of OTRA based controllers, namely P, PI, PD and PID controllers have been presented next. The controller parameters $K_p$, $K_d$ and $K_i$ can be adjusted independently and are elctronically tunable as well. The effect of the proposed controllers on a second order closed loop system was analyzed. Performance analysis reveals that PD controller improves percentage overshoot, PI controller refines settling time while PID as a combination of the two, enhances transient as well as steady state time response of the system.

All the circuits presented in this chapter are validated through SPICE simulations. Experimental results are also included for TIA. The simulated results are in line with the proposed theory. The effect of OTRA parasitics, on the performance of all proposed applications, is also analyzed. For high-frequency applications, compensation methods are employed, to account for the error introduced due to parasitics.