D.O.E:- 7/3/19 ; 14/3/19.
D.O.S:-

EXPERIMENT - 1.

Aim :- Realisation of AND, OR, NAND, XOR, Latch circuit and timer circuit using PLC.

Theory :-

• **PLC :-** A programable logic controller (PLC) is an industrial digital computer which has been adapted for the control of manufacturing process, such as assembly line or robotic devices or any activity that requires high reliability control and ease of programing and process fault diagonisis.

PLC's can range from small modular devices with tens of inputs and outputs (I/O), in a housing integral with the processor, to large rack-mounted modular devices with a count of thousands I/O, and which are often networked to other PLC and SCADA systems. They can be designed for multiple arrangements of digital and analog I/O, extended temperature ranges, immunity to electrical noise and resistance to vibration and impact.

· Siemens S7-200 ·

The S7-200 combines a microprocessor, an integrated power supply, input circuits and output circuits in a compact housing to create a powerful Micro PLC. It provides CPU modules that have a large number of I/O points onboard (upto 60 points). The new signal boards are designed with scalable communication ports, digital or analog channels. It is equiped with siemen's dedicated processor chip, the basic instruction execution time is upto 0.15 μs. All CPUs have integrated Ethernet interface to download the programs conviniently and quickly using the common cable.

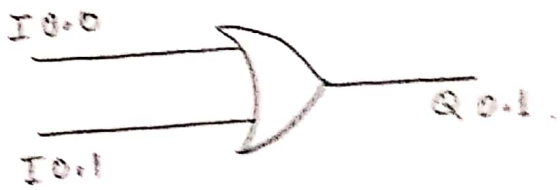
· Ladder Diagram :-

Ladder diagram is a graphical programing language which means that instead of text, the programming is done by combining different graphic elements. These graphic elements are called symbols. These diagram is used to program PLC. Ladder diagram is widely used to program PLCs, where sequential control of a process or manufacturing process is required. Ladder diagram is useful for simple but critical control systems or for reworking old hardwared relay circuits. As programmable logic controllers becomes more sophisticated it has also been used in very complex automation systems.

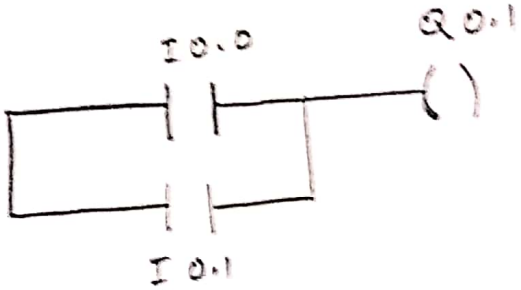
Realization of different logical gates using PLC.

1) OR :- The OR gate is a digital logic gate that implements logical disjunction. Truth Table :-

I 0.0	I 0.1	Q 0.1
0	0	0
0	1	1
1	0	1
1	1	1



Ladder Diagram :

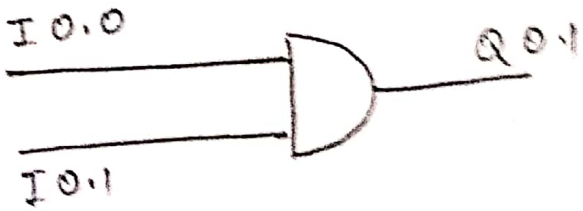


Both the inputs are generally open but when any one of the input is closed the circuit gets complete thereby giving output.

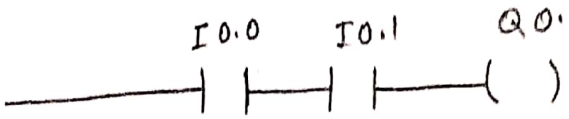
2) AND :- The and gate is a basic digital logical gate that implements logical conjuction.

Truth Table :-

I 0.0	I 0.1	Q 0.1
0	0	0
0	1	0
1	0	0
1	1	1



Ladder Diagram:

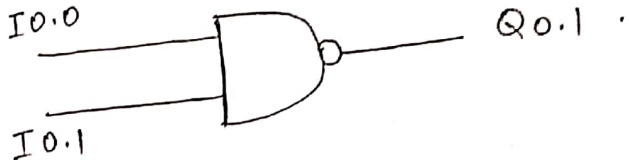


Both the inputs are generally open. When any one of the inputs are closed the circuit remains incomplete thereby giving no output. But when both the inputs are closed the circuit gets complete, producing output.

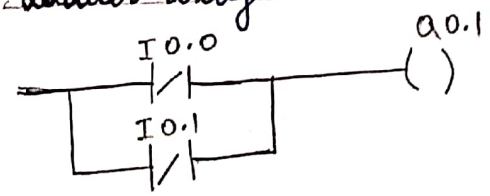
3) NAND :- In digital electronics, NAND gate is a logic gate which produces an output which is false if all its inputs are true.

Truth Table:-

I0.0	I0.1	Q0.1
0	0	1
0	1	1
1	0	1
1	1	0



Ladder Diagram:-

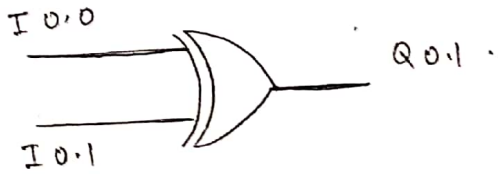


Both the inputs are normally closed so the circuit is complete thereby giving output. If any of the inputs are opened the circuit still remains closed. But if both the inputs are opened the circuit gets incomplete thereby producing no output.

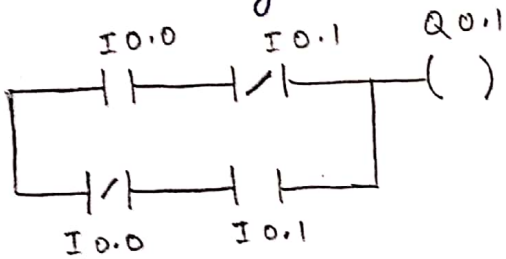
4) XOR:- It is a digital logic gate that gives a true output when the number of true inputs is odd.

Truth Table:-

I 0.0	I 0.1	Q 0.1
0	0	0
0	1	1
1	0	1
1	1	0



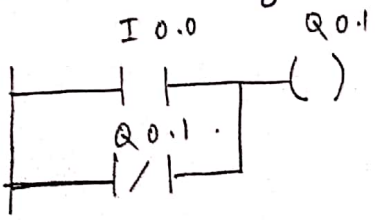
Ladder Diagram:-



When both the inputs are different the circuit gets complete thereby producing the output but when the inputs are equal the circuit is incomplete thereby producing no output.

5) Latch Circuit :- It is a self maintaining circuit, after being energized, it maintains that state until another input is received.

Ladder Diagram



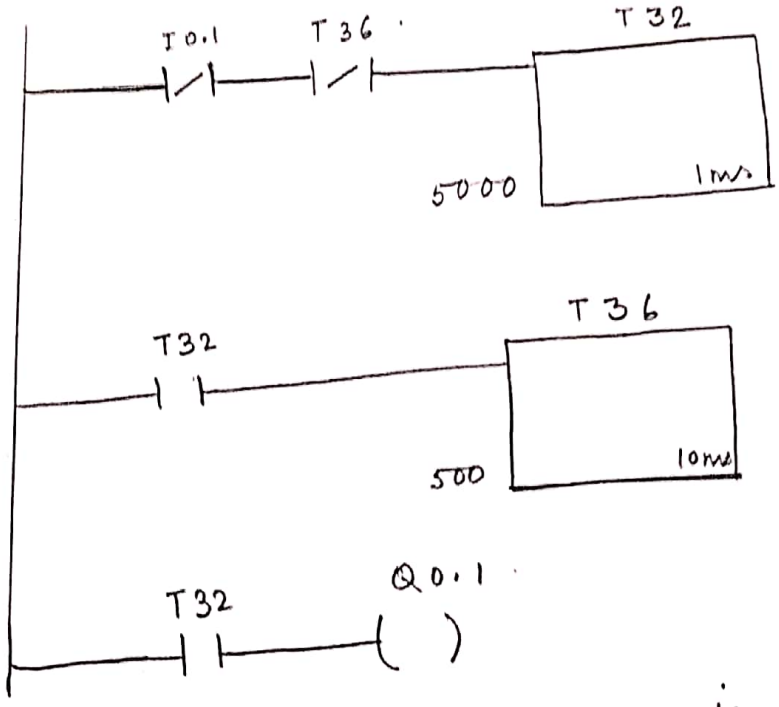
Initially the circuit is open. But the input I 0.0 is closed there is an output. This output is fedback

which inturn completes the circuit thereby maintaining a fixed state.

6) Timer Circuit :-

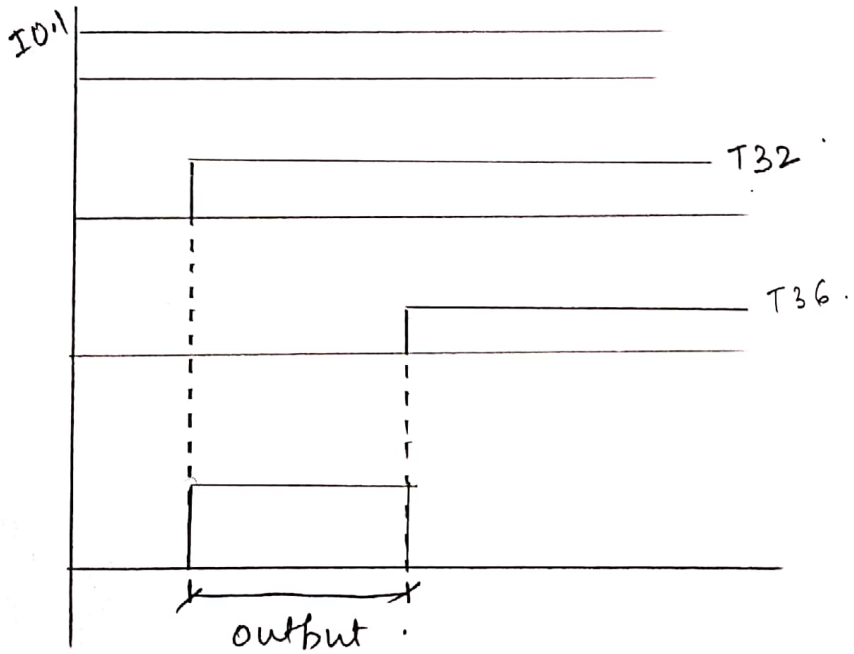
This circuit is used to give output for certain period of time after a given fixed interval.

Ladder Diagram :-



Initially the I 0.1 is normally closed. and T36 is the output of on-delay timer so the circuit is incomplete thereby no output. When I 0.1 is closed the T32 gets activated which is a on-delay timer of (5000 × 1) ms = 5 seconds. It gets high after 5 seconds thereby activating the output as well as the T 36 timer circuit which is also an on delay timer of

(500 x 10) ms = 5 seconds. The switch T36 ~~gets open~~ after generates one pulse thereby activating T32 after 10 seconds. Hence we get output for 5 seconds after an internal of every 10 seconds.



CONCLUSION

By performing this experiment we learnt how to use ladder diagrams to perform the actions of different gates (logical), timer circuit and latch circuit on PLC.

NAME :- SOUVIK SAHA

ROLL :- 11.

1 Draw the flow graph of 16 point DIT-FFT.

A Signal flow graph of 16 point DIT-FFT.