RITWIK SAHA

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https://github.com/ritzvik

EXPERIENCE

RESEARCH INTERN

Siemens Technology and Services Pvt. Ltd.

Jun 2019 – Present Bengaluru, India

- Set up infrastructure for running serverless applications using KNative, Kubernetes and Docker.
- Bechmark performance of KNative under various load conditions.

RESEARCH INTERN

Siemens Technology and Services Pvt. Ltd.

Dec 2018 – Feb 2019 Bengaluru, India

- Set up blockchain(Ethereum) infrastructure and benchmark transaction rates under various paremeters like variable block times, transaction loads, block size etc.
- Designing a supply chain system on blockchain infrasctructure.
- Analyzing other blockchain platforms like tendermint etc. against Ethereum.

TECHNICAL SKILLS

Programming Languages - C/C++, Python
Deep Learning
Blockchain
API Development
Communication/DSP
Web Development

SOFTWARE SKILLS

- Python Libraries and Frameworks :
  - TensorFlow, Keras, Flask
- Graph Databases :
  - Neo4J, ArangoDB
- Containerization and Orchestration :
  - Docker, Kubernetes
- Simulation :
  - MATLAB, Simulink, NI LabView

MISCELLENOUS POSITIONS

MENTOR

Summer of Code in Space, ESA

May 2019 – Present

- Assigned as project mentor in SOCIS(Summer of Code in Space) organized by ESA(European Space Agency).
- Mentoring a student for the EinsteinPy Project.

DELEGATE

Indian Youth Delegation to China

July 2018

- Represented India as a delegate in Indian Youth Delegation to China - 2018.

EDUCATION

B.Tech (Electrical Enginerring)

Indian Institute of Technology, Mandi

2016-2020 Mandi

- CGPA: 7.7/10

CBSE (Higher Secondary)

D.A.V Public School

2016 Shrestha Vihar, Delhi

- 94.4%

CBSE (Matriculation)

D.A.V Public School

2016 Shrestha Vihar, Delhi

- CGPA: 10/10

PROJECTS

PROTOCOLS DESIGNING & VERIFICATION

- UART IP, SPI, AMBA AHB & AXI—lite.

LZMA COMPRESSION MODULE FOR FPGA

- Designed Range Encoder Module of LZMA compression for VCU1525 Xilinx FPGA using HLS and SDx.

LC3 MICROCONTROLLER VERIFICATION

- Verifying LC3 Microcontroller using SV Testbench environment

2 STAGE PIPELINED ALU WITH FIFO DESIGNING & VERIFICATION

- Designing the 2 stage ALU along with FIFO and Analysing the coverage using SV & tcl scripts.

SMART DUSTBIN

- Automated interactive Dustbin with dynamic monitoring of the vacant space.

PUBLICATIONS

- R. Jain, H. Tulsani, A. Bansal, "A two- tier steganographic model based on (2,2)VCS and integer wavelet transform", in Preceding of The 5th International Conference on Computing for Sustainable Global Development organized by IEEE, pp. 4731-4734, (2018).