COMPUTER SCIENCE

Computer Organization and Architecture

Instruction Pipelining

Lecture_03

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TOPICS
TO BE
COVERED
01 Pipelining Concepts
01 Pipelining Hazards

PIPELINE Concept

Designing of pipeline

Execution Time of Pipeline

Performance Evaluation of Pipeline

Efficiency & Throughput

Uniform Delay & Non Uniform Delay pipeline.

Practice Question.

GATE - PyQ's.

Pipelining Strategy

To apply this concept
To instruction
Execution we must
Recognize that an
Instruction has a
Number of stages

Similar to the use of
An assembly line in a
Manufacturing plant

New inputs are
Accepted at one end
Before previously
Accepted inputs
Appear as output at
The other end

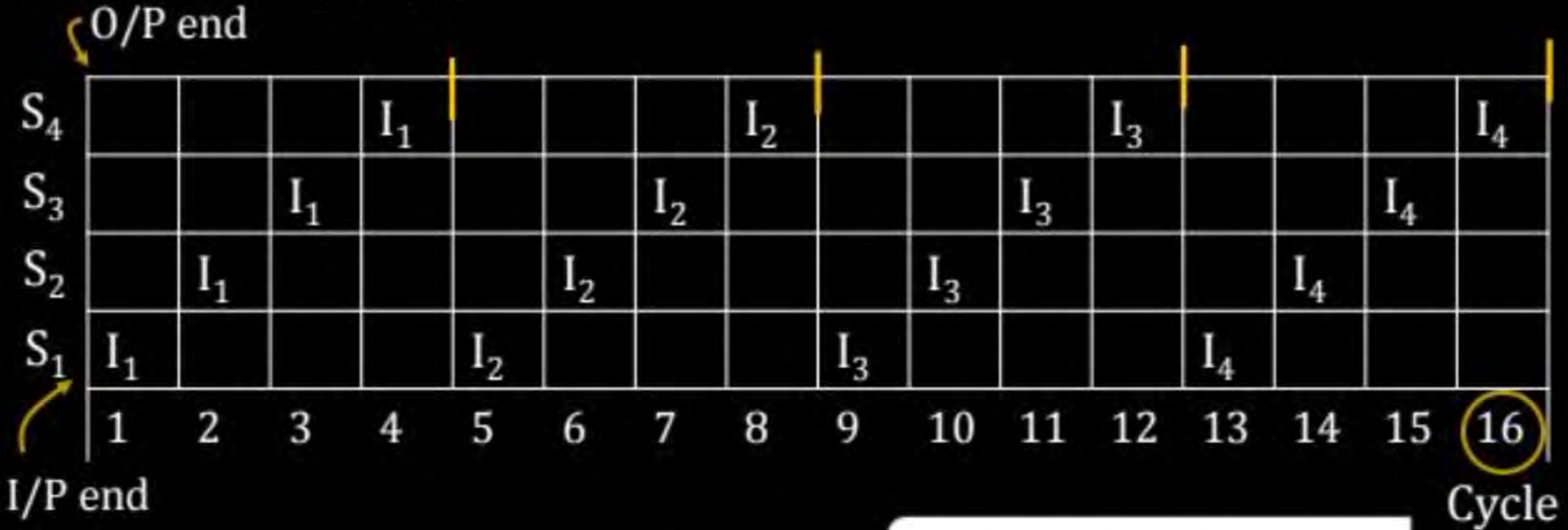
PIPELINE

- Pipelining is a mechanism which is used to improve the performance of the system in which task (Instruction) are executed in overlapping manner.
- Pipelining is a decomposition technique that means the problem is divided into sub problem & Assign the sub problem to the pipes then operate the pipe under the same clock.

Let us consider 4 segment pipeline used to execute 4 instruction the execution sequence as:

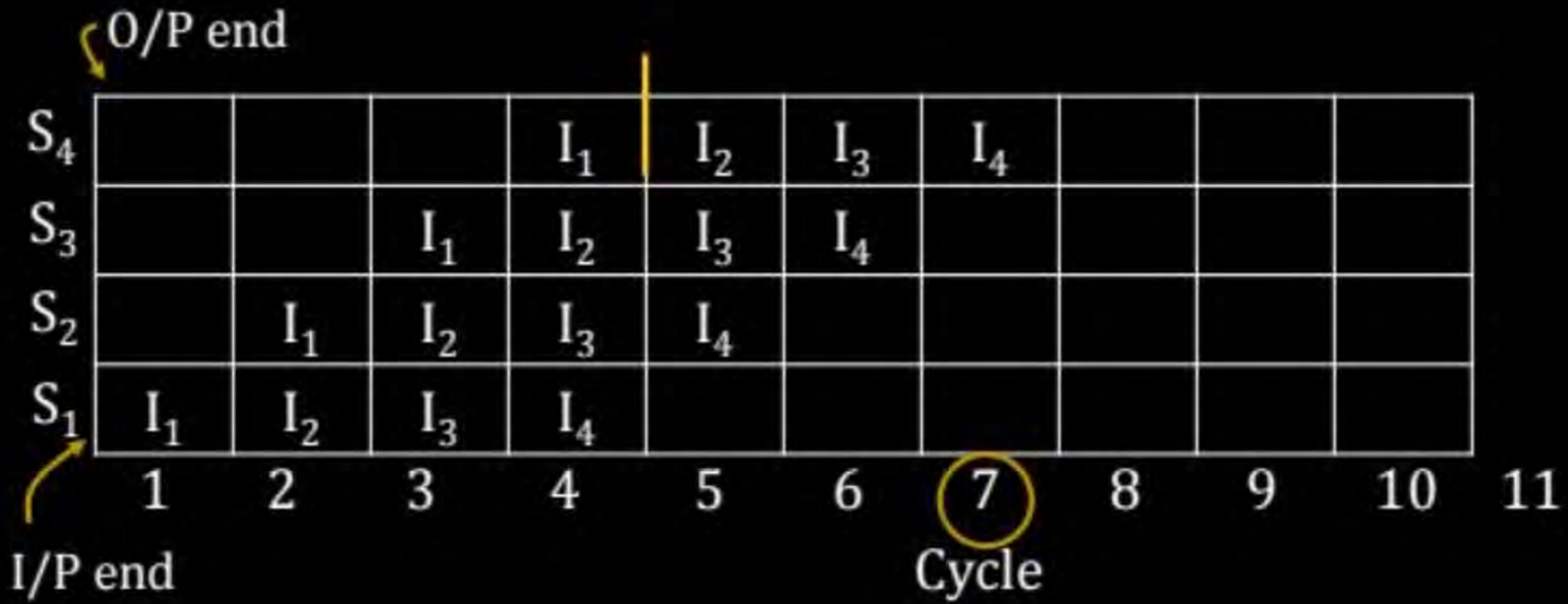
Segment/stages = $[S_1\ S_2\ S_3\ S_4]$

Instruction: $[I_1\ I_2\ I_3\ I_4]$



n = 4, t_n = 4, Non pipeline

Non-PIPELINE



PIPELINE

$k = 4$

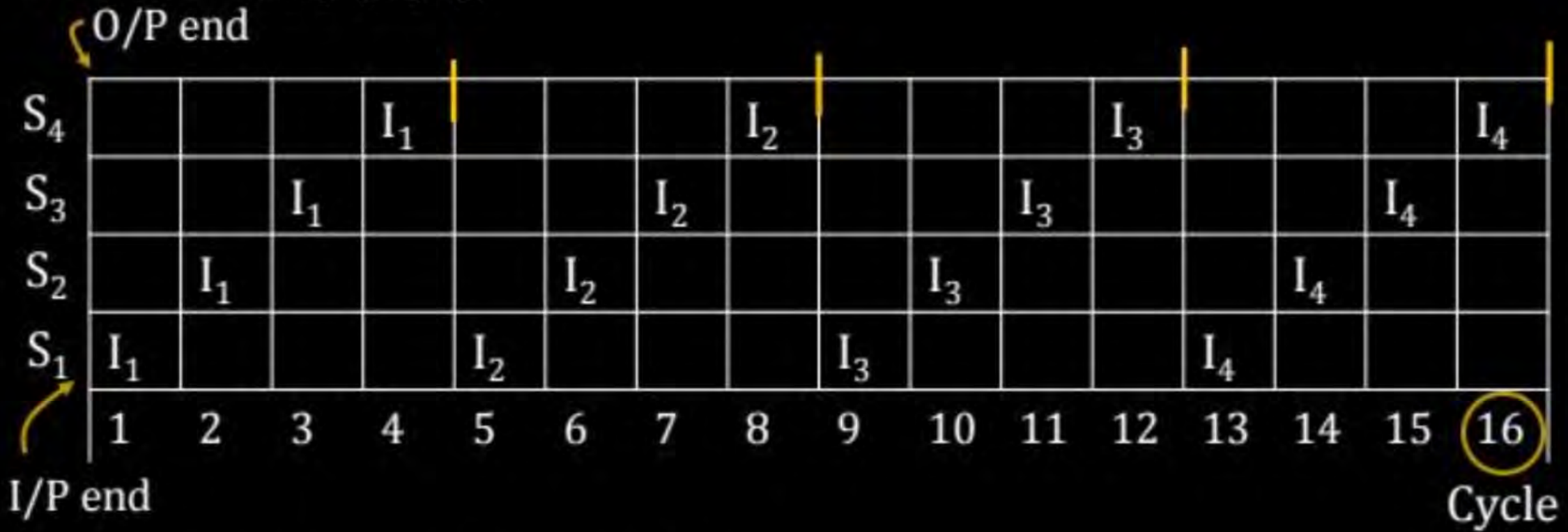
$n = 4$

PIPELINE

Let us consider 4 segment pipeline used to execute 4 instruction the execution sequence as: PIPELINING

Segment/stages = $[S_1\ S_2\ S_3\ S_4]$

Instruction: $[I_1\ I_2\ I_3\ I_4]$



n = 4, t_n = 4, Non pipeline

PIPELINE - CONCEPT

Successful.

In the Pipeline

$$CPI = 1$$

Cycle Per Instruction = 1

How CPI = 1 ?

for n Instⁿ $ET_{PIPELINE} = [k + (n-1)]$ Cycle

(k-1) Ignored

$$1 \text{ Instruction} = \frac{k + n - 1}{n} \Rightarrow \frac{n}{n} = 1$$

$$CPI = 1$$ Ans

$\therefore$

Q.1 How Design (Construct) the Pipeline ?

Q.2 What is meaning of CPI=1 in pipeline ?

Q.3 How to Set CPI in Uniform Delay Pipeline ?

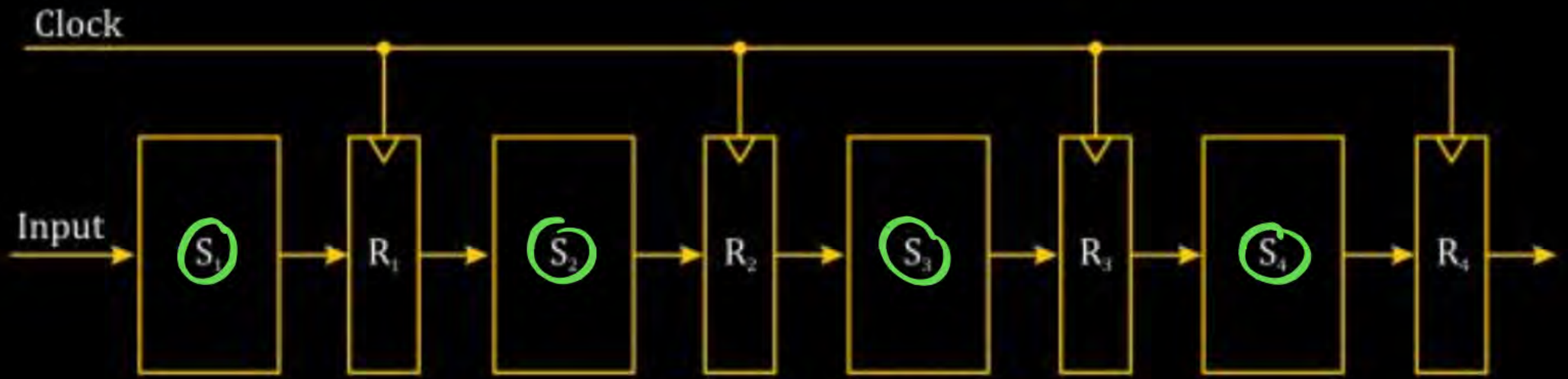
Q.4 How to Set this CPI in Non Uniform Delay Pipeline ?

Q.1 How Construct (Design) the Pipeline ?

PIPELINE Design

RISC ⇒ 5 Stage

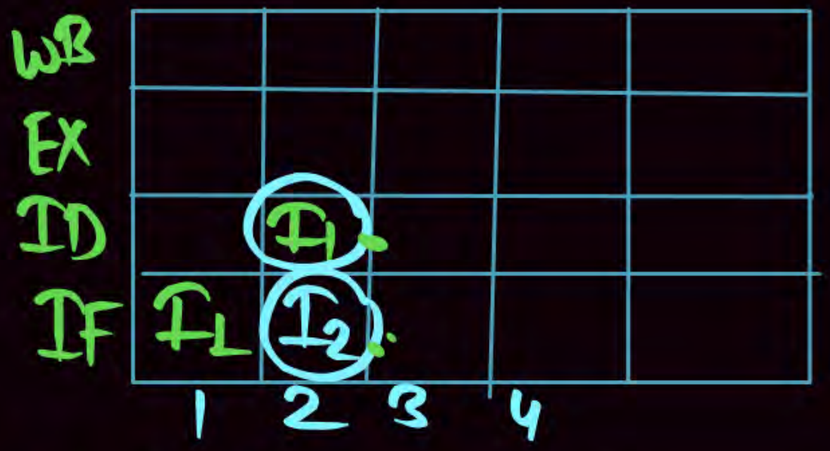
Sol^n If we want to construct 'N' Stage Pipeline, The entire CPU (Control Unit) is divided into 'N' functional Unit [Independent functional Unit] which is independent from each other.



Four-segment pipeline.

Indepent function Unit means when One functional Unit Performing the One task, At the Same time other functional Unit performing the other task (operation)

(e.g) Instruction pipeline.



At clock cycle NO 2.

I_1 is in Decode Stage,

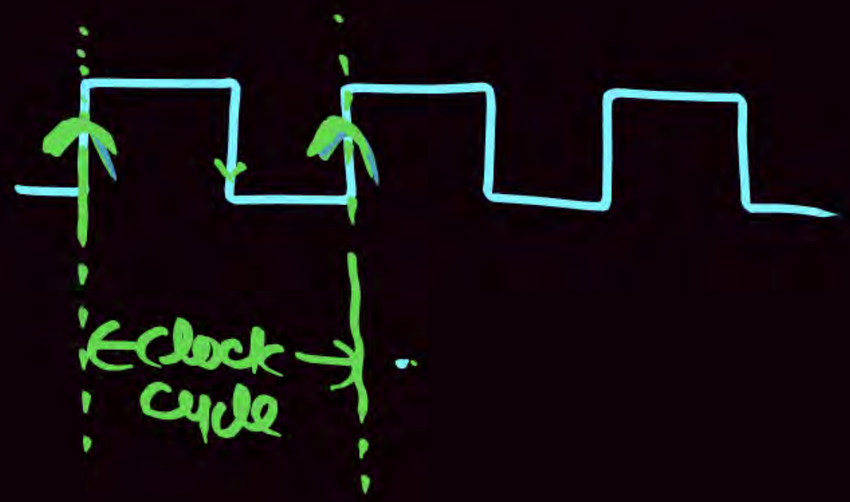
& I_2 is in Fetch Stage at the Same time (clock cycle 2).

Note

Characteristic of Pipeline is, in Every New Cycle New Input Must be inserted into the Pipeline.

$$CPI = 1$$

Clock cycle Per Instruction



(Q) How to Set this CPI & Why Clock is Required ?

WHy clock is Required ?

Sol^n Because whenever we Enable the clock then operations are performed.

&

To Provide the Synchronization between the Stages.

(Q.3) How to Set this CPI in Uniform Delay Pipeline ?

Uniform Delay

$$t_p = \text{Stage Delay}.$$

(OR)

If Buffer Delay is given

$$t_p = \text{Stage Delay} + \text{Buffer Delay}.$$

PIPELINE Design

$t_p = 20 + 2 = 22\,nsec$

Uniform Delay Pipeline

Time = 22 nsec

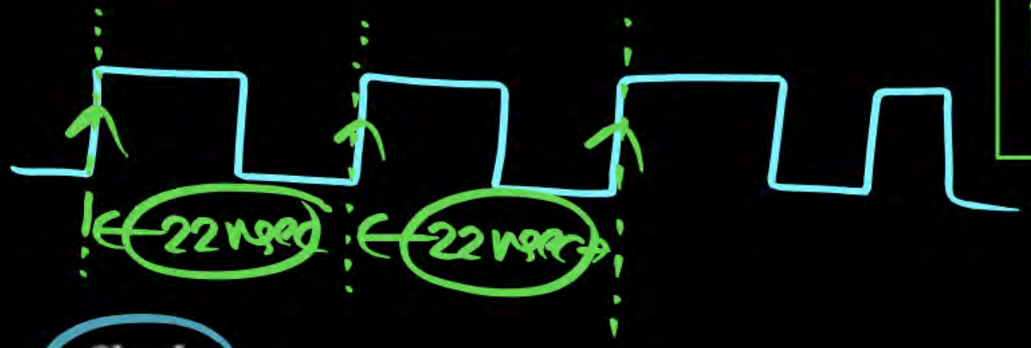
$$F = \frac{1}{22\,nsec}$$

CPI = 1

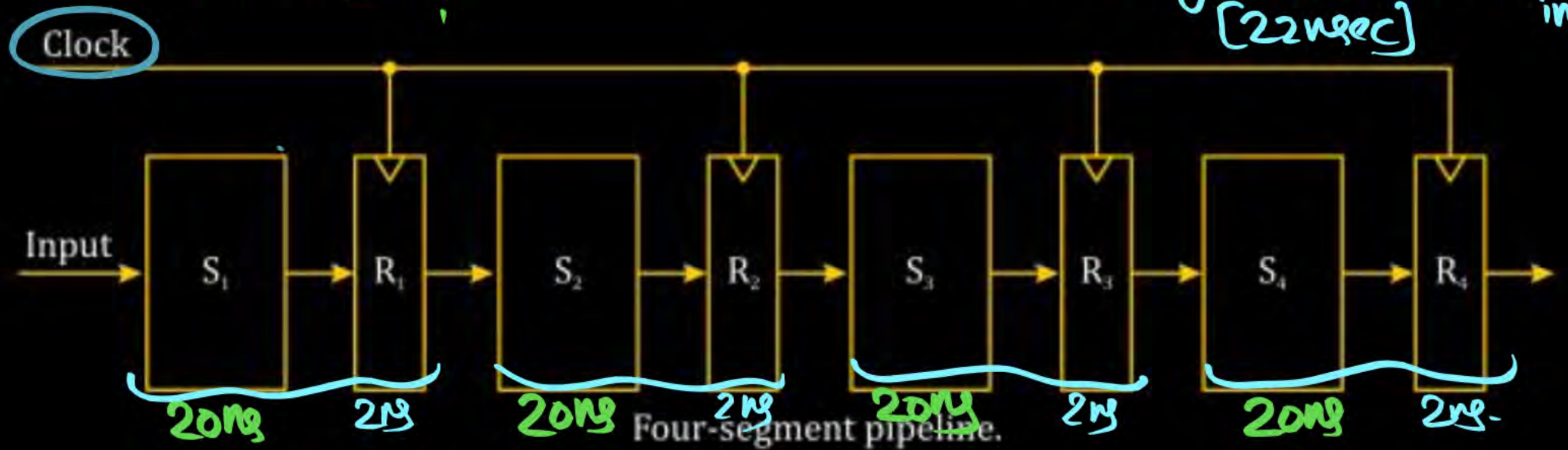
Clock Cycle Per Instn = 1

= 22 nsec

Cycle time = 22 nsec



Every CPI [22 nsec] New I/P inserted into Pipeline



Four-segment pipeline.

for Uniform Delay

Previous eg.
4 Stage

very first Inst^n take $\Rightarrow$ k*t*p

$4 * 22 + (n-1)22$ → After every cycle getting output

n Task

$\Downarrow$

Remaining (n-1) Inst^n every CPI

Q.4 How to Set this CPI in Non Uniform Delay ?

$$t_p = \max(\text{Stage Delay})$$

If Buffer Delay is Included.

$$t_p = \max(\text{Stage Delay} + \text{Buffer Delay})$$

PIPELINE Design

Sabmy

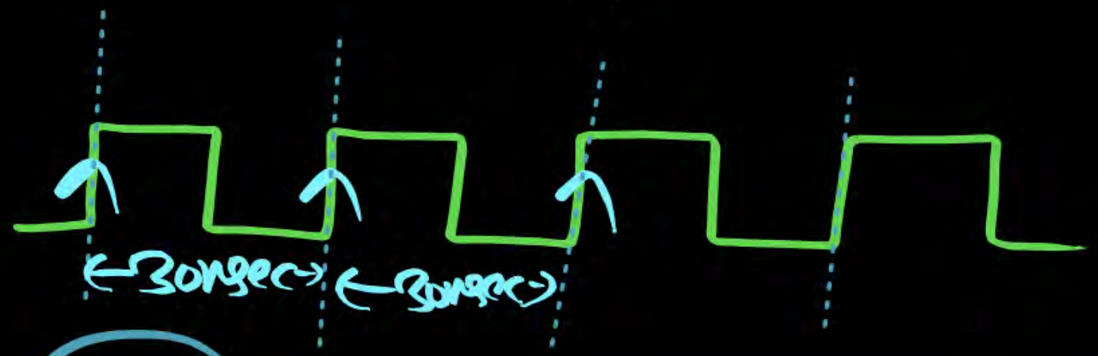
Non Uniform Delay Pipeline:

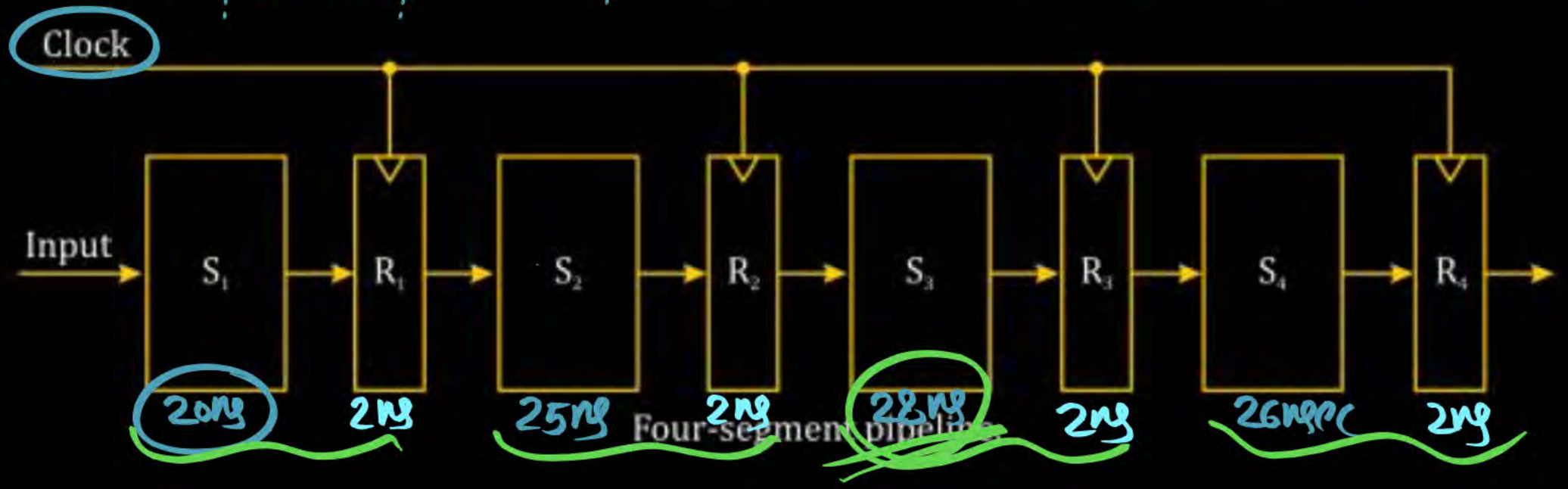
$t_p = \max(\text{StageDelay} + \text{Buffer Delay})$

$28+2$

$t_p = 30\text{nsec}$

$F = \frac{1}{30\text{nsec}}\ \text{Hz}$

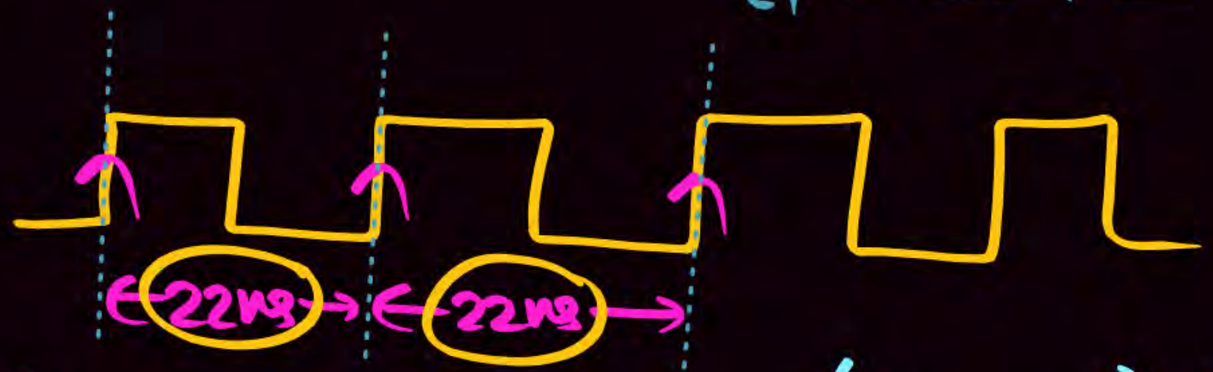




Q WHy we Not Take Minimum ?

$tp = 20 + 2 \Rightarrow$ **$tp = 22$ nsec**

$F = \frac{1}{22\,nsec}$



If we take Minimum (22nsec) then Stage1 Work finish & Data Move from Stage1 to Stage2 (in Previous example) Reference:

But in 22nsec Stage2, Stage3, & Stage4 Work Not finish.

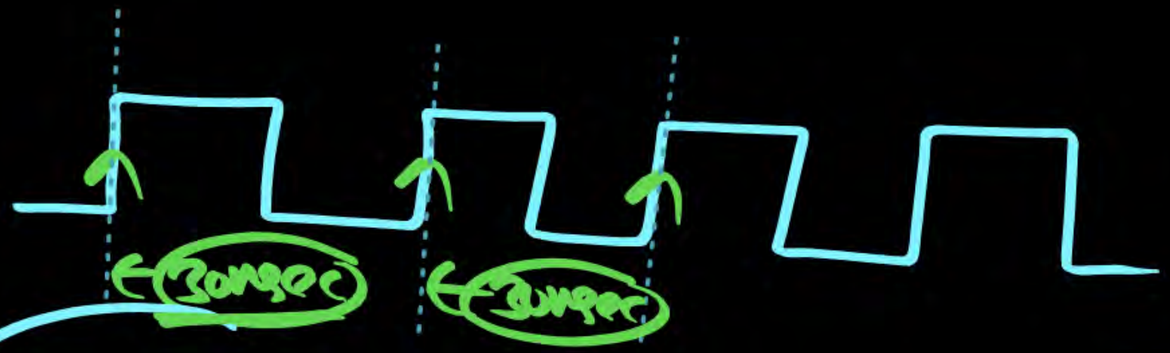
So Proper functioning & working we take Maximum.

So always takes maximum (Stage Delay + Buffer Delay)

If we take Maximum $t_p = 28 + 2$

$t_p = 30nsec$

$F = \frac{1}{30nsec}$ Hz



Synchronization

If we take Maximum 30ns But Stage 1 Task finish at 22nsec. But Clock is set to be 30nsec. Every Phase output will be available After 30nsec.

→ When One Cycle Complete the Data given from Stage 1 to Stage 2. So Synchronization.

Q Some time Buffer Delay is also Different?

$$t_p = \max\left(\text{Stage Delay} + \text{Buffer Delay}\right)$$

PIPELINE Design

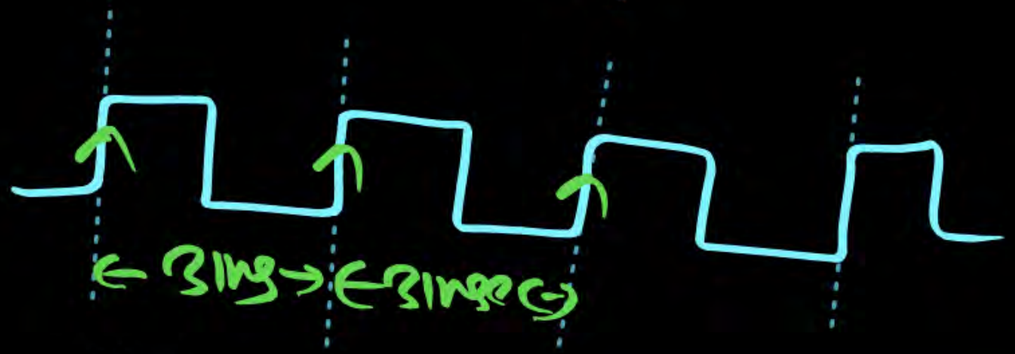
$t_p = \max(\text{StageDelay} + \text{Buffer Delay})$

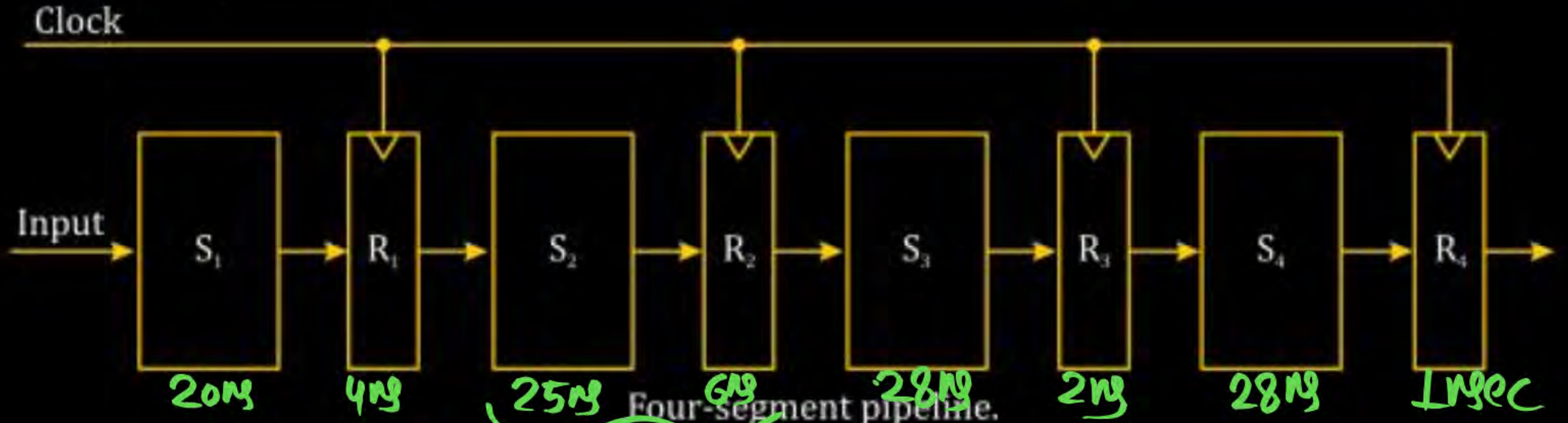
Solny **Non Uniform Delay Pipeline:**

$t_p = \max[(20+4), (25+6), (28+2), (28+1)]$

$\max(24, 31, 30, 29)$

$t_p = 31\text{nsec}$ Ans





Four-segment pipeline.

Additional Stages

- **Fetch Instruction (FI)**
  - Read the next expected Instruction into a buffer.
- **Decode Instruction (DI)**
  - Determine the opcode and the operand specifiers.
- **Calculate operands(CO)**
  - Calculate the effective address of each source operand.
  - This may involve displacement, register indirect or other forms of address calculations.
- **Fetch Operands(FO)**
  - Fetch each operand from memory.
  - Operands in register need not be fetched.
- **Executed Instruction(EI)**
  - Perform the indicated operation and store the result, if any, in the specified destination operand location
- **Write Operand(WO)**
  - Store the result in memory

Timing Diagram for Instruction pipeline operation

NAT Q. 10

Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume that there are no stalls in the pipeline. The speed up achieved in this pipelined processor is 3.2. Ans

[GATE-2015(Set-1)-CS: 2M]

Ans (3.2)

Non Pipeline

Each Instn takes = 4 cycle

$$\text{Cycle time} = \frac{1}{2.5G} \text{ sec}$$

Cycle time $\Rightarrow$ 0.4 nsec

ET in Non pipeline [t_n] = 4 X 0.4 nsec

= 1.6 nsec.

Pipeline

Each Instn takes = 1 cycle

CPI = 1 Cycle

2GHz Frequency

$$\text{Cycle time} = \frac{1}{2GHz} = 0.5 \text{ nsec}$$

$$t_p = 0.5 \text{ nsec}$$

$$S = \frac{ET_{NONPIPE}}{ET_{PIPE}} = \frac{1.6}{0.5} = 3.2$$ Ans

MCQ Q. 11

Consider a 4-stage pipeline processor. We want to execute a loop: For(i=1;i<=1000;i++){ I1, I2, I3, I4} where the time taken (in ns) by instruction I1 to I4 for stages S1, S2, S3, S4 is shown below:

	S1	S2	S3	S4
I1	1	2	1	2
I2	2	1	2	1
I3	1	1	2	1
I4	2	1	2	1

The Output of I1 for i=2 will be available after ?

[GATE-2004-CS: 2M]

A 11ns

B 12ns

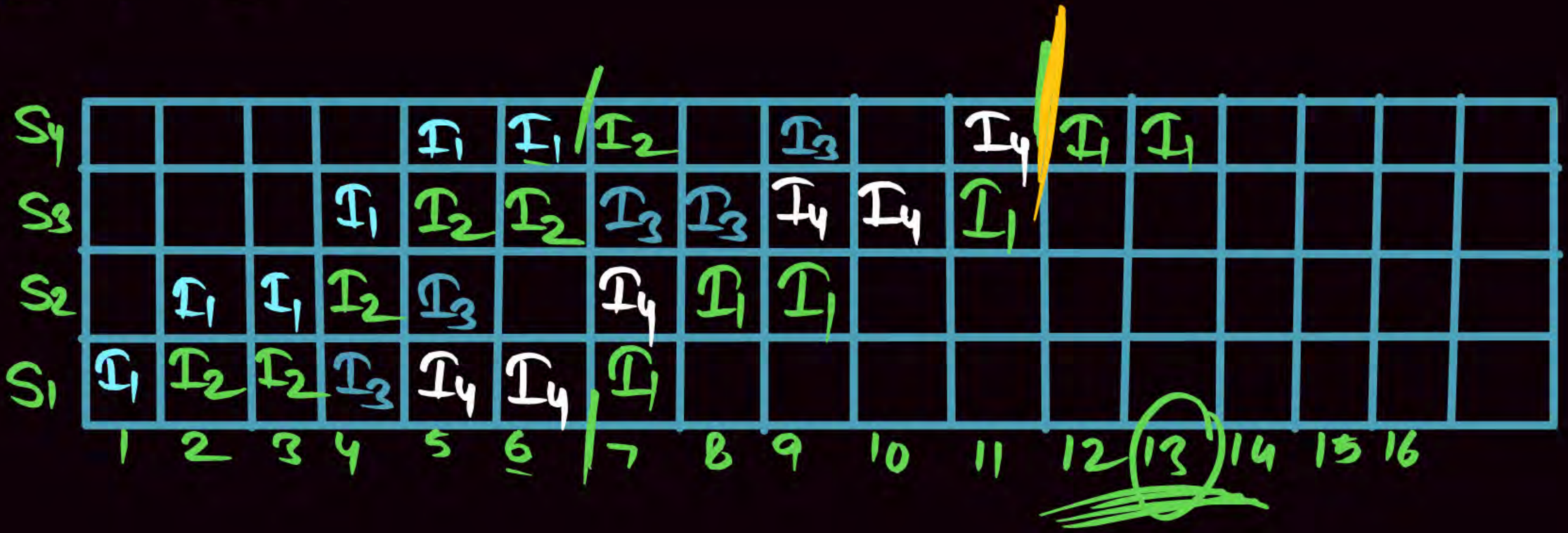
C 13ns

D 28ns

	S_1	S_2	S_3	S_4
I_1	1	2	1	2
I_2	2	1	2	1
I_3	1	1	2	1
I_4	2	1	2	1

$i=1 \quad [I_1 I_2 I_3 I_4) = (11)$

$i = 2 \Rightarrow (I_1)$




Alternate Method

	S_1	S_2	S_3	S_4
I_1	1	2	1	2
I_2	2	1	2	1
I_3	1	1	2	1
I_4	2	1	2	1

	S_1	S_2	S_3	S_4
I_1	1	3	4	6
I_2	3	4	6	7
I_3	4	5	8	9
I_4	6	7	10	11
I_1	7	9	11	(13)

Ans

MCQ Q. 12

Consider a 4-stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3, I4 in stages S1, S2, S3, S4 is shown below:

	S1	S2	S3	S4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

30
25
23
Avg

What is the number of cycles needed to execute the following loop?
for (i = 1 to 2) {I1; I2; I3; I4;}

[GATE-2009-CS: 2M]

A 16

B 23

C 28

D 30

	S_1	S_2	S_3	S_4
I_1	2	1	1	1
I_2	1	(3)	2	2
I_3	2	1	1	3
I_4	1	2	2	2

$i = 1$ to 2

Σ I_1
I_2
I_3
I_4
}

	S_1	S_2	S_3	S_4
I_1	2	3	4	5
I_2	3	6	8	10
I_3	5	7	9	13
I_4	6	9	11	15
I_1	8	10	12	16
I_2	9	13	15	18
I_3	11	14	16	21
I_4	12	16	18	23

$15 \times 2 = 30$

NAT **Q. 13**

Consider a 3 GH_z (gigahertz) processor with a three-stage pipeline and stage latencies τ_1, τ_2, and τ_3 such that $\tau_1 = 3\tau_2/4 = 2\tau_3$. If the longest pipeline stage is split into two pipeline stages of equal latency, the new frequency is 4 GHz, ignoring delays in the pipeline registers.

[GATE-2016(Set-2)-CS: 2M]

Ans(4)

$$\gamma_1 = \frac{3\gamma_2}{4} = 2\gamma_3$$

$$\gamma_1 : \gamma_2 : \gamma_3 \Rightarrow 6 : 8 : 3$$

$$\gamma_1 = \frac{3\gamma_2}{4} \qquad \frac{3\gamma_2}{4} = 2\gamma_3$$

$$\frac{\gamma_1}{\gamma_2} = \frac{3}{4}\left[\frac{6}{8}\right] \qquad \frac{\gamma_2}{\gamma_3} = \frac{8}{3}$$

$T_1 : T_2 : T_3 \Rightarrow 6 : 8 : 3$

Assume time = x

$T_1 = 6x \quad T_2 = 8x \quad T_3 = 3x$

$t_p = \max(6x, 8x, 3x)$

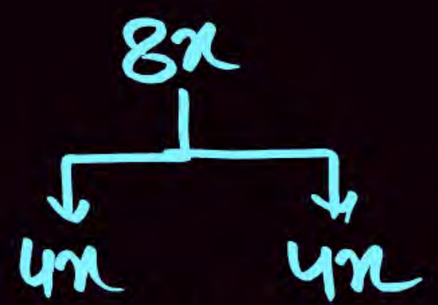
$\boxed{t_p = 8x}$

$\text{Frequency} = \frac{1}{\text{Time}}$

$3\text{GHz} = \frac{1}{8x}$

$\boxed{\frac{1}{x} = 24\text{GHz}}$ — (eq)

New Design



$t_{p\text{new}} = \max(6x, 4x, 4x, 3x)$

$\boxed{t_{p\text{new}} = 6x}$

$\text{Frequency}_{\text{new}} = \frac{1}{\text{Time}_{\text{new}}}$

$= \frac{1}{6x} \Rightarrow \frac{1}{6} \times \frac{1}{x}$

$\Rightarrow \frac{1}{6} \times 24\text{GHz}$

$\boxed{4\text{GHz}}$ Ans

NAT **Q. 14**

Consider two processors P_1 and P_2 executing the same instructions set. Assume that under identical conditions, for the same input, a program running on P_2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on P_1. If the clock frequency of P_1 is $1GH_Z$, then the clock frequency of P_2 (in GH_Z) is _____.

[GATE-2014(Set-1)-CS: 2M]

✓ ET = IC × CPI × cycle time.

ET = # Instⁿ × # cycle/Instⁿ × Cycle time.

In the Question Same No of Instⁿ (# Instⁿ Not given)

CPI × cycle time.

ET = Cycle/Instⁿ × Cycle time.

$ET_{P_1} = CPI \times Cycle\ time_1$

$ET_{P_2} = 1.2\ CPI \times Cycle\ time_2$ ✓

$ET_{P_2} = 0.75 * ET_{P_1}$ ✓

$Cycle\ time_{P_1} = \frac{1}{1\,GHz} = 1\,nsec$

$$ET_{P_2} = 1.2\,CPI \times Cycle\ time_2 \quad -(1)$$

$$ET_{P_2} = 0.75 * ET_{P_1} \quad -(2)$$

$$0.75 * (ET_{P_1}) = 1.2\,CPI \times Cycle\ time_2$$

$$0.75 \times (CPI * 1\,nsec) = 1.2\,CPI \times Cycle\ time_2$$

$$Cycle\ time_2 = \frac{0.75}{1.2} = 0.625\ nsec$$

$$Clock\ freq_{P_2} = \frac{1}{0.625\ nsec}\ Hz = 1.6\,GHz$$ Ans

MCQ Q. 15

Consider the following processor design characteristics:

I. Register-to-register arithmetic operations only.

II. Fixed-length instruction format.

III. Hardwired control unit.

Which of the characteristics above are used in the design of a RISC processor?

[GATE-2018-CS: 1M]

(A) I and II only

(B) II and III only

(C) I and III only

(D) I, II and III

Q.

COA 2022: CS

NIC PYQ SERIES

Consider a machine with 40 MHz processor which has run a benchmark program. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count. What will be the effective CPI, MIPS rate, and execution time.

Instruction Type	Instruction Count	Cycles/ Instructions
Integer arithmetic	45000	1
Data Transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

$$\text{Avg CPI} = .45 \times 1 + .32 \times 2 + .15 \times 2 + .8 \times 2$$

$$\boxed{\text{Avg CPI} = 1.55 \text{ cycle}}$$

$$\text{Cycle time} = \frac{1}{40\text{MHz}}$$

$$\text{Avg Instn ET} = 1.55 \times \frac{1}{40} \times 10^{-6} \text{ sec}$$

$$\boxed{\text{Avg Inst ET} = 0.03875 \times 10^{-6}}$$

1 Instn ET = 0.3875×10^{-6} sec

In 1 Sec How Many # Instn

$$= \frac{1}{0.03875} \times \underbrace{10^6}_{M.} \text{ Instn/sec}$$

$\Rightarrow$ 25.8 MIPS

Total Prog ET = $0.03875 \times 10^{-6} \times 100000\ (10^5)$

$\Rightarrow 0.03875 \times 10^{-1}$

$\Rightarrow 3.875 \times 10^{-3}$

$= 3.87$ msec.

A CPI:3.55; MIPS: 30; Execution time:1.87 ms

B CPI:1.55; MIPS: 25.8; Execution time:3.87 ms

C CPI:5.60; MIPS: 45.8; Execution time:2.87 ms

D CPI:2.55; MIPS: 35.8; Execution time:4.87 ms

Q.

COA 2017: IT

NIC PYQ SERIES

Which of the following is not a form of main memory ?

A. Instruction cache

B. Instruction register

C. Instruction opcode

D. Translation look-aside buffer

Q. COA 2017: CS

NIC PYQ SERIES

In a 10-bit computer instruction format, the size of address field is 3-bits. The computer uses expanding OP code technique and has 4 two-address instructions and 16 one-address instructions. The number of zero address instructions it can support is

A 256

B 356

C 640

D 756

Q.

COA 2017: CS

NIC PYQ SERIES

A micro programmed control unit

A is faster than a hardwired unit

B Facilitates easy implementation of a new instruction

C is useful when small programs are to be run

D All of the above

THANK YOU!