

Computer Organization & Architecture

Cache Memory

DPP Discussion Notes





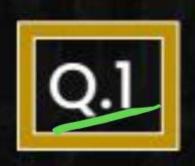




TOPICS TO BE COVERED

01 Question

02 Discussion



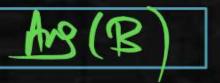
Consider a processor that can support a maximum memory of 8GB, where the memory is word-addressable (a word consists of 2 bytes). Then the size of the address bus of the processor is at least _____bits.











Memory Size = 8GByte Word Size = 2 Byte Memory is wood Addressable 84B Memory = 8GB 4GX (2R) 60

28th Words

4G Words

4G Words =) 32 Word Address = 32bit App

Q.2

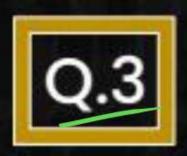
Assume a direct mapped cache having 8 cache lines, each cache line consists of 2 words and each word is of one byte. The address bus consists of 7 bits, then the tag field of the cache consists of ______ bits.



$$TAG = 7 - (3+1)$$

$$= 7 - 4$$

Line (Block) Size = Zwords [NAT] | Word Size = I Byte



Assume a 32-bit addressable physical memory and 2 MB cache block of size 8 kB each, then how many bits are required in the tag field of the cache address if the cache is 4-way set associative IS Avg

Ang (K)

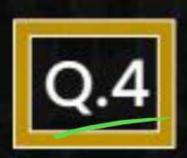


P.A=32 bit Galusize=2mB Block Size=8kB

4 Way Set Associative Cache
TAG bits ?

5.0 = 66it





Consider a 16-Kbyte cache with the following features, each block will hold 32 bytes of data (not including tag, valid, etc ...), The cache would be 2-way set associative, physical addresses are 32 bits and data is addressed to the word and words are of 32 bits long. Then how many blocks would be in this cache and how many bits of tag are stored with each block entry?

[MCQ]



512, 19



512, 22



256, 20



512, 21



Cache Size = 16 kB

Block Size = 32 Byte

P.A = 32 bit

2 way Set Associative

=32-13

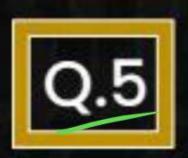
TAG = 19 bits A

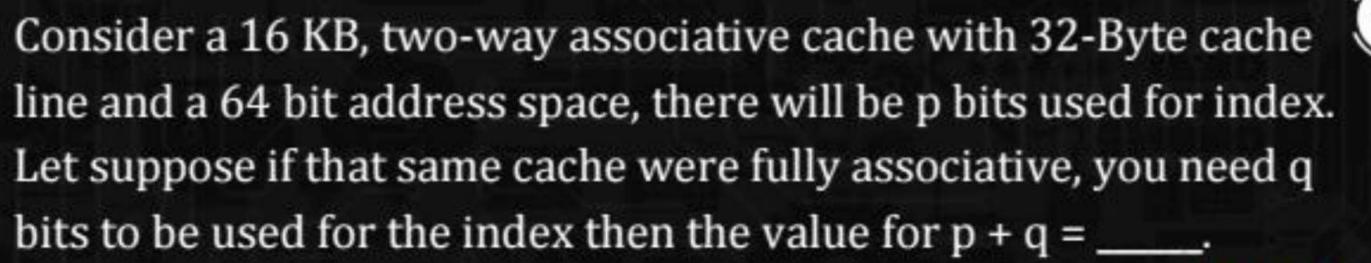
Black Size = 32Byte = 25Byte
Word offset (W.O) 75bit

#LINES: CMSize =) 16KB = 2500 #CM BENUKSize 32B = 2500 RIDUKS)

2 Way set Associative

Set [s.o] = 8bit

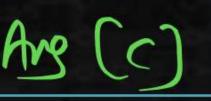












Couhe Size = 16KB = 2B 2 way Set Associative Block Size = 32 Byte = 2 Byte Physical address (P.A) = 64bit

#-UNES= COMSIZE = 21/25=69

SET = #LINES = 29 = (28 Set)

Physical adolfsess(PH) -64bit (Set-dbset = 8bit)

Phit is used to Index the Galle in 2 way Set Associative (Point to)

Galle Set

9 bit is used to Index in fully Associative Malphing.

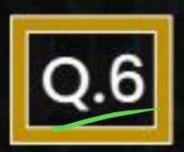
2 Way TAG Set WORD
Set OFFSET Associotive 516it 86it 56it

Set offset is used to Index the Guhe in set Associative Kmods=i

So P=861+ 149=840

C-PA = Gubit ->
TAG W.O Fully Associative TAG W.O. 59bit 5bit

Here No Mapping function. Mm Blode Mapped to Earth Cache Booth have Comparates Q=0

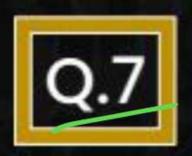


Consider a system having 512KB, 16-way set associative L2 cache with a 128 byte cache line size, Then how many cache lines are present? 4096 Ma (4096)

Cache Size = 512 kB = 29B 16 Way Set Associative

CMLINE (Block) Size - 128 Byte = 2B

NAT



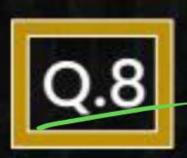
Assume a cache with 32-bit address, 768 blocks and a block size of 128 bytes, tags are 17 bits then what is the associativity of the cache (NAT)





Physical address (P.A) = 32bil Block Size = 128 Byte Tog = 17bit

#CMBlouks(LINES) = 768
What is the aesociativity?



Assume a direct mapped cache memory with 16 cache block (0 – 15) and a main memory having 256 blocks (0 to 255). Assume that, initially the cache did not have any memory block, Consider the following sequence of memory block references:

3, 180, 43, 2, 191, 881, 190, 14, 181, 44, 186 and 253, Then which memory blocks will be present in the cache after the above sequence of memory block reference?





2,3, 180, 43, 2, 191, 190, 88, 14, 181, 44, 186



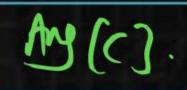
2,3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 181, 44, 186, 253



2, 3, 180, 181, 881, 186, 43, 44, 253, 14, 191



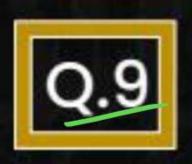
None of the above



3, 180, 43, 2, 191, 881, 190, 14, 181, 44, 186, 253.

#CM LINE-16 SO KMODN > KMODIG. LINEO .180 1.16 = 43 1.16 2 1/16 = 2 . 19/1/16 = 15 .881 1/16 =1 1901.16 = 14 14 1/16 = 14-. 121 1/16 = 5 44 1/16 = 12

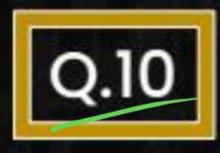
· 186 1/16 = 13

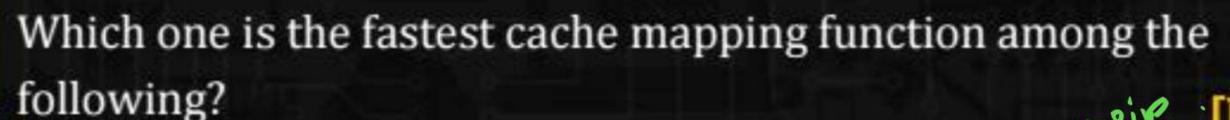


Assume the access patterns x, y, z, y, x where each letter corresponds to a unique cache block and also assume that there was no access to any block before this and all conflicts are random. Then what is the probability of the second access to x being a hit on a direct mapped cache with 4 line (closet to)?

[MCQ]

A. 40%		X
B. 50%	Second Access ob X is Hit	N Z
c. 80%	Ang (D)	
100%		d









- B. Set associative mapping | MODS J
- C. Direct mapping KMODN=1 -> Simple But Very large No. of Conflict Miss
- D. None of these

Ars (A)



Suppose a cache has 70% hit ratio, an access time of 50 ns on a cache hit and an access time of 120 ns on a cache miss then what is the effective access time (using hierarchical memory)

EMAT Tavg = $h \times tc + (1-h)(tm+tc)$ tc: song=) $0.7 \times so + (1-0.7)[120+so)$ tm:120 mg= $3s + (0.3) \times 170$

$$=86$$
 rgec

= 35+5



Suppose local hit rate for L_1 cache is 20% and the local hit rate for L_2 cache is also 30%. The hit time for the L_1 cache is 8 cycle, the hit time for L_2 cache is 20 cycles and access time for main memory is 30 cycles then what is average memory access time in cycle? (approximately)

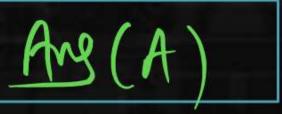
[MCQ]











another Abbreach Main Hittime MissRate Memory. Miss Penalty , 2ocycle 30cycle. TI + (1-h1) T2 + (1-h2) $\Rightarrow 8 + (1-0.2)[20 + (1-0.3) \times 30)$ $78+0.8[20+(0.7)*30) \rightarrow 8+0.8[20+21]$ = 8+ 0.8/41)-8+32.8 = 40.8 % 41 cycle.



Choose the correct statements from the following.





Instruction, and data stored in cache are regularly used by the CPU, if data not present in cache then it always transfers from main memory.

No (is Simulaness According them Direct from MM



Data is stored on temporary basis in cache memory. first toareful



Programs stored in cache takes more time to execute. Then Cache to CPU



Cache memory has limited capacity.

ess time.





Consider the following statements.

Ang(A)



If size of the block is increased then compulsory misses can be reduced.

If associativity of cache is increased then that can lead to increasing conflict misses. Compulsary Miss: Increasing Caulle Brock Size

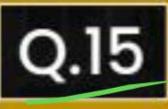
Only S₁ is true

Only S₂ is true

Both S₁ and S₂ are true

Neither S₁ nor S₂ is true

Capacity Miss Processing Cache Size Conflict Miss Processing the associativity



Consider a 128 word cache and the main memory is divided into 32 word blocks. The main memory access time is 50 µs / word and the cache access time is 20 µs/word. The hit ratio for read operation is 80% and for the write operation is 90%. Whenever a cache miss happens, associated block must be the brought from main memory to cache for both read and write operation. Let there be 40% references for write operations. If the write back updation policy is used and at any point of time 80% cache blocks are modified, then what is the T_{avg} ? (upto 1 decimal in μ sec)

Ang 1480.8)

ho = 80% = 0.8 (te) Cache Access = 20 nsec/word =) | Word give to CPU. Main Memory Access time = 50 week word hw = 90.1 = 0.9 80.1. Block is modified (Disty bit 32 Word Block. Tangread = hot to + (1-ho) [Modified Limits with Back Not modified Not modified to the to] + /cleam [tm tte]

= 0.8 x 20.1 (1) $\Rightarrow 0.8 \times 20 + (1-0.8) \left[0.8 \left(1600 + 1600 + 20\right) + \cdot 20 \left(1600 + 20\right)\right]$ => 16+ 0.2 (0.8 (3220) + (.20 (1620)) 2576+324 16 + 0.2x2900 by 1000 = 596 WEC

hr = 80% = 0.8 (te) Cache Access = 20 nsec/word =) I word give to CPU. Main Memory Access time = 50 week word hw = 90.1. = 0.9 80.1. Block is mudified (Dioty bit 32 Word Block. Tang = hw * tc + (1-hw) [Modified with the Back . Clean = 0.2]

Not middled the tc] + /clean [tm +tc] + /clean [tm +tc] $= 0.9 \times 20 + (1-0.9) \left[0.8 \left(1600 + 1600 + 20\right) + \cdot 20 \left(1600 + 20\right)\right]$ = 18 + O·L (0.8 (3220) + (.20 (1620)) 2576+324 =) 18+ O.L[2900] =18+290 wite = 308 WEC

40.1. Ref. Write operation 601. Reference for Read Decration

=) ·60×596 + ·40×308

Toyg = 480.8 wec Toyg = 481 wec.

Q.16

A 16-way set associative cache of size 128KB is used in a system with 32-bit address. For such cache memory, the memory size is (in Kbytes) Provided block size is 4 bytes.





#SET X Bloucher X Tag bits (00) Tog Memory = # LINES X Tay bit ョ25米19 7 32KX19 bits Byte

> 4KX19 Byte > 76KByte Ang



