CS & IT ENGINEERING

Computer Organization and Architecture

Instructions Pipelining

DPP Discussion Notes

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01 Question

02 Discussion

Q.1

Consider a non-pipelined processor with 25 ns cycle time is divided into 5 stages with latencies of 5ns, 7ns, 3ns, 6ns and 4ns. If the pipeline latch latency is 1 ns then the maximum clock frequency to be applied is 125 MHz **[NAT]**

Stage Delays = 5ns, 7ns, 3ns, 6ns, 4ns.

Buffer Delay = 1nsec

$t_p = \max(\text{Stage Delay} + \text{Buffer Delay})$

$t_p = 8\text{nsec}$

Freq. = $\frac{1}{\text{Time}}$

$= \frac{1}{8\text{nsec}}$ Hz

$= \frac{1}{8\times10^{-9}} = \frac{1}{8}\times1000\times10^{6}$

$= 125\times10^{6}$ Hz

$= 125$ MHz Ans

Ans (125)

Q.2

Consider a 4-stage pipeline with delays of 320 ns, 260 ns, 340 ns and 300 ns respectively. Inter stage buffer delay is 10 ns, register uses constant clock rate, then what is the total time taken to process 2000 data items on this pipelined system _____ (in micro seconds)

[NAT]

A. 700.05

B. 701.05

C. 142.05

D. None of these

Ans (B)

Stage Delay = (320ns, 260ns, 340ns, 300ns)

Bubber Delay = 10nsec.

$t_p = \max(\text{Stage Delay} + \text{Bubber Delay}) \Rightarrow 340 + 10 \Rightarrow \boxed{t_p = 350\,\text{nsec}}$

$k = 4, \quad n = 2000$

$ET_{PIPE} = [k + (n-1)]\, t_p$

$= [4 + (2000 - 1)] \times 350\,\text{nsec}$

$\Rightarrow 2003 \times 350 \times 10^{-9}\,\text{sec} \Rightarrow 701.05 \times 10^{-6}$

Q.3

Assume a 5-segment single cycle processor (non-pipelined) and a 5-segment pipelined processor. Cycle time of non-pipelined processor is 10 times that of pipelined processor. Assume also that there are no stalls in the pipelined processor then what is the speed up achieved over non-pipelined processor if pipelined processor phase time is 2ns?

[MCQ]

A. 5

B. 10

C. 15

D. 20

Ans (B)

In Pipeline Processor. Cycle time = 2ns.

Cycle time of Non pipeline processor is

10 times more that of Pipeline Processor.

In Nonpipeline Processor Cycle time[tn] = 2×10 = 20nsec

$$S = \frac{tn}{tp} = \frac{20}{2} = 10$$ Ans

Q.4

Consider a pipelined machine X operating at 1 GHz that has speed up factor of 5 and operating upto 60% efficiency, then how many segments are present in the machine X? ____

[MCQ]

A. 4

B. 6

C. 7

D. 9

$$\eta = \frac{S}{k}$$

η : efficiency
S : speed up Factor
k : Number of Stages

$$60\% = \frac{5}{k}$$

$$k = \frac{5}{60} \times 100 = \frac{50}{6} = 8.33$$

9 Ans

Ans (D)

Q.5

Consider a machine with frequencies of instruction, type of instructions, and cycles. Given below.

	Instruction type	Frequency	Cycles
1	Load	40%	1
2	Store	15%	2
3	Branch	20%	2
4	ALU	25%	2

What is the average CPI?

[MCQ]

A. 2.0

B. 1.5

C. 1.6

D. 3.0

Ans (C)

$$CPI = \frac{\left(\sum_{i=1} IC_i \times CPI_i\right)}{\#Instn}$$

$$\text{Avg CPI} = .40 \times 1 + .15 \times 2 + .20 \times 2 + .25 \times 2$$

$$\Rightarrow 0.40 + 0.30 + 0.40 + 0.50$$

CPI = 1.60 Avg

1.6 cycle [Assume 1 GHz cycle time 1 nsec]

ET = 1.6 × 1 nsec

= 1.6 nsec

Q.6

Consider 5 stage of two processors x and y have the following latencies:

Type	IF	ID	EX	MA	WB
x	400	500	450	650	200
y	300	250	200	290	240

Also consider that each pipeline costs 20ps extra for the register between pipeline stages. Which of the following pairs of tuples represent the cycle time, latency of one instruction and the throughput for a pipelined processor for both types x and y? [MCQ]

X: 400 500 450 650 200

y: 300 250 200 290 240

Buffer / Register Delay = 20 PS.

$t_{P_x} = \max(\text{Stage Delay} + \text{Buffer Delay})$

$t_{P_x} = 650 + 20$

$\boxed{t_{P_x} = 670 \text{ PS}}$

$t_{P_y} = \max[\text{Stage Delay} + \text{Buffer Delay}]$

$300 + 20$

$\boxed{t_{P_y} = 320 \text{ PS}}$

$k = 5, \; n = 1$

ET of 1 Instn in Pipeline P_x

$ET_x = [k + (n-1)] t_{P_x}$

$\Rightarrow [5 + (1-1)] \times 670 \Rightarrow 5 \times 670$

$\boxed{ET_x = 3350 \text{ PS}.}$

ET of 1 Instn in Pipeline for P_y

$ET_y = [k + (n-1)] t_{P_y}$

$= [5 + (1-1)] \times 320 \text{ PS} = 5 \times 320 \text{ PS}$

$\boxed{ET_y = 1600 \text{ PS}}$

$$\text{Throughput}_x = \frac{1}{t_{P_x}} = \frac{1}{670}$$

$$\text{Throughput}_y = \frac{1}{t_{P_y}} = \frac{1}{320}$$

(X)

670, 3350, $\frac{1}{670}$

(y)

320, 1600, $\frac{1}{320}$.

x y

A. $\left(670,3350,\frac{1}{670}\right)\left(320,1600,\frac{1}{320}\right)$

B. $\left(670,3350,\frac{1}{3350}\right)\left(320,1600,\frac{1}{1600}\right)$

C. $\left(3350,670,\frac{1}{3350}\right)\left(1600,320,\frac{1}{1600}\right)$

D. None of the above

Ans (A)

Q.7

Consider the sequence of instruction and a 5-stage pipeline (IF, ID, EX, MEM, and WB).

	Opcode	Destination	Source1	Source 2
I_1:	ADD	R_2	R_3	R_4 (1^{st} instruction to enter the pipeline)
I_2:	SUB	R_3	R_4	R_2
I_3:	MUL	R_2	R_3	R_4(last instruction to enter the pipeline)

How many RAW data hazards does the ID stage need to detect for this instruction sequence? [MCQ]

A. 1

B. 2

C. 3

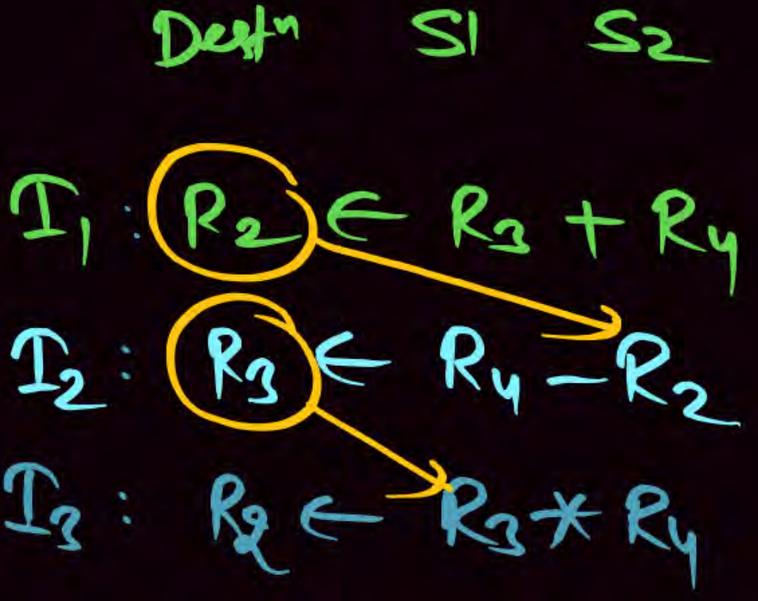
D. 4

Ans (B).

Data Hazard | Data Dependency

1. RAW Hazards | True Data Dep.
2. WAR Hazards | Anti Dep.
3. WAW Hazards | Output Dep.

But in the Question asking Only RAW Data Hazards.



RAW (True Data Dep.) = $I_2 - I_1$, $I_3 - I_2$ ②

Q.8

Consider a 5-stage pipelined processor having instruction fetch (IF), instruction decode (ID), instruction execution (IE), memory access (MA) and write back (WB) segments. The segments mentioned takes 1 clock cycle each for any instructions. Consider the given code fragment below.

Operand Fetch

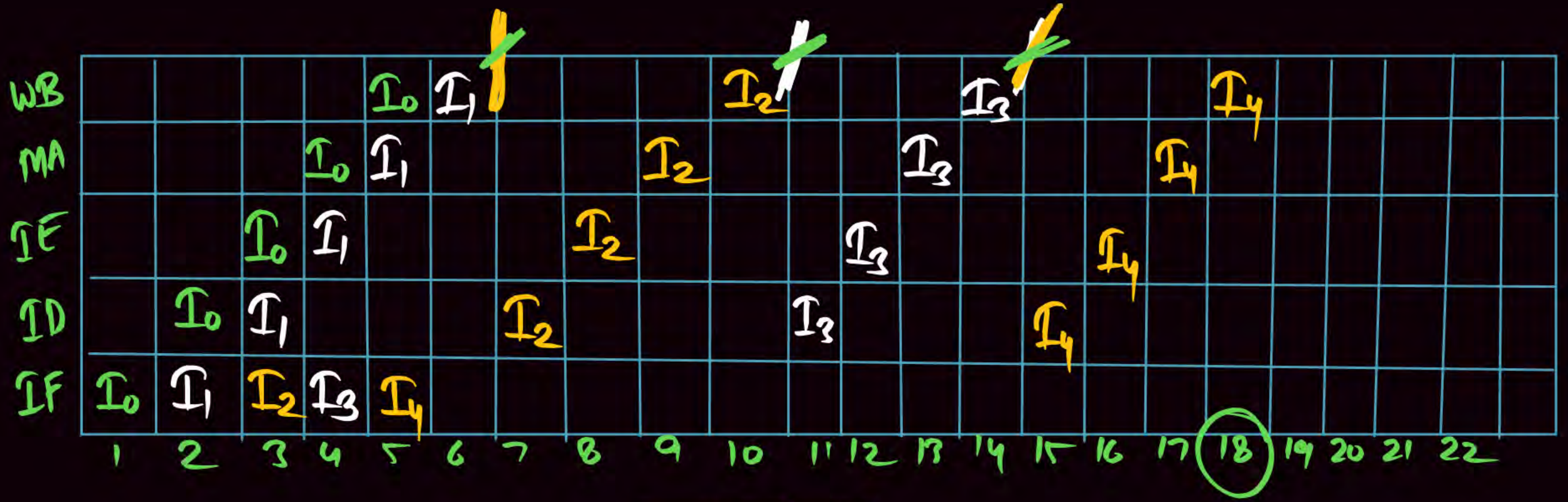
Instruction	Meaning of instruction
I_0: load R_2, [100]	$//R_2 = MEM[100]$
I_1: load R_4, 5[R_3]	$//R_4 = MEM[R_3 + 5]$
I_2: MUL R_5, R_2, R_4	$//R_5 = R_2 * R_4$
I_3: DIV R_6, R_2, R_5	$//R_6 = R_2 / R_5$
I_4: SUB R_7, R_5, R_6	$//R_7 = R_5 - R_6$

Avg (IB)

What is the number of clock cycle needed to execute the above sequence of instruction?

[MSQ]

NAT


WB
MA
IE
ID
IF
I0 I1 I2 I3 I4
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

Ans (18)


THANK YOU GW
SOLDIERS !