COMPUTER SCIENCE

Computer Organization and Architecture

Introduction of COA

Lecture_05

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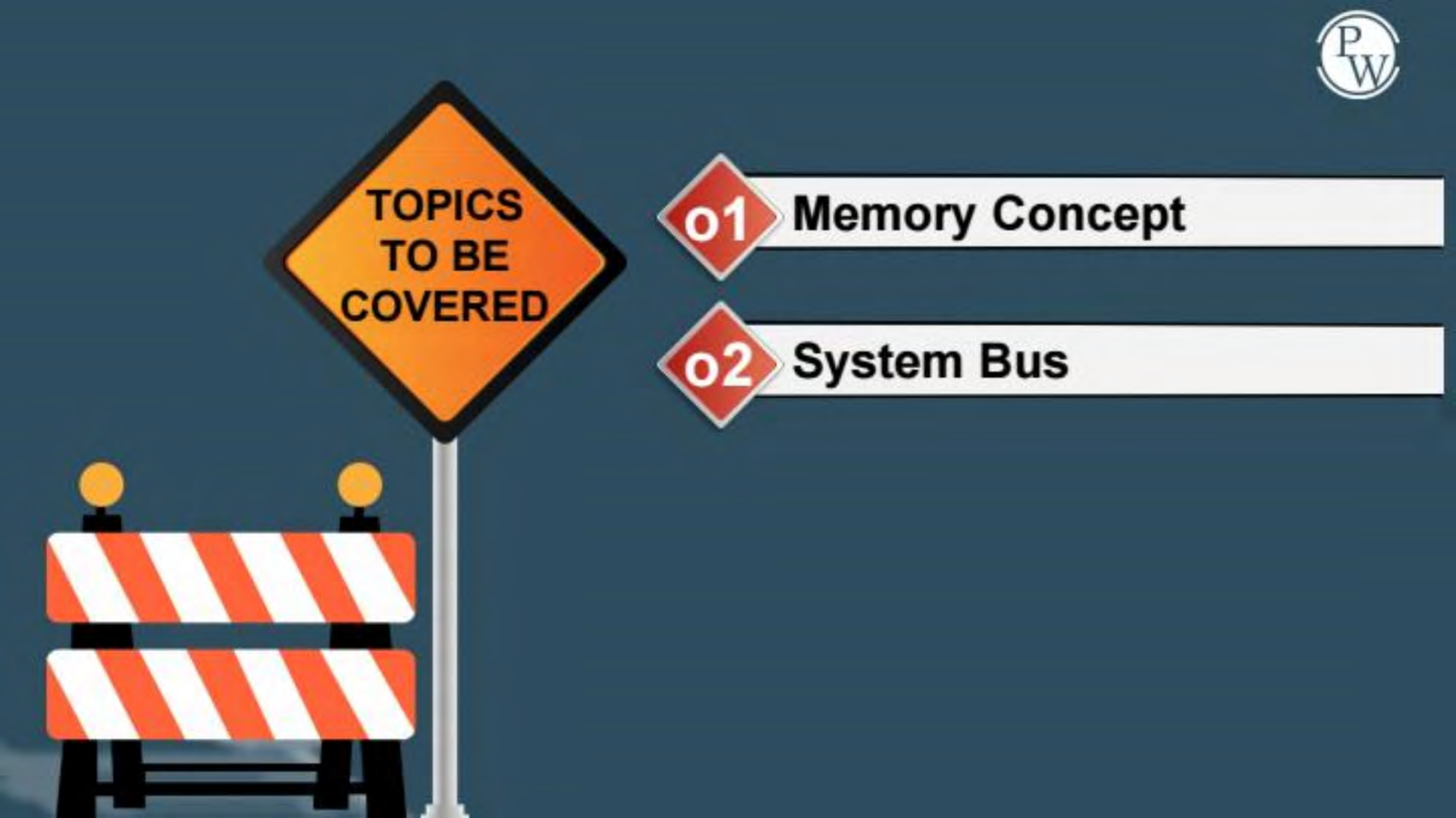


01 Memory Concept

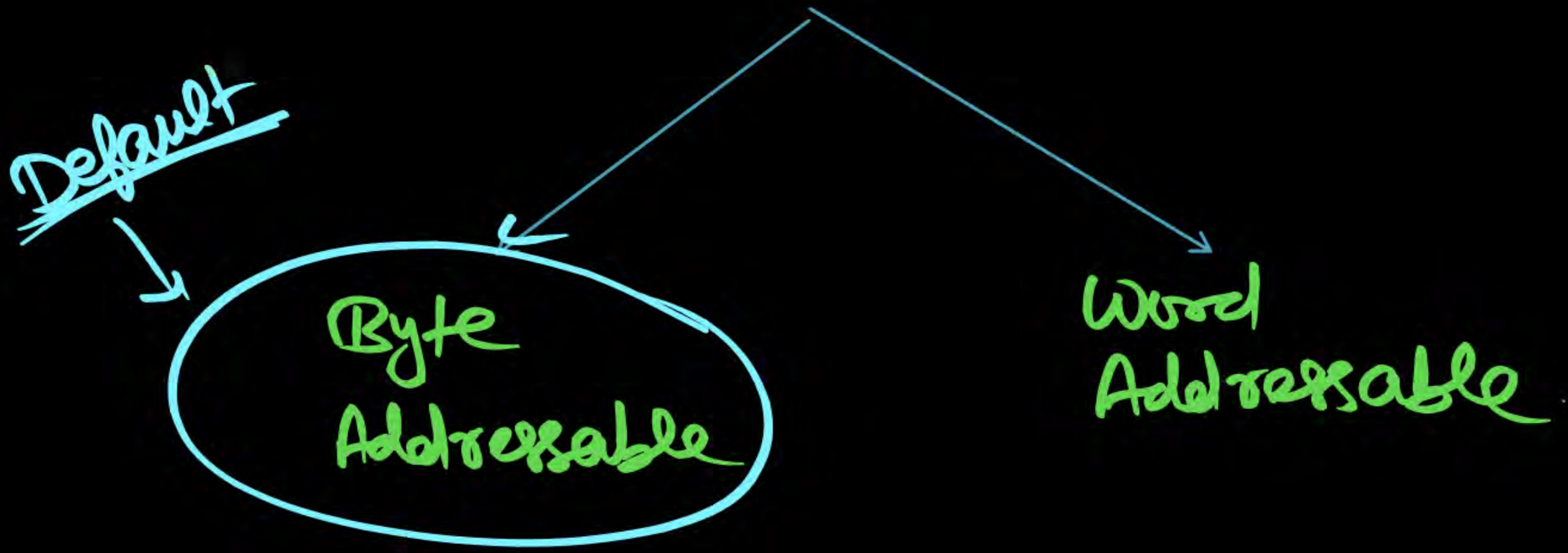
02 System Bus

Memory Concept:

$2^n \times m$

n: # Address line [A.L]

m: # Data Line [D.L]


Default
Byte Addressable
Word Addressable

	Byte	Word (word length)
8bit Processor	8 bit	8bit
16 bit Processor	8bit	16bit
32 bit Processor	8bit	32bit
64 bit Processor	8bit	64 bit
n bit Processor.	8bit	n bit.

Byte ⟶ Word

Word ⟶ Byte.

1 Word Size given in Question.

Q1 Memory Size 4G Byte then Size of Address line ?

Soln

4G Byte.

$2^{2^{30}}$ Byte

2^{32} Byte

Address = 32 bit. Ans

Q.2 Memory Size 4GByte, memory is Word Addressable (1 Word Consist 2 Byte) the Size of address line ?

Sol^n 2 4GByte [Word Addressable]

1 Word = 2 Byte

$\frac{4GByte}{2Byte}$ Words $\Rightarrow$ 2G Words.

$\Rightarrow 2 \cdot 2^{30} W \Rightarrow 2^{31} W \Rightarrow$ A.L = 31 bit

Ans

Pins : Processor Contain Set of Hardware Pins to Perform the operations.

1. Active Low Pins.
2. Active High Pins.
3. Dual Pin
4. Time Multiplexed Pin.

① Active Low Pin : This Pin is Enabled when the Input is '0' (or) Clock Pulse is in Low State.

It's Denoted as Pinname.

(eg) $\overline{RD}$, $\overline{WR}$ etc.

② Active High Pins : This Pin is Enabled when the Input is '1' (or) Clock Pulse is in High State.

(eg) INTR, HLDA, ALE.

③ Dual Pins : (eg) $M/\overline{IO}$

1 : then Memory operation (Read (or) write)

0 : then IO operation (IO Read (or) IO write)

④ Time Multiplexed Pins: This Pin carries the Multiple Meaning but one only at a time.

Address Pins are Time Multiplexed with Data Pin to Carry the Address & Data. (But only one at a time.)

eg In 8085 Processor.

$AD_0 - AD_7$

Address

Data.

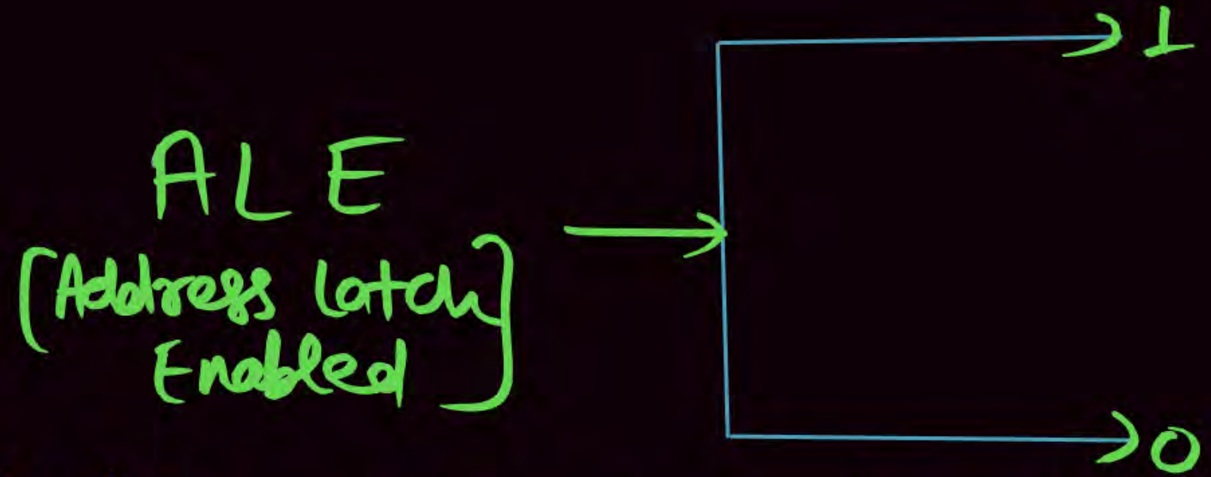
eg In 8086 Processor.

$AD_0 - AD_{15}$

Address

Data.

Like In 8085 AD_0-AD_7; Address Pins are Time Multiplexed with Data Pin to Carry the Data But Only one at a time.



Time Multiplexed Pin Carries the Address.

Time Multiplexed Pin Carries the Data.

Advantage: Number of Hardware Pins Reduced.

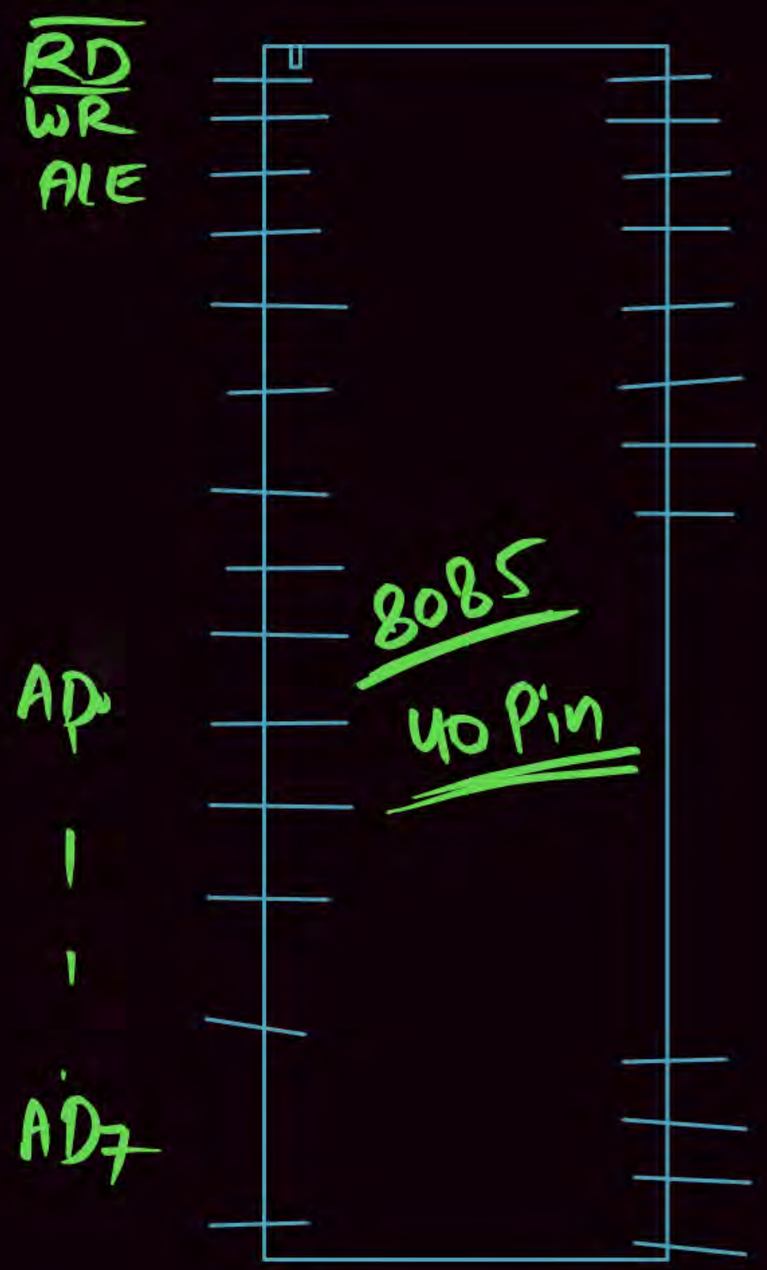
In 8085

$AD_0 - AD_7$

⇓

if ALE = 1 ⇒ Carries Address

if ALE = 0 ⇒ Carries Data.



System Bus

System Bus Contain 3 Category of Lines.

1. Address line [A.L]
2. Data line [D.L]
3. Control line [C.L]

System Bus

① Address line [A.L] : Address Lines are used to Carry the Address Towards Memory & I/O [Unidirectional]

Note Based on Address line we Can Determine Capacity of the Memory

Eg In 8085 Processor.

$AD_0 - AD_7$ & $A_8 - A_{15}$

Address = 16 bit

$\Rightarrow 2^{16}$ Cells

$\Rightarrow$ 64K Cells

$\Rightarrow$ 64KB.

Eg In 8086 Processor.

$AD_0 - AD_{15}$ & $A_{16} - A_{19}$

Address = 20 bit

2^{20} Cells

1MCells.

System Bus

② DATA Lines (D.L) :

Data line are used to Carry the Data (Bidirectional)

Based on the Data line we can Determine the Word length of the CPU. (Processor).

The Performance of the Processor is measured by Word length of the CPU.

(eg) In 8085

$AD_0 - AD_7$

Word length = 8 bit

Operation Performed on 8 bit Data format.

(eg) In 8086

$AD_0 - AD_{15}$

Word length = 16 bit

Operation Performed on 16 bit Data Format.

∴

System Bus

③ Control Lines :
- Carries the Control Signal
- Unidirectional (individually)

System Bus

Q.1 64K x 8

64K → 64K memory cells (2^{16} cells)

8 → each cell size / size of each word

16 bit Required to Represent Any of the cells.

Width of Address bus = $\lceil \log_2 \text{Memory Size} \rceil \Rightarrow \lceil \log_2 64K \rceil = 16$ bit

Width of Data bus = 8 bit

64K x 8

$2^{16} \times 8$

A.L = 16 bit

D.L = 8 bit

System Bus

Q.2 64K x 16.

64K memory cells (2^{16} cells) → 16 bit Required to Represent Any of the cells.

16 → each cell Size / Size of each word

64K x 16

2^{16} x 16

A.L = 16 bit

D.L = 16 bit

Width of Address bus = $\lceil \log_2 \text{Memory Size} \rceil \Rightarrow \lceil \log_2 64K \rceil = 16$ bit

Width of Data bus = 16 bit.

System Bus

Q.3 $4G \times 32$.

Width of Address Bus = 32 bit

Width of Data Bus = 32 bit

System Bus

Q.4 2G X 64

Width of Address Bus = 31 bit

Width of Data Bus = 64 bit

16 bit Processor

Data line = 16

Data Bus = 16

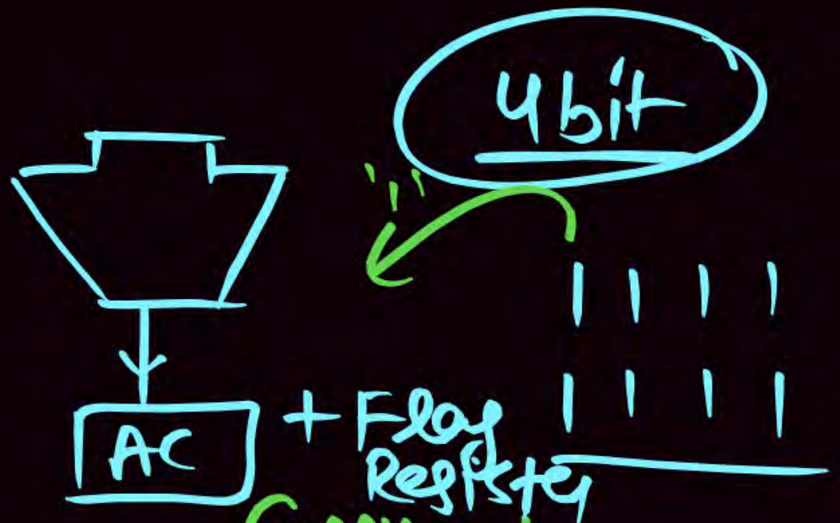
Word Size = 16

ALU = 16

AC = 16

MBR/MDR = 16

Registers = 16.



PSW [Program Status Flag]

① Carry ② Parity ③ Auxilliary Carry ④ Sign ⑤ zero ⑥ overflow.

32 bit Processor.

Data line = 32 bit

Data Bus = 32 bit

Word Size = 32 bit

ALU = 32 bit

AC = 32 bit

DR/MBR/MDR = 32 bit

Registers = 32 bit

4096 x 16 → Data Line.

- Data line = 16bit
- Data Bus = 16bit
- Word Size = 16bit

- ALU = 16bit
- AC = 16bit
- DR/MBR/MDR = 16bit
- Registers = 16bit

Memory 4096 words
16bit Per word.

4096 x 16 → D.L

2^{12} x 16

Address = 12bit

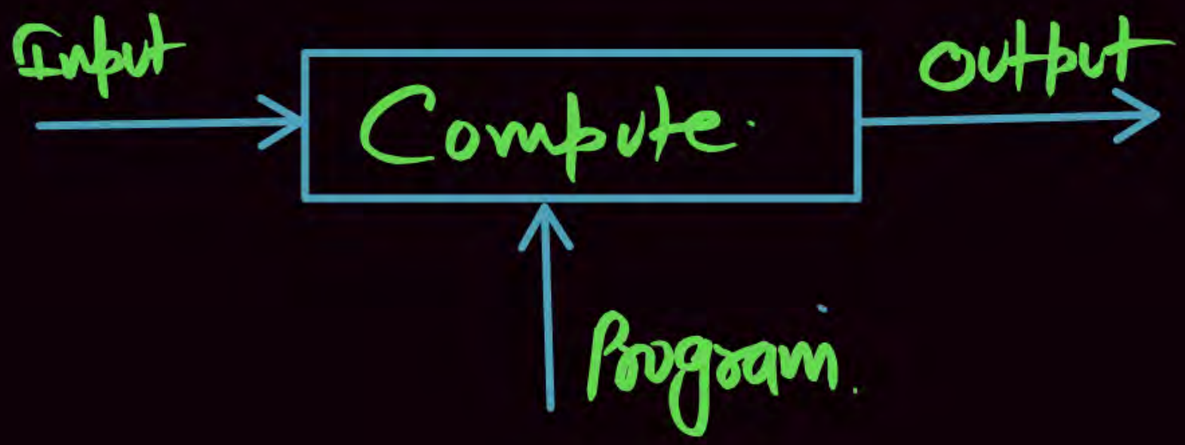
Data = 16bit

AR/MAR = 12bit

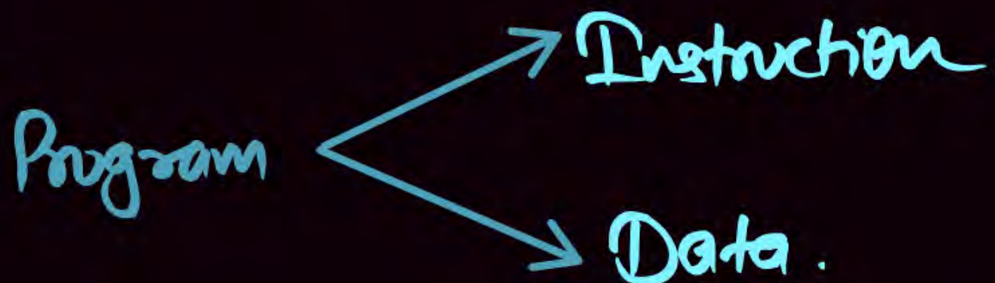
PC = 12bit

IR = 16bit.

Computer: Computer is a Computational Device used to Process the Data Under the Control of Program.



Program: Sequence (set) of Instruction along with Data.



Instruction: It is a binary sequence (code) which is designed inside the Processor to perform the operation.

Instruction is a Set (Sequence) (OR) of binary bits to Instruct the Computer to perform the operations.

(OR)

Binary bits — Bind with — operation.

Assume in Processor

(9). 0110 → ADD.

1011 → MUL.

Microprocessor Lab.

Booklet

OPCODE : 5bit

ADD : 01011

DATA : Binary

Data: Data is Binary Sequence bind with the Value (Data format BCD, Hex, etc).

4 bit in Binary

2 : 0010

11 : 1011

2 Type of Architecture.

1. Von Neumann Architecture

2. Harvard Architecture.

Computer Works on STORED Program Concept.

Vonn Neumann Architecture. (Stored Program Concept)

- Main Memory Contain the Instruction & Data.
- ALU operating on Binary Data.
- Control Unit Interpreteing the Instruction from Memory & Executing.
- Input / Output Equipment operated by Control Unit.

THANK YOU!