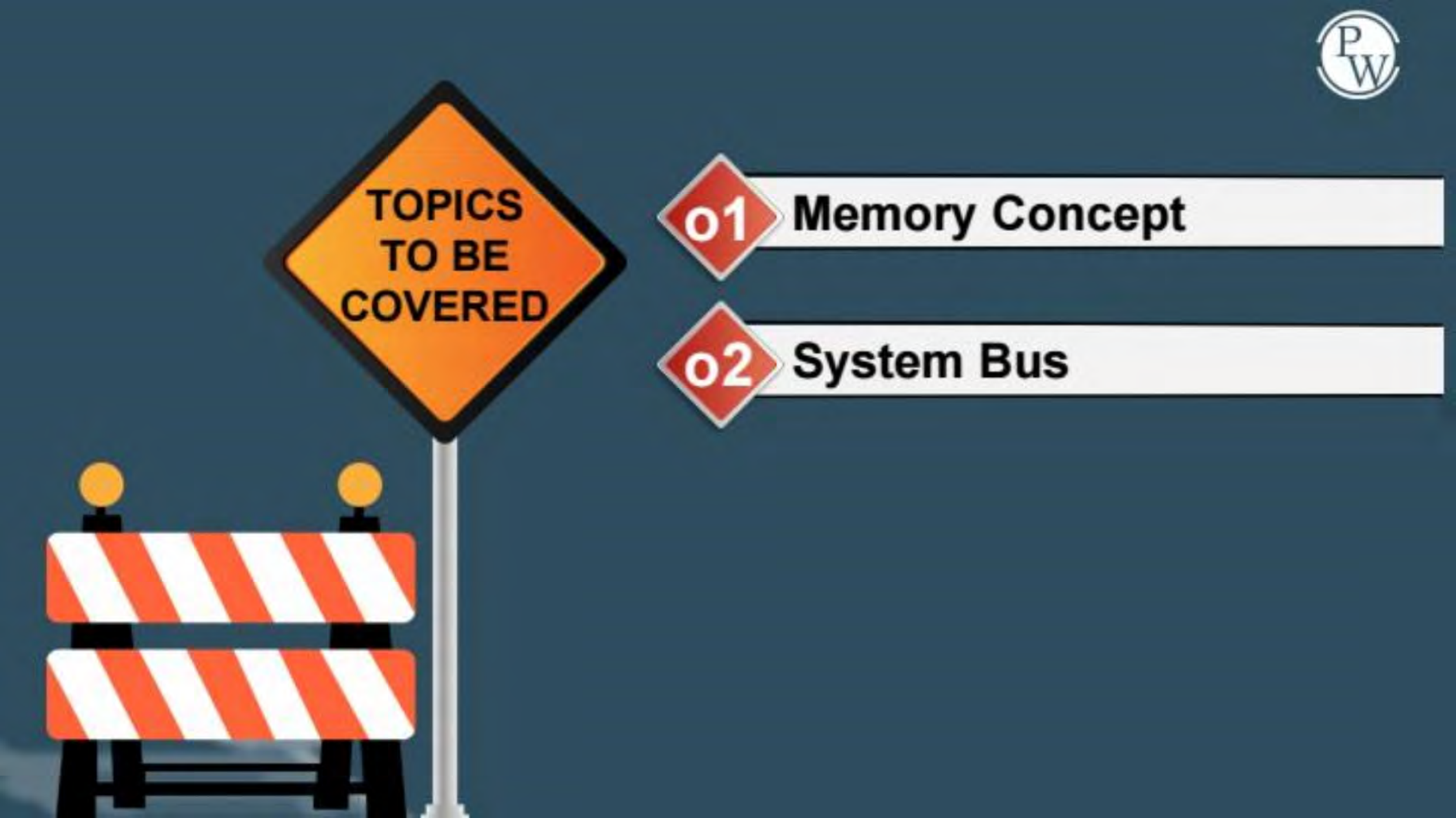
COMPUTER SCIENCE

Computer Organization and Architecture

Introduction of COA

Lecture_04

Vijay Agarwal sir



01 Memory Concept

02 System Bus

Introduction of COA

Generation

CO & CA

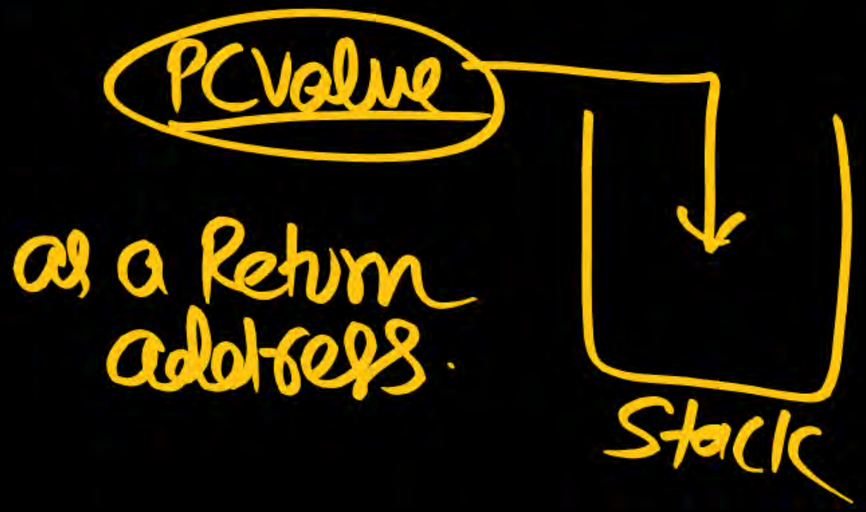
Component of the Computer

- CPU
- Memory
- I/O

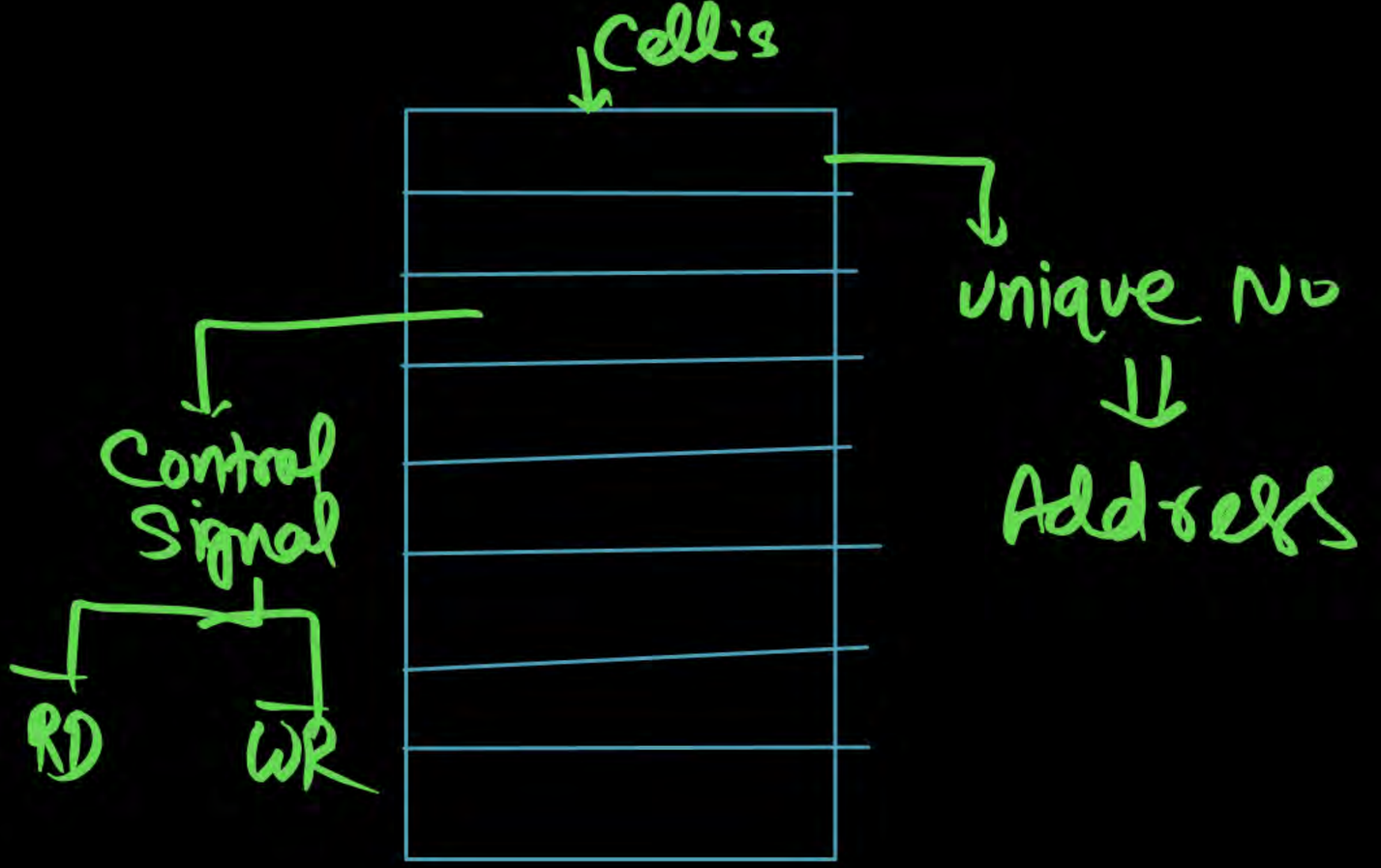
Instruction cycle.

1. Fetch cycle [Mem to CPU(IR)]
2. Execute cycle

Instruction cycle with Interrupt



Memory



$2^n \times m$

n: # of Address line (A.L)

m: # of Data line (D.L)

Address line Capacity of memory cells.

Ex: 1K Byte

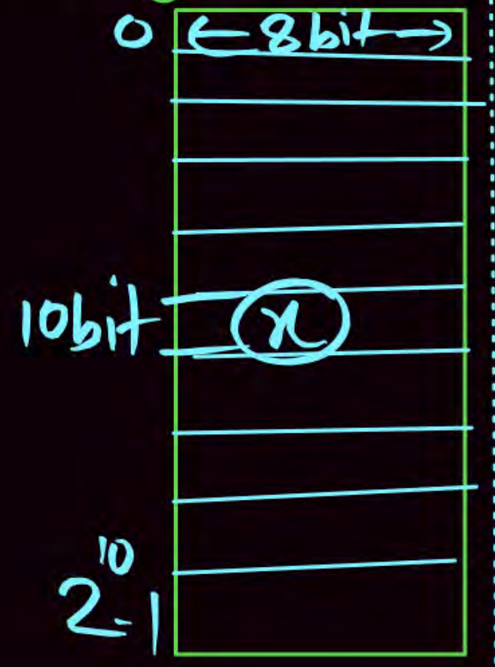
$2^{10} \times 8$ bit

10bit Address line (A.L)

8 bit Data line (D.L)

2^{10} Memory Cells are Present.

10bit Address Required to Represent any cell.



N x m

N: # Memory Cells.

m: # Data line.

Ex: 1K Byte

$2^{10} \times 8$ bit

N: 2^{10} [1024] Cells [0-1023]

m: 8 bit.

eg 50

$\downarrow\downarrow$

$\lceil \log_2 50 \rceil$

$\downarrow\downarrow$

6 bit

$50 = 2^n$

$n = 6$ bit Ans

$2^1 = 2$ [0-1]

$2^2 = 4$ [0-3]

$2^3 = 8$ [0-7]

$2^4 = 16$ [0-15]

$2^5 = 32$ [0-31]

$2^6 = 64$ [0-63]

$2^7 = 128$

$2^8 = 256$

$2^9 = 512$

$2^{10} = 1024$

$2^{10} = 1K$

$2^{20} = 1M$

$2^{30} = 1G$

$2^{40} = 1T$.

① 70 $= 2^n = 7$ bit

② 110 = 7bit

③ 38 = 6bit

④ 45 = 6bit

⑤ 51 = 6bit

⑥ 90 = 7bit

⑦ 32 = 5bit

( )$_{16}$ or 0x

Hexa Decimal

0x 00000 0

1MByte.

2^{20} x 8bit

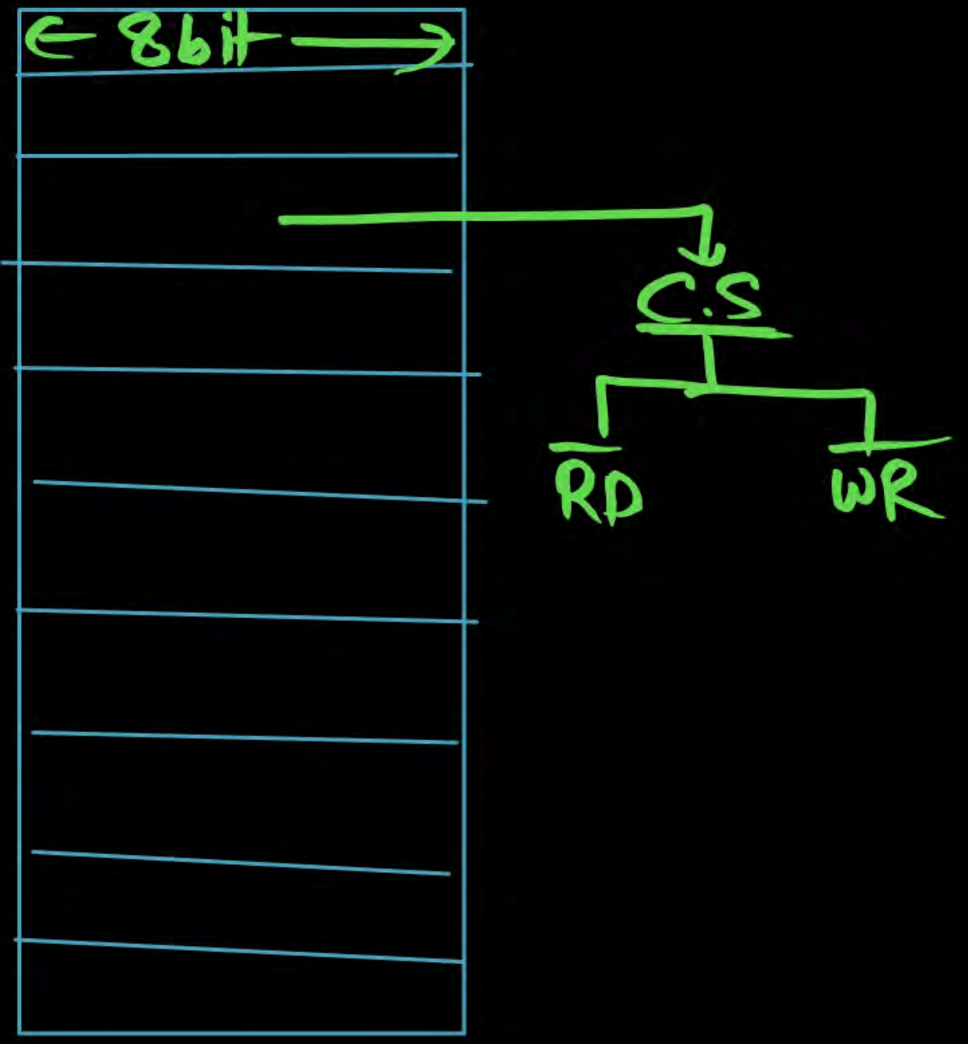
20 bit Address line

8 bit Data line.

2^{20} Memory cells.

20 bit Address Required to Represent Any Cell.

FFFFF$_{2^{20}-1}$



$2^6 \cdot 2^{10}$

64KByte

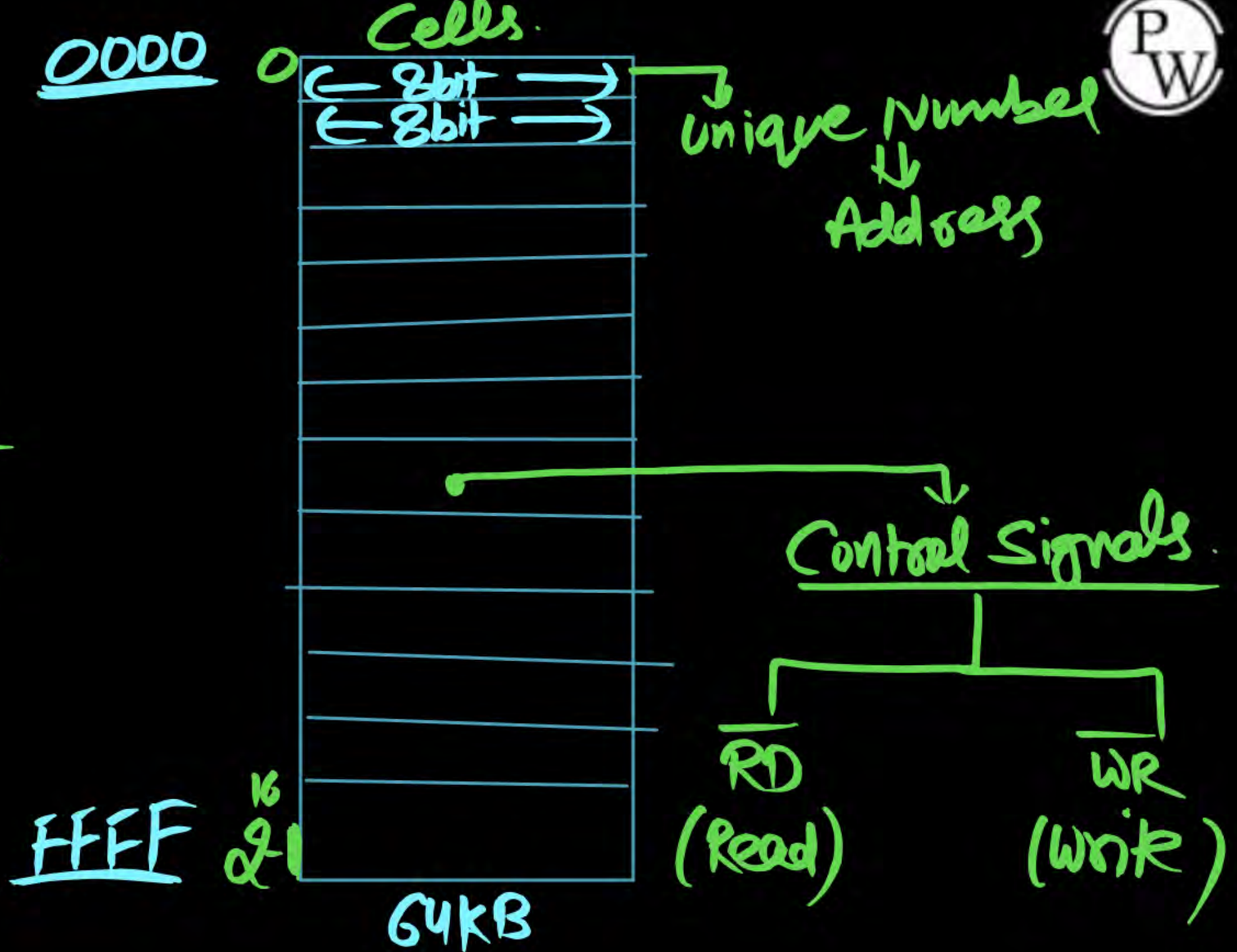
$2^{16} \times 8bit$

16 bit Address line

8 bit Data line.

2^{16} Memory Cells.

16 bit A.L Required to Represent any Cells.



8bit

8 Byte

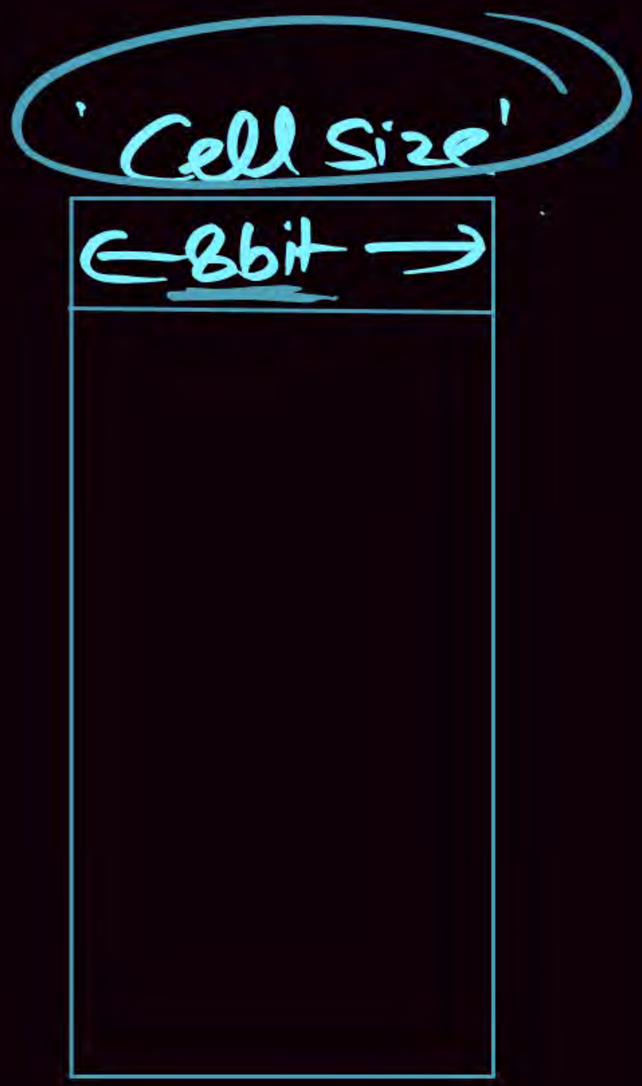
16 Byte

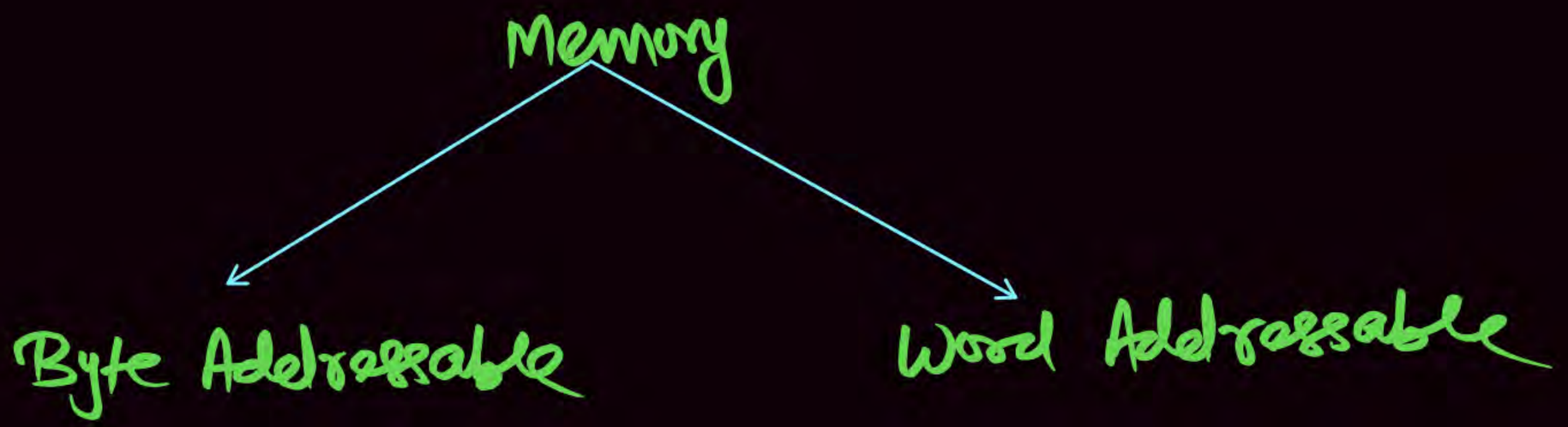
1k Byte

1m Byte

4G Byte

16G Byte

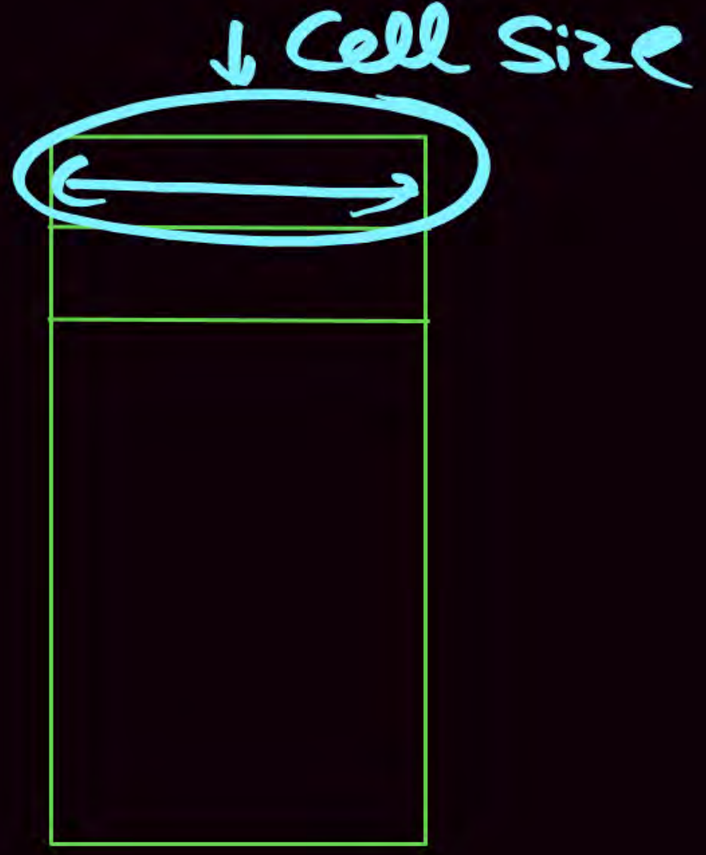



Memory
Byte Addressable
Word Addressable

Based on the Cell Size Memory Configuration is Divided into 2 Type.

① Byte addressable Memory.

② Word Addressable Memory.



① Byte Addressable Memory : When the Cell Size is '8bit' then Corresponding address is Called Byte addressable Memory.

eg

(2^2) 4 × 8 ; 2 bit Address

(2^4) 16 × 8 ; 4 bit ''

(2^6) 64 × 8 ; 6 bit ''

(2^8) 256 × 8 ; 8 bit ''

(2^{10}) 1K × 8 ; 10 bit ''

(2^{20}) 1M × 8 ; 20 bit ''

(2^{30}) 1G × 8 ; 30 bit ''

(2^n) 2^n × 8 ; n bit Address

Byte address (Cell size is 8 bit)

② Word Addressable Memory : When the Cell Size is given in the form of Words [Word Length] then Corresponding Address is Word Addressable Memory

Eg

(2^2) 4 × W : 2 bit Address

(2^4) 16 × W : 4 bit

(2^6) 64 × W : 6 bit

(2^8) 256 × W : 8 bit

(2^{10}) 1K × W : 10 bit

(2^{20}) 1M × W : 20 bit

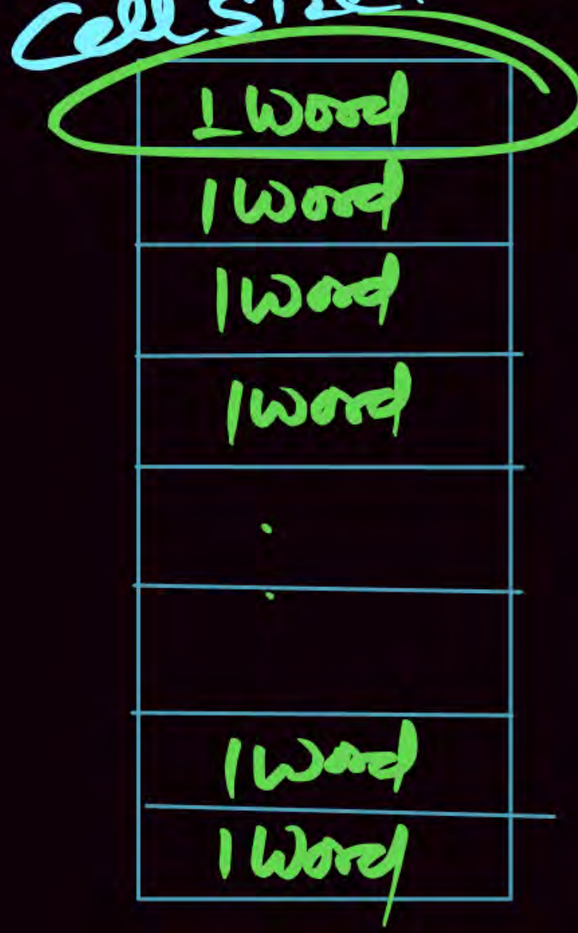
(2^{30}) 1G × W : 30 bit

(2^n) 2^n × W : n bit Address

Word Addressable

(W : Word)

Cell Size Must be a Word.



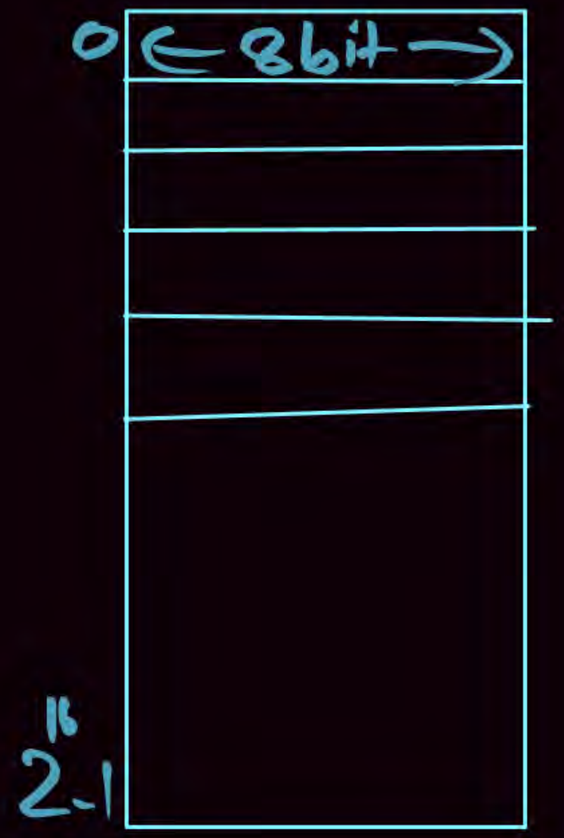
[B]

Microprocessor(up)	Byte Addressable	Word Addressable
① 8bit Processor	8bit	8bit
② 16bit Processor	8bit	16bit
③ 32bit Processor	8bit	32bit
④ 64bit Processor	8bit	64bit
⑤ n bit Processor	8bit	n bit

1 Word = Word Length

unique meaning
⇓
No Ambiguity.

Multiple meaning
⇓
Ambiguity.



64KB

$2^{16} \times$ Byte

$\Downarrow$

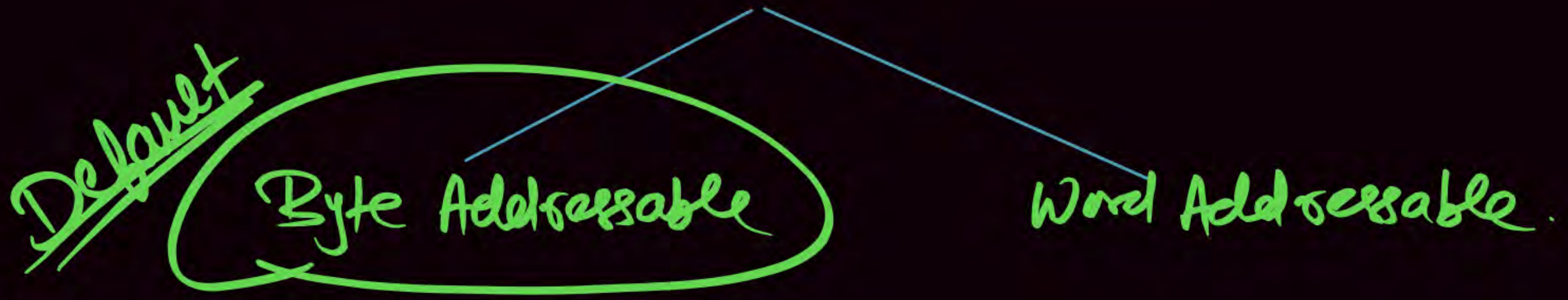
$2^{16} \times$ 8bit

64K Words.

$2^{16} \times$ Word.

$\Downarrow$

$2^{16} \times$?


Default
Byte Addressable
Word Addressable.

Note

(Data type in Memory is Byte)

Default Configuration in Memory is Byte Addressable

So in the Memory Data always Stored Byte Wise.

Note

Default Data type in the CPU is Word. So operations are performed on a CPU Based on Word format.

Note

So to Synchronize the Memory Data (Byte) type with a CPU Data type (Word) Memory interfacing will be adjusted by the designeer According to the Word Length of the CPU. To Access the Data from Memory to CPU in the form of words.

(eg) 16 bit Processor.

Word Length = 16 bit

Operation are performed on 16 bit Data.

(eg) 32 bit Processor.

Word Length = 32 bit

∴ operation are performed on 32 bit Data.

(eg) 64 bit Processor.

Word Length = 64 bit

∴ operation performed on 64 bit Data.

8086

① 16 bit Processor.

MOV Ax [1000]

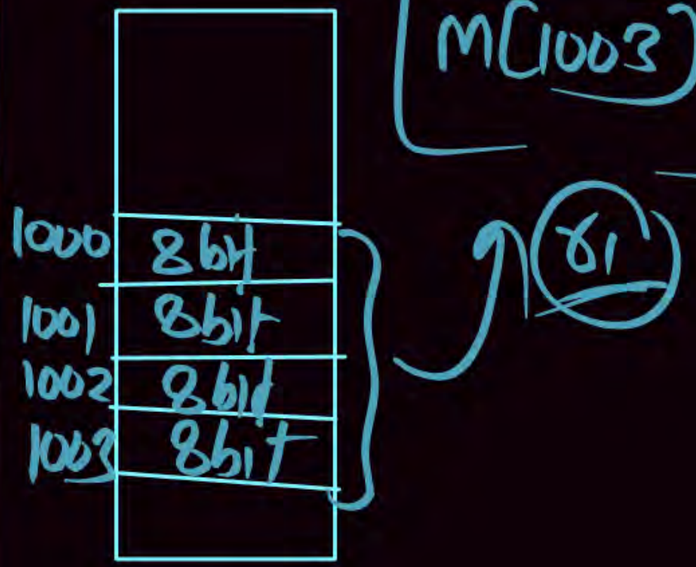
↑ OPCODE ↑ Destination ↑ Source.

Ax ← [M[1000] M[1001]]

32bit Processor

MOV R1 [1000]

R1 ← [M[1000] M[1001] M[1002] M[1003]]



16bit Processor

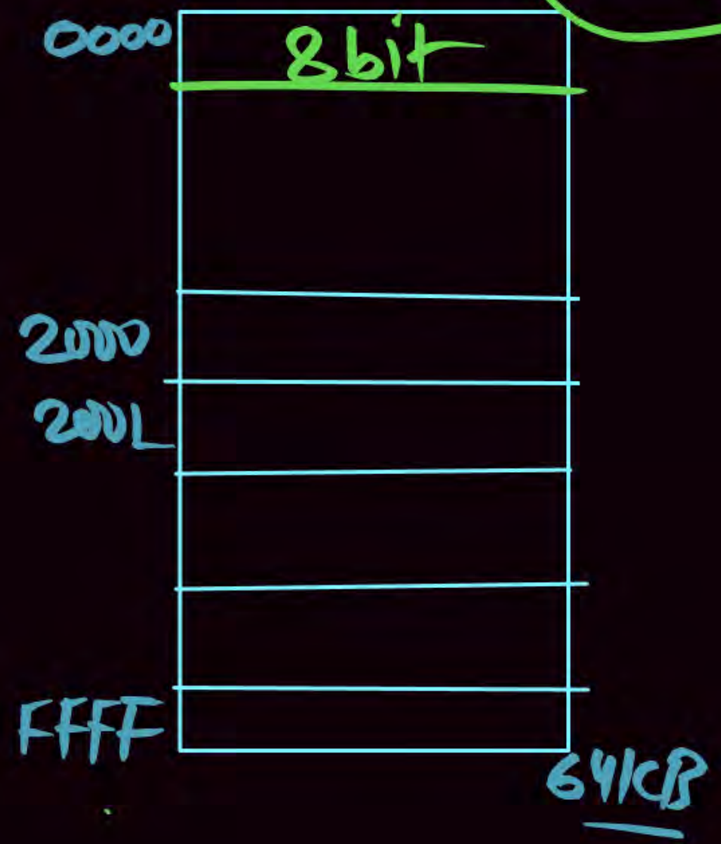
≤ 2Byte

Little Endian
Big Endian

(eg) Mov Ax [2000]

Ax ! Register

Ax ← [M[2000] M[2001]]



32bit Processor.

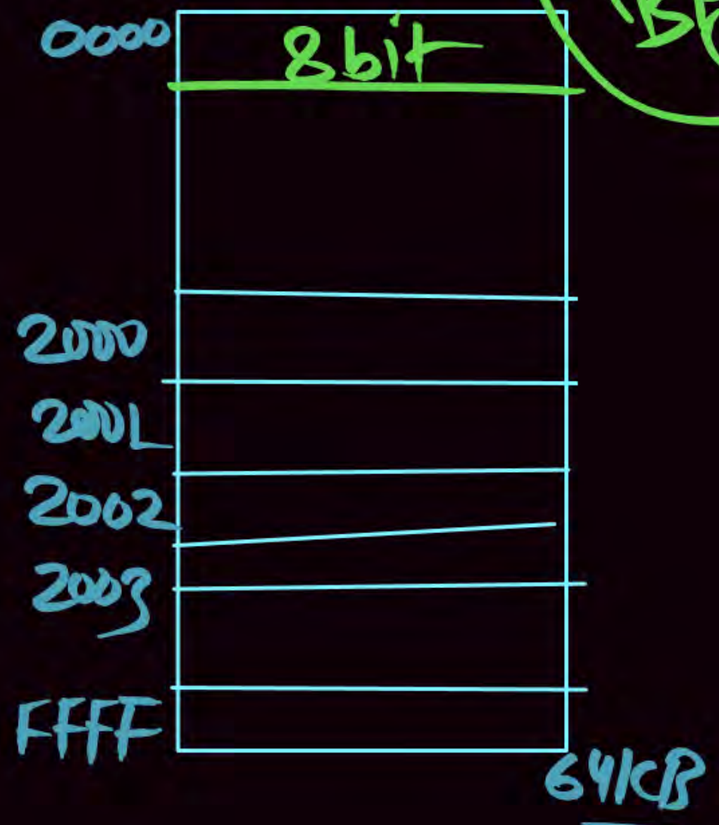
≈ 4Byte.

Little Endian
Big Endian

e.g. MOV r0 [2000]

A: Register.

r0 ← [M[2000] M[2001] M[2002] M[2003]]



Q. The Capacity of a memory unit is defined by the Number of word Multiplied by the number of bits/word. How many separate address and data lines are needed for a memory of 64K×16?

(a) 8 address, 8 data line

(b) 16 address, 8 Data line

(c) 15 address, 16 Data line

(d) 16 address, 16 Data line

$2^{16} \times 16$.

16 bit A.L.

16 bit D.L.

Q. Consider a system which has 1024 k words. Each word has the size of 32 bits then what is the capacity of memory in MB (Mega Byte) 4 Ans

1024 K word

$2^{10} \times 2^{10}$ Words

$2^{20} \times$ 4 Byte

4 MByte Ans

1 Word = 32 bit
≈ 4 Byte

Q. The Capacity of a memory unit is defined by the Number of word Multiplied by the number of bits/word. How many separate address and data lines are needed for a memory of 4K×16?

(a) 10 address, 16 data line
(b) 11 address, 8 Data line
(c) 12 address, 16 Data line
(d) 12 address, 12 Data line

[GATE-2 Marks]

4K x 16.

2^{12} x 16

12 bit Address line
16 bit Data line.

1km = 1000 meter.

Kilometer ⟶ Meter.

Meter ⟶ Kilometer (km)

If Word Size (word length) Given

Word ⟶ Byte.

Byte ⟶ Word.

Q. A processor can support a maximum memory of 4GB, where the memory is word-addressable (a word consists of two bytes). The size of the address bus of the processor is at least____ bits.

[GATE-2016]

$4\,GByte \Rightarrow 2^2 \cdot 2^{30}\,Byte$

$2^{32}\,Byte$

$\Downarrow$

Address = 32 bit

But Read Question Carefully.

Q. A processor can support a maximum memory of 4GB, where the memory is word-addressable (a word consists of two bytes). The size of the address bus of the processor is at least 31 bits. [GATE-2016]

4GByte.

Memory : Word Addressable.

4GB

2G × 2Byte / Word

$\frac{4GB}{2B}$ Words

1 Word = 2 Byte.

2 Byte ⇒ 1 Word

2G Words.

$2^1 . 2^{30}$ Words

2^{31} Word → 31 bit Ans

Ans (31).

1 Byte = 8 bit

4 Byte = 4 × 8 = 32 bit

OR

32 bit ≒ 4 Byte

1 Byte ≒ 8 bit

OR

8 bit ≒ 1 Byte

Q.

Consider a 32 bit Hypothetical processor which support 128 MByte memory. System is enhanced (New Design) with a word addressable memory. Then how many address lines are required in the new system?

128 MByte.

128 MByte

=

32M x 4Byte

32M Words

2^{25} Word ⇒ Address = 25 bit

New Design.

Word Addressable.

1 Word = 32 bit = 4 Byte.

1 Word = 4 Byte.

⇒ 4B = 1 Word

New Design
Word Addressable

Q.

Consider a 32 bit Hypothetical processor which support 128 MByte memory. System is enhanced (New Design) with a word addressable memory. Then how many address lines are required in the new system?

128 MByte.

New Design.
Word Addressable.

1 Word = 32 bit = 4 Byte.

1 Word = 4 Byte.

∵ 4B = 1 Word

128 MByte

New Design
Word Addressable

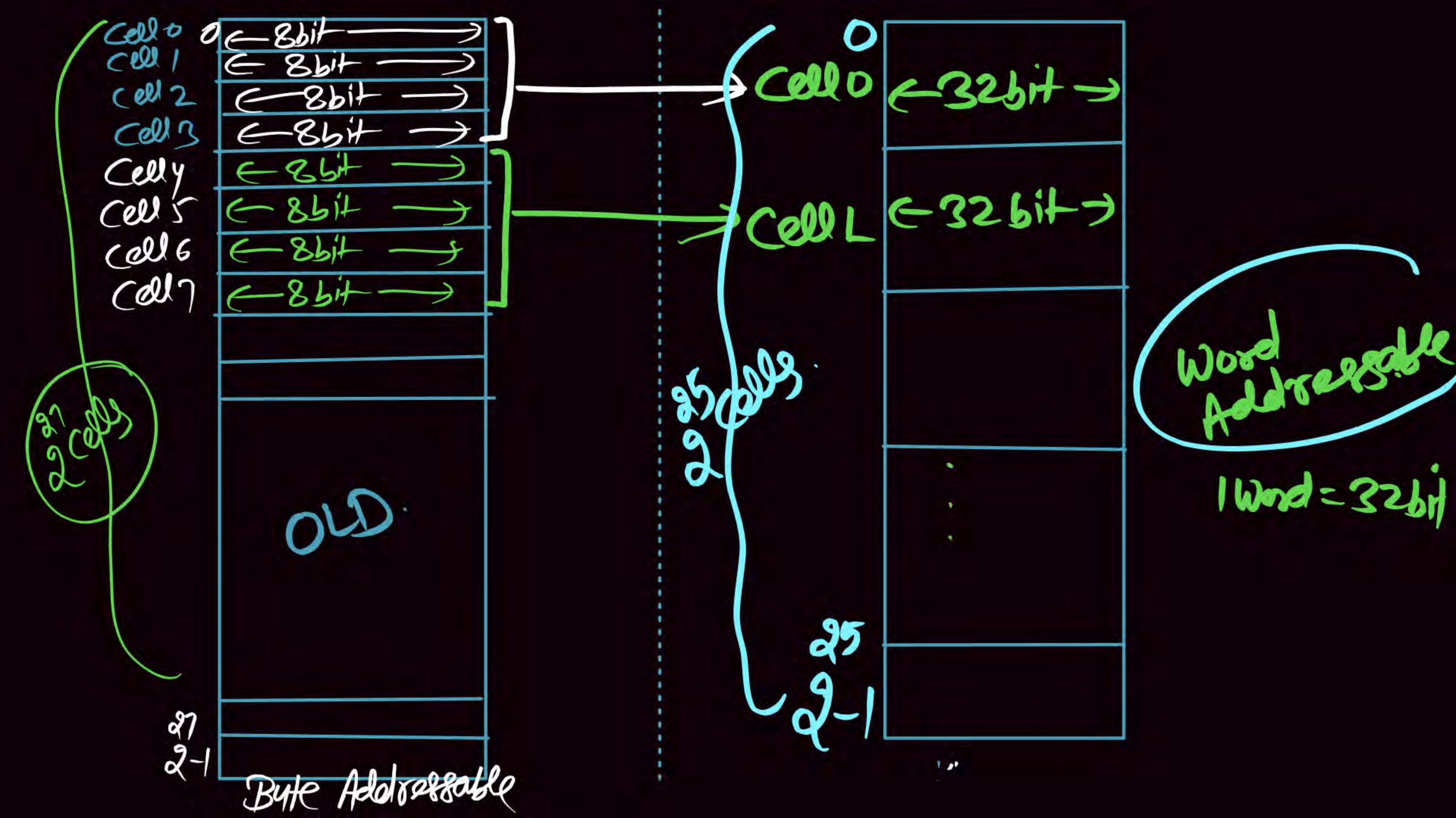
$\frac{128\ MB}{4B}$ Words

32 MWords.

$2^5 \cdot 2^{20}$ Word

2^{25} Words ⇒ Address = 25 bit

∴


Cell 0
Cell 1
Cell 2
Cell 3
Cell 4
Cell 5
Cell 6
Cell 7
0
8bit
8bit
8bit
8bit
8bit
8bit
8bit
8bit
2^{27} cells
OLD
$2^{27}-1$
Byte Addressable
0
Cell 0
32bit
Cell L
32bit
2^{25} cells
$2^{25}-1$
Word Addressable
1 Word = 32bit

2^{27} Cells

1 Cell = 8bit = 1Byte

2^{27} Byte

⇓

128 MByte

2^{25} Cells

1 Cells = 1 Word = 32bit = 4B

$2^{25} * 4$ Byte

2^{27} Byte

128 MByte

2^{25} Word

32M Word

Byte Addressable

2^{27} Byte [128 MB]

$2^{25} \times 2^2$ Byte

$2^{25} \times$ 4 Byte

2^{25} Words

or

32 M Word

Word Addressable

2^{25} Words. [32 M Words]

1 Word = 4 Byte.

$2^{25} \times$ 4 Byte

2^{27} Byte

128 M Byte

Q.

Consider a 64 bit Hypothetical processor which support 2G words memory. System is enhanced (New Design) with a Byte addressable memory. Then how many Extra address lines are required in the new system? 3bit

OLD Design

2G Words.

$2^1 \cdot 2^{30}$ Word

2^{31} words.

Address = 31 bit

Ans (3)

Q.

Consider a 64 bit Hypothetical processor which support 2G words memory. System is enhanced (New Design) with a Byte addressable memory. Then how many Extra address lines are required in the new system?

2G Words

New Design : Byte Addressable.

1 Word = 64 bit ⇒ 8 Byte.

1 Word = 8 Byte

2G Words ⇒ 2G * 8 Byte

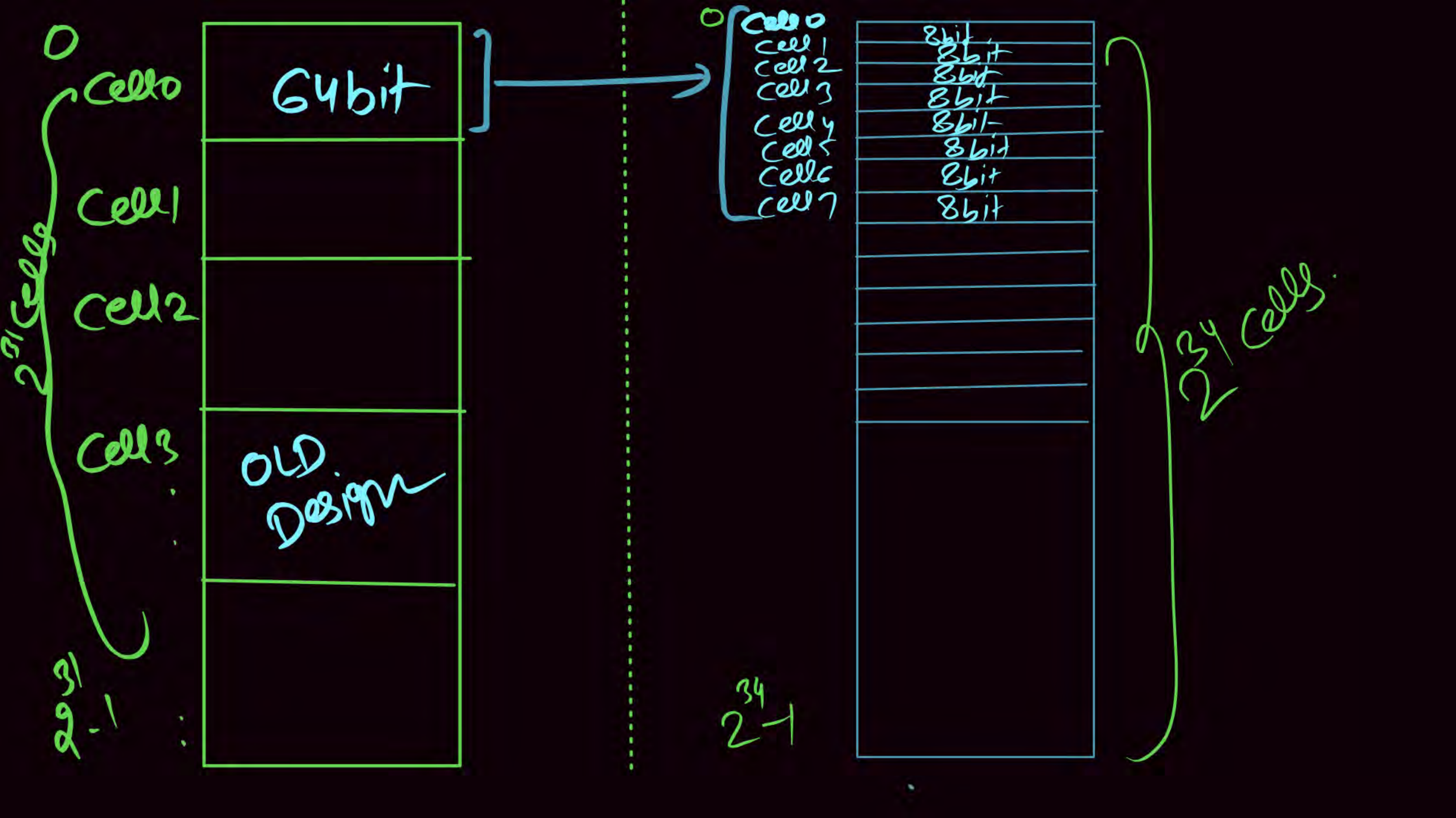
⇒ 16G Byte. ⇒ $2^{4} \cdot 2^{30}$ B

⇒ 2^{34} Byte ⇒ Address = 34 bit

Extra = 34 − 31

= 3 bit

Ans


0
Cell0
64bit
Cell1
Cell2
Cell3
OLD Design
2^{31} Cells
$2^{31}-1$
0
Cell 0
Cell 1
Cell 2
Cell 3
Cell 4
Cell 5
Cell 6
Cell 7
8bit
2^{34} Cells.
$2^{34}-1$

2G Words.

2^{31} Words.

1 Word = 8 Byte

$2^{31} \times 8$ Byte

$2^{31} \times 2^{3}$ Byte

2^{34} Byte

16 G Byte.

2^{34} Byte

1 Word = 8 Byte.

$\frac{16\text{ G Byte}}{8\text{ Byte}}$ Word

2G Words

2^{31} words

THANK YOU!