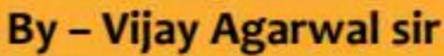
## CS & IT ENGINEERING

Computer Organization & Architecture

Secondary Memory & I/O Interface

**DDP** Discussion Notes









TOPICS TO BE COVERED

01 Question

02 Discussion

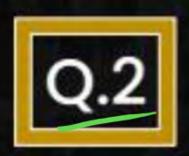


Which of the following is/are not the major functions for an IO woodule?



[MCQ]

- A. Control and timing
- B. Error détection
- c. Processor communication
- Single instruction multiple data stream (SIMD)



Consider a system with data transfer rate is 10 KBPS. Data are exchanged between the processor and I/O interface. The performance gain when IO device is operating under interrupt mode over programmed IO mode ) 6.66.

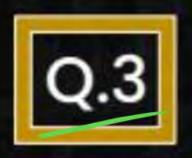
Note (Interrupt interface over head is 15 µsec) (round off 1 decimal places)



Programmed I/o: 10 KB þs 10k Sec = 154 sec = 100 mgec ETROGIN = 100 ngec Etamerault = 15 ugec = 100 ngec = 6.66 Ang S = Performance of Interuit = ETIMENH = ETROS

In Programmed I/O Speed of.
CPU Debands on I/O Device

Performance of



In programmed I/O execution, the transfer time depends on \_









- C. Latency of I/O interface chip
- D. None of these

In Programmed Cfu time Depands on Speed of Ilo Devices

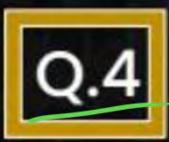
2 Amount of Data

. No High Speed Interface Chip is

ee) IKB by =) IKB - ISEC

1 Byte - 1 sec = 10 sec 2 Byte - XX I msec = Imilli Second

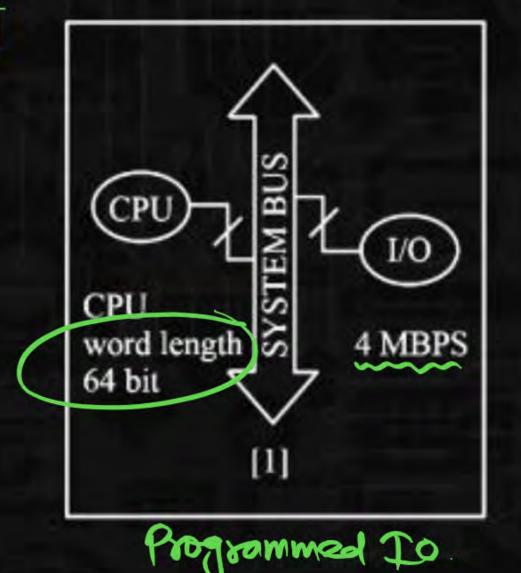
1 (A) 4 (B)

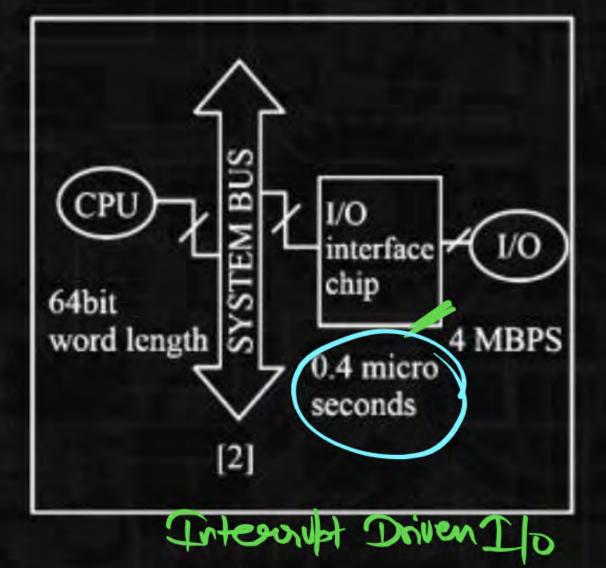


## Consider the following scenario



Ang(0.2)

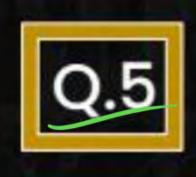




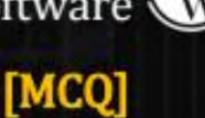
Calculate the speedup when I/O device is operating under programmed I/O over interrupt mode <u>O2</u> My [NAT]

Paugrammed I/o	CPU times	Depands	en s	beed o	6 Do Device
No Speed. 41	MBPS	Word length:	- Gubit	55	3 Byte
4 mByk ->	2 Sec. 28 Sec. Sec. MMBJE 50	(=) 2×156	Sec	ETProg	110 = 2 WgC
ETIMORPHITO = 0.4	ugec. CPU Tim	e Debauels Mc	speed o		Interface.
Speed up factor = (Performance Goin)	Performance of B	Of Ilo Intervet Ito	= 0	4 - (	0.2) Ame

= ETANGAI.

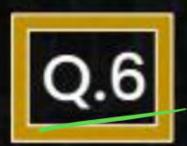


Which of the following interrupts are caused by software instructions are known as?



- Hardware interrupt
- Exception interrupt В.
- Maskable interrupt
- Normal interrupt





Consider 16 MBPS I/O device interfaced to 32-bit CPU using DMA interface. DMA contain 16-bit count register, 32 bit data register and five, 8 bit address register. Data file size is 512 kB. How many DMA cycles are required to transfer the file?

Arg (2)

Court Register = 1661

Wood Length = 32bit







-65536 Words

Data file Size = 512 KByk

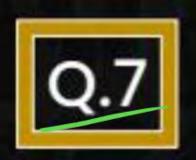
= 216 XYByte [Iwned=]
= 216 XYByte

Number of DMA = 512kB

Cycle Required = 256kB

218 Byke + 256kB

in due DMA Cycle.

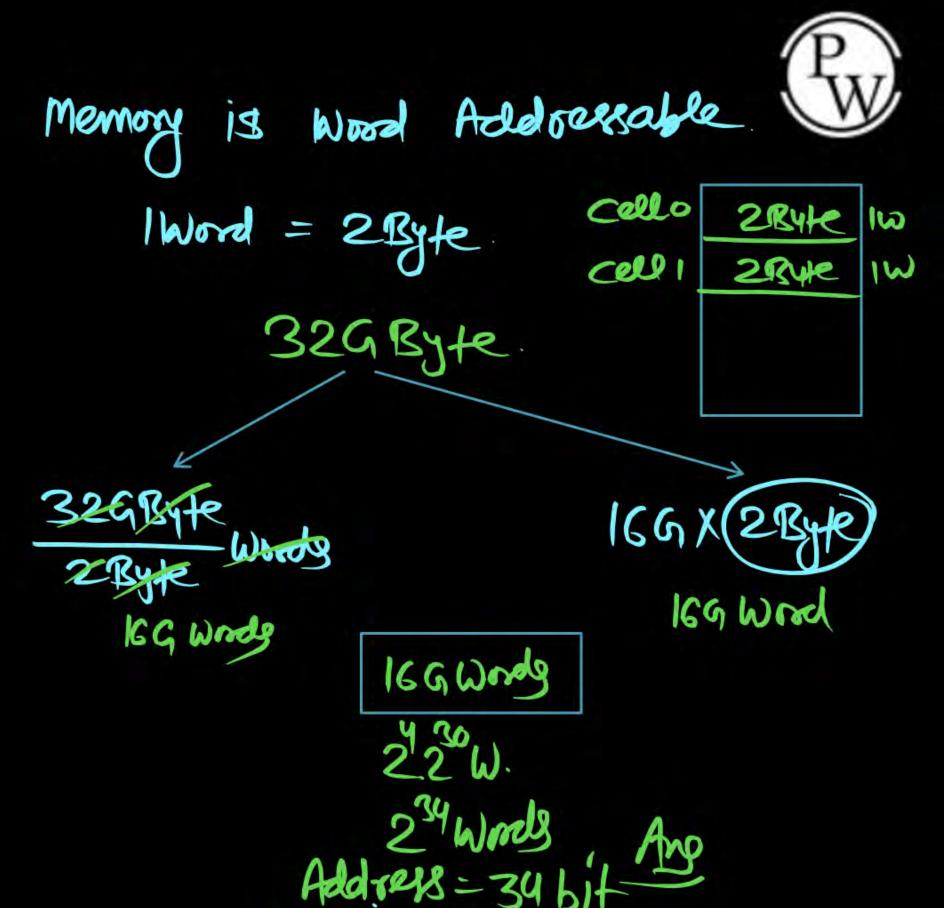


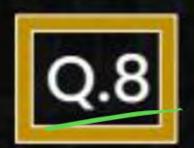
A processor can support a maximum memory of 32 GB, where the memory is word addressable (a word consist of 2 bytes). The size of the address bus of the processor is at least 34 bits.

[NAT]



32 G Byte 5.2° Byte 35 Byte Address = (35 bit But this is Not Gorcet Because Memory is word Address & Wood Size 19 also given.

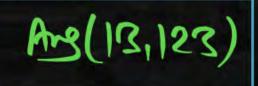




A hard disk has 32 sectors per track, 10 platters each with 2 recording surface and 500 cylinders.



The address of a sector is given as a triple <c, h, s>, where c is cylinder number, h is surface number and s is the sector number. Thus the  $0^{th}$  sector is addressed as <0, 0, 0>, the  $1^{st}$  sector as <0, 0, 1> and so on. The address of the <20, 10, 3> corresponds to sector number?



32 Sector Pertoack

10 Platter, each with 2 Record Surface

500 cyclinder

10x2 = 20

CO10117 2nd sector

CC. h. S> Sector Cylinder Surface Sector

C20,10, 3>

To Reach At Cross 20 cylinder = 20x lox2 x32 this cylinder [0-19] +325ech



10th surface => 10×32

Cross 3 Sector (or1,2) = 3

Sector Number = 20x20x32 + 10x32 + 3 => 12800 + 320 + 3

= 13123 Are



