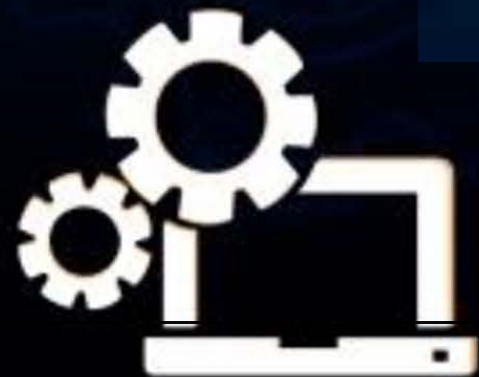


# CS & IT ENGINEERING

Computer Organization and Architecture

Machine Instructions and Addressing Mode

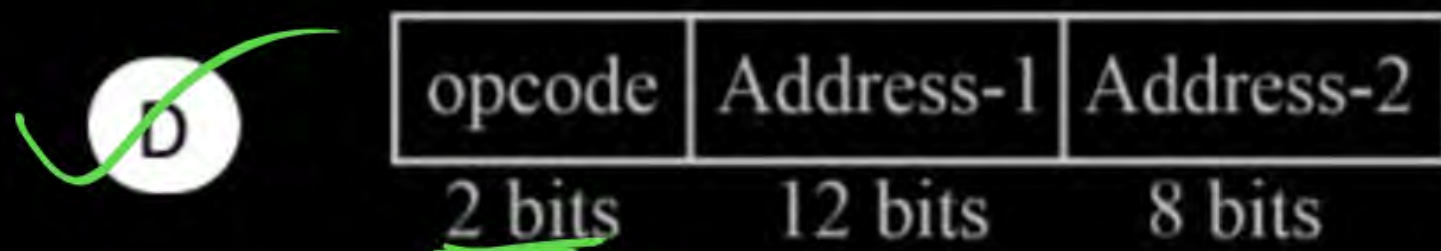
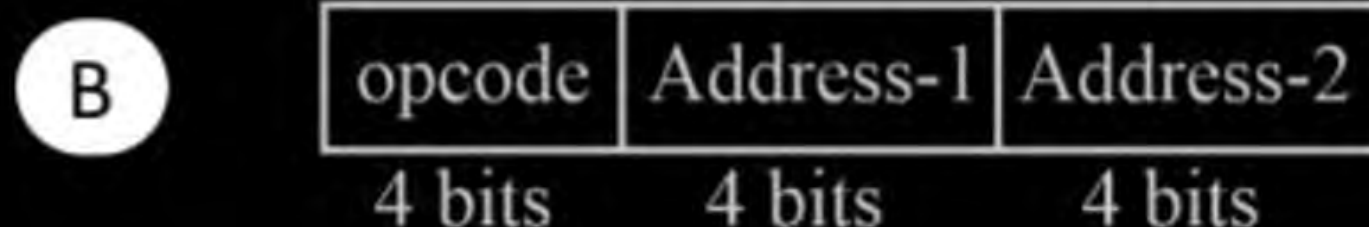
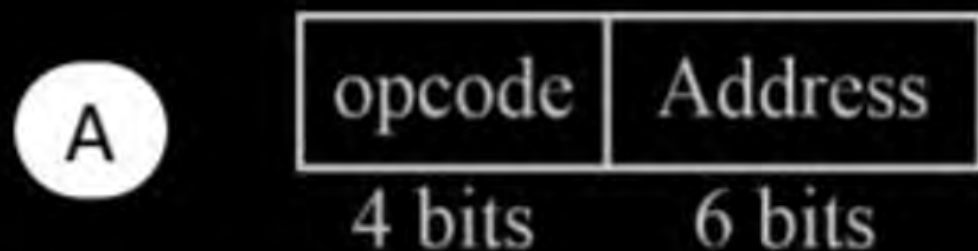


**DPP Discussion Notes**



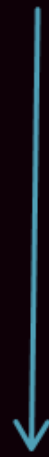
**By-Vijay Agarwal sir**

Which of the following is primitive instruction in the CPU?



Ans (D)

Primitive Instruction: Lowest [Smallest] bit  
in opcode.



Smallest opcode bit

Derived Inst<sup>n</sup>: More Opcode bits

More @ further Derived Inst<sup>n</sup>: more & more bit in opcode.



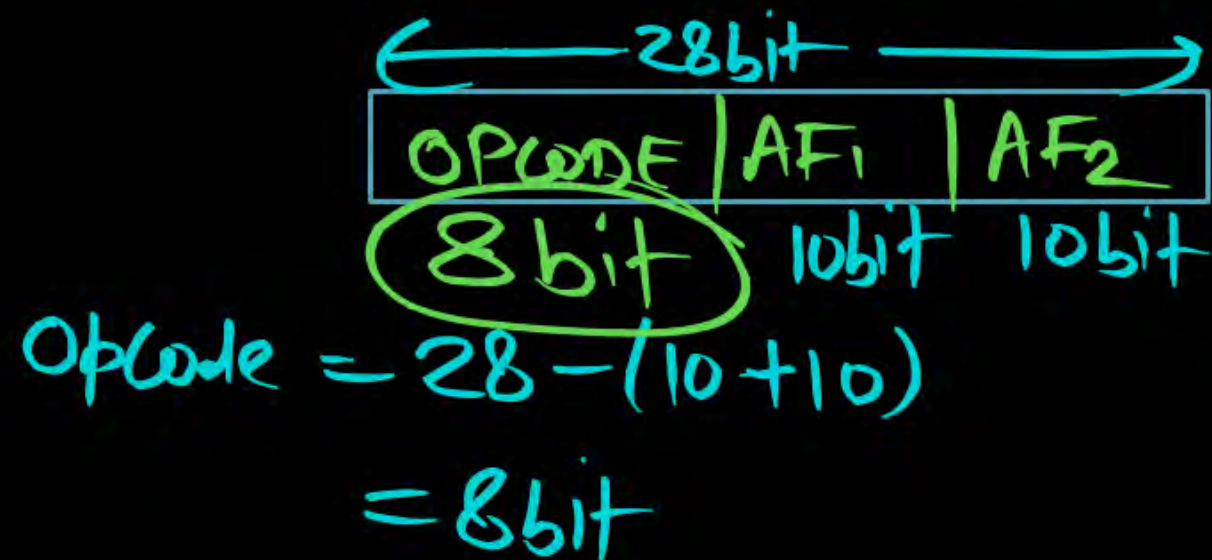
[NAT]



Consider a hypothetical system which support only 2 address instructions. If size of the instruction is 28 bit and size of each address is 10 bits then, the maximum number of instructions the system can support \_\_\_\_.

Instruction Size = 28 bits

Address field = 10 bit



n bit op code Can perform  $2^n$  operation

Total Number of  
Operation/Inst<sup>n</sup> =  $2^8$   
= 256

Ans (256)

Consider a digital computer which support 64 3-address instruction. If the size of each address is 14 bits, then the instruction is of 6 bytes.

64 3AI

↓

64 operation Performed

Ans (6)

3AF / 3AI (Addresses Instruction is given

AF = 14 bits



$$64 \text{ operation} \Rightarrow \text{opcode} = 2^n = 64 \Rightarrow 2^n = 2^6$$

$$n = 6 \text{ bit}$$

$$AF = 14 \text{ bit}$$

OPCODE	AF <sub>1</sub>	AF <sub>2</sub>	AF <sub>3</sub>
6 bits	14 bit	14 bit	14 bit

$$\begin{aligned} \text{Instruction Length} &= 6 + 14 + 14 + 14 \\ &= 48 \text{ bits} \Rightarrow \frac{48}{8} \text{ Byte} \\ &= 6 \text{ Byte } \underline{\text{Ans}} \end{aligned}$$

## [MCQ]



The correct sequence in Fetch-Execute cycle is:

- ☐ A Decode, Fetch, Execute
- ☐ B Fetch, Execute, Decode
- ☒ C Fetch, Decode, Execute
- ☐ D None of the above

Ans (C).

**Instruction Cycle:** The process required for each instruction execution is called Instruction cycle.

① Fetch cycle

② Execute cycle



```
graph LR; A[② Execute cycle] --> B[Decode]; A --> C[Execute.]
```



## Steps in Instruction Cycle

Fetch cycle

- ① IAC (Instruction Address Calculation)
- ② IF (Instruction Fetch) [Mem to CPU [IR]]

Execute cycle

Decode

- ③ Decoding (Analysis of the Instruction (what opcode, How many operands, where operands are available etc.))
- ④ OAC (Operand Address Calculation)
- ⑤ OF (Operand Fetch) (Addressing Modes Required)

Execute

- ⑥ Data Processing
- ⑦ Result Storage



## [MCQ]



Consider a system which supports 2 - address instructions only. The system has  $2^P$  K bytes of memory. If there are 'q' distinct instructions supported by system then, what is the size of instruction?

A  $(q + p)$  bits

☒ B  $[\log_2 q + 2(P + 10)]$  bits

C  $(\log q + 2P)$  bits

D  $\log(p + q)$  bits

Ans (B).

2AF / 2AI

Memory Size =  $2^p$  k Byte

$$\Rightarrow 2^p \times 2^{10} \text{ Byte} \Rightarrow \boxed{2^{p+10} \text{ Byte}}$$

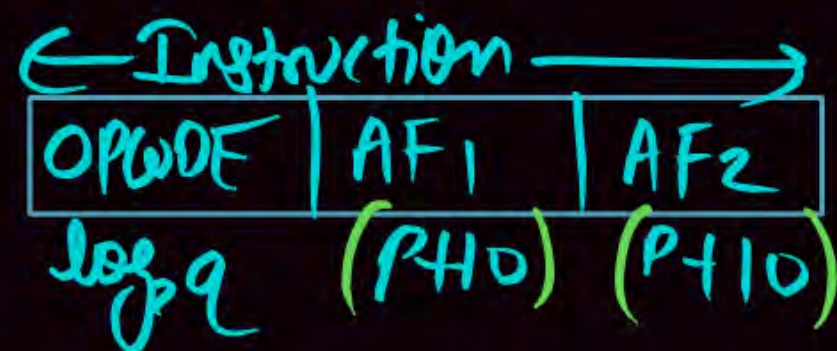
Total No. of Distinct operation 'q'

Instruction Size?

$$\log_2(2^{p+10}) \text{ or } 2^n = 2^{p+10}$$

Memory Size =  $2^{p+10}$  Byte then  $\boxed{AF = \underline{p+10}}$

$$\text{opcode bit} = \lceil \log_2 \# \text{operation} \rceil \Rightarrow \lceil \log_2 q \rceil$$



$$\begin{aligned} \text{Instruction Size} &= \log_2 q + (p+10) + (p+10) \\ &= \log_2 q + 2(p+10) \text{ Ans} \end{aligned}$$



## [MCQ]



Consider a system which support 2 - address instructions add 1-address instruction both. Suppose, the system has 6 bits instruction and 2 - bits addresses. If there are three, 2 - address in the system then, maximum and minimum how many 1 - address instruction the system can support?

A 15, 1

☒ B 4, 1

C 16, 0

Ans (B)

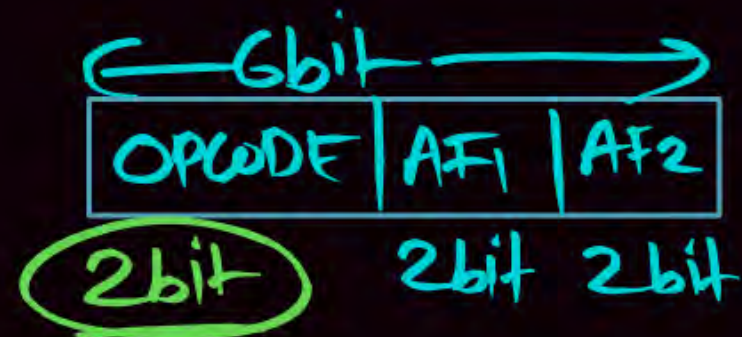
D None

Instruction Size = 6 bit

Address field(AF) = 2 bit

Given  $2AI = 3$  then Asking about LAI ?

Step 1



$$\text{opcode} = 6 - (2 + 2) = \text{2 bit}$$

Step 2

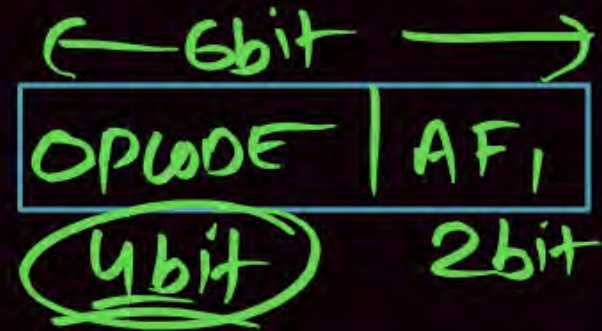
Total # operation in  $2AI = 2^2 = 4$  operation

GIVEN  $2AI = 3$

Number of Free opcode After Allocating  $2AI = 4 - 3 = 1$



LAI



Expand opcode Technique,  
Fixed Length Instruction

$$\begin{aligned} \text{Total \# operation in LAI} &= \text{Free opcode} \times \text{Increment bit in opcode} \\ &\Rightarrow 1 \times 2^{4-2} \Rightarrow 1 \times 2^2 \end{aligned}$$

$$\boxed{\text{LAI} = 4 \text{ operation}}$$

Minimum operation in LAI = 1

Maximum operation in LAI  $\leq 4$



# [MCQ]



Consider a PC - relative mode type branch instruction, which takes branch on addresses 680 in memory. The instruction has offset value 420. What is the address of this instruction in memory. If each instruction is stored in memory on 2 - locations?

$$\text{(Branch) Target Address} = \text{Current PC Value} + \text{Relative Value (OFFSET)}$$

Instn Starting Address = 258

☒ A 258

☐ B 280

☐ C 282

☐ D 260

$$680 = PC + 420$$

Ans(A)

$$PC = 680 - 420$$

$$PC = 260$$

258	I <sub>1</sub>
259	I <sub>2</sub>
	Next Instn

PC 260

PC [Program Counter] Denote Next Instn Starting Address.



## [MCQ]



Consider a 6 - word instruction which is of the following type:



The first operand (destination) uses register indirect mode and second operand uses indirect mode. Assume each operand of size 2 - words, each address is of 2 word and main memory takes 20 ns for each word access. What is the different between fetch cycle of instruction time and execution cycle of instruction time?

[Note : Register access time is negligible.]

A 260 ns

B 20 ns

Ans (C).

✓ C 40 ns

D 120 ns



OPCODE	MODE1	MODE2	AF1	AF2
--------	-------	-------	-----	-----

Instruction Size = 6 Word

A.F = 2 Word

operand Size = 2 Word

memory Access = 20 nsec  
for each word

Fetch Cycle

Total Time taken in Fetch cycle =  $6 \times 20 \text{ ns} = \underline{120 \text{ nsec}}$

Execute cycle

Source 1: Register Indirect  $\rightarrow (1 \text{ Reg Ref} + 1 \text{ Mem Ref})$

$\Rightarrow 1 \text{ Mem Ref [2 Word]} (\because \text{AF} = 2 \text{ Word})$

$\Rightarrow 2 \times 20 = \underline{40 \text{ nsec}}$



1 mem Ref for EA  
1 mem Ref for Data (Read)

Source 2 Memory Indirect : 2 mem Ref. & each mem Ref = 20

$$\Rightarrow A.F = 2 \text{ word} \Rightarrow 2 \times (2 \times 20) = \underline{80 \text{ nsec.}}$$

Destination : Register Indirect : (1 Reg + 1 mem)  
(Source!)

$$\Rightarrow 2 \text{ word} \times 20 = 40 \text{ nsec.}$$

Total time in Execution Cycle -  $40 + 80 + 40 = 160 \text{ nsec.}$

$$\text{Difference} = 160 - 120 = \underline{40 \text{ nsec}} \quad \underline{\text{Ans}}$$

## [MCQ]



Consider a computer with 34 bits instruction and 14 bits addresses. If there are 60 2 - address instruction and 65000 - address instruction then, how many maximum 0 - address instruction can be formulated?

65000

A 65536 K

☒ B 8576 K

C 16384 K

D none

Ans (B)

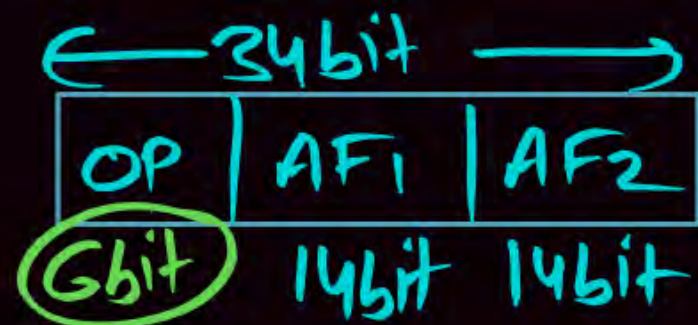


Instruction Size = 34 bit

AF = 14 bit

2AI/operation = 60

1AI/operation = 65000



Expand opcode Technique.

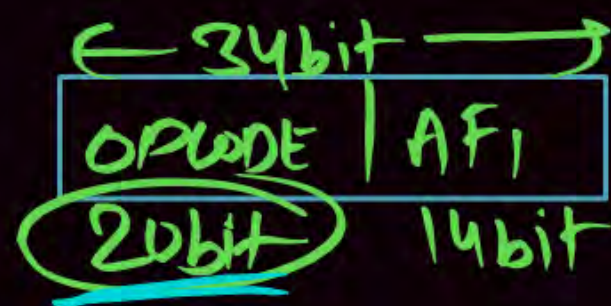
$$\text{OPCODE} = 34 - (14 + 14) = \text{6 bit}$$

Total # operation in 2AI =  $2^6 = 64$  operation / Instruction.

GIVEN 2AI = 60

#Free opcode After Allocating 1AI =  $64 - 60 = \text{4}$





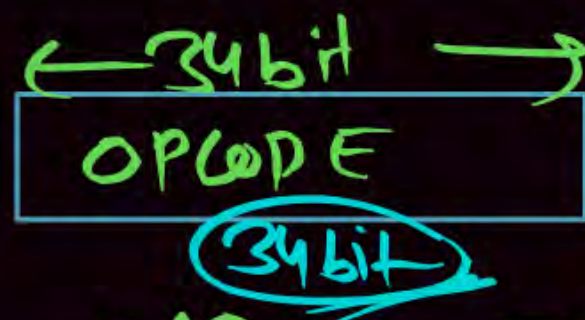
$$= \text{Free opcode} \times \overset{\text{Increment bit in opcode}}{2}$$

$$\text{In IAF Total \# operation} = 4 \times 2^{20-6} \Rightarrow 4 \times 2^{16} = 65536 \text{ operation}$$

$$\text{Given IAI} = 65000$$

$$\# \text{Free opcode After Allocating IAI} = 65536 - 65000 = 536$$


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$$\text{OAI} = 536 \times 2^{34-20}$$

$$\Rightarrow 536 \times 2^{14} \Rightarrow 536 \times 2^4 \times \overset{k}{(2^{10})}$$

$$\Rightarrow 536 \times 16 \times k \\ = 8576k$$

## [MCQ]



If an opcode is of 4 bit then, how many maximum minimum type of instruction supported by CPU?

$n$  bit opcode can perform  $2^n$  operation.

A 15, 1

B 15, 0

☒ C 16, 1

D 16, 0

OPCODE Size = 4 bit

Total Number of operation =  $2^4 = 16$  operation

Maximum = 16

Minimum = 1

Ans [C]



