Branch : CSE & IT Batch : Hinglish

Computer Organization and Architecture
Secondary memory & I/O interface

DPP

[MCQ]

1. Which of the following is/are not the major functions for an IO module?

(a) Control and timing

(b) Error detection

(c) Processor communication

(d) Single instruction multiple data stream (SIMD)

[NAT]

2. Consider a system with data transfer rate is 10 KBPS. Data are exchanged between the processor and I/O interface. The performance gain when IO device is operating under interrupt mode over programmed IO mode)__.

Note (Interrupt interface over head is 15 μsec)

(round off 1 decimal places)

[MSQ]

3. In programmed I/O execution, the transfer time depends on _____.

(a) I/O speed

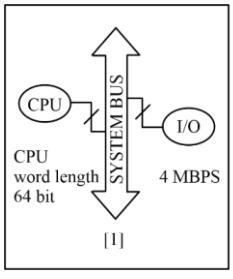
(b) Data size

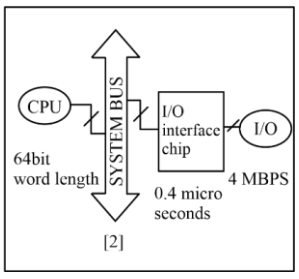
(c) Latency of I/O interface chip

(d) None of these

[NAT]

4. Consider the following scenario





Calculate the speedup when I/O device is operating under programmed I/O over interrupt mode ____.

[MCQ]

5. Which of the following interrupts are caused by software instructions are known as ?

(a) Hardware interrupt

(b) Exception interrupt

(c) Maskable interrupt

(d) Normal interrupt

6. [NAT]

Consider 16 MBPS I/O device interfaced to 32-bit CPU using DMA interface. DMA contain 16-bit count register, 32 bit data register and five, 8 bit address register. Data file size is 512 kB. How many DMA cycles are required to transfer the file?

7. [NAT]

A processor can support a maximum memory of 32 GB, where the memory is word addressable (a word consist of 2 bytes). The size of the address bus of the processor is at least _____bits.

8. [MCQ]

A hard disk has 32 sectors per track, 10 platters each with 2 recording surface and 500 cylinders.

The address of a sector is given as a triple <c, h, s>, where c is cylinder number, h is surface number and s is the sector number. Thus the 0^{th} sector is addressed as <0, 0, 0>, the 1^{st} sector as <0, 0, 1> and so on. The address of the <20, 10, 3> corresponds to sector number?

Answer Key

1. **(d)**
2. **(6.66 to 6.66)**
3. **(a, b)**
4. **(0.2 to 0.2)**
5. **(d)**
6. **(2)**
7. **(34)**
8 **(13123)**

Hints & Solutions

1. (d)

- The major functions for an IO module are
- Control and timing
- Error detection
- Device communication
- Data buffering
- Processor communication
- SIMD is one of the types of parallel processor system.

2. (6.66 to 6.66)

Data are exchanged between processor and I/O (programmed I/O)

- Word length not given, assume byte addressable.
- **Programmed IO**

10 KB _____1 sec

1B _____?

$= \frac{1}{10}$

$= 100\ \mu$ sec

$ET_{\text{programmed I/O}} = 100\mu$ sec

$$S \text{ (performance gain)} = \frac{ET_{\text{programmed I/O}}}{ET_{\text{interface I/O}}}$$

$$= \frac{100}{15} = 6.66$$

3. (a, b)

In interrupt driven I/O mode CPU time (execution per transfer) depends on latency of an I/O interface chip. Where as in programmed I/O CPU time depends on data size and I/O speed.

4. (0.2 to 0.2)

Programmed I/O mode:

CPU time = depends on I/O speed and data size

Word length = 64 bits (8 bytes)

$ET_{\text{programmed I/O}}$ = 4 MB _____1 sec

8 B _____?

$$ET_{\text{programmed I/O}} = \frac{8B}{4MB}$$

= 2 microseconds

Interrupt I/O:

CPU time = latency of an I/O interface chip

$ET_{\text{interface I/O}} = 0.4\mu$ sec

$$\text{Speedup(s)} = \frac{ET_{\text{interfaceI/O}}}{ET_{\text{programmed I/O}}} = \frac{0.4}{2}$$

= 0.2.

5. (d)

The definition of normal interrupts is interrupts which are caused by the software instructions are called software interrupt.

Hence, option (d) is correct.

6. (2)

DMA operation cycle is controlled by the count register.

Count register = 16 bit, so it maintains 65536 counts.

In every count one word data will be transferred.

Therefore, data transmission/DMA cycle = 65536 W

65536 × 32 bit

65536 × 4-byte

$2^{16} \times 2^2 = 2^{18}$ B = 256 kB

1 DMA cycle → 256 kB

Number of DMA cycle – 1 file (512 kB)

$$\Rightarrow \frac{512\ \cancel{kB}}{256\ \cancel{kB}} = 2 \text{ cycles}$$

7. (34)

Given 1word = 2 Byte, 1 byte = $\frac{1}{2}$ word

Memory = 32 GB $\Rightarrow 32G \times \frac{1}{2}$ word

$\Rightarrow$ 16 G words = 2^{34}

The size of the address bus of the processor = $\lceil \log_2 2^{34} \rceil$

$\Rightarrow$ 34 bits

8. (13123)

$20 \times 32 \times 2 \times 10 + 10 \times 32 + 3 \Rightarrow 12800 + 320 + 3$

$\Rightarrow 13123$