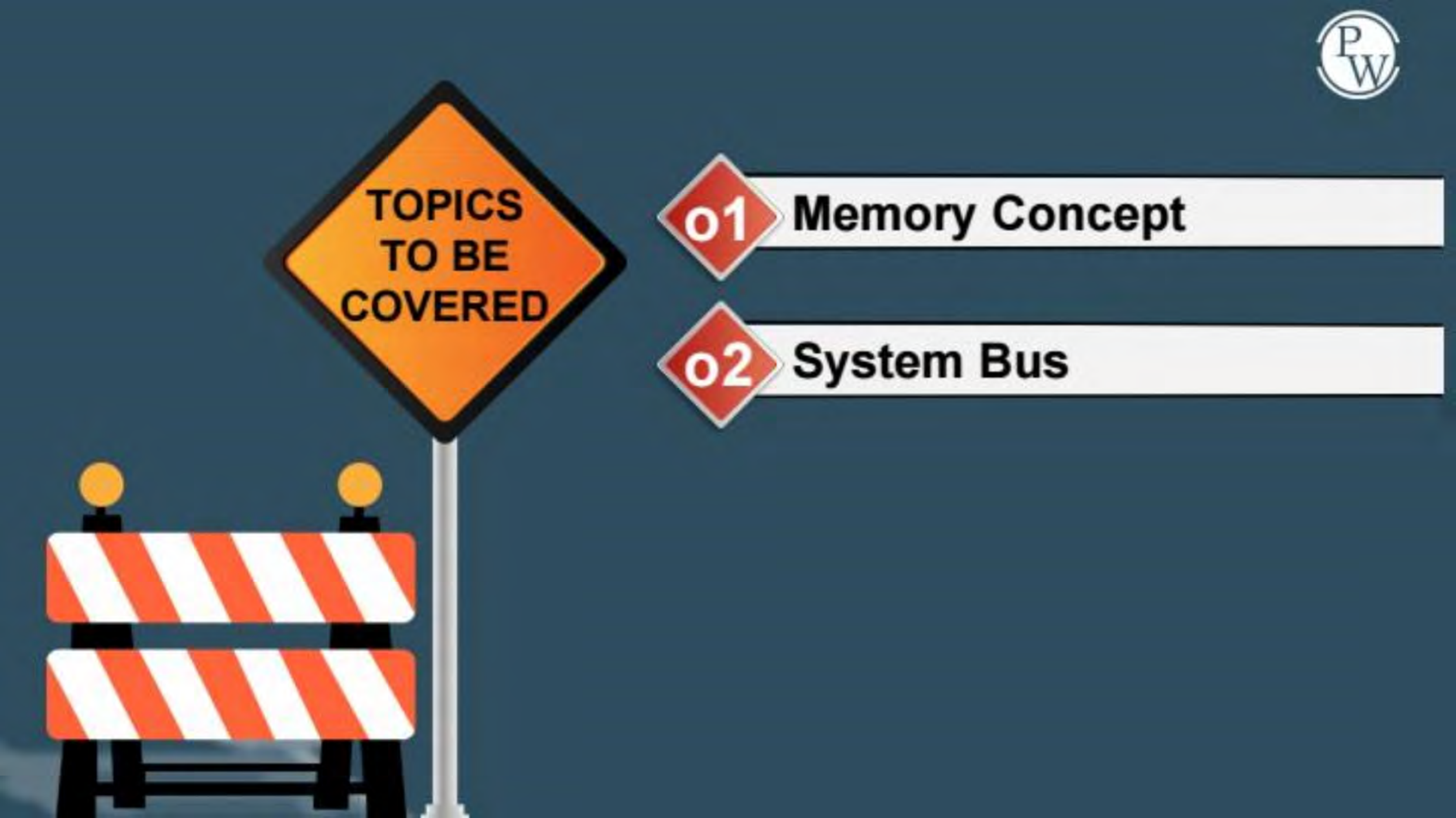
COMPUTER SCIENCE

Computer Organization and Architecture

Introduction of COA

Lecture_03

Vijay Agarwal sir



01 Memory Concept

02 System Bus

Introduction.

Computer Generation.

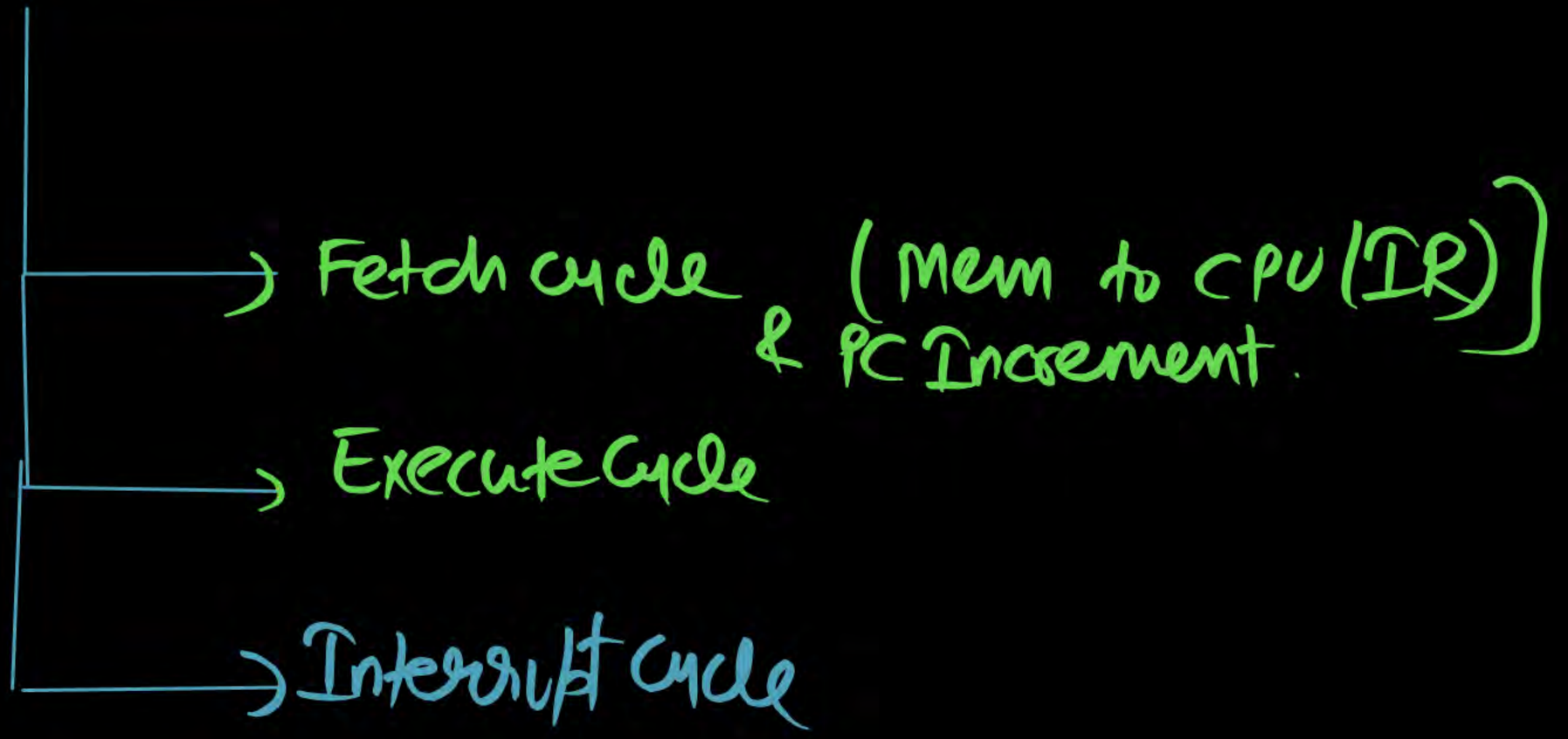
CO & CA

Component of the Compute

1. CPU
2. memory
3. Io

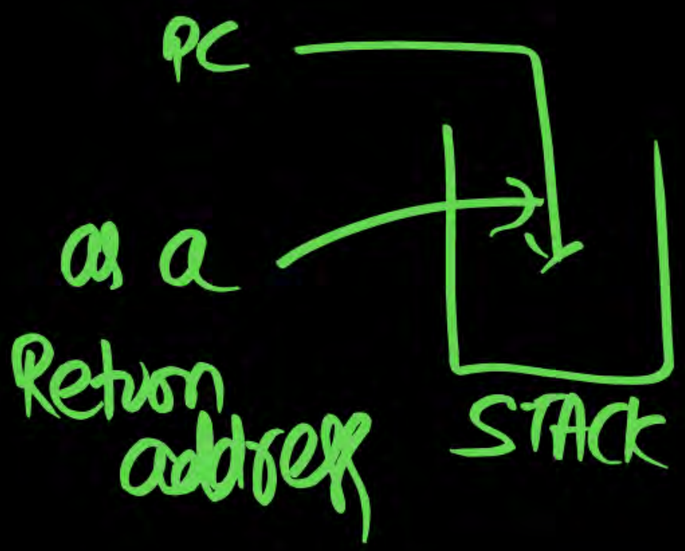
PC
MAR
MBR
IR
AC
GPR
SP
PSW.

Instruction cycle.



Interrupt

After completion of Current Instn Execution Interrupt will be Serived.



Word Addressable Memory (eg 8M Words)

Byte Addressable Memory (eg 8M Byte)

Q.1 Consider the following program segment execute on Hypothetical processor. [4 Marks]

Assume that program is stored in the memory address 1000(Decimal) onwards. During the execution of I_6 what could be value present in the Program counter. Assume that word size is 32 bit & memory is Byte Addressable?

Instruction	Size (in words)
I_1	2
I_2	1
I_3	1
I_4	3
I_5	1
I_6	2
I_7	1

Q.2 Consider the following program segment execute on Hypothetical processor. [4 Marks]

Assume that word size is 32 bit & memory is word addressable. The program is stored in the memory at address 1000 (Decimal) onwards. During the execution of I_5. What could be value present in the program counter?

Instruction	Size (in words)
I_1	2
I_2	1
I_3	1
I_4	3
I_5	1
I_6	2
I_7	1

Q. Consider the following Program Segment for a hypothetical CN.

Instruction	Meaning	Instruction size (in words)	F&D	
I_1 MOV r_0, 2000	$r_0 \leftarrow M[2000]$	3w	3×3	+4 = 13
I_2 MOV r_1, 3000	$r_1 \leftarrow M[3000]$	3w	3×3	+4 = 13
I_3 MUL r_0, r_1	$r_0 \leftarrow r_0 * r_1$	1w	1×3	+6 = 9
I_4 MOV 6000, r_0	$M[6000] \leftarrow r_0$	3w	3*3	+4 = 13
I_6 HALT	Machine Halt	1w	1*3	= 3

51 cycle

Let the Clock Cycle required for various operation be as follows:
Instruction Fetch & Decode: 3 clock cycle per word
MUL with both operand & stored in register: 6 Clock Cycle.
Register to/from memory transfer: 4 clock cycle
The total number of clock cycle required to execute the program is___

Q. Consider the following program segment for a hypothetical CPU Having three users registers R1, R2 and R3.

[GATE-2 Marks]

Instruction	Operation	Instruction size (in words)
MOV R1, 5000	R1 ← Memory[5000]	2
MOVR2, (R1)	R2 ← Memory[(R1)]	1
ADD R2, R3	R2 ← R2 + R3	1
MOV 6000, R2	Memory [6000] ← R2	2
HALT	Machine Halts	1

1000–1001
1002
1003
1004–1005
1006.

Consider that the memory is word addressable with size 32 bits and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs during the ADD instruction, what will be the return address pushed on to the stack

(a) 1007 (b) 1004 (c) 1005 (d) 1016

1 Word Size = 32 bit

= 4 Byte

Q.

Consider the following program segment for a hypothetical CPU Having three users registers R1, R2 and R3.

[GATE-2 Marks]

Instruction	Operation	Instruction size (in words)
MOV R1, 5000	R1 ← Memory[5000]	2
MOVR2, (R1)	R2 ← Memory[(R1)]	1
ADD R2, R3	R2 ← R2 + R3	1
MOV 6000, R2	Memory [6000] ← R2	2
HALT	Machine Halts	1

1000 – 1007
1008 – 1011
1012 – 1015
1016 – 1023
1024 – 1027

Consider that the memory is Byte addressable with size 32 bits and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the MOV 6000R, instruction, the return address (in decimal) saved in the stack will be

(a) 1007 (b) 1020 (c) 1024 (d) 1028

Byte Addressable.

1 Word = 32 bit

$\leq$ 4 Byte.

2 Word = 2 × 4 = 8 Byte

Q. Consider the following program segment for a hypothetical CPU Having three users registers R1, R2 and R3. [GATE- 2 Marks]

	Instruction	Operation	Instruction size (in words)	F&D + Execute.
I_1	MOV R1, 5000	R1 ← Memory[5000]	2W	2×2 + 3 = 7
I_2	MOVR2, (R1)	R2 ←Memory [(R1)]	1W	1×2 + 3 = 5
I_3	ADD R2, R3	R2 ← R2 + R3	1W	1*2 + 1 = 3
I_4	MOV 6000, R2	Memory [6000] ← R2	2W	2*2 + 3 = 7
I_5	HALT	Machine Halts	1W	1*2 + 0 = 2

24 Cycle.

Let the clock cycles required for various operations be as follows:

Register to/from memory transfer:

3. Clock cycles.

ADD with both operand in register

1. Clock cycle

Instruction fetch and decode:

2. Clock cycles per word.

The total number of clock cycle required to execute the program is

(a) 29 (b) 24 (c) 23 (d) 20

COMMON DATA QUESTION (5 - 7)

Consider the following program segment, Here R1, R2 and R3 are the general purpose register.

Instruction	Operation	Instruction size (no. of words)
MOV R1, (3000)	R1←M[3000]	2
LOOP;		
MOV R2, M[R3] ADD R2, R1	R2←M[R3] R2←R1 + R2	1 1
MOV (R3), R2	M[R3] ←R2	1
INC R3	R3←R3+1	1
DEC R1	R1←R1-1	1
BNZ LOOP	Branch on not zero	2
HALT		Stop

Assume that the content of memory location 3000 is 10 and the content of the Register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the Numbers are in decimal.

Q.5 Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is

[2 marks]

(a) 10 (b) 11 (c) 20 (d) 21

$1 + 2 * 10$

$= 21$

COMMON DATA QUESTION (5 - 7)

Consider the following program segment, Here R1, R2 and R3 are the general purpose register.

Instruction	Operation	Instruction size (no. of words)
MOV R1, (3000)	R1←M[3000]	2
LOOP:		
MOV R2, M[R3] ADD R2, R1	R2←M[R3] R2←R1 + R2	1 1
MOV (R3), R2	M[R3] ←R2	1
INC R3	R3←R3 + 1	1
DEC R1	R1←R1 - 1	1
BNZ LOOP	Branch on not zero	2
HALT		Stop

Assume that the content of memory location 3000 is 10 and the content of the Register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the Numbers are in decimal.

Q.6 Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is

[2 marks]

(a) 100 (b) 101 (c) 102 (d) 110

COMMON DATA QUESTION (5 - 7)

Consider the following program segment, Here R1, R2 and R3 are the general purpose register.

Instruction	Operation	Instruction size (no. of words)
MOV R1, (3000)	R1←M[3000]	2
LOOP:		
MOV R2, M[R3]	R2←M[R3]	1
ADD R2, R1	R2←R1 + R2	1
MOV (R3), R2	M[R3] ←R2	1
INC R3	R3←R3+1	1
DEC R1	R1←R1-1	1
BNZ LOOP	Branch on not zero	2
HALT		Stop

Assume that the content of memory location 3000 is 10 and the content of the Register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the Numbers are in decimal.

Q.7 Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction "INC R3", what return address will be pushed on to the stack? [2 marks]

(a) 1005 (b) 1020 (c) 1024 (d) 1040

1 Word = 32 bit

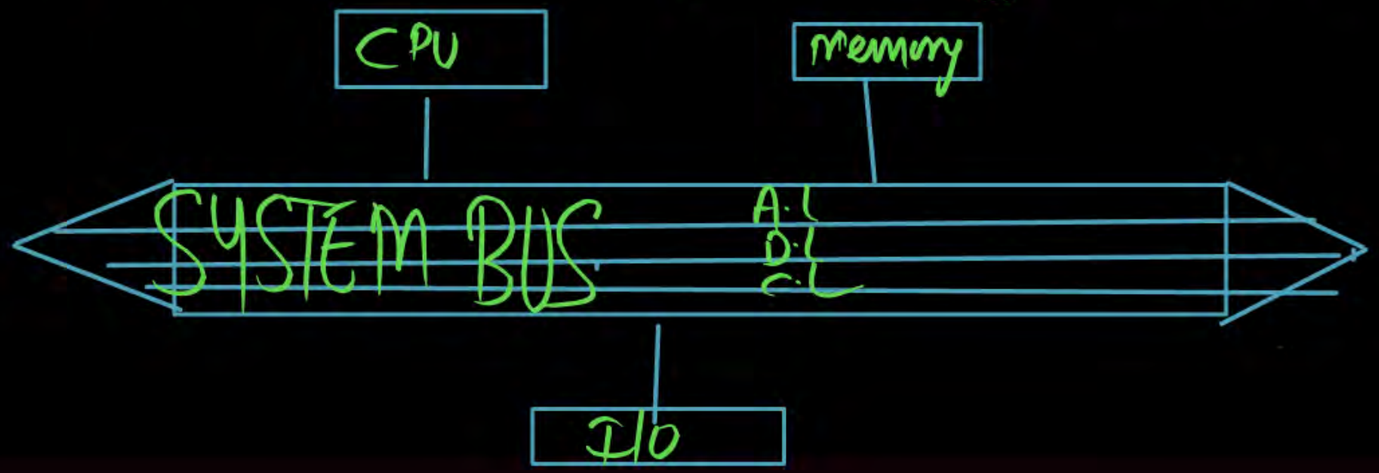
1 Word ⇒ 4 Byte.

Component of Computer.

1. CPU
2. Memory
3. I/O.

SYSTEM BUS

System bus is a Collections of Lines which are Used to Provide the Communication between major Component of the Computer. (Memory, I/O, CPU)



System Bus Contain 3 type of Lines/Bus.

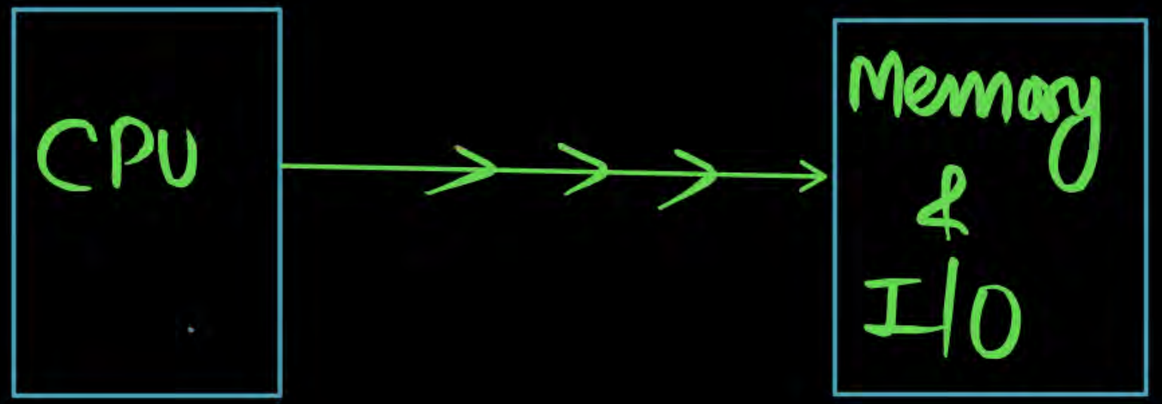
① Address Line | Address Bus.

② Data Line | Data Bus.

③ Control Line | Control Bus.

① Address Line [AL] / Address Bus : Address line are used to carry the Address towards memory & I/O.

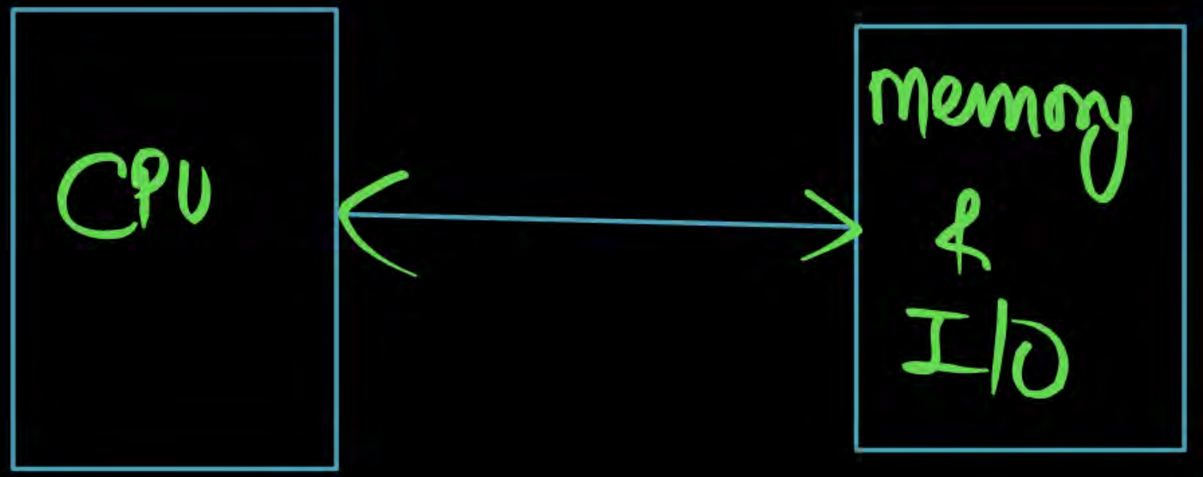
Note Address line are Unidirectional.



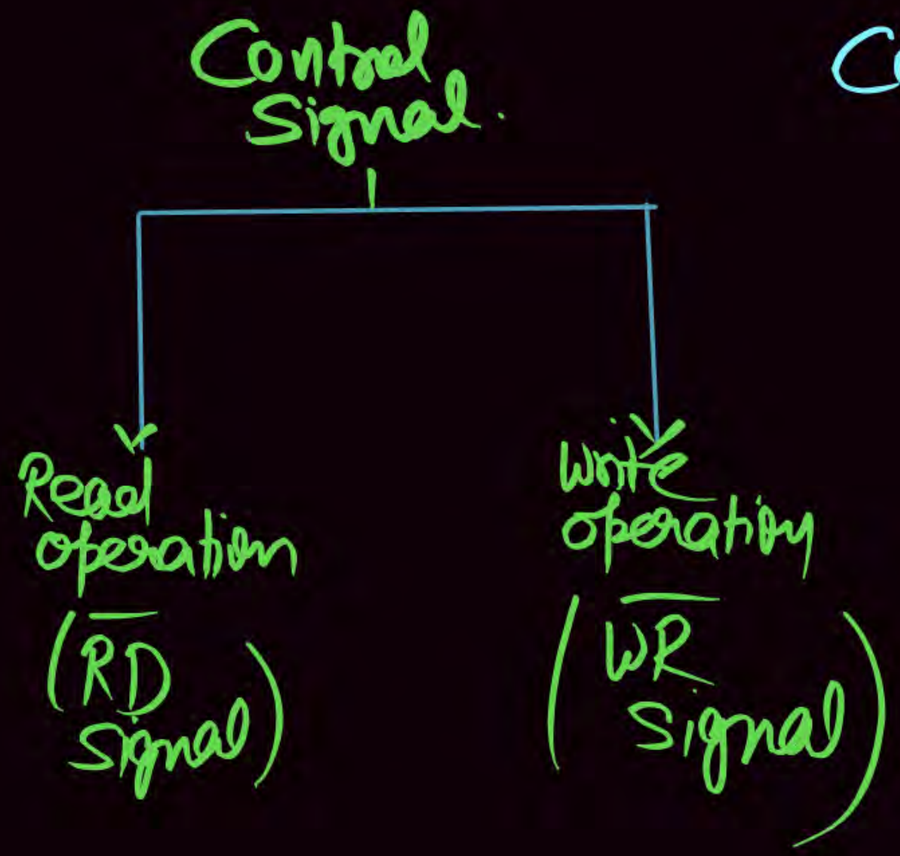
② Data Line : [D.L] : Data Line are Used to Carry the Data (Binary Sequence)

Note

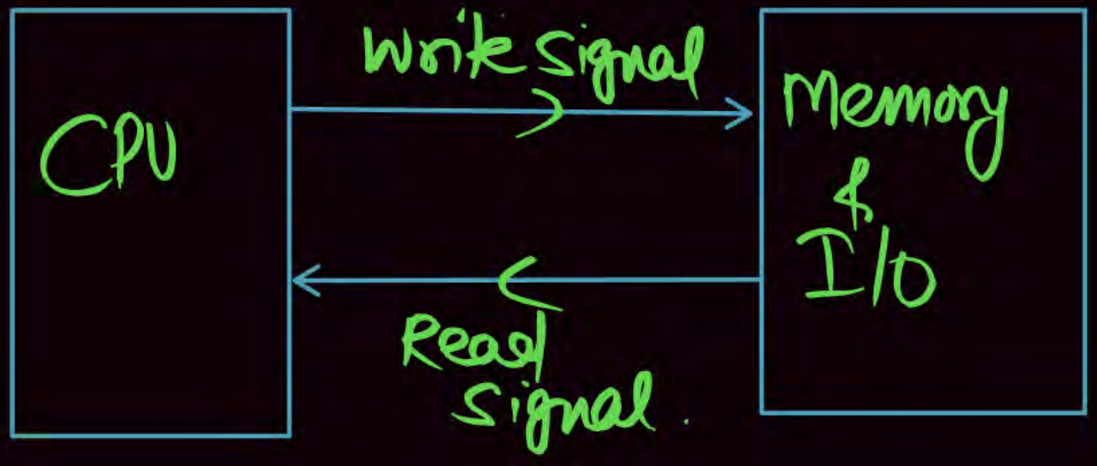
Data line are Bidirectional.



③ Control Line [C.L] : Control Line are Used to Carry the Control Signal.



Control Lines individually Unidirectional & Collectively Bidirectional.



Memory

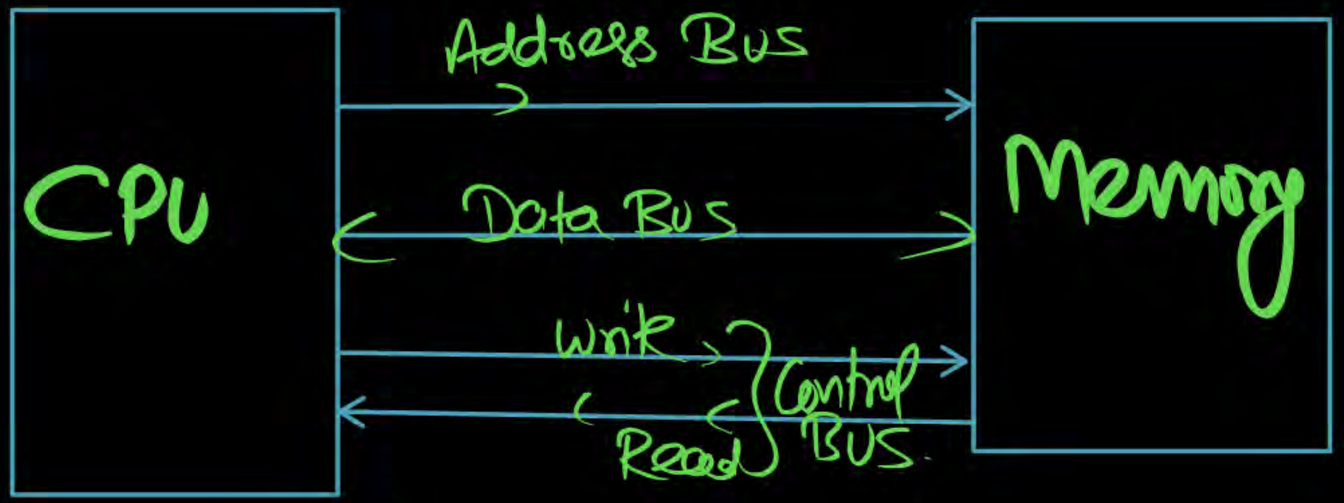
Memory Read : Memory to CPU.

Memory Write : CPU to Memory.

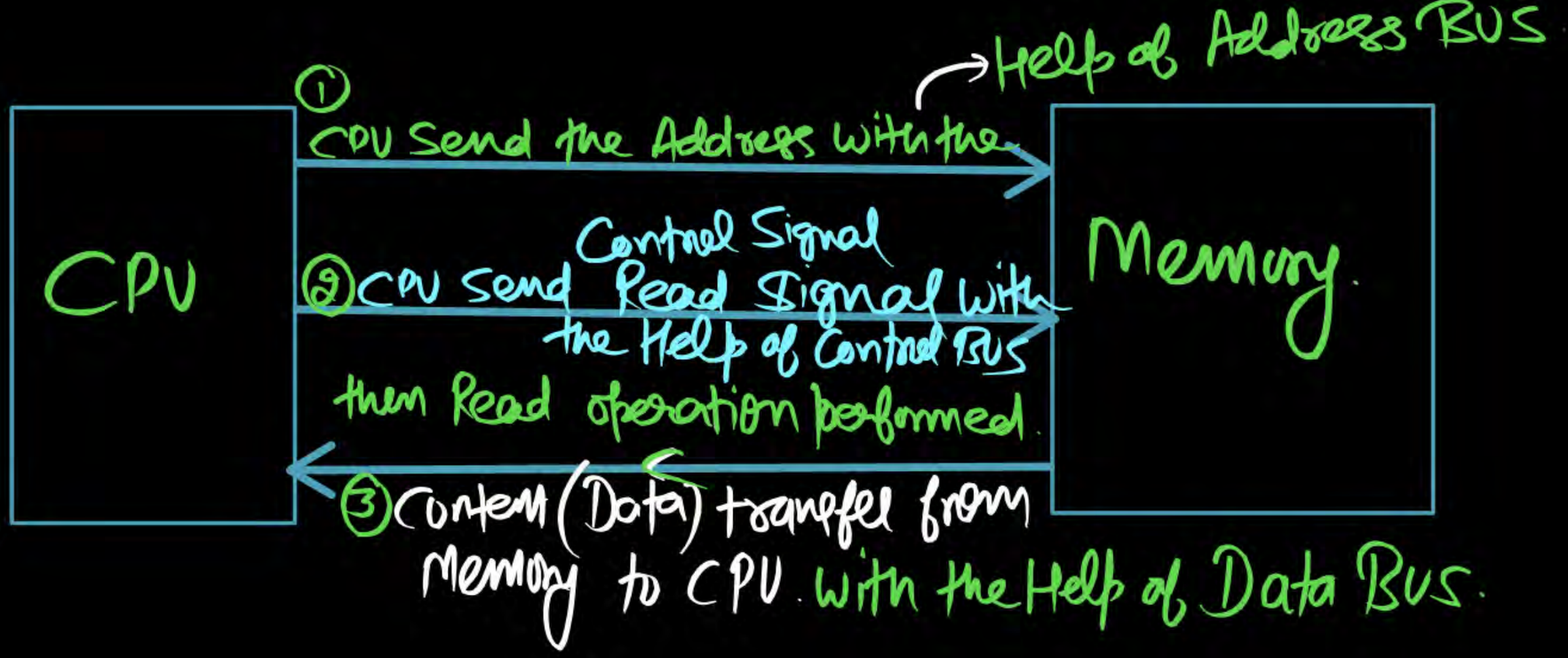
(LD)
LOAD : Memory Read

STORE (ST) : Memory Write.

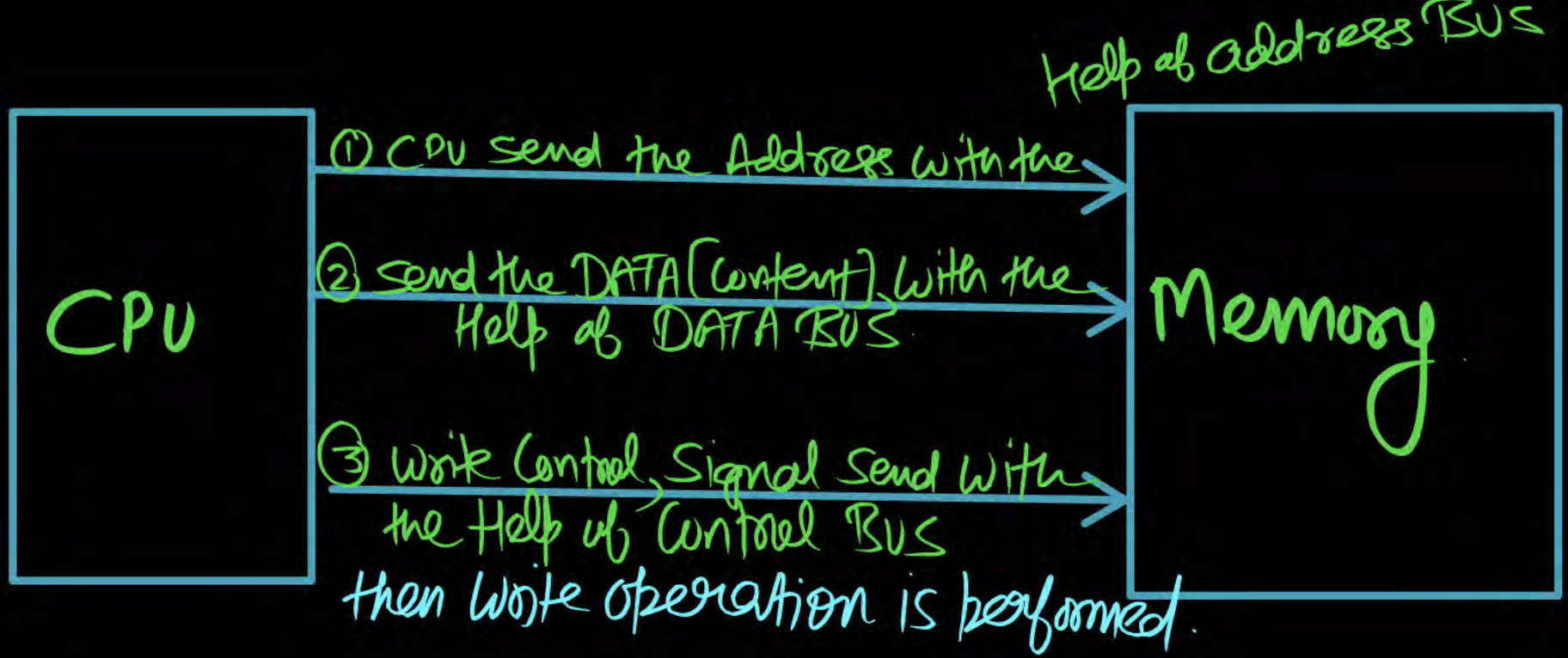
SYSTEM BUS:



Read operation (Memory Read)



Write operation (Memory Write).

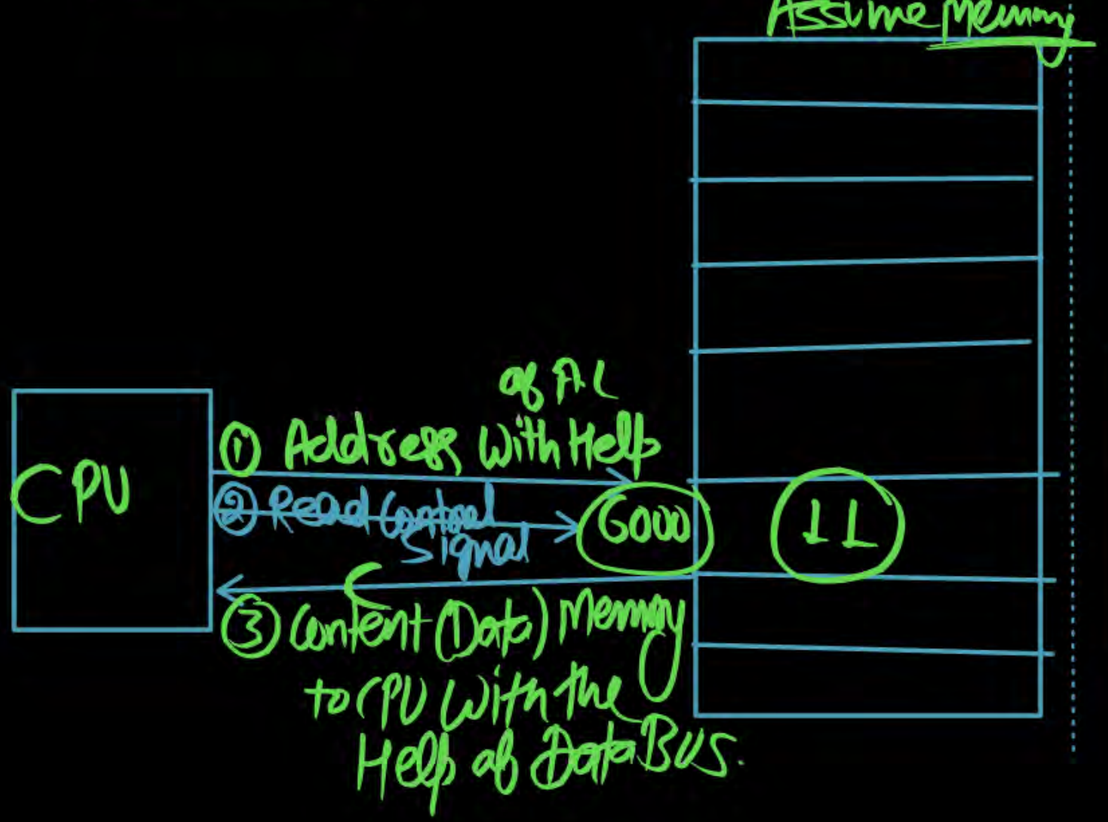


Memory Read

LOAD R_0 [6000]

$R_0 \leftarrow M[6000]$

$R_0 \leftarrow 11$



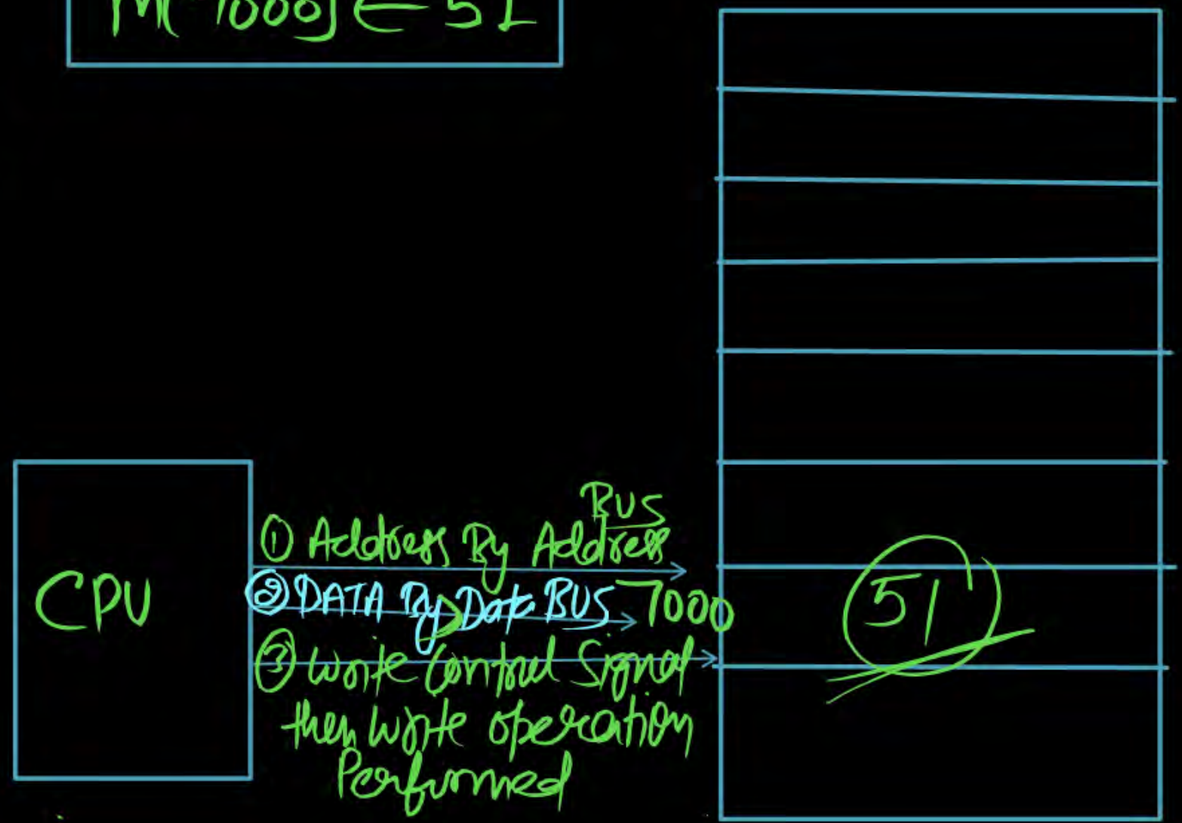
Memory Write

STORE [7000], R_L

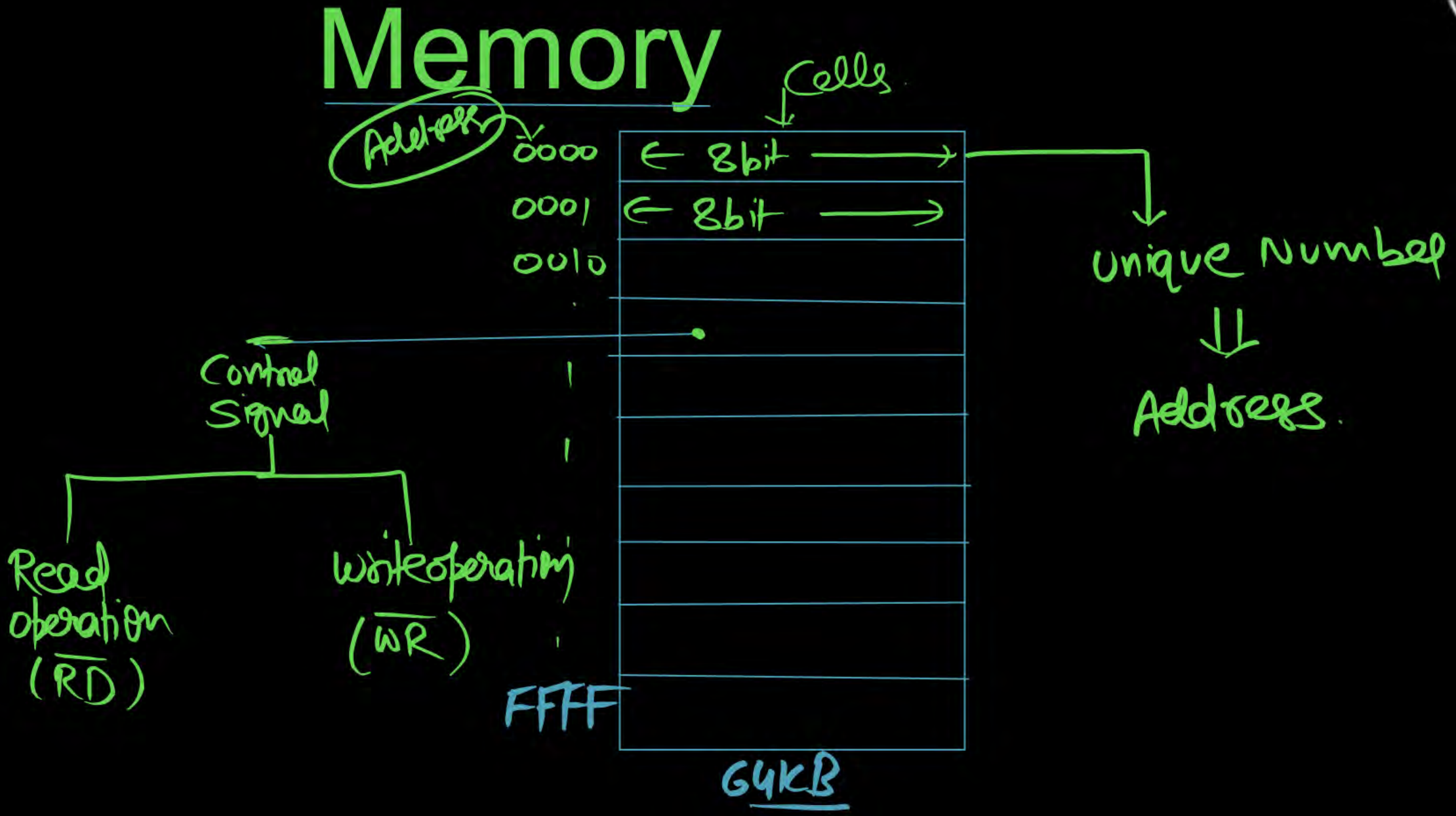
$M[7000] \leftarrow R_L$

$M[7000] \leftarrow 51$

Assume $R_1 = 51$



Memory


Cells
Address
0000
0001
0010
FFFF
← 8bit →
← 8bit →
Unique Number
Address
Control Signal
Read operation (RD)
Write operation (WR)
64KB

Memory

- Memory is organized into equal parts. each part is called cells.
- Each cell is Identified by a unique Number called as address.

Memory is Represented as $2^n \times m$.

n : Number of Address line (A.L)

m : Number of Data line (D.L)

A.L ⇒ Specifies the Capacity of the Memory

D.L ⇒ Specifies the Capacity of the Data [Cell Size]

n bit Address line Can Represent 2^n Memory Cells.

(Range 0 to $2^n - 1$) Memory Starts from '0'.

$2^1 = 2$

$2^2 = 4$

$2^3 = 8$

$2^4 = 16$

$2^5 = 32$

$2^6 = 64$

$2^7 = 128$

$2^8 = 256$

$2^9 = 512$

$2^{10} = 1024$ [1K].

1Byte = 8bit.

1Nibble = 4bit.

2^{10}_B = 1K (Kilo) B. $\approx 10^3$

2^{20}_B = 1M [Mega] B = [1024 KB] $\approx 10^6$

2^{30}_B = 1G (Giga) B [1024 MB] $\approx 10^9$

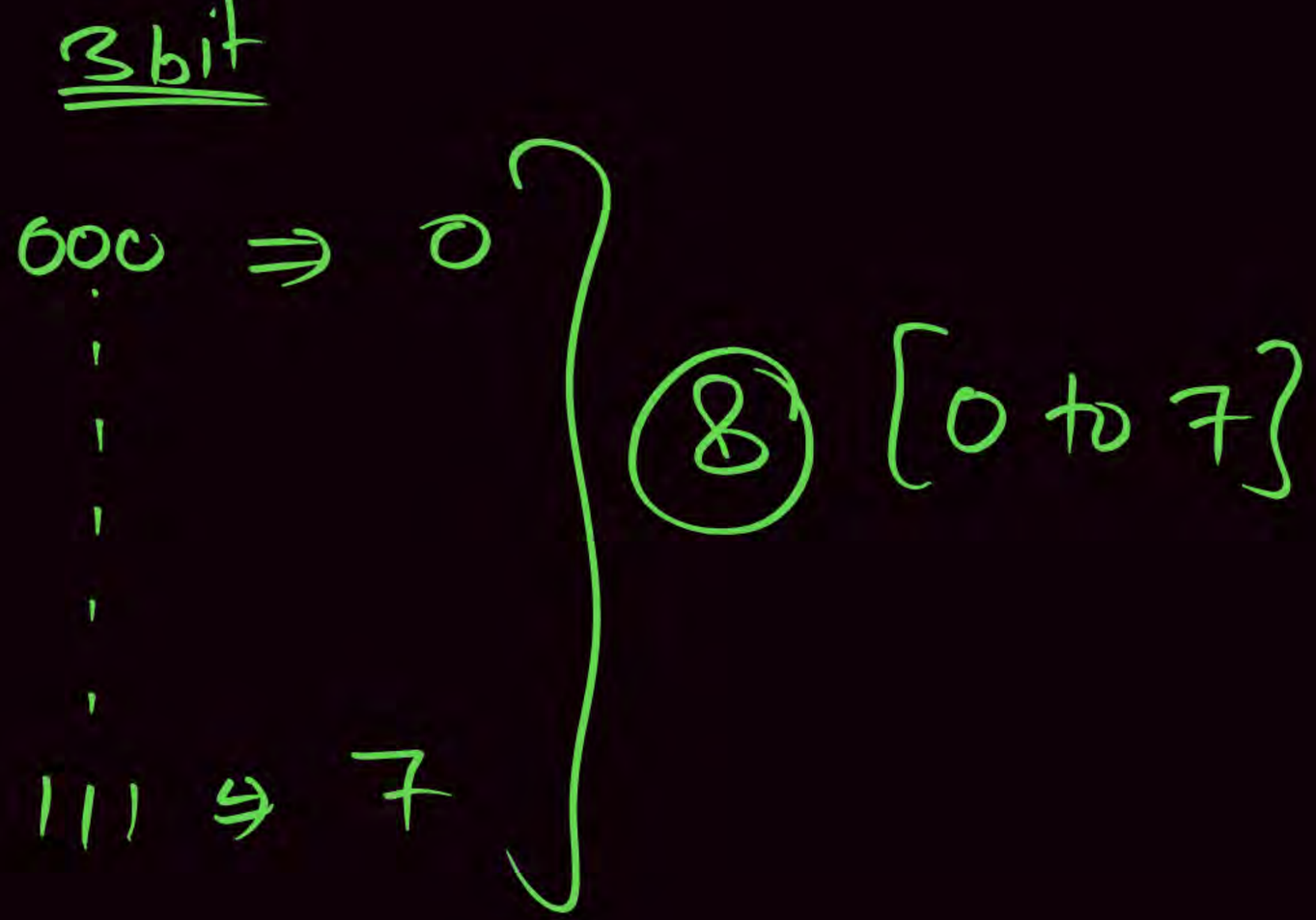
2^{40}_B = 1T (Tera) B [1024 GB] $\approx 10^{12}$

2^{50}_B = 1P (Peta) B [1024 TB]

2^{60}_B = 1E [Exa) B [1024 PB]

2^{70}_B = 1Z (zecta) B [1024 EB]

2^{80}_B = 1Y (Yotta) B [1024 ZB]


3bit
000 ⇒ 0
111 ⇒ 7
8 [0 to 7]

Memory is Represented as $2^n \times m$.

n: Number of Address line (A.L)

m: Number of Data line (D.L)

A.L ⇒ Specifies the Capacity of the Memory.

D.L ⇒ Specifies the Capacity of the Data [Cell Size]

n bit Address line Can Represent 2^n Memory cells.

(Range 0 to $2^n - 1$) Memory Starts from '0'.

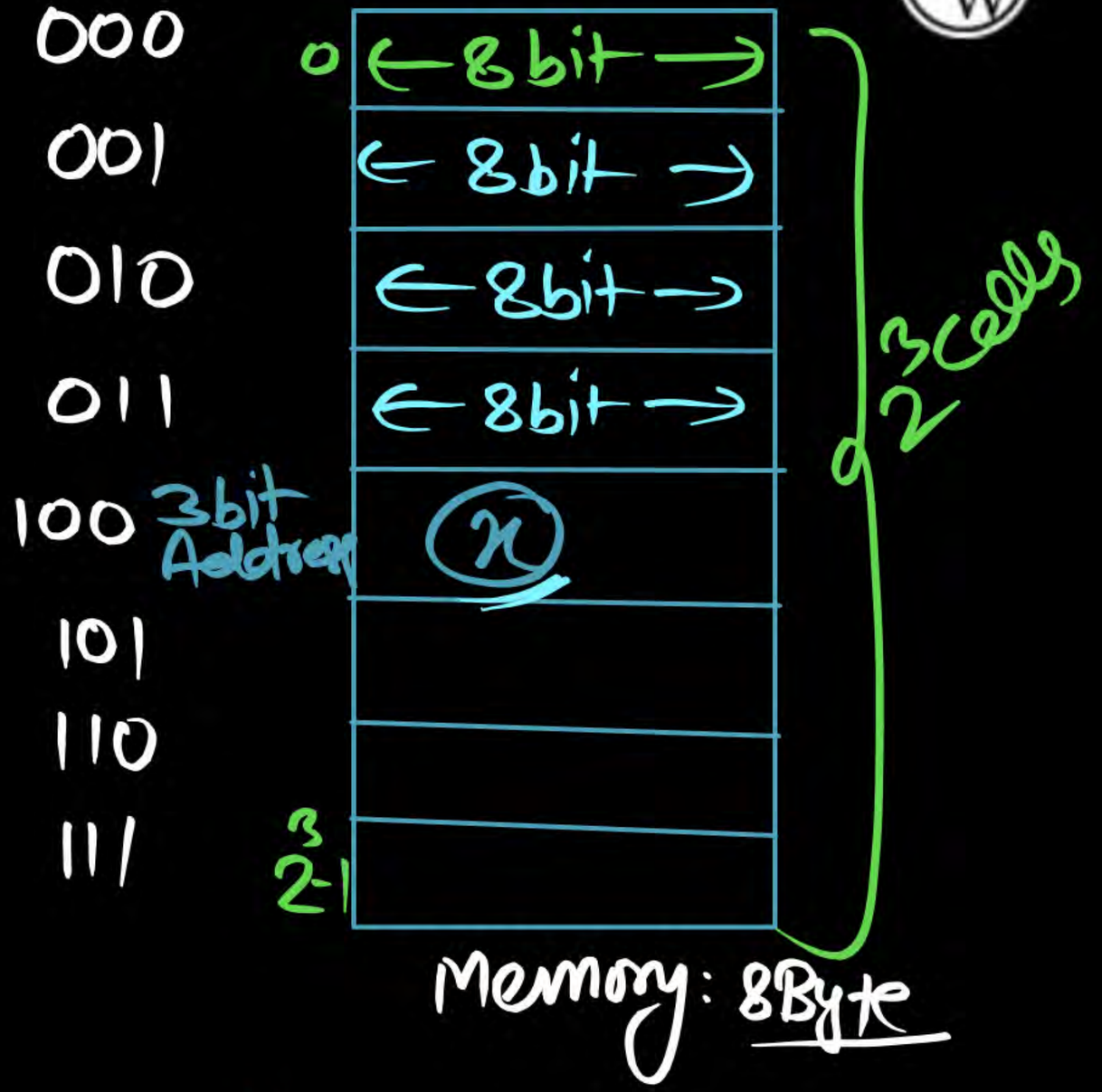
① 8 Byte

$2^3 \times 8$ bit

3 bit Address Line [AL]

8 bit Data Line [D.L]

3 bit Address line Can Represent 2^3 cells [0 to 2^3-1]



② 16 Byte

2^4 x 8bit

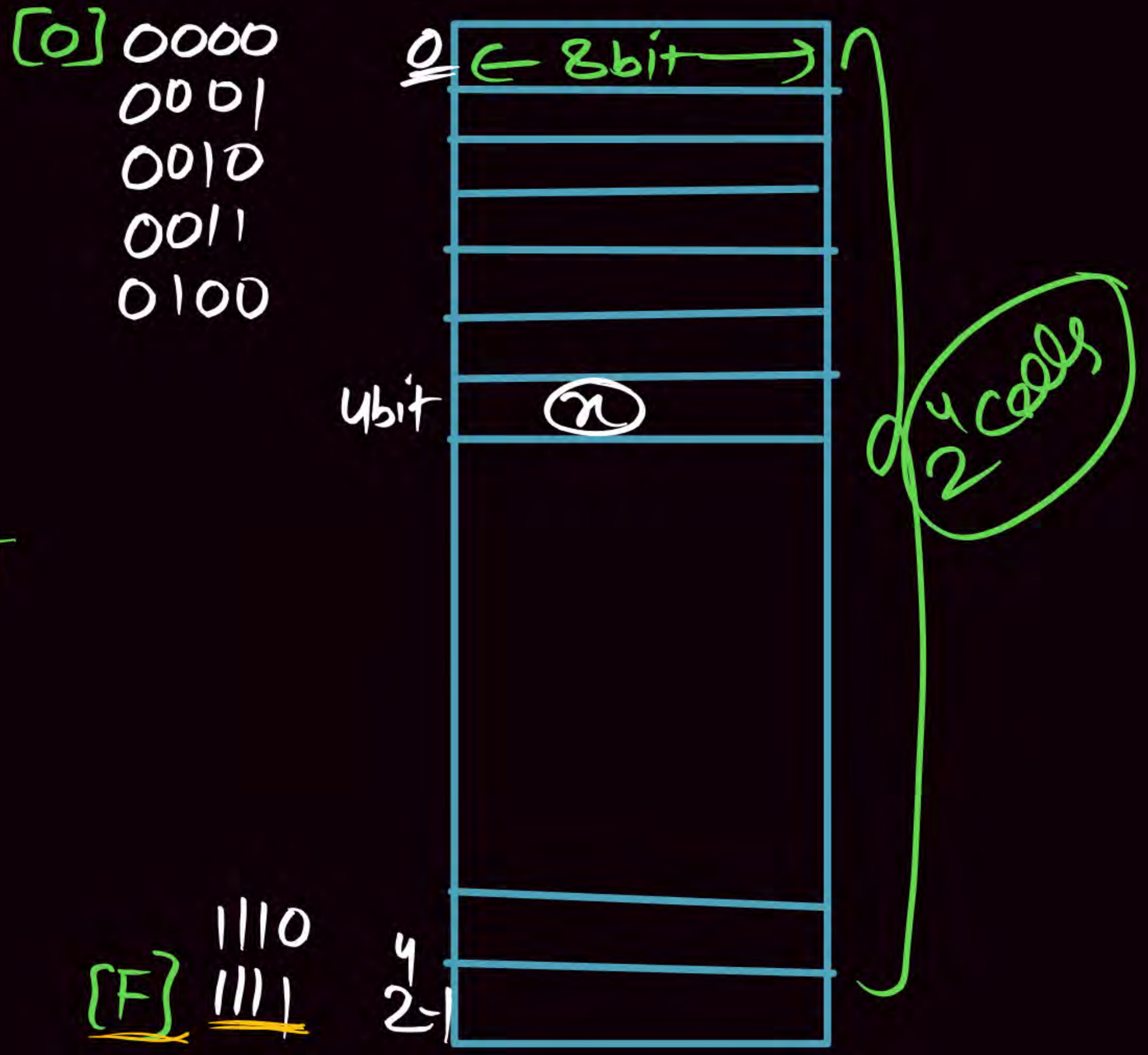
4 bit Adelress line

8bit Data line.

4 bit A.L Can Reporesent

2^4 Memory Cells.

[0 to 2^4 - 1]



③ 1 K Byte $[2^n \times m]$ [000] 0000 0000 00
0000 0000 01
0000 0000 10

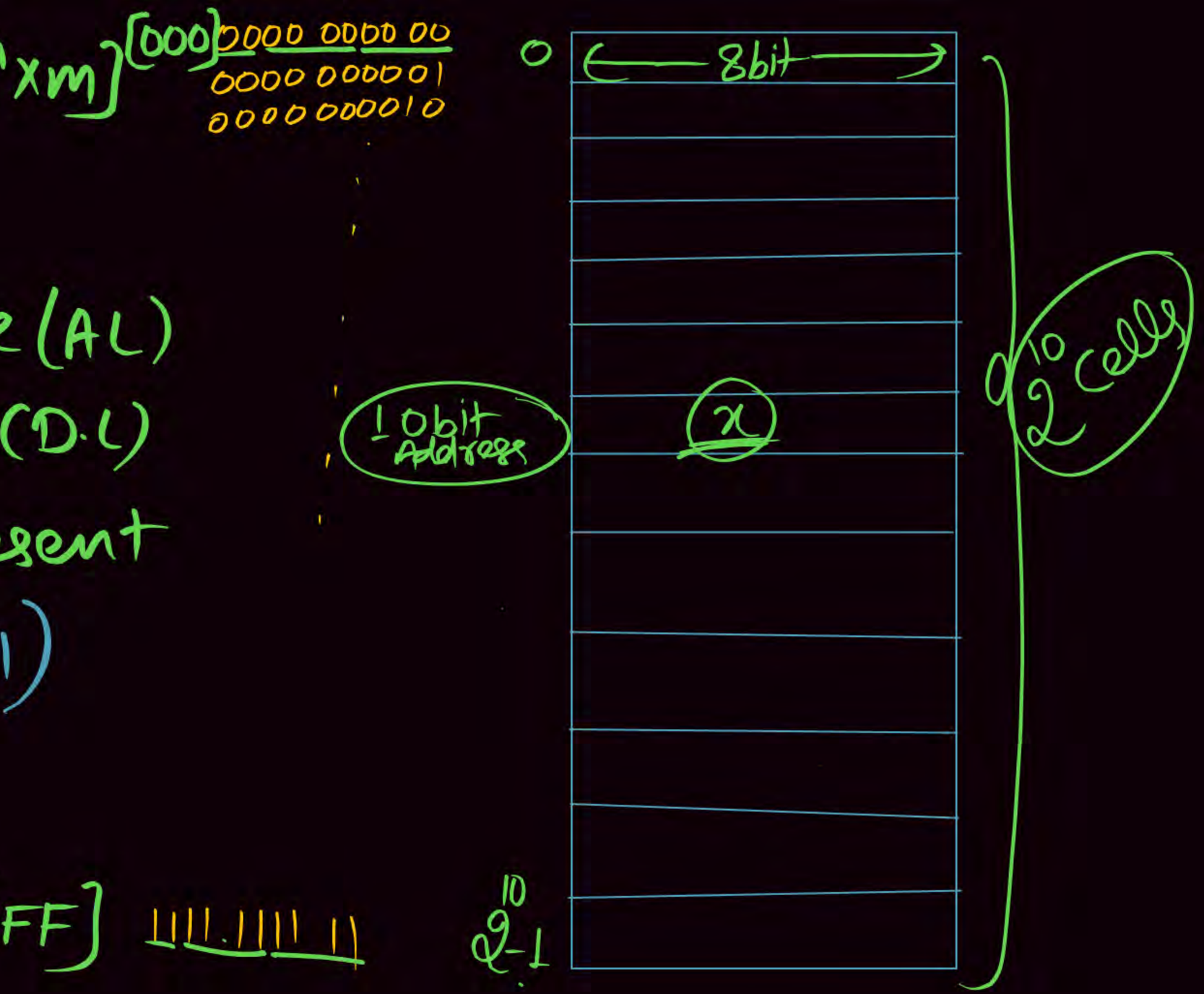
$2^{10} \times 8$ bit

10 bit Address line (A.L)

8 bit Data line (D.L)

10 bit A.L Can Represent

2^{10} Cells (0 to $2^{10}-1$)



[3FF] 11 1111 1111

$2^{10}-1$

④ 64 KByte

$2^6 \cdot 2^{10} \times 8$ bit

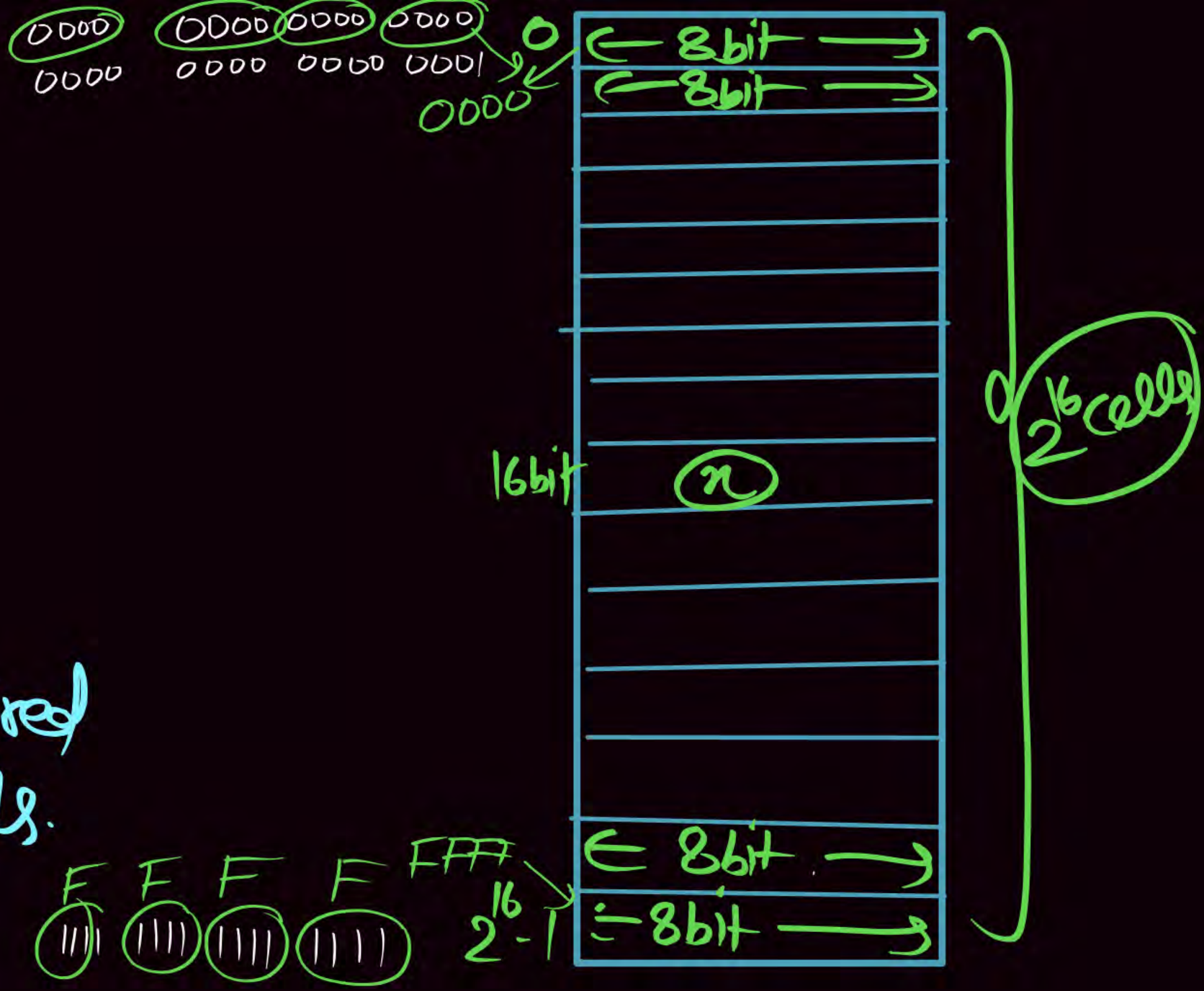
$2^{16} \times 8$ bit

16 bit Address line

8 bit Data line.

2^{16} memory cells.

16 bit Address are Required to Represent any Cells.



④ 64 KByte

⑤ 1MByte

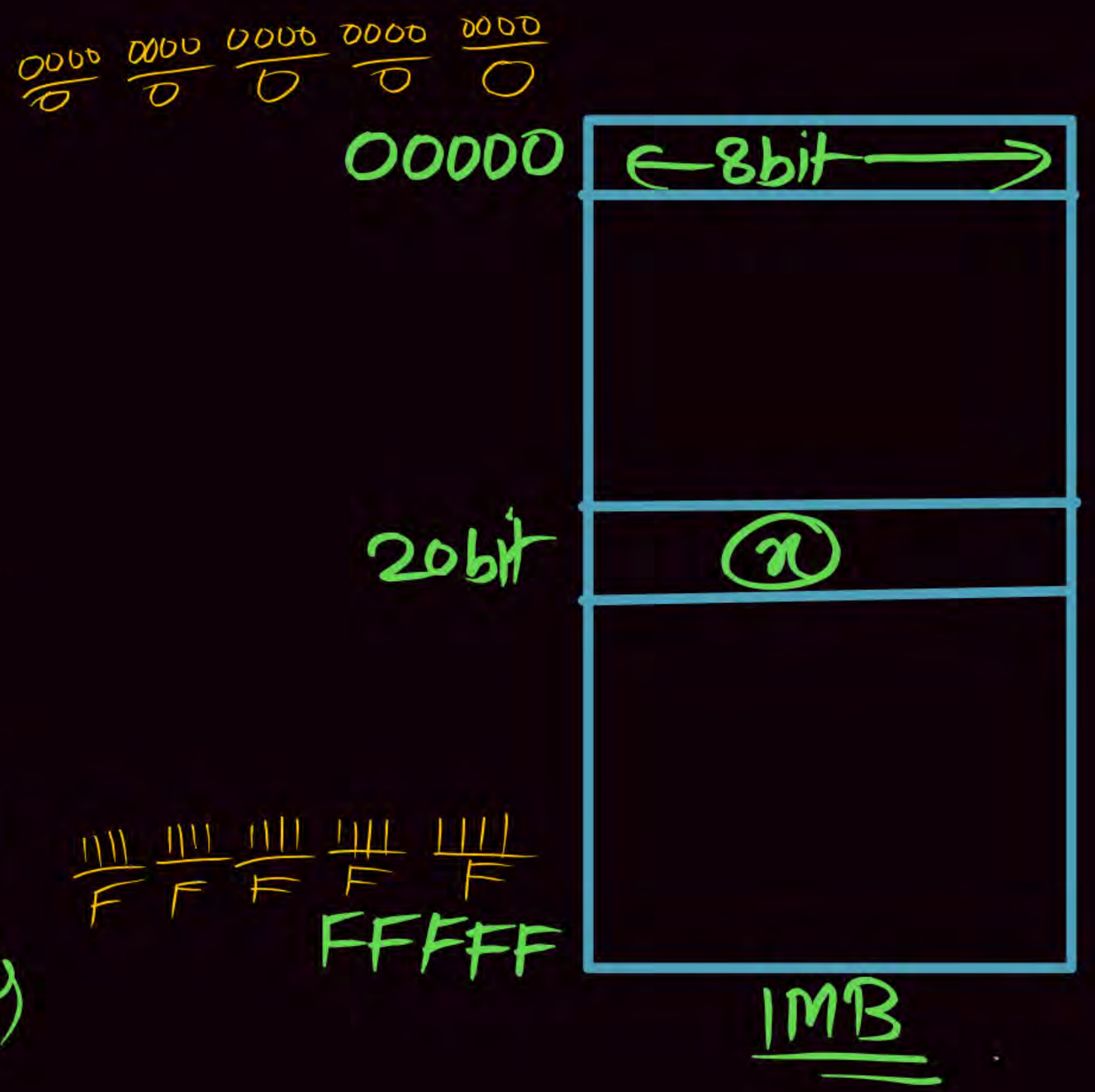
$2^{20} \times 8$ bit

20 bit Address

8 bit Data line

2^{20} memory Cells

20 bit Address Required to Represent Any Cells



⑥ 4GByte.

$2^2 \cdot 2^{30} \times 8bit$

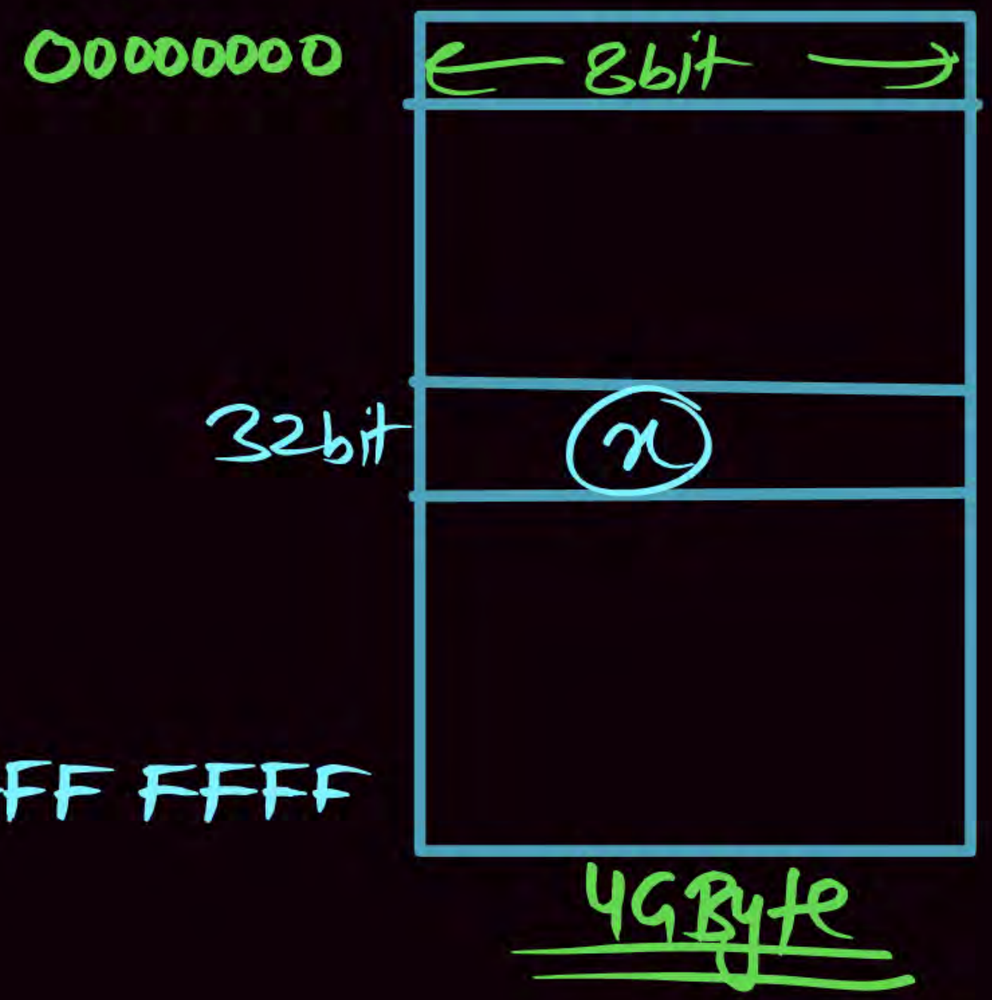
$2^{32} \times 8bit$

32 bit Address line (A.L)

8 bit Data line (D.L)

2^{32} Memory cells.

32bit Hexadecimal value



Q. The Capacity of a memory unit is defined by the Number of word Multiplied by the number of bits/word. How many separate address and data lines are needed for a memory of 64K×16?

(a) 8 address, 8 data line
(b) 16 address, 8 Data line
(c) 15 address, 16 Data line
(d) ~~16~~ address, 16 Data line

[GATE : 2Marks]

64K X 16

$2^6 \cdot 2^{10} \times 16$

$2^{16} \times 16$

16 bit Address
16 bit Data.

Q. Consider a system which has 1024 k words. Each word has the size of 32 bits then what is the capacity of memory in MB (Mega Byte) _____

1 Word = 32 bit
= 4 Byte

1024 k Words

$1024\ k \times 4\ Byte$

$2^{10} \cdot 2^{10} \times 2^{2}$ Byte

2^{22} Byte $\Rightarrow 2^{2} \cdot 2^{20}$ Byte

4 MByte

Q. A processor can support a maximum memory of 4GB, where the memory is word-addressable (a word consists of two bytes). The size of the address bus of the processor is at least____ bits.

[GATE-2016]

THANK YOU!