CS & IT ENGINEERING

Computer Organization & Architecture

1500 Series

Lecture No.- 07

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Recap of Previous Lecture

- Topic: Cache Memory
- Topic: Cache mapping Technique
- Topic: Cache Replacement Algorithm
- Topic: Cache Updating Technique

Topics to be Covered

- Topic: Cache Memory
- Topic: Disk Access Time
- Topic: Disk Addressing
- Topic: IO Interface & DMA

[MCQ]

#Q. Consider three cache organizations each of size 16 KB, with associativity as C_1 – 2 WSA, C_2–4 WSA and C_3–8 WSA, and in all such organizations the block size is of 32 bytes and the size of physical address is 30 bits. A (4 × 1) multiplexer having latency of "0.4" nsec along with "T" bits tag comparator latency of (T/10) nsec. If the hit latencies of cache organizations C_1, C_2 and C_3 are H_1, H_2 and H_3 then the relationship that can be established between hit latencies is _____

A $H_1 > H_2 > H_3$

B $H_1 > H_3 > H_2$

C $H_1 < H_3 < H_2$

D $H_1 < H_2 < H_3$

Ans (D)

$H_1 = 2.1$

$H_2 = 2.2$

$H_3 = 2.3$

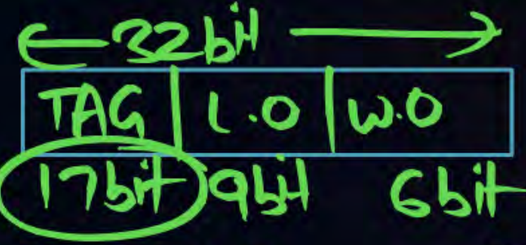
$= \frac{17}{10} + 0.4 = 2.1$

$= \frac{18}{10} + 0.4 = 2.2$

$= \frac{19}{10} + 0.4 = 2.3$

[NAT]

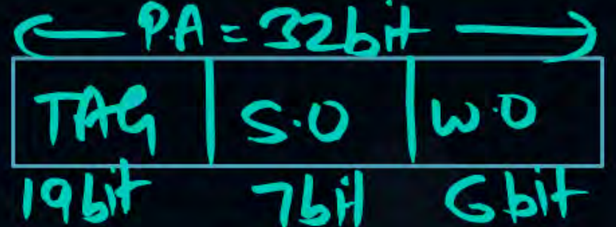
#Q. Consider a direct mapped cache of size 32 KB and block size of 64 bytes. CPU generates 32- bit addresses. The difference in number of bits in tag meta(Memory) data in this organization with respect to 4-way set associative implementation is 1024 Ans



Ans (1024)

$\#lines = \frac{32KB}{64Byte} = \frac{2^{15}}{2^6} = 2^9$

Tag Memory Size = $17 \times 2^9 = 8704$



$\#SET = \frac{2^9}{2^2} = 2^7$

Tag Memory = 19×2^9
= 9728

$$9728 - 8704$$

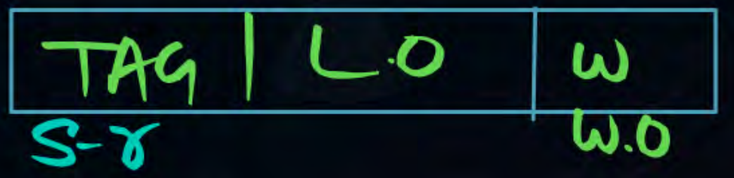
$$= 1024 \text{ Ans}$$

[MCQ]

#Q. The main memory address is divided into three field. The least significant 'w' bits can identify a unique word or byte within a block of main memory. Main memory has 2^s blocks to represent there blocks we need 's' bits. The cache logic interprets there 's ' bit as a tag of 's–r' bits and a line field of 'r' bits.

The number of lines in cache will be

After Mapping



A 2^r

B 2^{r+w}

C 2^{s+w}

D undetermined

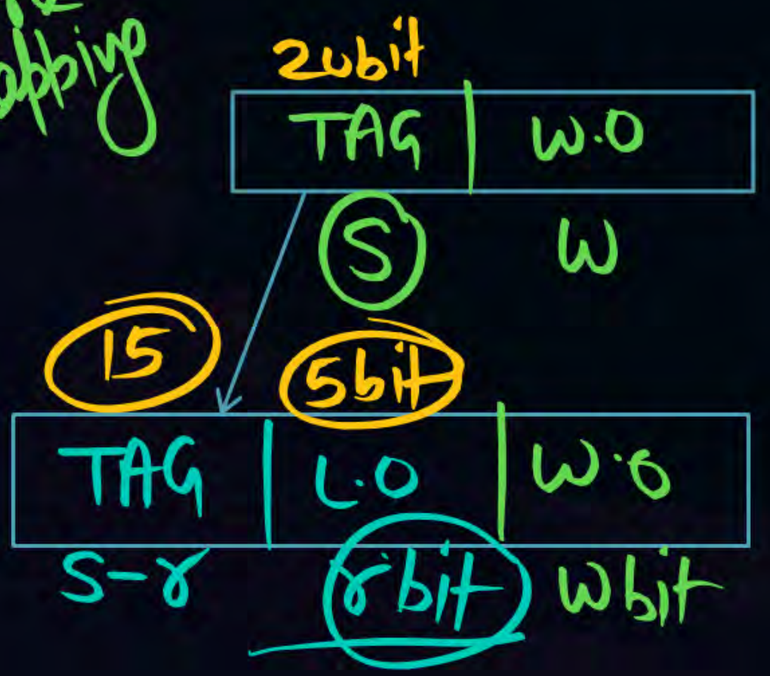
$\#mm\ Blocks = 2^{s}$

Before Mapping

$L.O = S - (S - \gamma)$

$= S - S + \gamma$

$= \gamma$



[MSQ]

#Q. Consider a computer system with a byte addressable main memory of size 2^32 byte and 64 k Byte write back direct mapped cache with block of size 64 byte. Cache controller maintains the tag information for each cache block comprising of the following 1 bit for valid/invalid and 1 modified bit.Which of the fllowing is correct?

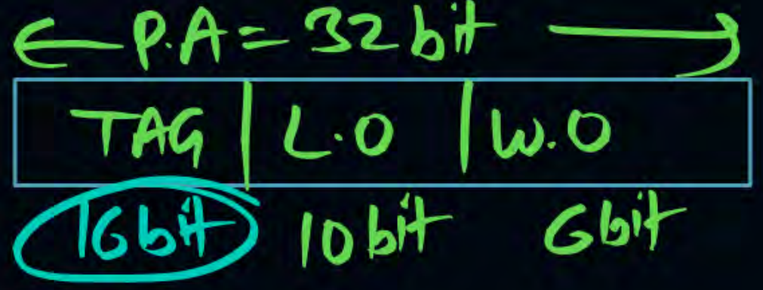
A. Tag memory size is 16 K bits.

B. Tag memory size is 18 k bits.

C. A total of 2^{16} main memory block map to each cache line

D. A total of 2^{18} main memory block map to each cache line.

Ans (B) & (C)



$$\#\text{Lines} = \frac{\text{CM Size}}{\text{Block Size}} = \frac{64\text{KB}}{64\text{B}} = 2^{10}$$

TAG = 16 bit $\Rightarrow$ 2^{16} Main Memory are fighting for each Cache Line.

Tag Entry Size = 16 + 1 + 1 = 18 bits

Tag Memory Size = #Lines × Tag entry Size

$\Rightarrow 2^{10} \times 18$

= 18K bits Ans

[MCQ]

#Q. Consider a p-way set associative cache with (8*p) blocks. Assume that main memory has (16*p) blocks. What is the tag size in this organization?

A $\text{Log}_2 P + 4$

B $\text{Log}_2 P - 1$

C $\text{Log}_2 P + 1$

D None of these

Done

[MSQ]

Consider a computer system which has 4GB, byte addressable main memory and cache size 8MB, 4way set associative cache memory with block size 4096 byte. (2^{12})
Consider the following six physical addresses represented in a hexadecimal notation.

$A_1 = 0 \times 47\ CA4\ ABC$
$A_2 = 0 \times 56\ ECF\ 38D$
$A_3 = 0 \times 29\ FDB\ 4CF$
$A_4 = 0 \times 38\ 8A4\ DAC$
$A_5 = 0 \times C3\ EFC\ A47$
$A_6 = 0 \times AB\ 9DB\ 128$

Which of the following is correct ?

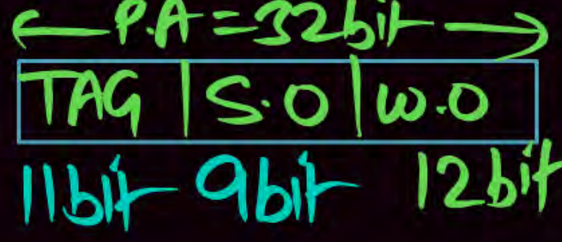
A. A_1 and A_4 are mapped to the same cache set.

B. A_2 and A_5 are mapped to the same cache set.

C. A_2 and A_5 are mapped to the different cache set.

D. A_3 and A_6 are mapped to the same cache set.

Ans (A) (C) & (D)



$$\#Lines = \frac{CM\,Size}{Block\,Size} \Rightarrow \frac{8MB}{4096B} \Rightarrow \frac{2^{23}B}{2^{12}B} = 2^{11}\ Lines$$

$$\#SET = \frac{\#Lines}{N\text{-}way} = \frac{2^{11}}{2^{2}} = 2^{9}\ set$$

$S.O = 9bit$

A1 : 0x 47 CA4 ABC

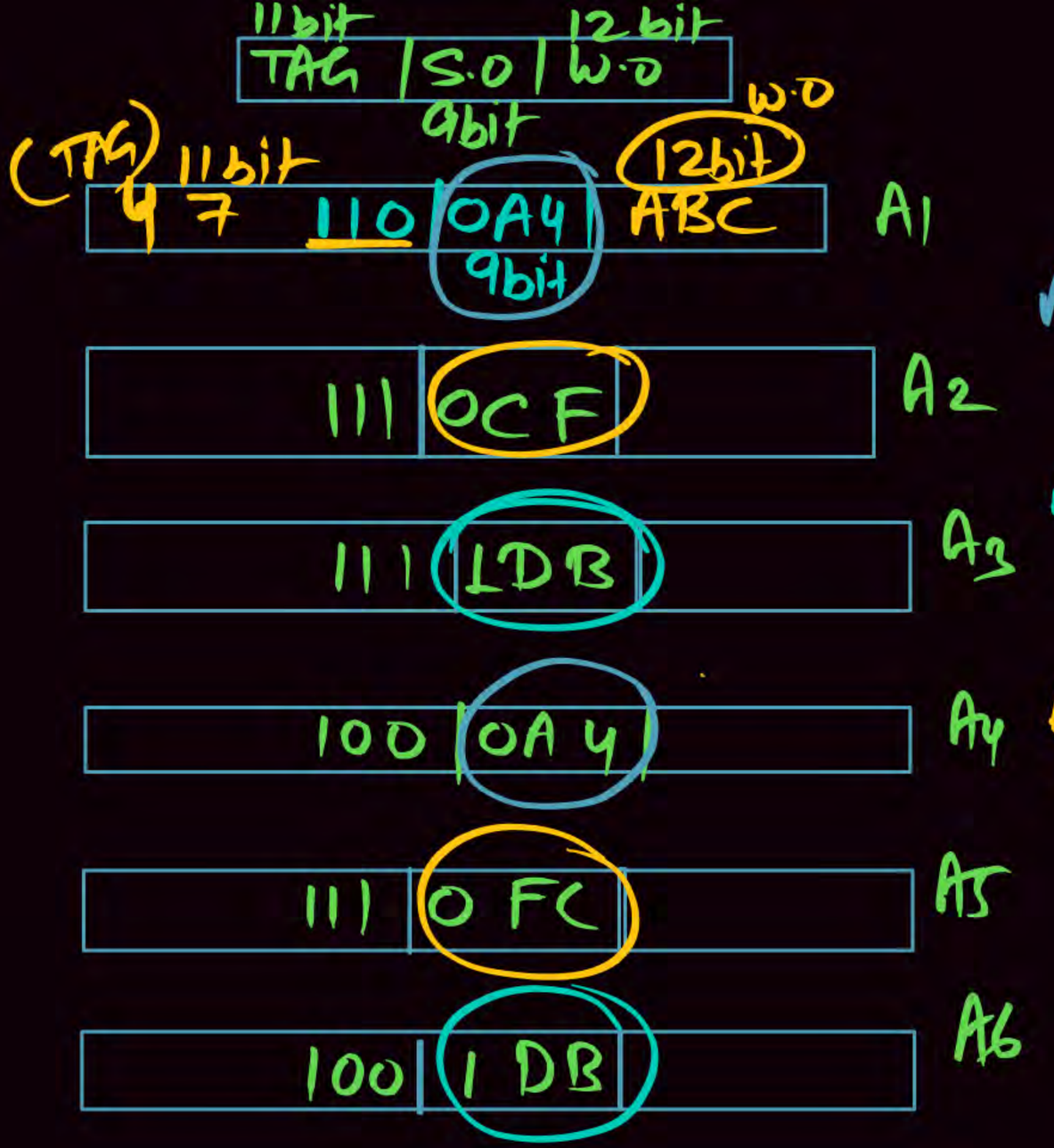
A2: 0x 56 ECF 38D

A3: 0x 29 FDB 4CF

A4: 0x 38 8A4 DAC

A5: 0x C3 EFC A47

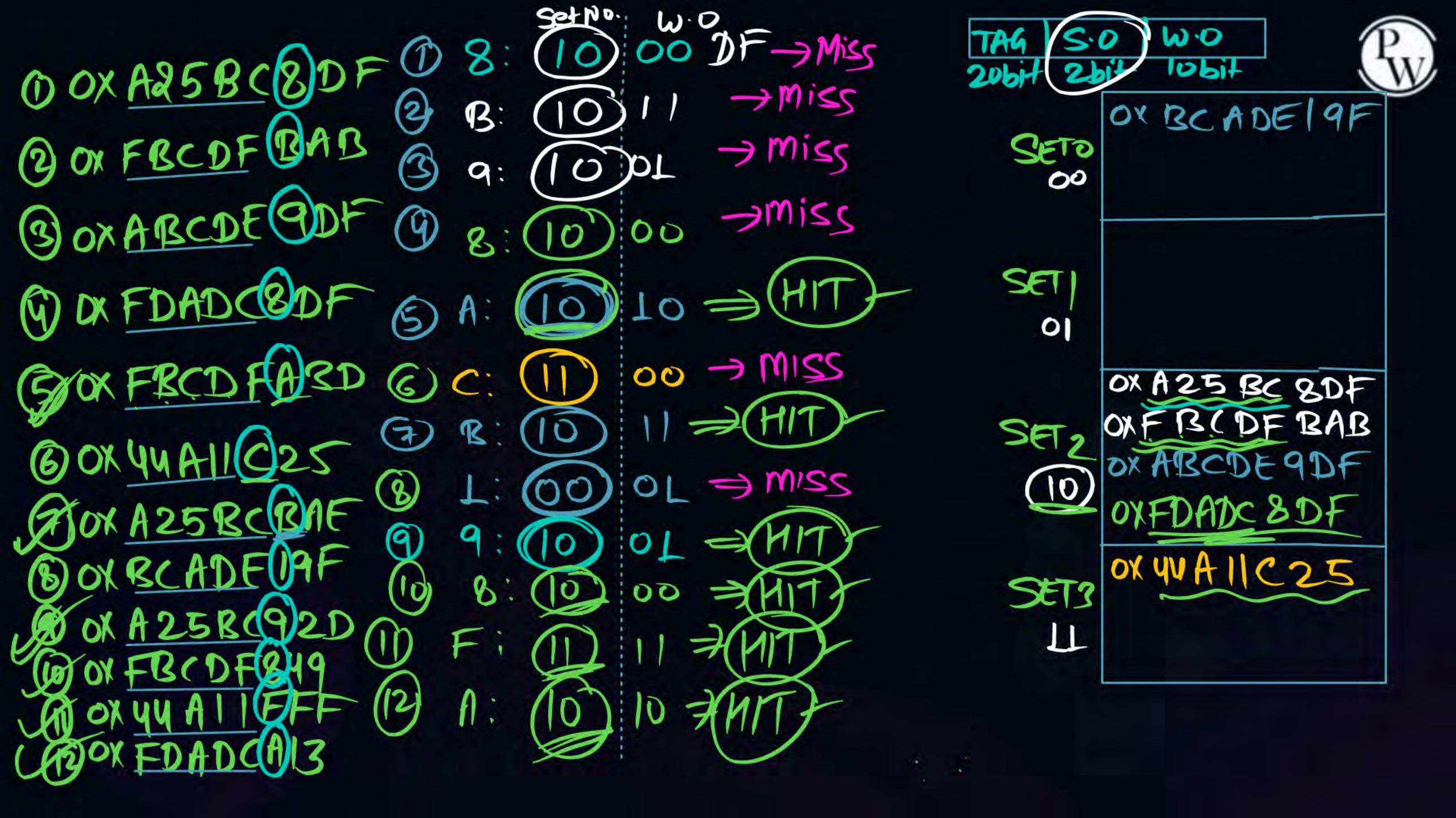
A6: 0x AB 9DB 128



A1 & A4 Same Cache Set.

A3 & A6 Same Cache Set

A2 & A5 Different Cache Set.


Set No.
W.O
1 0x A25BC8DF
2 0x FBCDFBAB
3 0x ABCDE9DF
4 0x FDADC8DF
5 0x FBCDFA3D
6 0x 44A11C25
7 0x A25BCBAE
8 0x BCADE19F
9 0x A25BC92D
10 0x FBCDF849
11 0x 44A11EFF
12 0x FDADCA13
1 8: 10 00 DF → Miss
2 B: 10 11 → miss
3 9: 10 01 → miss
4 8: 10 00 → miss
5 A: 10 10 ⇒ HIT
6 C: 11 00 → MISS
7 B: 10 11 ⇒ HIT
8 1: 00 01 ⇒ miss
9 9: 10 01 ⇒ HIT
10 8: 10 00 ⇒ HIT
11 F: 11 11 ⇒ HIT
12 A: 10 10 ⇒ HIT
TAG | S.O | W.O
20bit | 2bit | 10bit
SET 0
00
0x BCADE19F
SET 1
01
SET 2
10
0x A25BC8DF
0x FBCDFBAB
0x ABCDE9DF
0xFDADC8DF
SET 3
11
0x 44A11C25

Disk

1. Disk Structure
2. Disk Access time
3. Disk Addressing

I/O Interface

[MSQ]

Consider a disk which has 16 platter each platter has two surfaces. Every surface has 1k tracks and every track is further divided into 512 sector and every sector can store the 2kB data. Then which of the following is correct?

(i) $16 \times 2 \times 1k \times 512 \times 2kB$

$2^4 \times 2^1 \times 2^{10} \times 2^9 \times 2^{11} \Rightarrow 2^{35}$ Byte = 32GB

(ii) #bits $= 2^4 \times 2^1 \times 2^{10} \times 2^9 = 2^{24}$ = 24 bits

A The capacity of Disk is 16 GB.

B The capacity of Disk is 32 GB

C 24 bits are required to identify any particular sector of the disk.

D 35 bits are required to identify any particular sector of the Disk.

Ans (B) & (C).

[NAT]

Consider a typical disk that rotates at 12000 RPM (Rotation per minutes) and has a transfer rate of 30 MBps [30×10^6 bytes/sec]. If the average seek time of the disk is thrice the average rotational delay and the controllers transfer time is 40 times the disk transfer time. The average time (in milliseconds) to read or write 256 byte sector of the disk is 10.35 msec Ans

Disk Access time (Tavg) = Avg S.T + Avg R.L + D.T.T + Controller overhead

Avg (10.35)

12000 Rotation in 60sec

In 1 Rotation = $\frac{60}{12000/200}$ $\Rightarrow$ $\frac{1}{200}$ sec $\times \frac{1000}{1000}$

$\Rightarrow$ 5 msec

R.L = $\frac{1}{2} \times 5$ msec $\Rightarrow$ **R.L = 2.5 msec**

Avg S.T = 3* R.T $\Rightarrow$ 3 X 2.5 = 7.5 msec

Avg S.T = 7.5 msec

30MBps

30×10^6 Byte ——————— 1 Sec.

256 Byte → $\frac{256\,B}{30 \times 10^6\,B}$ sec ⇒ $\frac{250}{30} \times 10^{-6}$ sec

D.T.T = 8.33×10^{-6} sec ⇒ 0.00853×10^{-3} sec ⇒ 8.53×10^{-6} sec.

D.T.T = 0.00853 msec

Controller overhead = $40 \times (0.00853)$ ⇒ 0.341 msec.

D.A.T = 7.5 + 2.5 + 0.00853 + 0.341

= 10.35 msec Ans

[NAT]

A hard disk has 63 sector per track, 20 platters each with 2 recording surface and 1600 cylinders.

The address of a sector is given as a triple <C, H, S> where C is the cylinder number, h is the surface number and S is sector number. Thus the 0th sector is addressed as <0,0,0> and the 1st sector is <0,0,1> and So on.

The sector number of the corresponding address < 600, 38, 47 > is_____.

(#track | Cylinder)

Total # Surface = 2×20 = 40 Surface

#Sector Per track = 63 sector.

<C h S>
<600, 38, 47>

To Cross (Traversed) 600 Cylinder (0-599) ⇒ 600 X 40 X 63 = 1512000

To Cross (Traversed) 38 Surface (0-37) = 38 X 63 = 2394

To Cross 47 sector (0-46) = 47 = 47

1514441.

$\langle c, h, s \rangle$ $\quad$ $\overset{c}{\langle} \overset{h}{600}, \overset{s}{38}, 47 \rangle$

$$\text{Sector Number} = S + ST * h + \underbrace{ST * TC}_{SC} * C$$

$47 + 63 * 38 + 63 * 40 \times 600$

$= 1514441$ Ans

ST: # Sector per track

TC: # Track per cylinder

SC: # Sector per cylinder.

[MCQ]

Suppose, in a disk addressing cylinder number is C, surface number is P and sector number Q. Suppose, number of sectors per cylinder are R and number of sectors per track are S then, the sector sequence number will be:

C h S

<C, h, S> ⇒ <C, P, Q>

Sector Number = Q + ST * P + ST * TC * C

Q | S | SC(R)

#sector/cylinder

Sector Number = Q + SP + RC

A. CR + PS + Q

B. PRQS + Q

C. (CR + PS)Q

D. None of the above

Ans(A)

Number of Records per Sector = $\frac{512B}{256B}$ = 2 Record per Sector

Sector per track = 63

Tracks per cylinder = 10

Sector per Cylinder = 63 X 10 = 630 sector

Records Per Cylinder = 630 X 2 = 1260 Records Per Cylinder

Total # Records = 92,900

Cylinder Needed = $\left\lceil \frac{92,900}{1260} \right\rceil$ = 74 Ans

[NAT]

#Q. A device With data transfer rate 10 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 4 μsec. The byte transfer time between the device interface register and CPU or memory' is negligible. The minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode is (25) Ans

Prog I/O : 10KB — 1 sec

1Byte — $\frac{1}{10K}$ sec ⇒ 100 μsec.

Ans(25)

Interrupt = 4 μsec

Speedup Factor = $\frac{100}{4}$ = (25) Ans

$$S = \frac{\text{Performance of Interrupt}}{\text{Performance of Programmed I/O}}$$

$$\Rightarrow \frac{1/ET_{Interrupt}}{1/ET_{Prog}} \Rightarrow \frac{ET_{Prog}}{ET_{Intr}}$$

$$\Rightarrow \frac{100}{4} = 25$$

[MCQ]

#Q. On a non-pipelined sequential processor, a program segment, which is a part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.

Initialize the address register
Initialize the count to 500
LOOP: Load a byte from device
Store in memory at address given by address register
Increment the address register
Decrement the court
If count! = 0 go to LOOP

Assume that each statement in this program is equivalent to a machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute.

The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DM controller requires 20 clock cycles for initialization and other overhead. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from interrupt driven program-based input-output?

A 3.4

B 4.4

C 5.1

D 6.7

[NAT]

The size of the data count register of DMA controller is 16 bits. The processor needs to transfer a file of 28,824 kilo bytes from disk to main memory. The memory is byte addressable. The minimum number of times the DMA controller need to get the control of the system bus from the processor to transfer the file from the disk to main memory is _____.

Count = 16 bit $\Rightarrow 2^{16}$ Byte $\Rightarrow$ 65,535 B

Total File Size = 28,824 KByte

$$\#\text{Times DMA Controller Need the Control} = \frac{28824 \times 1024\ B}{65535\ B}$$

$= 451$ Ans

[NAT]

#Q. A hypothetical DMA is designed to transfer the data from i/o device to main memory under burst transfer mode. The count register size is 36 bits and gets the control of the system buses 8 times then the maximum size of the data transferred by controller is (in Giga Byte) 512 Ans

Count Register = 36 bits $\Rightarrow 2^{36}$ Byte. in One time

In 8 time $\Rightarrow 2^{36} \times 8(2^3)$

$\Rightarrow 2^6 \times 8^3 \times 2^{30} = 2^9$ GB.

$= 512$ GB Ans

Common Data for next Four questions:

A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces and 1000 cylinders. The address of a sector is given as a triple ⟨c,h,s⟩, where c is the cylinder number, h is the surface number and s is the sector number. Thus, the 0^{th} sector is addressed as⟨0,0,0⟩, the 1^{st} sector as ⟨0,0,1⟩, and so on.

Surface = 10 × 2 = 20 Surface

sector per track = 63

Sector per Cylinder = 20 × 63

= 1260 sector per Cylinder.

: 20

[MCQ]

#Q. The address ⟨400,16,29⟩ corresponds to sector number:

(i) To cross 400 Cylinder (0-399) = 400 × 20 × 63 = 504000

(ii) To cross 16 Surface (0-15) ⇒ 16 × 63 = 1008

(iii) To cross 29 Sector (0-28) = 29 = 29

505037

A 505035

B 505036

C 505037

D 505038

[MCQ]

#Sector Per Cylinder $= 20 \times 63 = 1260$

#Q. The address of 1039th sector is

A ⟨0,15,31⟩

B ⟨0,16,30⟩

C ⟨0,16,31⟩

D ⟨0,17,31⟩

Ans (C)

@ $15 \times 63 + 31 = 976$

(b) $16 \times 63 + 30 = 1038$

(c) $16 \times 63 + 31 = 1039$

(d) $17 \times 63 + 31 = 1102$

[MCQ]

#Q. In the Previous Question what is the sector address of 4734th sector is ?

<c, h, s>

$$c = \text{Cylinder No.} = \left\lfloor \frac{\text{Given Sector}}{\#\text{Sector Per Cylinder}} \right\rfloor$$

$$h = \text{Surface No.} = \left\lfloor \left[\text{Given Sector} \,/\, \#\text{sector Per Cylinder} \right] \Big/ \#\text{Sector Per track} \right\rfloor$$

Q 4734

#Sector Per Cylinder = 1260

$$C = \left\lfloor \frac{4734}{1260} \right\rfloor = 3$$

$4734 - 3 \times 1260$

$\Rightarrow 4734 - 3780$

$= 954$

$$h = \text{Surface} = \left\lfloor (4734 \% 1260) / 63 \right\rfloor = \frac{954}{63} = \lfloor 15.14 \rfloor = 15$$

$$S = \text{Sector} = 954 - 15 * 63 = 9$$

<3, 15, 9> Ans

[MCQ]

#Q. In the Previous Question what is the sector address of 5433 th sector is ?

$$c = \left\lfloor \frac{5433}{1260} \right\rfloor = \lfloor 4.311 \rfloor = 4$$

$5433 - 4 \times 1260$

$= 393$

$$h = \left\lfloor \frac{393}{63} \right\rfloor = \lfloor 6.2 \rfloor = 6$$

$$s = 393 - 6 \times 63 = 15$$

$\langle 4, 6, 15 \rangle$ Ans

2 mins Summary

- Topic: Cache Memory
- Topic: Disk Access Time
- Topic: Disk Addressing
- Topic: IO Interface & DMA

THANK - YOU