Branch : CSE & IT Batch - (Hinglish)

Computer Organisation and Architecture

Cache Memory

DPP

[MCQ]

1. Consider a processor that can support a maximum memory of 8GB, where the memory is word-addressable (a word consists of 2 bytes). Then the size of the address bus of the processor is at least _____bits.

(a) 31 (b) 32
(c) 33 (d) 34

[NAT]

2. Assume a direct mapped cache having 8 cache lines, each cache line consists of 2 words and each word is of one byte. The address bus consists of 7 bits, then the tag field of the cache consists of _____ bits.

[NAT]

3. Assume a 32-bit addressable physical memory and 2 MB cache block of size 8 kB each, then how many bits are required in the tag field of the cache address if the cache is 4-way set associative _____

[MCQ]

4. Consider a 16-Kbyte cache with the following features, each block will hold 32 bytes of data (not including tag, valid, etc …), The cache would be 2-way set associative, physical addresses are 32 bits and data is addressed to the word and words are of 32 bits long. Then how many blocks would be in this cache and how many bits of tag are stored with each block entry?

(a) 512, 19 (b) 512,22
(c) 256, 20 (d) 512, 21

[MCQ]

5. Consider a 16 KB, two-way associative cache with 32-Byte cache line and a 64 bits address space, there will be p bits used for index. Let suppose if that same cache were fully associative, you need q bits to be used for the index then the value for p + q = _____.

(a) 6 (b) 7
(c) 8 (d) 9

[NAT]

6. Consider a system having 512KB, 16-way set associative L_2 cache with a 128 byte cache line size, Then how many cache lines are present? ____

[NAT]

7. Assume a cache with 32-bit address, 768 blocks and a block size of 128 bytes, tags are 17 bits then what is the associativity of the cache_____?

[MCQ]

8. Assume a direct mapped cache memory with 16 cache block (0 – 15) and a main memory having 256 blocks (0 to 255). Assume that, initially the cache did not have any memory block, Consider the following sequence of memory block references:
3, 180, 43, 2, 191, 881, 190, 14, 181, 44, 186 and 253, Then which memory blocks will be present in the cache after the above sequence of memory block reference?

(a) 2,3, 180, 43, 2, 191, 190, 88, 14, 181, 44, 186
(b) 2,3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 181, 44, 186, 253
(c) 2, 3, 180, 181, 881, 186, 43, 44, 253, 14, 191
(d) None of the above

[MCQ]

9. Assume the access patterns x, y, z, y, x where each letter corresponds to a unique cache block and also assume that there was no access to any block before this and all conflicts are random. Then what is the probability of the second access to x being a hit on a direct mapped cache with 4 line (closet to)?

(a) 40% (b) 50%
(c) 80% (d) 100%

[MCQ]

10. Which one is the fastest cache mapping function among the following?

(a) Fully associative mapping
(b) Set associative mapping
(c) Direct mapping
(d) None of these

[MCQ]

11. Suppose a cache has 70% hit ratio, an access time of 50 ns on a cache hit and an access time of 120 ns on a cache miss then what is the effective access time_____(using hierarchical memory)

(a) 90 ns (b) 92ns
(c) 86 ns (d) 96ns

[MCQ]

12. Suppose local hit rate for L_1 cache is 20% and the local hit rate for L_2 cache is also 30%. The hit time for the L_1 cache is 8 cycle, the hit time for L_2 cache is 20 cycles and access time for main memory is 30 cycles then what is average memory access time in cycle? (approximately)

(a) 41 (b) 45
(c) 46 (d) 44

[MSQ]

13. Choose the correct statements from the following.

(a) Instruction, and data stored in cache are regularly used by the CPU, if data not present in cache then it always transfers from main memory.
(b) Data is stored on temporary basis in cache memory.
(c) Programs stored in cache takes more time to execute.
(d) Cache memory has limited capacity.

[MCQ]

14. Consider the following statements.

S_1: If size of the block is increased then compulsory misses can be reduced.

S_2 : If associativity of cache is increased then that can lead to increasing conflict misses.

(a) only S_1 is true
(b) only S_2 is true
(c) both S_1 and S_2 are true
(d) neither S_1 nor S_2 is true

[NAT]

15. Consider a 128 word cache and the main memory is divided into 32 word blocks. The main memory access time is 50 μs / word and the cache access time is 20 μs/word. The hit ratio for read operation is 80% and for the write operation is 90%. Whenever a cache miss happens, associated block must be the brought from main memory to cache for both read and write operation. Let there be 40% references for write operations. If the write back updation policy is used and at any point of time 80% cache blocks are modified, then what is the T_{avg}? (upto 1 decimal in μ sec)

[NAT]

16. A 16-way set associative cache of size 128KB is used in a system with 32-bit address. For such cache memory, the memory size is ___. (in Kbytes) Provided block size is 4 bytes.

Answer Key

1. **(b)**
2. **(3)**
3. **(13)**
4. **(a)**
5. **(c)**
6. **(4096)**
7. **(3)**
8. **(c)**
9. **(d)**
10. **(a)**
11. **(c)**
12. **(a)**
13. **(b, d)**
14. **(a)**
15. **(481)**
16. **(76)**

Hints & Solutions

1. (b)

8GB

$2^3 \times$ GB

$2^3 \times 2^{30} / 2^1$

↓

32 address lines

2. (3)

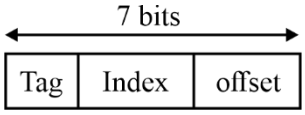
8 cache lines = 2^3 cache lines

$\therefore$ 3 bits for index

As given 1 line = 2 words = 2 bytes

$\therefore$ 1 bit for offset

Address size = 7 bits



Tag bits = 7 – 3 – 1 = 3 bits

3. (13)

$$\text{Number of lines in cache} = \frac{\text{cache size}}{\text{block size}}$$

$$= \frac{2 \times 2^{20}}{8 \times 2^{10}} = 2^8$$

$$\text{Number of sets in cache} = \frac{2^8}{4 - \text{way of associativity}}$$

$$= \frac{2^8}{2^2} = 2^6$$

$\therefore$ 6 bits for index

Block size = 2^{13}, means 13 bits are required for offset.

Tag bits = 32 – 6 – 13 = 13 bits.

4. (a)

Cache size = 2^{14} bytes

Block size = 2^5 bytes

$$\text{Word size} = \frac{32}{8}\text{ bytes} = 4 \text{ bytes} = 2^2 \text{ bytes}$$

$$\text{Number of lines} = \frac{\text{cache size}}{\text{block size}} \quad \frac{2^{14}}{2^5} = 2^9 = 512 \text{ blocks}$$

Now, Tag bits

As 2^9 lines are in cache and cache is 2-way set associative.

$2^8 = 8$ bits for a set.

Tag bits = PA – (index + offset)

= 32 – (8 + 5)

= 19 bits.

5. (c)

Cache size = 2^{14} bytes

Line size = 2^5 bytes

$$\text{Lines} = \frac{2^{14}}{2^5} = 2^9 \text{ lines}$$

2-way set associative cache = 2^8 sets.

8 bits for index = p

As index bits in fully associative = 0 = q

$\therefore$ p + q = 8 + 0 $\Rightarrow$ 8 which is option (c).

6. (4096)

Cache size = 512×2^{10} bytes = 2^{19} bytes

Cache line size = 2^7 bytes

$$\text{Number of lines} = \frac{512 \times 2^{10}}{2^7} = 2^9 \times 2^3$$

$= 2^9 \times 2^3$

$= 2^{12}$

= 4096.

7. (3)

Tag= 17 bits.

Block size = 2^7 bytes

7 bits for offset field.

Index bits = 32- (17 + 7) = 8

2^8 sets = 256 blocks

Total 768 block, therefore $\Rightarrow \frac{768}{256}$ = 3 way set associative.

8. (c)

Number of blocks = Memory address block mod number of blocks

	0
881	1
2	2
3	3
180	4
181	5
	6
	7
	8
	9
186	10
43	11
44	12
253	13
~~190~~ 14	14
191	15

8 mod 16 = 8
180 mod 16 = 4
43 mod 16 = 11
4 mod 16 = 4
191 mod 16 = 15
881 mod 16 = 1
190 mod 16 = 14
14 mod 16 = 14
181 mod 16 = 5
44 mod 16 = 12
186 mod 16 = 10
253 mod 16 = 13
Blocks present in cache after execution of sequence of jobs are:
2, 3, 180, 181, 881, 186, 43, 44, 253, 14, 191
$\therefore$ option (c) is correct.

9. (d)

x, y, z all of the of them corresponds to unique cache block, if they come in different block and we have 4 cache blocks in the cache.

x
y
z

The probability of hit on second accesses is 1 which is 100%.

10. (a)

In associative mapping both the address and data of the memory word are stored. The associative mapping method used by cache memory is very fast as well as flexible.

11. (c)

Effective access time = cache hit × cache access time + cache miss (cache access + mm access)
= 0.70(50) + 0.30(50 + 120)
= 35 + 51 = 86ns.

12. (a)

$AMAT = (L_{1H}T + (L_{1M}R \times (L_{2H}T + (L_{2M}R \times MEM))))$
$= 8 + (0.8 \times (20 + (0.7 \times 30))$
$= 8 + 0.8\ (20 + 21)$
$= \lceil 40.8 \rceil = 41$

13. (b, d)

(a): Instruction, and data stored in cache are regularly used by the CPU, if data not present in cache then it always transfers from main memory. **False**

b: Data is stored on temporary basis in cache memory. **True**

c: Programs stored in cache takes less time to execute. **False**

d: Cache memory has limited capacity. **True**

14. (a)

S_1 (True): Compulsory misses can be reduced by increasing the line size.

S_2 (False): Increasing the associativity decreases conflict misses.

15. (481)

Here dirty bit signifies the modified bit.

$T_{avgR} = h_r \times t_c + (1 - h_r)$ [% dirty bit $(t_m + t_c + t_m)$ + % clean bit $(t_m + t_c)$]

$\Rightarrow 0.8 \times 20 + 0.2\ (0.8\ (1600 + 20 + 1600) + .02\ (1600 + 20))$

$\Rightarrow 16 + 0.2 \times 2900$

$16 + 580$

$\Rightarrow 596$

$T_{avgW} = h_w \times t_c + (1 - h_w)$ [% dirty bit $(t_m + t_c + t_m)$ + % clean bit $(t_m + t_c)$]

$\Rightarrow 0.9 \times 20 + (0.1)\ (0.8\ (1600 + 20 + 1600) + 0.2\ (1600 + 20))$

$\Rightarrow 18 + 0.1 \times 2900$

$\Rightarrow 308$

$T_{avg} \Rightarrow 0.6(596) + 0.4(308)$

$\Rightarrow 357.6 + 123.2$

$\Rightarrow 480.8 \cong 481$ µsec.

Note: main memory access time $\Rightarrow$ 32 words* 50µsec

$\Rightarrow 1600$ µsec.

16. (76)

Cache memory size = 128KB = 2^{17}B

Main memory size = 32 bits

P = 16-way set associative

The block size = 2^2 Bytes

Number of cache block = $\frac{2^{17}}{2^2} = 2^{15}$

Number of sets $\Rightarrow \frac{2^{15}}{2^4} = 2^{11}$

For set associative mapping technique:

Tag bits + set bits + block offset bits = main memory

$\Rightarrow$ Tag bits + 11 + 2 = 32 bits

Tag bits = 19 bits

Tag memory size = S*P* tag space line

$\Rightarrow 2^{11} * 2^4 * 19$ bits

$\Rightarrow 2^{15} * 19$ bits

$\Rightarrow$ 32K * 19 bits

$\Rightarrow$ 608 K bits

$\Rightarrow$ 76 KB.