COMPUTER SCIENCE

Computer Organization and Architecture

Machine Instruction and Addressing Modes

Lecture_02

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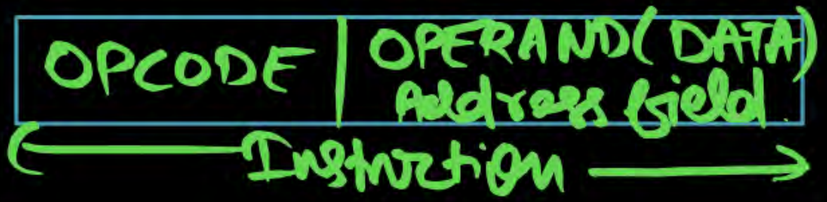
01 Machine Instruction

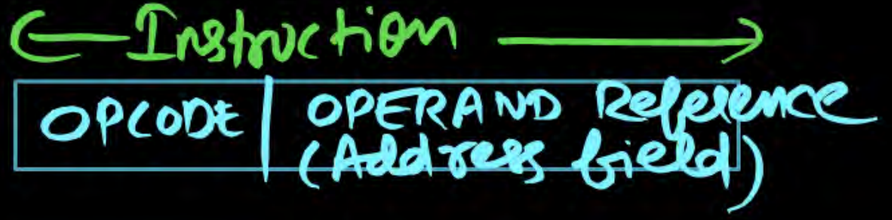
02 Instruction Set Architecture

Introduction of COA.

Instruction



Instruction Format



OPCODE (Mnemonics) ⇒ operational Code.

↳ Type of operations.

n bit opcode can perform 2^n operation/Instruction.

A.F = n bit ⇒ 2^n memory Capacity.

Instruction Representation

- Opcodes are represented by abbreviations called mnemonics
- Examples includes:
  - ADD — Add
  - SUB — Subtract
  - MUL — Multiply
  - DIV — Divide
  - LOAD (LD) — Load data from memory
  - STORE (ST) — Store data to memory
- Operands are also represented symbolically
- Each symbolic opcode has a fixed binary representation

Instruction Format

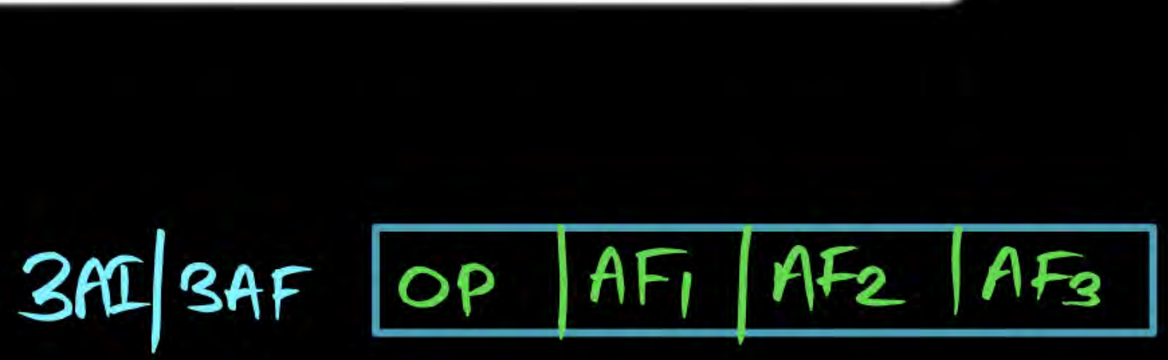
ALU operation

↓

MUL
or
ADD

Destination Source 1 Source 2.

Instruction Format



Storage

Registers [Fastest]

Memory
- Cache Memory [CM]
- Main / Primary Memory [MM]
- Secondary / Auxilliary Memory [SM]

Fastest

Register > CM > MM > SM.

Size

SM > MM > CM > Register.

Instruction Format

Storage

- Register → Reg A.F
- Memory → Mem A.F

Address Field

Instruction Format

Q.1 Memory 4 MB $\Rightarrow 2^{22}$ Byte $\Rightarrow$ Mem AF = 22 bits.

Q.2 50 Registers $\Rightarrow 2^n$ $\Rightarrow$ Reg AF = 6 bits.

$2^5 = 32$

$2^6 = 64\,[33-64]$

↳ 6 bit

Instruction Format

Sometimes Instruction having Immediate field also along with AF

If Immediate field = n bit

n bit Immediate unsigned Range = 0 to $2^n - 1$

n bit Immediate signed Range = -2^{n-1} to $+(2^{n-1} - 1)$

Assume

(eg) If Immediate field is 7 bits.

Unsigned = 0 to $2^n - 1$ ⇒ 0 to $2^7 - 1$ ⇒ 0 to 127

Signed = $-(2^{n-1})$ to $+(2^{n-1} - 1)$ ⇒ -2^{7-1} to $+2^{7-1} - 1$

$= -2^6$ to $+2^6 - 1$

⇒ −64 to +63.

Elements of a Machine Instruction

Operation Code (opcode)

- Specifies the operation to be performed. The operation is specified by a binary code, known as the operation code, or opcode.

Source Operand Reference

- The operation may involve one or more source operands, that is, operands that are inputs for the operation

Result Operand Reference

- The operation may produce a result

Next Instruction Reference

- This tells the processor where to fetch the next instruction after the execution of this instruction is complete

Instruction Representation

- Within the computer each instruction is represented by a sequence of bits
- The instruction is divided into fields, corresponding to the constituent elements of the instruction

Q.1

Consider a Hypothetical Processor which support 128 byte memory and instruction length is 16 bit.

(i) If 2AF (2AI (Address Instruction) same size) is used then How many total number of operation supported (formulated)?

(ii) If 1AF (Address field) is used then how many total number of operation supported formulated?

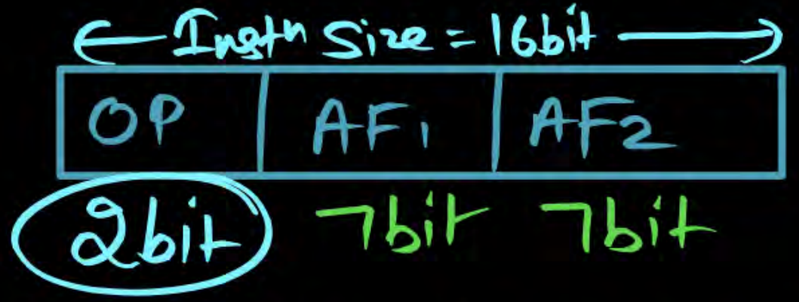
Q.2 How Many Minimum # operation / Instn supported in 2AI & 1AI ?

Soln

Instruction length = 16bit

Memory = 128 Byte $\Rightarrow 2^7 B \Rightarrow$ A.F = 7 bits

(i) 2 AI



OPCODE = $16 - (7+7) \Rightarrow 16 - 14 = 2$ bit

Total # operation = $2^2 = 4$ operation/Instruction. Ans

(ii)

$16 - 7 = 9$

Total # operations = $2^9 = 512$ operation. Ans

In 2AI (or) 2AF

Total Number of operation/Instruction = 4

2 Address field (AF)

(or)

2 Address Instruction (AI)

Maximum operation/Instruction = 4
Minimum operation/Instruction = 1

In 1AF (or) 1AI

Total Number of operation/Instruction = 512

1AI (or)

1AF

Maximum operation/Instruction = 512
Minimum operation/Instruction = 1

Instruction Set Size of 10.

⇓

10 Different type of operation/Instruction Performed

⇓

OPCODE = 4bit Ans

$\lceil \log_2 10 \rceil$

⇓

4bit

eg

Number of Instruction/operation Performed is '200'

OPCODE = 8 bit Ans

Q.2 A Hypothetical Processor support 100 different operation and 3 address memory field (same size). Instruction is stored in 1 MB memory. Then what is the length of the instruction?

Opcode

100 operation ⇒ 7 bit

1 MB Memory = 20 bit

Length of Instruction = 67 bits Ans

Q.1 Consider a Hypothetical CPU which supports 110 instruction, 50 registers and 512KB memory space. Instruction contain 2 register operands, Memory operands and 13 bit Immediate constant fields. Program contain 300 instruction. Memory storage space required in Bytes to store the program is _____.

Sol^{n}

110 Instruction/operation $\Rightarrow$ OPCODE = 7 bit

50 Register $\Rightarrow$ Reg AF = 6 bit

512 KB Memory $\Rightarrow$ Mem AF = 19 bit

2^{19}B

OPCODE	Reg$_1^{AF}$	Reg AF$_2$	MemAF	Immediate

OPCODE	Reg AF1	Reg AF2	mem AF	Immediate field
7bit	6bit	6bit	19bit	13bit

1 Byte = 8bit

1 Instruction size (legth) = 7 + 6 + 6 + 19 + 13 = 51 bits.

1 Instruction Size = $\left\lceil \frac{51\text{bit}}{8\text{bit}} \right\rceil$ Byte = 7Byte.

Program Contain 300 Instruction.

Program Size = 300 X 7 Byte

= 2100 Byte Ans

How its Instruction size (legth) = 7 + 6 + 6 + 19 + 13 = 51 bits.

look like

Q.

Consider a processor which contain the following pin structure

$AD_0 - AD_{23}$, $A_{24} - A_{39}$ AF = 40bit Wordlength = 24 bit = 3Byte

Processor contain 250 register instruction is designed with 4 fields i.e OPCODE, register address, memory address and 16 bit immediate field.

Processor support 180 instruction (operation). A program contain 400 instruction then how much space is required for the program

(i) In Byte? 3600 Byte

(ii) Words? 1200 Words.

OP	Reg	mem	Immediate.
8	8	40	16

$= \frac{72 bit}{8} = 9 Byte$

400 × 9 = 3600 B Ans

1200 Word Ans

Q.

Consider a processor which contain the following pin structure

$AD_0 - AD_{23}$, $A_{24} - A_{39}$

Processor contain 250 register instruction is designed with 4 fields i.e OPCODE, register address, memory address and 16 bit immediate field.

Processor support 180 instruction (operation). A program contain 400 instruction then how much space is required for the program

(i) In Byte? 3600 Byte

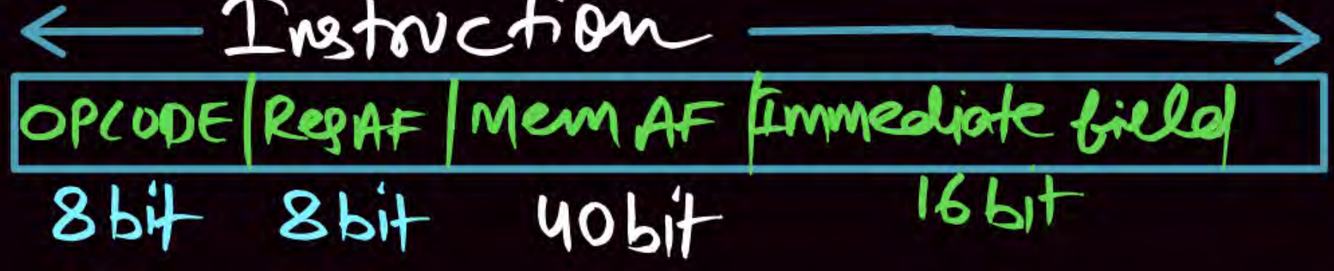
(ii) Words? 1200 Words.

$AD_0 - AD_{23}$, $A_{24} - A_{39}$ $\Rightarrow$ mem Address = 40 bit (A0 - A39)

Data Line [Word Size] = 24 bit (AD0 - AD23)

250 Register. $\Rightarrow$ Reg AF = 8 bit

180 operation / Instruction $\Rightarrow$ opcode = 8 bit



Instruction Length (Size) = 8 + 8 + 40 + 16 = 72 bits.

1 Instruction Size = $\frac{72 \text{ bits}}{8 \text{ bits}}$ = 9 Byte.

1 Instruction Size = 9 Byte.

Program Contain = 400 Instruction

So Program Size = 9 × 400 = 3600 Byte Ans

Program Size in Word.

$AD_0 - AD_{23}$ Data = $D_0 - D_{23}$ = 24bit

1 Word Size = 24bit ≒ 3Byte.

Program Size = 3600 Byte

in Word = $\frac{3600\ \text{Byte}}{3\ \text{Byte}}$ Words = 1200 Words Ans

Note:

Immediate field is n bit

Unsigned Range = $(0 \text{ to } 2^n - 1)$

Signed Range = $-(2^{n-1}) \text{ to } + (2^{n-1} - 1)$

Example

If immediate field is 4 bit

Then unsigned range = $(0 \text{ to } 2^4 - 1) \Rightarrow 0 \text{ to } 15$ Ans

Signed Range = $-(2^{4-1}) \text{ to } + (2^{4-1} - 1)$

$\Rightarrow -2^3 \text{ to } +2^3 - 1$

$= -8 \text{ to } +7$ Ans

D.L = 32 bit

Word length
Data Line
Data BUS
} 32

ALU = 32

AC = 32

Registel = 32

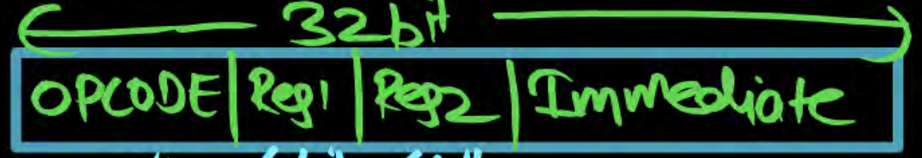
Q. A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instruction, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer the maximum value of the immediate operand is _____. **[GATE-2014 (Set-1)]**

1 word Long Instn

∴ 1 Instruction Size = 32bit

64 Register ⇒ Reg AF = 6bit

45 Instruction/operation ⇒ opcode = 6bit



Immediate field = 32 − (6+6+6)

= 14bits

Unsigned Immediate field

Maximum = 0 to $2^{14}-1$

= 0 to 16383

Ans (16,383)

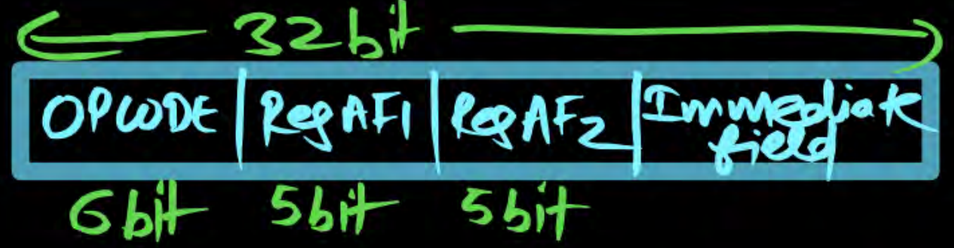
Q. A processor has 40 distinct instructions and 24 general purpose registers. A 32-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is _____.

[GATE-2016 (Set-2)]

40 Instruction ⇒ OPCODE = 6bit

24 Registers ⇒ Reg AF = 5 bit

Ans (16)



Immediate field = 32 − [6 + 5 + 5]

= 16 bit Ans

Q.

Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and a twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is 500 Byte Ans

[GATE-2016 (Set-2): 2Marks]

64 → 6bit

4bit opcode

OPCODE	Reg 1	Reg AF2	Reg AF3	Immediate field
4bit	6bit	6bit	6bit	12bit

Instruction size = 4+6+6+6+12 = 34 bits

1 Instruction size = 5 Byte

Prog Contain = 100 Instruction

Prog Size = 100 × 5 B

= 500 Byte Ans

THANK YOU!