# COMPUTER SCIENCE

## Computer Organization and Architecture

Secondary Memory & IO Interface



Lecture_04

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## 01 IO Organization

# Disk

- Disk Capacity
- Disk Access time (S.T. Avg R.L, D.T.T & Data transfer Rate)
- Disk structure (Platter, Surface, Cylinder, track, Arm, R/w Head, Arm Assembly)
- Disk Addressing

# Disk Addressing <C, h, S>

$$\text{Sector Number} = S + ST * h + \underbrace{ST * TC}_{SC} * C$$

ST: #sector per track

TC: #Track per cylind(#surface)

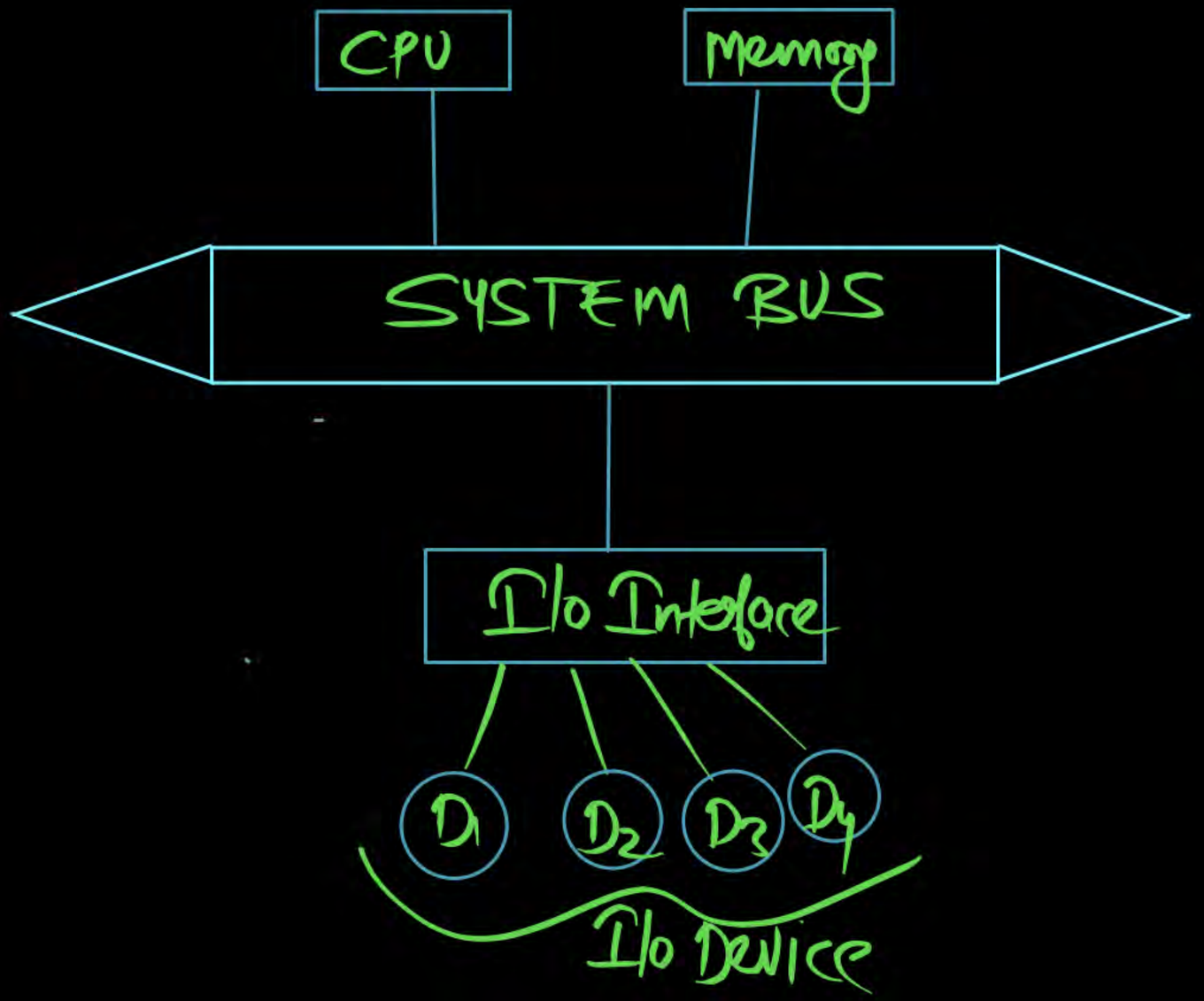
SC: #sector per cylinder

# I/O Org. : (Input output org)

(Slowest) I/O : Electromagnetic

(Fastest) CPU : Electronic

I/O Interface chip


CPU
Memory
SYSTEM BUS
I/o Interface
D1
D2
D3
D4
I/o Device

# Input-Output Interface

I/O Device

Input-output interface provides a method for transferring information between internal storage and external I/O devices. Peripherals connected to a computer need special communication links for interfacing them with the central processing unit. The purpose of the communication link is to resolve the differences that exist between the central computer and each peripheral. The major differences are:

1. Peripherals are electromechanical and electromagnetic devices and their manner of operation is different from the operation of the CPU and memory, which are electronic devices. Therefore, a conversion of signal values may be required.
2. The data transfer rate of peripherals is usually slower than the transfer rate of the CPU, and consequently, a synchronization mechanism may be needed.

3. Data codes and formats in peripheral differ from the word format in the CPU and memory.
4. The operating modes of peripherals are different from each other and each must be controlled so as not to disturb the operation of other peripherals connected to the CPU.

## Modes of Transfer

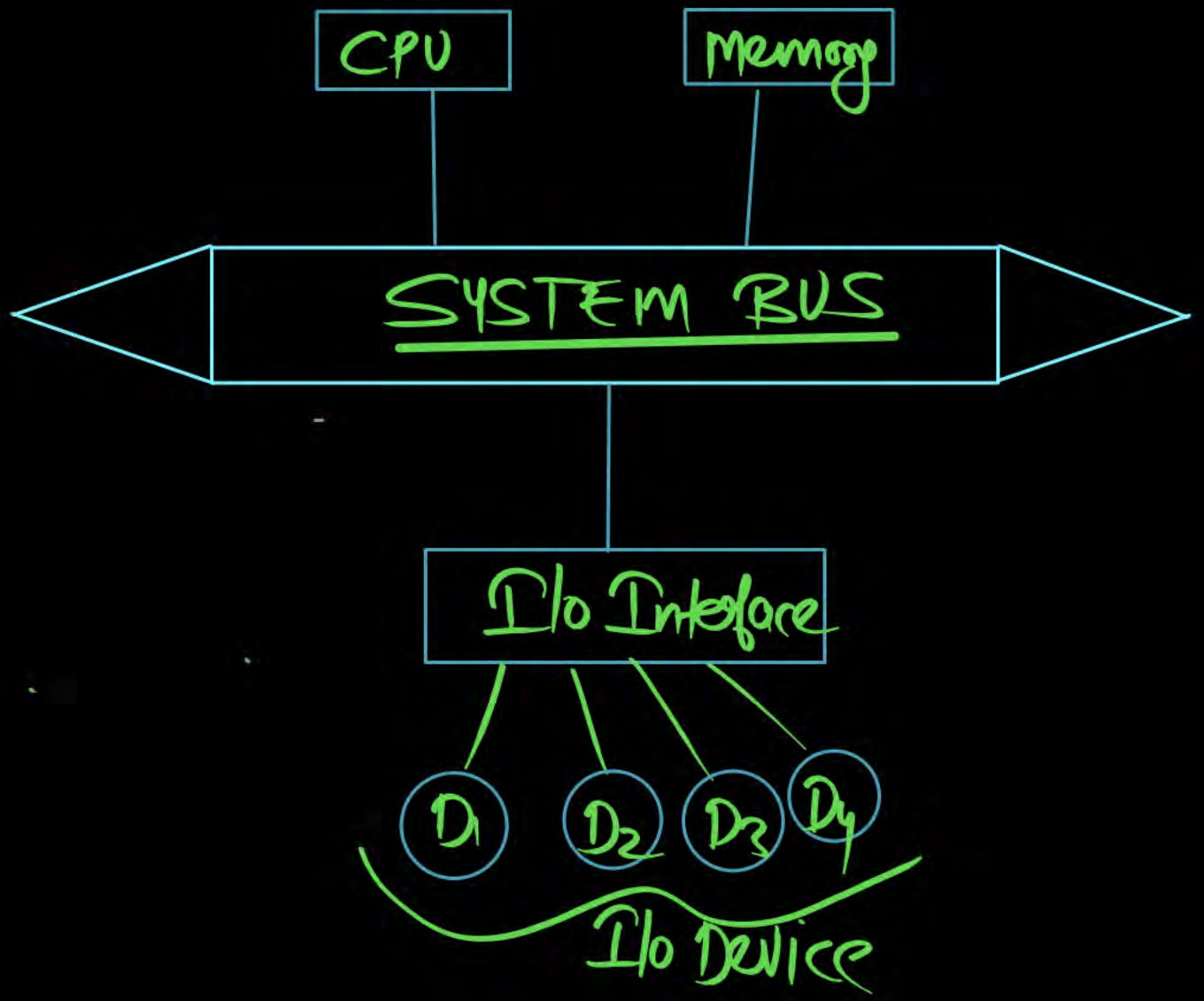
1. Programmed I/O
2. Interrupt-initiated I/O
3. Direct memory access (DMA)

# I/O ORGANIZATION

(1) I/O devices are electro-magnetic components and CPU is a electronic component. So, there is a difference exist in term of operating modes, data transfer rate and word formats. & Speed.

(2) To synchronize the I/O speed with a CPU, high speed interface chip is used named as I/O interface or I/O module.

(3) I/O interface chip is responsible for I/O Operations so, in the computer design I/O devices are connected to system bus via I/O interface Chip.:


CPU
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SYSTEM BUS
I/o Interface
D1
D2
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I/o Device

# I/O ORGANIZATION

## System without IO – Interface [Programmed- IO]

1 kB – 1Sec

1 B – ?

$$ETIO = \frac{1B}{1kB}\text{sec} = 10^{-3}\text{sec} = 1millisec$$

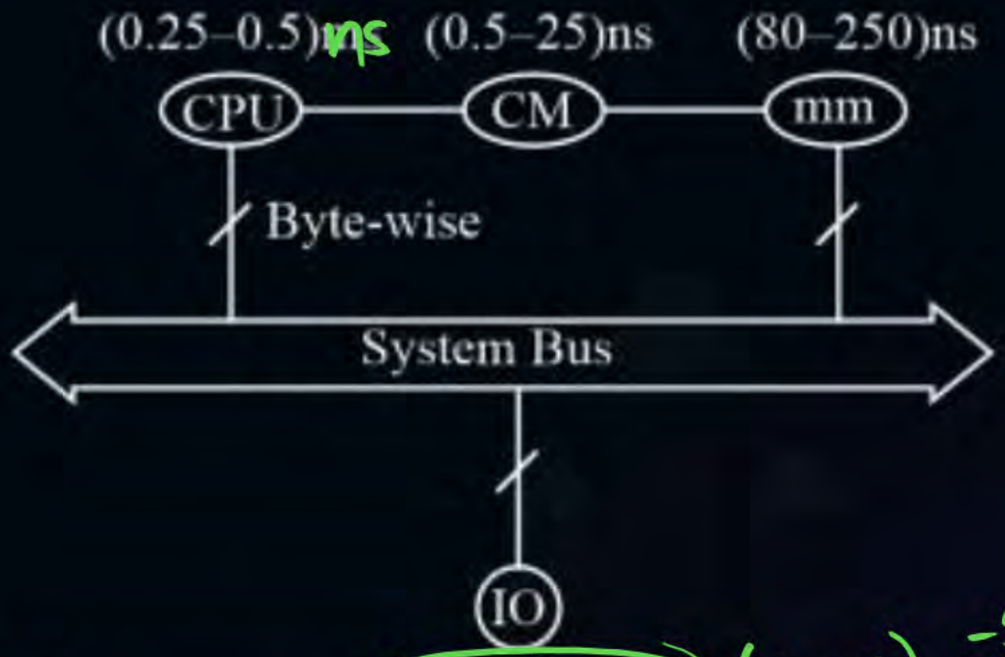
1kBps

1kB —— 1Sec

1Byte —— $\frac{1}{1k}$ sec $= 10^{-3}$ sec

= 1msec

1 sec = $10^{-9}$ sec



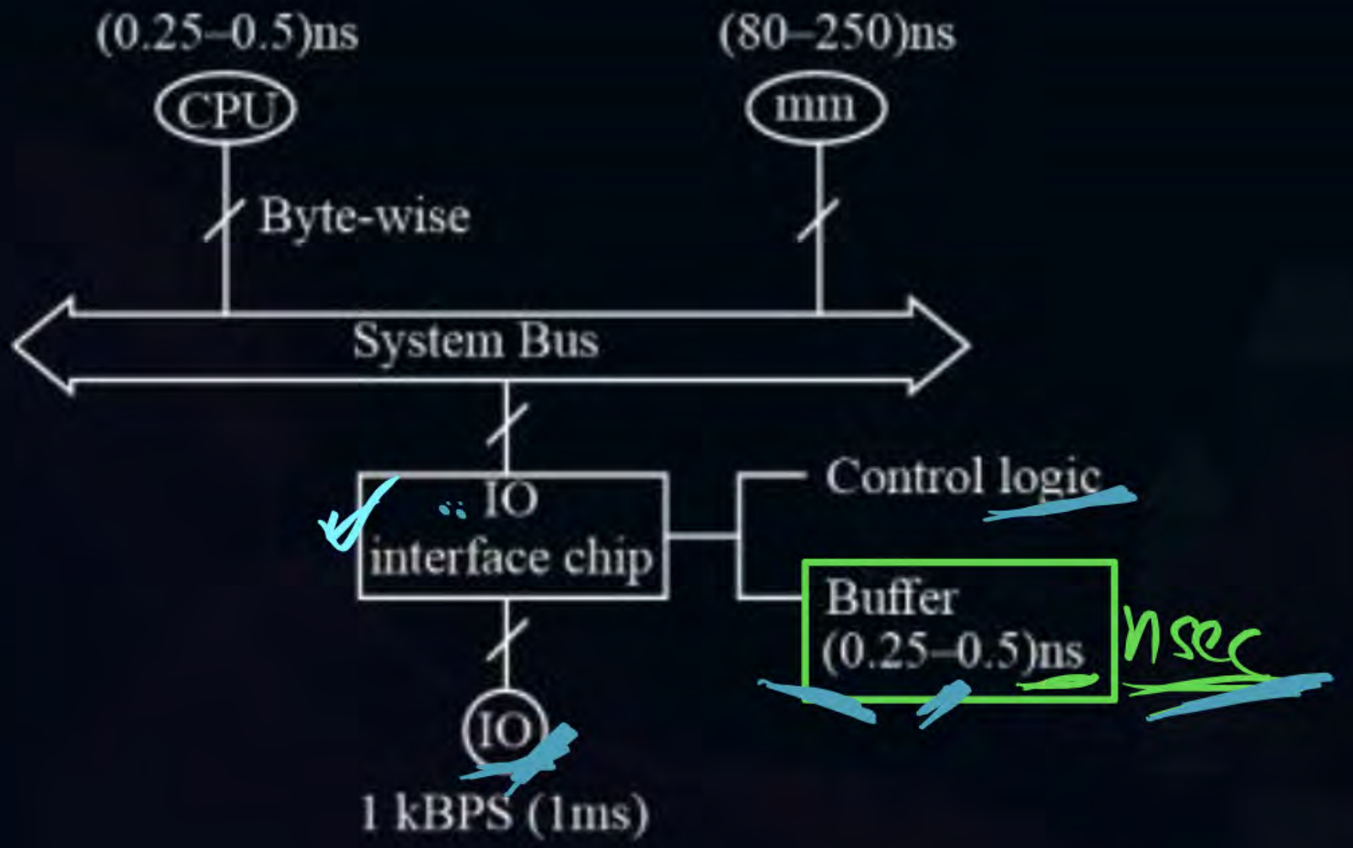

(1ms) $10^{-3}$ sec.

Difference $10^6$ (10 lakh) times

So IO Interface required.

# I/O ORGANIZATION

## System with IO – Interface Chip [INT- Driven IO]



Working

# ACCESS SEQUENCE/Working Process

(1) CPU initializes the I/O interface chip along with a I/O command( Operations), & then CPU will go & performing other useful task.

(2) IO – interface control logic interprets the IO – Commands and Accordingly IO port will be enables for the IO operation.

(3) Based on the speed of a IO device, & Amount of data to be transfer Consume the time to prepare the data(preparation time), then data is transferred from IO device to a interface buffer.

(4) When the Data is available in the buffer IO interface generates the interrupt signals & send to the CPU and waiting for ack. Signal..

# ACCESS SEQUENCE

(4) After receiving the ack. Signal, buffer content will be transferred to CPU. In this process, CPU will be accessing the IO – data from interface buffer therefore speed gap is synchronized & Time saved.(Bcz IO interface fast).

Different IO – interface chip used in the computer design is.

(1) 8255 PPI. [Programable Peripherial Interface]

(2) 8251 USART (Universal Synchronous Asynchronous Receiver Transmitter)

(3) 8259 A INT. Controller

(4) 8237/8257 DMA etc.

# Till Now

(i) WHY I/o Interface ?

(ii) WHAT I/o Interface ?

(iii) WHEN I/o Interface used ?

(iv) How I/o Interface / Module work ?

# IO – MODES

Three types of IO – transfer modes are present in the computer system , Used to transfer the data from the IO to other Component of a Computer. [CPU, memory ]

Named as —

(1) Programmed – IO .

(2) Interrupt Driven IO.

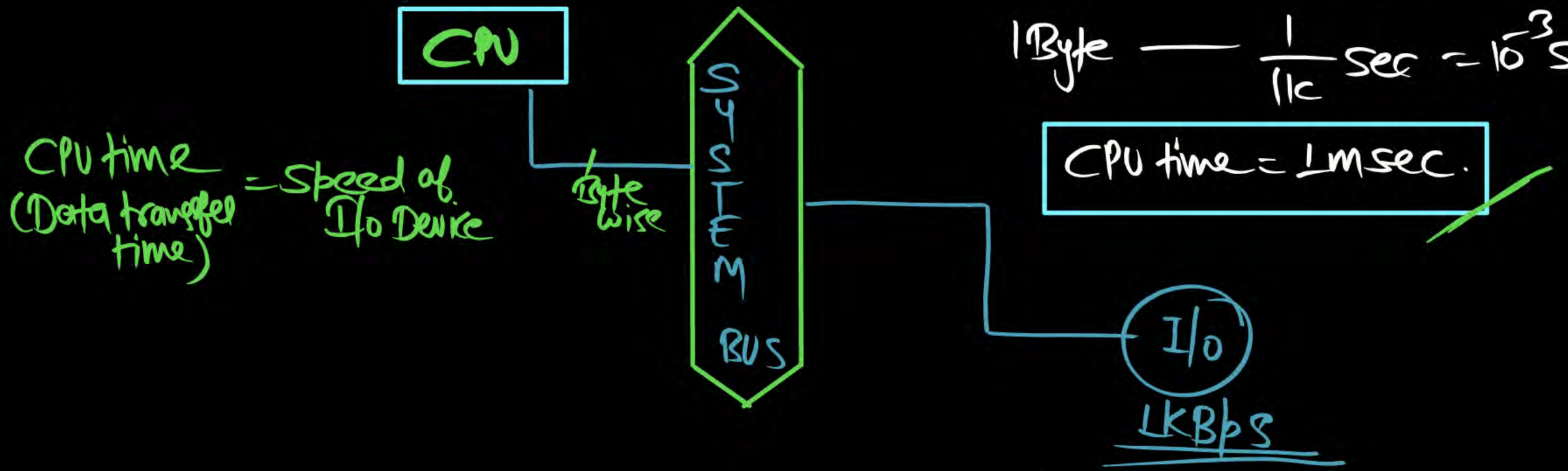
(3) DMA (Direct Memory Access)

# Modes of Transfer

1. Programmed I/O
2. Interrupt-initiated I/O
3. Direct memory access (DMA)

# 1 PROGRAMMED IO

There is No High Speed Interface Logic Used.



# PROGRAMMED IO

(1) In this mode, IO– devices are directly, Connected to CPU without IO– interface chip.

(2) In this mode, CPU takes the responsibility to complete the IO operation, So CPU will be blocked [waiting] until the IO – operation is completed.

(3) In this mode CPU Utilization is inefficient. (Depends On Speed of I/o Device)

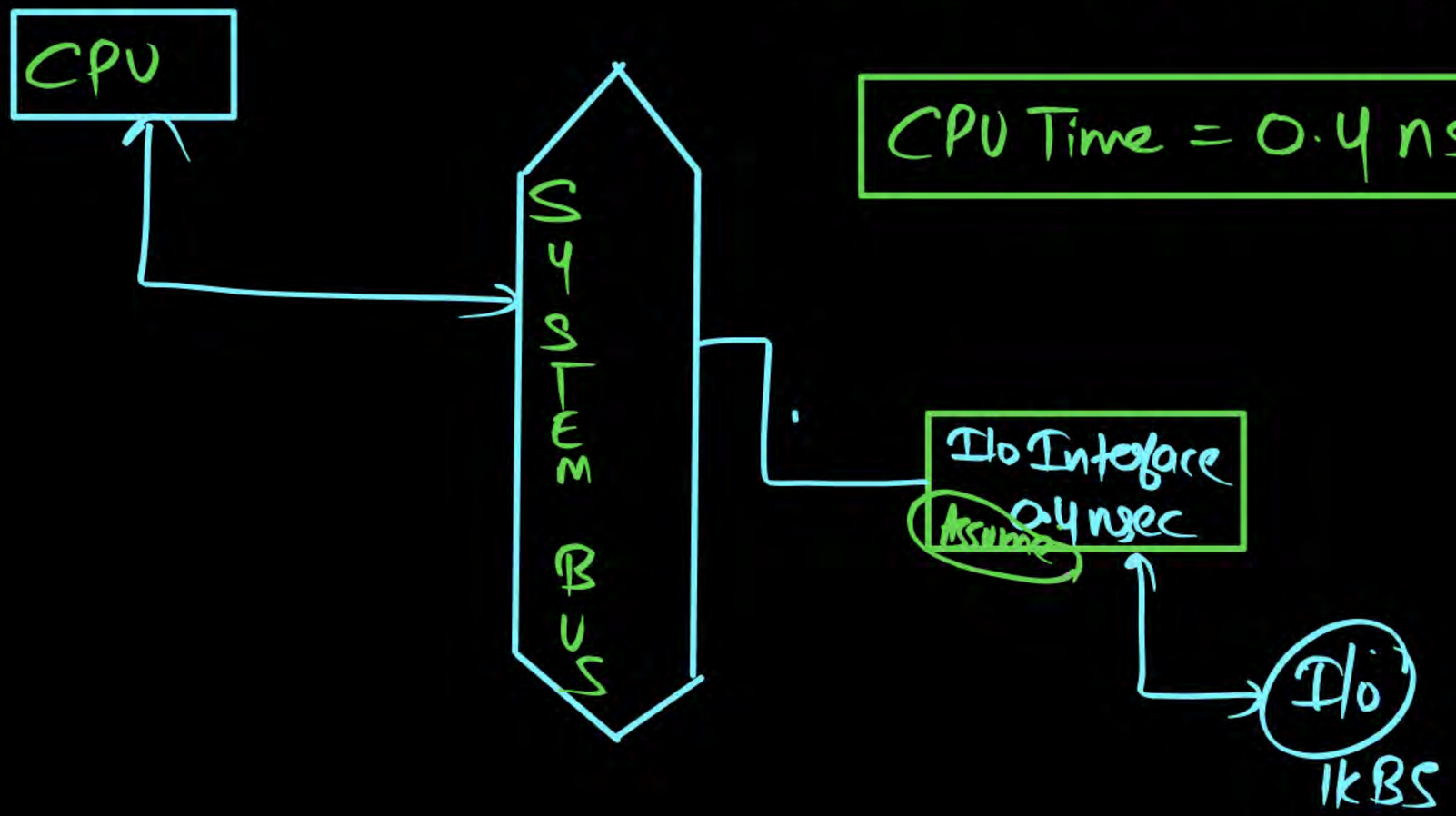
(4) In this mode CPU time depends on the speed of a IO – device and the size of a data unit to be transferred.

(5) This mode is suitable in the system centric application where the IO time is important than CPU time.

# 2 INTERRUPT DRIVEN IO

CPU Time = I/O Interface time (Latency)

CPU Time = 0.4 nsec.



# INTERRUPT DRIVEN IO

(1) In this mode, IO– operation are controlled based on the interrupt signals.

(2) In this mode, IO– devices are connected to a system bus via IO – interface chip So, IO – interface takes the responsibility of a IO open (operation)

(3) In this mode processor utilization is efficient so CPU executing the other useful task during the IO Open.

(4) In this mode CPU time is depends on the Latency of a interface chip rather than the speed of a IO device.

A device with data transfer rate 10 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 4 usec. The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode?

(a) 15 (b) 25 (c) 35 (d) 45

**[GATE-2005 : 2 Marks]**

# THANK YOU!