COMPUTER SCIENCE

Computer Organization and Architecture

ALU & Control unit

Lecture_05

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TOPICS
TO BE
COVERED
01
Control Unit
02
CPU Time Calculation

Control unit

1. Hardwired CU Design.
2. Micro programmed CU Design.

Control Signal

① Decoded format

[Horizontal uprog.]

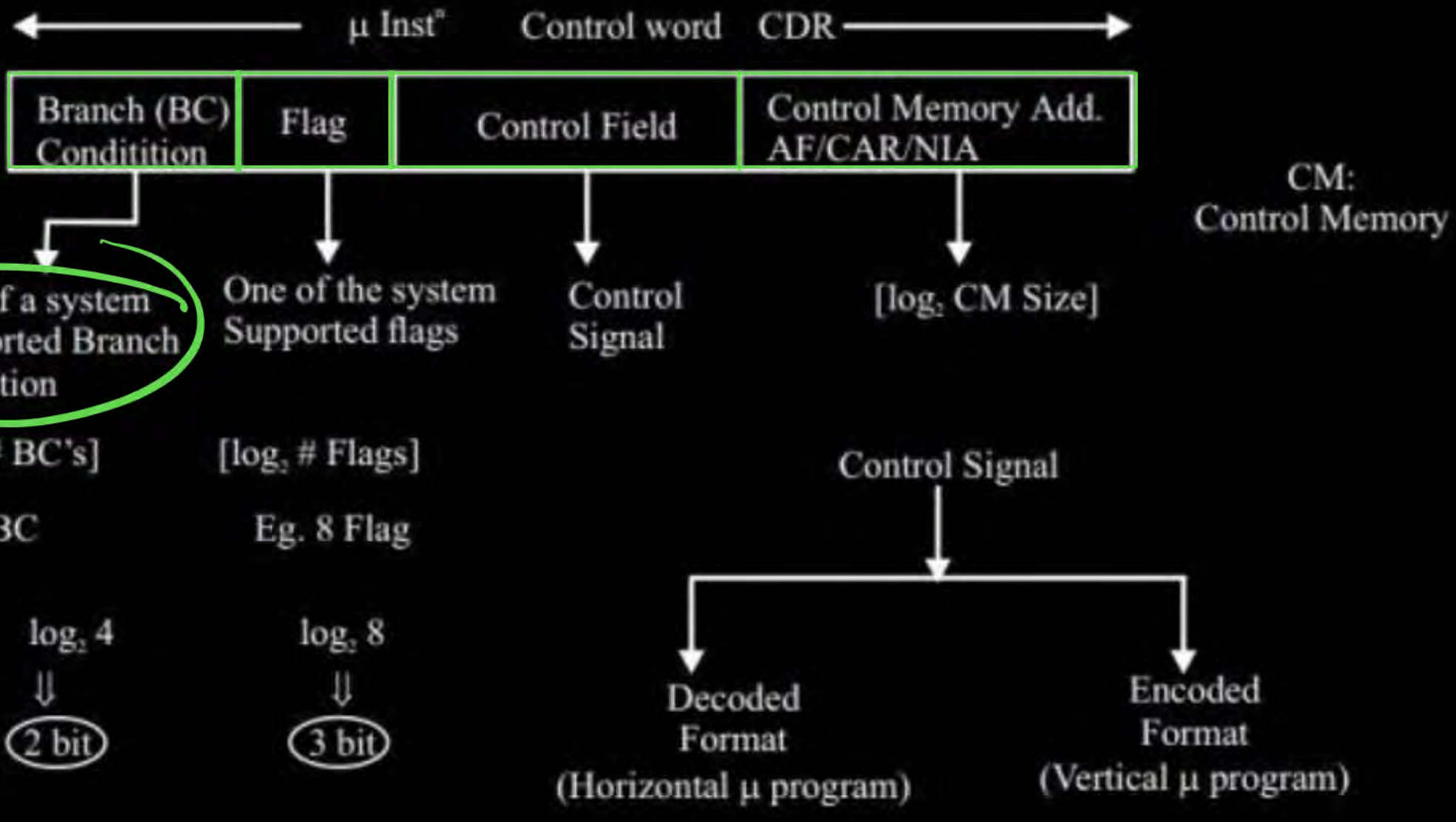
[1 bit | 1 CS
NCS ⇒ N bit]

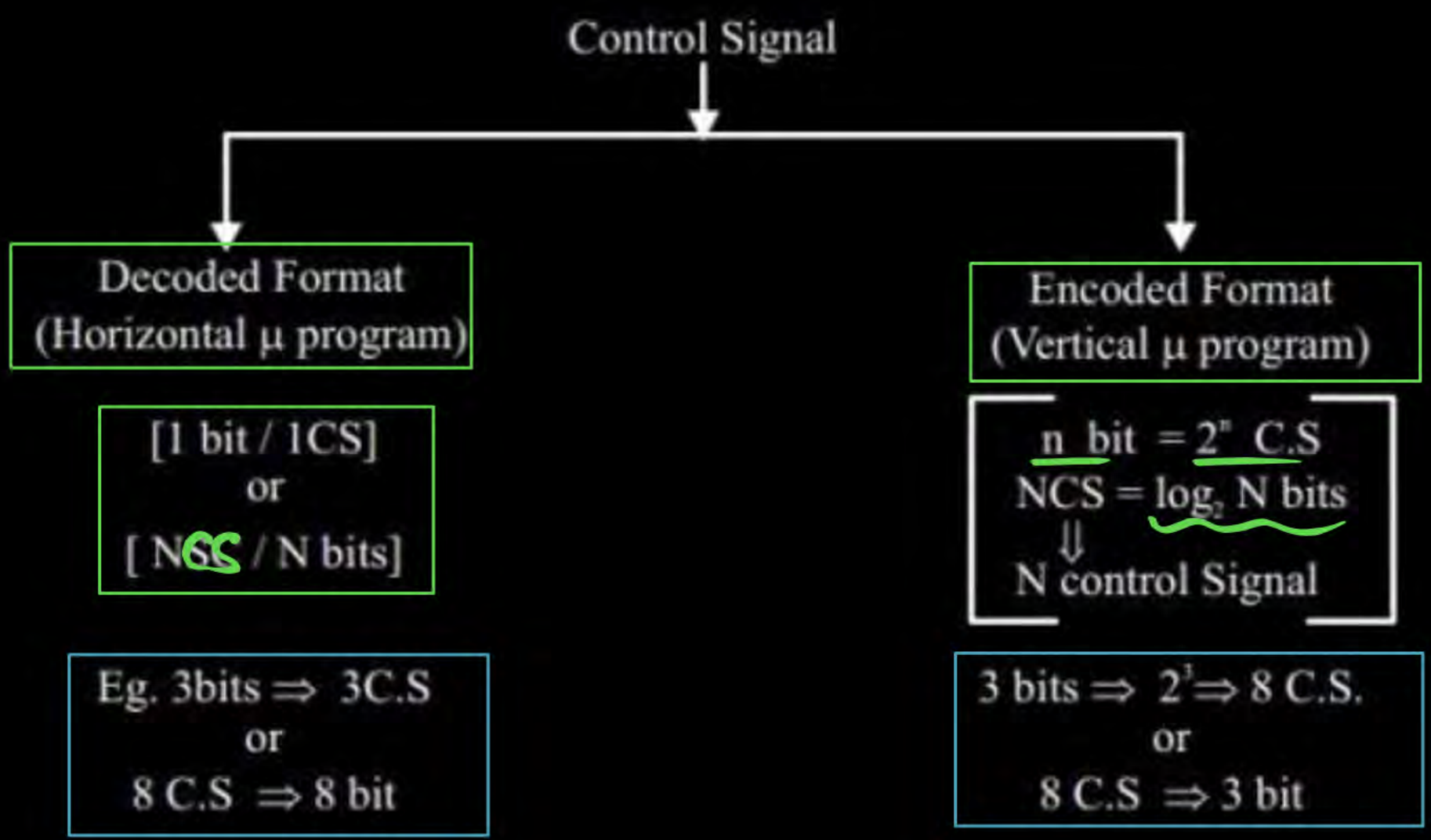
② Encoded Format

[Vertical uprog.]

[n bit ⇒ 2^n CS
NCS ⇒ $\log_2 N$ bits]

MICRO INSTRUCTION FORMAT




Control Signal
Decoded Format
(Horizontal μ program)
[1 bit / 1CS]
or
[N CS / N bits]
Eg. 3bits ⇒ 3C.S
or
8 C.S ⇒ 8 bit
Encoded Format
(Vertical μ program)
n bit = 2^n C.S
NCS = log2 N bits
⇓
N control Signal
3 bits ⇒ 2^3 ⇒ 8 C.S.
or
8 C.S ⇒ 3 bit

Q.1

GATE

Arrange the following configuration for CPU in decreasing order of operating speeds: Hardwired control, vertical micro-programming, horizontal micro-programming.

(a) Hardwired control, vertical micro programming, horizontal micro programming.

(b) Hardwired control, horizontal micro programming, vertical microprogramming

(c) Horizontal micro programming, vertical micro programming. Hardwired control

(d) Vertical micro programming, horizontal micro programming, hardwired control

Q.2

GATE

Horizontal microprogramming.

(a) does not require use of signal decoders

(b) Results in larger sized microinstructions than vertical microprogramming

(c) use one bit each control signal

(d) All of the above

Q.3

GATE 2Marks

An instruction set of a processor has 125 signals which can be divided into 5 groups of mutually exclusive signals as follows:

Group 1 : 20 signals. Group 2 : 70 signals, Groups 3 : 2 signals. Groups 4 : 10 signals, Groups 5 : 23 signals.

How many bits of the control words can be saved by using vertical microprogramming over horizontal microprogramming?

(a) 0

(b) 103

(c) 22

(d) 55

	Horizontal	Vertical
G_1 : 20CS	20	5bit
G_2 : 70CS	70	7bit
G_3 : 2CS	2	1 bit
G_4 : 10CS	10	4bit
G_5 : 23CS	23	5bit
	125 bit	22bit

(7)

#bit Saved = 125 - 22

= 103 Ans

Q. Consider a Hypothetical CU it has 1024 control words memory. Is support 48 control signals & 16 Flags. What is the size of the control words in bits & control memory in byte using

(i) Horizonal Programming?

(ii) Vertical Programming?

Control Memory = 1024 Control Word $\Rightarrow 2^{10}$ CW $\Rightarrow$ CM Address AF | NIA | CAR = 10 bit

Flags = 16 Flag $\Rightarrow 2^{4}$ Flag $\Rightarrow$ Flag = 4 bit

Horizontal Programming

48 Control signal $\Rightarrow$ CF = 48 bit

Flag	CF	AF | NIA
4bit	48bit	10bit

Vertical Programming

48 Control Signal $\Rightarrow$ CF = 6 bit

Flag	CF	AF | NIA | CAR
4bit	6bit	10bit

$48 = 2^{n}$ ⑤ = 32

33-64 ↓ 6bit

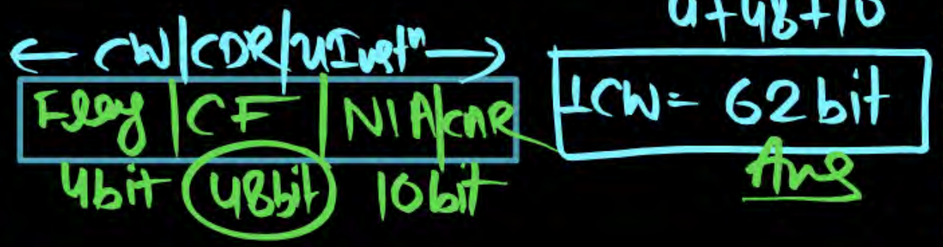
Q.

Consider a Hypothetical CU it has 1024 control words memory. Is support 48 control signals & 16 Flags. What is the size of the control words in bits & control memory in byte using

(i) Horizonal Programming?

(ii) Vertical Programming?

Horizontal Programming



4+48+10

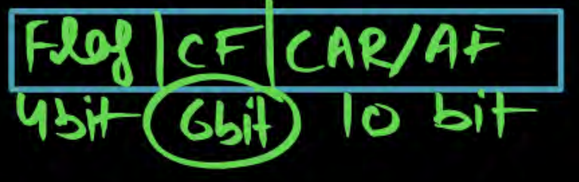
ICW = 62 bit Ans

Control Memory = 1024 CW

⇒ 1024 × 62 bit ⇒ 1024 × 62 / 8 B

⇒ 8K Byte Ans

Vertical Programming



1 Control word = 4+6+10 = 20 bit Ans

Control Memory = 1024 CW

⇒ 1024 × 20 bit ⇒ 1024 × 20 / 8 B

⇒ 3K Byte Ans

Q.

Control field of a micro Instruction support 2 groups of control signal in which Group 1 Indicate None/One of 400 control signal & Group 2 (Horizontal) Indicate 6 signals. Hardwire contain 16 Flags & 32 Branch condition.

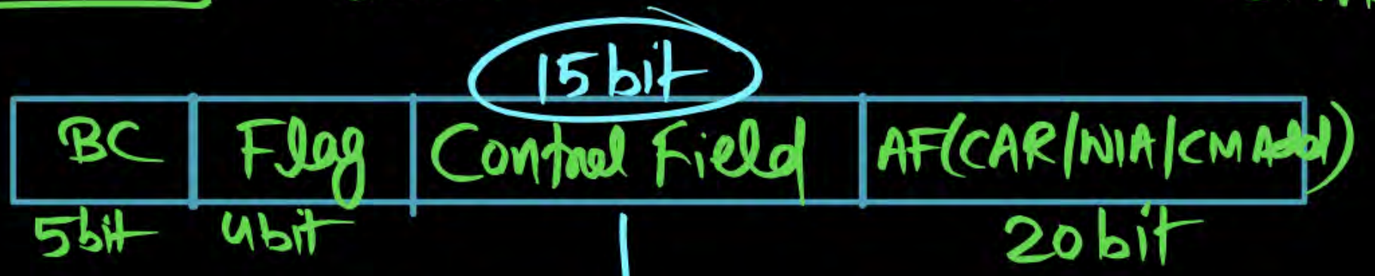
Vertical

If CAR Register size is 20 bit then what is CDR in bits & control memory in bits?

16 Flag ⇒ Flag = 4 bit

32 Branch Condition ⇒ (2^n) ⇒ BC = 5 bit

CAR/AF/NIA/CM Address = 20 bit



$2^8 = 256$

257-512

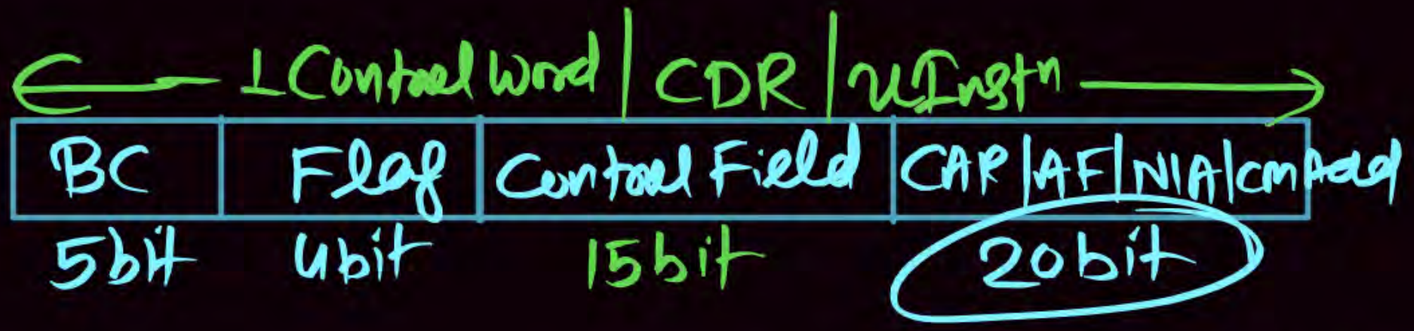
9 bit

$\lceil \log_2 400 \rceil$

Vertical G_1 (None/One) 400 CS ⇒ 9 bit

G_{12} Horizontal 6 CS ⇒ 6 bit.

Control Field = 9 + 6 = 15 bit



LCW [CDR] Size = 5+4+15+20 = 44 bit

LCW | CDR = 44 bits

Control Memory = 2^{20} CW

$\Rightarrow 2^{20} \times 44$ bit

$\Rightarrow$ 44M bits Ans

Q. Consider a CPU where all the instructions require 7 clock cycles to complete execution. There are 140 instructions in the instruction set. It is found that 125 control signals are needed to be generated by the control unit. While designing the horizontal micro-programming control unit, single address field format is used for branch control logic. What is the minimum size of the control word and control address register?

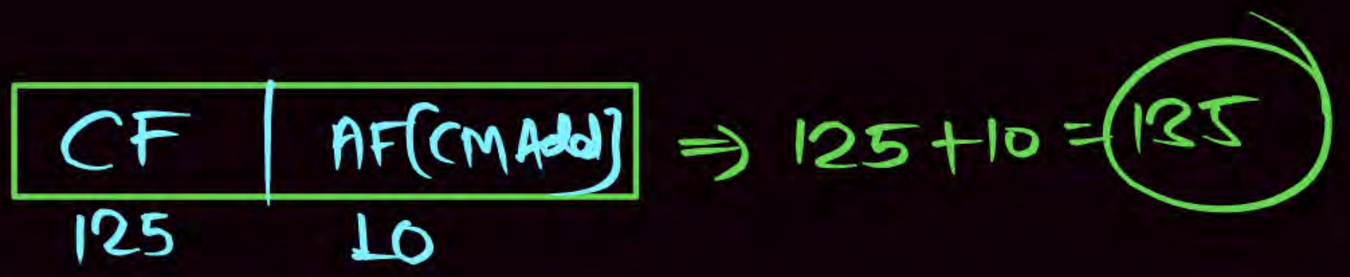
[GATE IT 2008]

(a) 125, 7
(b) 125, 10
(c) 135, 7
(d) 135, 10

Total Number of Instruction = 140.
#cycle/Instⁿ = 7 cycle.
Total #cycle/μoperⁿ/nInstⁿ = 140×7 = 980 μInstⁿ/CW.
Control memory = 980 CW. ≈ 2^n
AF/CAR/NIA/CM Addr = 10 bit

Horizontal

125 CS = CF = 125 bit.



135, 10

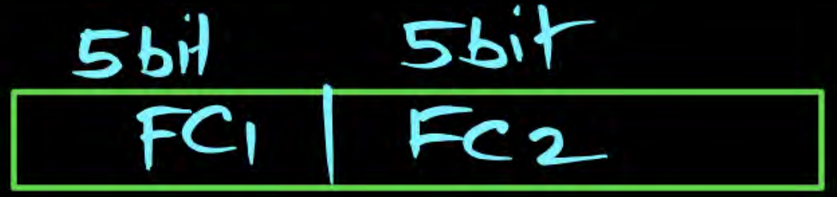
Q.

A micro program control unit is required to generate a total of 25 control signals. Assume that during any microinstruction at most ~~tow~~ two control signals are active. Minimum number of bits required in the control word to generate the required control signal.

(a) 2
(b) 2.5
(c) 10
(d) 12

[GATE CSE 1996]

25 CS ⇒ 5 bit



Q. A Hypothetical processor contain word length of 12 bits. It support 1 word opcode. Each Instruction takes 8 cycles to compete the execution. Processor contain 256 control signal & 16 flags. Processor used Horizontal Control Unit. 64 Branch is used then what is the size of CAR & CDR in bits of control memory?

Word length = 12 bit

OPCODE = 1 Word = 12 bit

Total # Instⁿ/operation = 2^{12} Instruction

cycle / Instⁿ = 8 cycle / Instⁿ

Total # uInstⁿ/uoperation/CW = $2^{12} \times 8$

$\Rightarrow 2^{15}$ uInstⁿ/CW

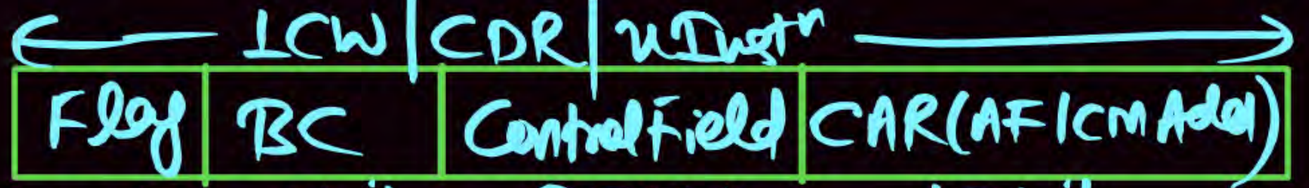
Control Memory = 2^{15} CW.

AF/cm Add [CAR] = 15 bit

16 Flag ⇒ Flag = 4 bit

64 Branch Condition = BC = 6 bit

Horizontal: 256 CS ⇒ 256 bits



ICW = 281 bit

Control memory = 2^{15} CW

$= 2^{15} \times 281$ bits Ans

RISC Reduced Instruction set computer	CISC Complex Instruction set computer
1. It support less number of addressing Mode (AM)	1. It support more number of AM.
2. It support smaller Instruction set	2. It support larger Instruction set.
3. It support more number of Register	3. It support less number of Register
4. It support fixed length Instruction	4. It support variable length Instruction
5. It support 1 Instruction per cycle (CPI=1) (Cycle per Instruction =1)	5. It support number 1 Instruction Per cycle (CPI ≠1)
6. It support pipeline successfully	6. It support unsuccessful Pipeline
7. It is the expensive processor used in Real Time application	7. It is the low expensive processor
8. It is a super computer	8. General Purpose computer
9. It uses hardwired control unit. (Motorola processor, power processer, ARM processor)	9. It uses microprogrammed (vertical) control unit (Pentium processer)

Q.

Consider the following processor design characteristics:

I. Register-to-register arithmetic operations only.

II. Fixed-length instruction format.

III. Hardwired control unit.

Which of the characteristics above are used in the design of a RISC processor? [2018: MCQ 1M]

A. I and II only

B. II and III only

C. I and III only

D. I, II, and III only

Q.

Consider three floating point numbers A, B and C stored in registers R_A, R_B and R_C, respectively as per IEEE-754 single precision floating point format. The 32-bit content stored in these registers (in hexadecimal form) are as follows.

R_A=0×C1400000	R_B=0×42100000	R_C=0×41400000

Which one of the following is FALSE? [2022: MCQ 2M]

H.W

A. $A + C = 0$

B. $C = A + B$

C. $B = 3C$

D. $(B - C) > 0$

1. Introduction of COA
2. M/C Instn & AM
3. Floating Point Representation
4. ALU Data Path & Control Unit
5. **Pipelining**

V.V. Imp.

My Computer Properties.

2/3/3.8 GHZ Processor.

32 bit Processor. ⇒ word length = 32 bit

4 GB RAM ⇒ $2^{32} \times 8$ bit

1 TB Hard Disk.

① Cycle

② Cycle Time

→ Prog ET

CPU Time Calculation

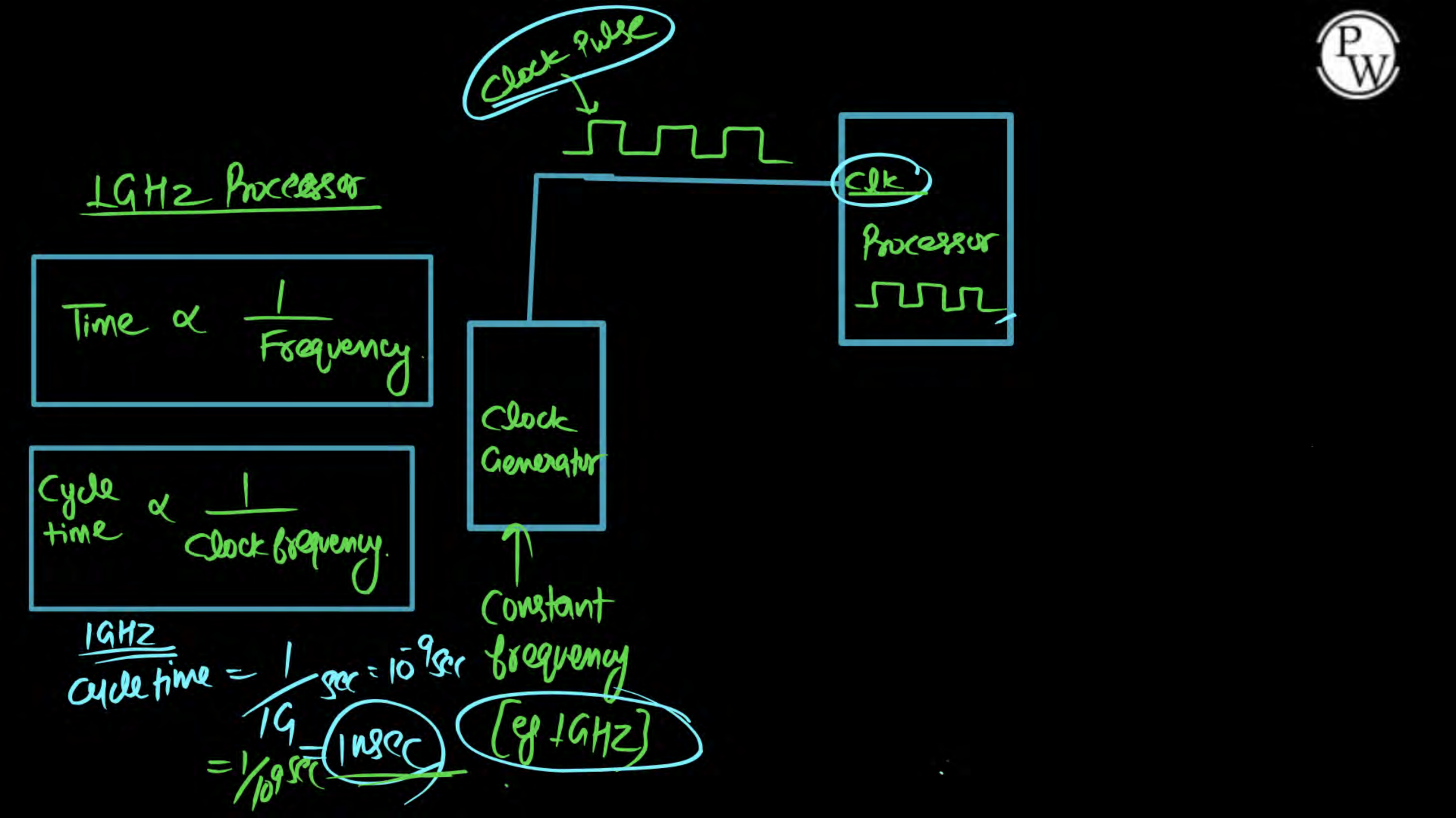
10^3 = 1 Kilo

10^6 = 1 Mega / million

10^9 = 1 Giga

MIPS [Millions of Instn Per Second]

SUPER Computer : FLOPS (Floating Point operation Per Second)



1GHz Processor

Time $\propto \frac{1}{\text{Frequency}}$

Cycle time $\propto \frac{1}{\text{Clock frequency}}$

1GHz

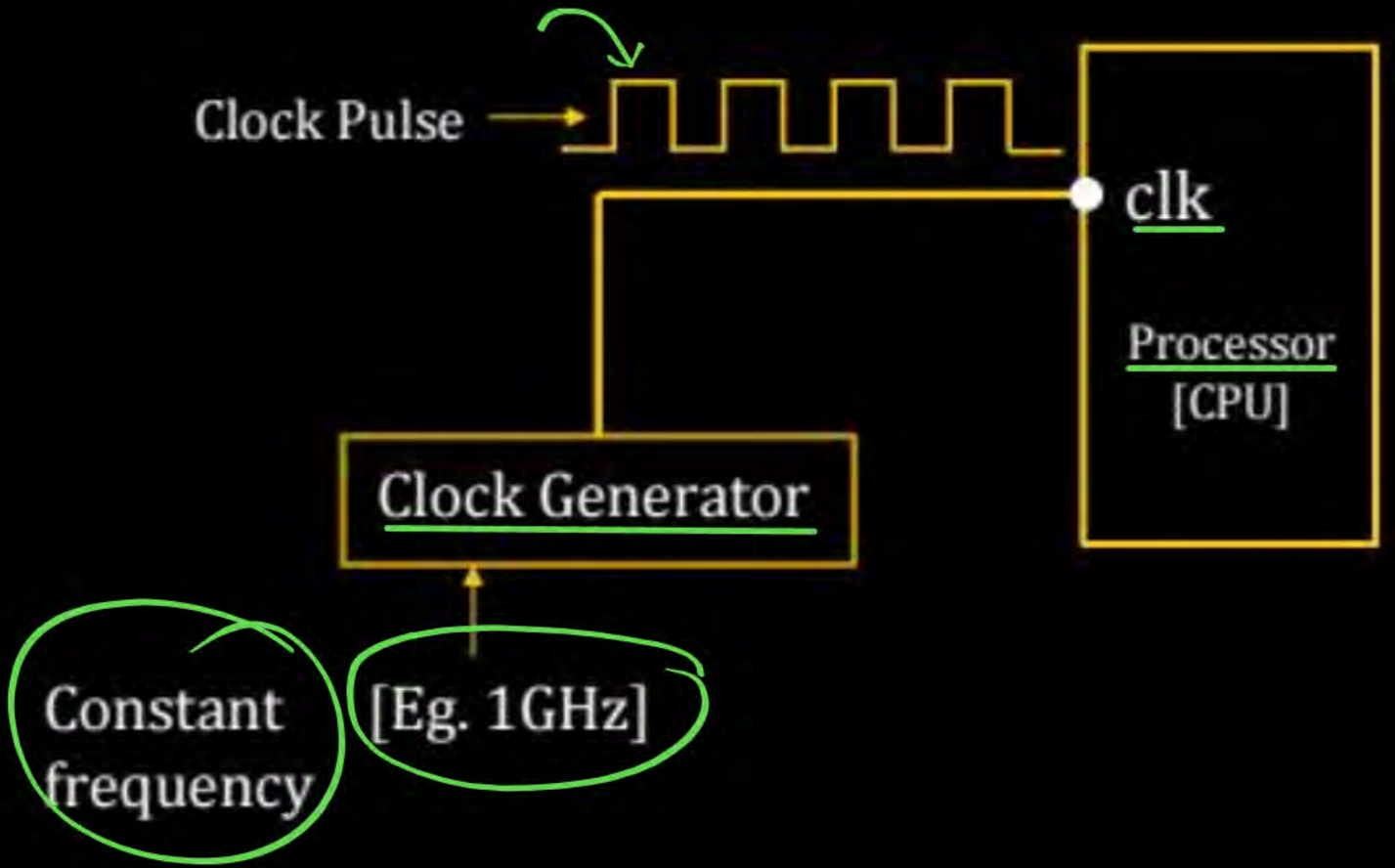
Cycle time $= \frac{1}{1G}$ sec $= 10^{-9}$ sec

$= 1/10^9$ sec $=$ 1nsec

CPU Time Calculations

- CPU Time Calculations Program Execution Time.
- Program Execution time is calculated based on the clock.
- Processor contain clock pins & these clock pin is externally connected with the clock generator.
- (or)
- So in the computer system all the operation are controlled by the clock, so CPU contain clock pins which is externally connected with clock generator.

- Clock Generator is operating with a constant frequency to generate the clock pulse [clock signal].
- These clock signals are carried into the CPU through (with the help of) Clock pin. So CPU operation are controlled by the clock signal.



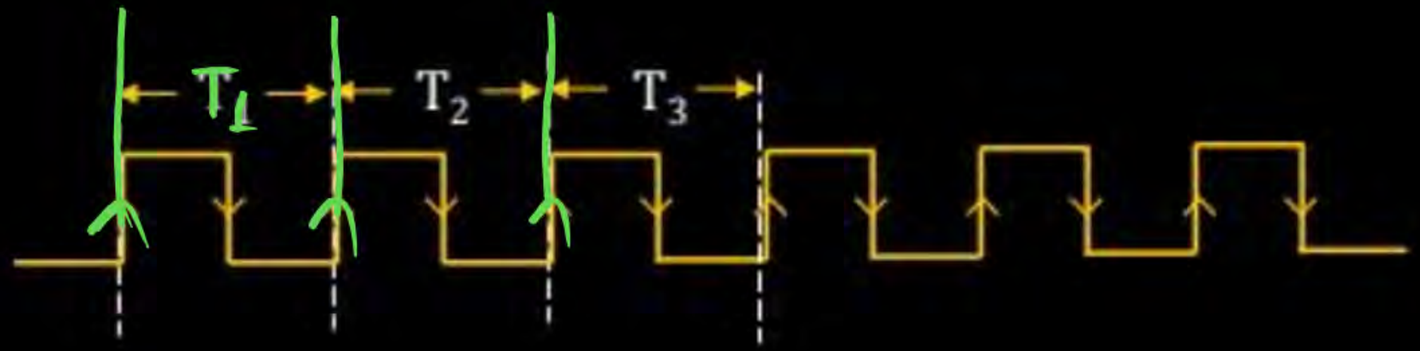
- Program E.T (Execution Time) is calculated based on 2 factor

  1) Cycle

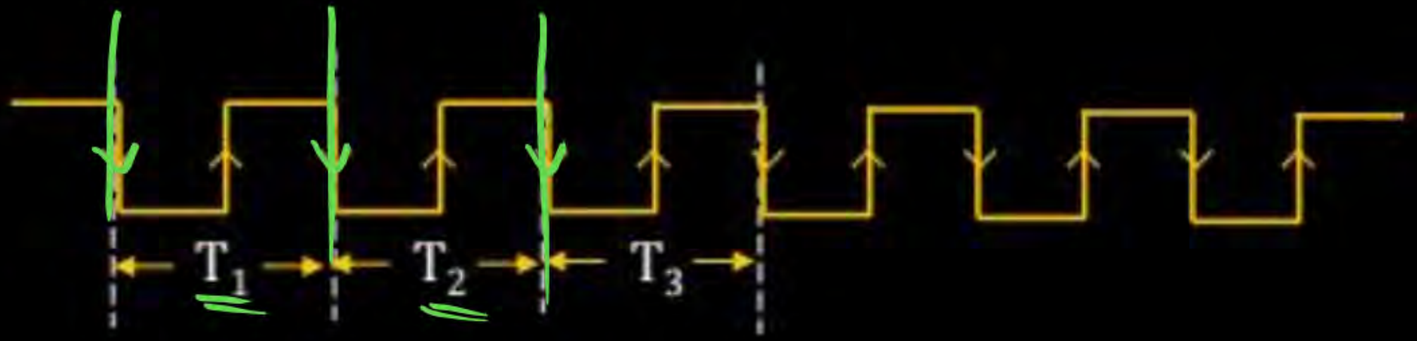
  2) Cycle Time

1) Cycle: Cycle is defined as clock pulse transition either from rising edge to rising edge (or) falling edge to falling edge.

Rising edge



Falling edge



2) Cycle Time: The time required to transfer the pulse either from rising edge to rising edge or falling edge to falling edge is called as cycle time.

Cycle time depends on the clock frequency.

$$\text{Cycle time} \propto \frac{1}{\text{Clock frequency}}$$

$$\text{Cycle time} \propto \frac{1}{\text{Clock frequency}}$$

Example: 1 GHz clock is used.

$$\text{Cycle time} = \frac{1}{1\text{GHZ}} \text{ sec}$$

$$= \frac{1}{10^9} \text{ sec}$$

$$= 10^{-9} \text{ sec}$$

Cycle time = 1ns (nanosecond)

2 GHz Processor.

$$\text{Cycle time} = \frac{1}{2\text{GHz}} \text{ sec}$$

$$\Rightarrow \frac{1}{2} \times 10^{-9} \text{ sec}$$

Cycle time = 0.5 nsec. Ans

1980 → KHz / MHz

1985

Todays – GHz

Q) In Program we have 100 Instn, & each Instn takes 6 clock cycle. Operating at 1GHz Processor Prog. ET ?

cycle time $= \frac{1}{1GHz} = 1nsec$

Soln

100 Instn Each takes 6 cycle.

Total cycle in Program $= 100 \times 6 = 600$ cycle

Prog. ET $= 600 \times 1$ nsec

$= 600$ nsec.

Q) In Program we have 100 Instn, & each Instn takes 6 clock cycle. Operating at 2GHz Processor Prog. ET ?

$\text{Cycle time} = \frac{1}{2\text{GHz}} = 0.5\text{nsec}$

Soln

100 Instn Each takes 6 cycle.

Total cycle in Program = $100 \times 6 = 600$ cycle

Prog. ET = $600 \times 0.5\text{nsec}$

= 300nsec

Q) In Program we have 100 Instn, & each Instn takes 6 clock cycle. Operating at 4GHz Processor Prog. ET ?

$$\text{Cycle time} = \frac{1}{4\text{GHz}} = 0.25\text{nsec}$$

Soln

100 Instn Each takes 6 cycle.

Total cycle in Program = $100 \times 6 = 600$ cycle

Prog. ET = 600×0.25 nsec

= 150 nsec

∴

Instruction count

100 Instⁿ ⟹ Each take 6 cycles (CPI) ⇒ 100 × 6 = 600 cycle

1GHz ⇒ cycle time = 1nsec

⇒ 600 × 1ns = 600nsec Ans

100

40 Inst ⇒ 8 cycle

30 Inst ⇒ 6 cycle

30 Inst ⇒ 5 cycle

40 × 8 + 30 × 6 + 30 × 5

⇒ 320 + 180 + 150

= 650 cycle

⇒ 650 × 1ns

= 650nsec Ans

Program [CPU] Time:

1. Instruction Count [IC]
2. CPI [Cycle Per Instⁿ]
3. Cycle time.

CPU Time Calculation / Program ET

CPU Time means program Execution Time.

Program Execution time = # Seconds / Program

= # Instruction/ program × #Cycle / Instruction × #Second / cycle

eg 100 × 6 × 1nsec = 600nsec

(IC) (CPI) (cycletime)

- # Instruction/ program → Instruction Count
- #Cycle / Instruction → Cycle per Instruction (CPI)
- #Second / cycle → Cycle time

100 × 6 × 1nsec = 600nsec .

Prog. ET / CPU time = IC × CPI × cycle time

CPU Time Calculation / Program ET

CPU Time means program Execution Time.

Program Execution time = # Seconds / Program

= # Instruction/ program × #Cycle / Instruction × #Second / cycle

- # Instruction/ program → Instruction Count
- #Cycle / Instruction → Cycle per Instruction (CPI)
- #Second / cycle → Cycle time

Prog. ET / CPU time = IC × CPI × cycle time

- Program is a combination of Data transfer, Data manipulation, & Transfer of control (TOC) Instruction. Different Instruction takes (consume) different cycle to complete the execution so,

i = Instruction type

$$\text{Prog. CPU Time} = \left[\sum (IC_i \times CPI_i)\right] \text{ Cycle time}$$

$\sum (IC_i \times CPI_i)$

$40 \times 8 + 30 \times 6 + 30 \times 5$

$= 650$ cycle

650×1 nsec

$\times$ cycle time

650 nsec

100 Instⁿ

40 ⇒ 8
30 ⇒ 6
30 ⇒ 5

40×8 + 30×6 + 30×5

100 Instⁿ ⇒ Total Cycle = 650 cycle

$$\text{Avg CPI} = \frac{650}{100} = 6.5$$

Avg CPI = 6.5

Let CPI_i be the number of cycles required for instruction type i, and I_i be the number of executed instructions of type i for a given program. Then we can calculate an overall(Average) CPI as follows:

$$CPI = \frac{\sum_{i=1}^{n}(CPIi \times Ii)}{I_c}$$

The processor time T needed to execute a given program can be expressed as $T = Ic \times CPI \times \tau$ (Where, $\tau = 1/f$, & I_c instruction count)

$\Rightarrow 950 \times 8.36 \times 0.66 \text{ sec}$
$= 5234.5 \times 10^{9}$

A common measure of performance for a processor is the rate at which instructions are executed, expressed as millions of instructions per second (MIPS) referred to as the MIPS rate. We can express the MIPS rate in terms of the clock rate and CPI as follows:

$$\text{MIPS rate} = \frac{Ic}{T \times 10^6} = \frac{f}{CPI \times 10^6} \text{ MIPS}$$

1.5

Q.

Common Data for Question 1, 2 & 3
Consider a 1.5 GHZ clock frequency processor used to execute the following program segment.

Instruction type	Instruction count	CPI
LOAD	300	11
STORE	200	9
ARITHMATIC	250	7
SHIFT	150	6
BRANCH	50	4

950

Q. 1 What is Average Instruction Execution of the program?

$$\text{Avg CPI} = \frac{300\times11 + 200\times9 + 250\times7 + 150\times6 + 50\times4}{950}$$

Avg CPI = 8.36 Cycle

Cycle time $= \frac{1}{1.5G}\,\text{sec} = \frac{1}{1.5}\times10^{-9}$

Cycle time = 0.66 nsec

Avg Instn ET = 8.36 cycle

$\Rightarrow 8.36 \times 0.66$ nsec

Avg Instn ET = 5.51 nsec Ans

Q. 2 What is the MIPS Rate of a program?

1 Instn Avg Instn ET = 5.51×10^{-9} sec

$$1 \text{ Instn} = 5.51 \times 10^{-9} \text{ sec}$$

In 1 sec = ? # Instn $\Rightarrow \frac{1}{5.51 \times 10^{-9}}$ Instn/sec.

$\Rightarrow \frac{1}{5.51} \times 10^{9}$ Instn/sec.

$\Rightarrow 0.1814 \times 10^{9}$ Instn/sec

$\Rightarrow 0.1814 \times 1000 \times 10^{6}$ Instn/sec

$\Rightarrow 181.4$ MIPS.

M

Q. 3 What is the total Program ET?

Avg Instn ET = 5.51 nsec

Prog Contain = 950 Instn

$$\text{Program ET} = 950 \times 5.51 \text{ nsec}$$

$$= 5234.5 \times 10^{-9}$$

$$\Rightarrow 5.234 \times 10^{-6}$$

Prog ET $\Rightarrow$ 5.234 usec Ans

Solution for Question 1

$$\text{Average Instruction ET} = \frac{\text{\# of cycle/prog}}{\text{\#of Instruction /prog}}$$

$$\Rightarrow \frac{(300\times11)+(200\times9)+(250\times7)+(150\times6)+(50\times4)}{950}$$

$$\Rightarrow \frac{3300+1800+1750+900+200}{950} = 8.36 \text{ Cycle}$$

$$\text{Cycle Time} = \frac{1}{\text{clock frequency}} = \frac{1}{1.5 \text{ Ghz}} \Rightarrow \frac{1}{1.5} \text{ nsec} \Rightarrow 0.66 \text{ nsec}$$

$$\text{Average Instruction ET} = 8.36 \times 0.66 \text{ nsec}$$

Average Instruction ET = 5.51 nsec

Solution for Question 2

Average Instruction ET $= 5.51 \times 10^{-9}$ sec

In 1 second $\rightarrow$ # Instruction

$= \frac{1}{5.5 \times 10^{-9}}$ Instruction / second

$= \frac{1}{5.51} \times 10^{9}$ Instruction / second

$= 0.1814 \times 10^{9}$ Instruction / second

$= 181.4 \times 10^{6}$ Instruction / second

$= 181.4$ MIPS

Solution for Question 3

Total Program ET = # Instruction / Program × Average Instruction ET

$= 950 \times 5.51$ nsec

$= 5234.5$ nsec

Program ET = 5.234 nsec

Q.2 1 nsec clock cycle processor consume 4 cycle for load and store operation and 6 cycle for ALU operation and 2 cycle for branch operation. The relative frequency of these operation are 40%, 40% and 20% respectively.

(i) What is the average instruction ET?

(ii). What is the performance in term of MIPS?

(iii). If program contain 10^6 instruction them what is total program ET?

(i) What is the average instruction ET?

Avg CPI = .40 × 4 + .40 × 6 + .20 × 2

⇒ 1.6 + 2.4 + 0.4

Avg CPI = 4.4 cycle

Avg Instn ET = 4.4 cycle

⇒ 4.4 × 1 nsec

⇒ 4.4 nsec Ans

(ii). What is the performance in term of MIPS?

$1\ \text{Instn} = 4.4 \times 10^{-9}\ \text{sec}$.

$\text{In } 1\ \text{sec} \Rightarrow \frac{1}{4.4} \times 10^9\ \text{Instn/sec}$.

$\Rightarrow \frac{1000}{4.4} \times 10^6\ \text{Instn/sec}$

$\Rightarrow 227.2 \times 10^6\ \text{Instn/sec}$

$\Rightarrow 227.2\ \text{MIPS}$ Ans

(iii). If program contain 10^6 instruction them what is total program ET?

1 Instn = 4.4×10^{-9} Sec.

Prog Contain = 10^6 Instn

Prog ET = $4.4 \times 10^{-9} \times 10^6$

$\Rightarrow 4.4 \times 10^{-3}$

$= 4.4$ msec Ans

Q.

Consider a 2.3ns clock cycle processor which consume 9 cycle for load and store instruction and 7 cycle for ALU instruction and 3 cycle for branch instruction. Relative frequency of their instruction are 40% , 40% and 20% respectively. New Processor is enhanced with an average CPI of 1. During the enhancement, cycle time is increased by 40%, them what is performance GAIN [speed up factor] of new and OLD Design?

$3.6 + 2.8 + 0.6$

Avg CPI = $[.40 \times 9 + .40 \times 7 + .20 \times 3]$ cycle

Avg CPI = 7 cycle & cycle time = 2.3 nsec

Avg Instⁿ ET = $7 \times 2.3 = 16.1$ nsec

$ET_{OLD} = 16.1$ nsec

40% Increased

$\Rightarrow 2.3 + 0.92$

New

CPI = 1

Cycle time $\Rightarrow$ 2.3 + (40% of 2.3 nsec)

$= 3.22$ ns

Avg Instn ET $= [0.4 \times 1 + 0.4 \times 1 + 0.2 \times 1]$ 3.22 nsec.

$ET_{New} = 3.22$ nsec

Performance GAIN $= \frac{\text{Performance of New}}{\text{Performance of OLD}} \Rightarrow \frac{ET_{OLD}}{ET_{New}} = \frac{10.1 \text{ ns}}{3.22 \text{ ns}} = 5$ Ans

RAM = 10 Hours

SHYAM = 4 Hours.

$$\text{Performance} \propto \frac{1}{ET}$$

SHYAM Performance is Best.

Q. Consider the execution of a program that results in the execution of 2 million instructions on a 400-MHz processor. The program consists of four major types of instruction. The instructions mix and the CPI for each instruction type are given below, based on the result of a program trace experiment:

Instruction Type	CPI	Instruction Mix (%)
Arithmetic and logic	1	60%
load/store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

The average CPI when the program is executed on a uniprocessor with the above trace results is CPI = $0.6 + (2 \times 0.18) + (4 \times 0.12) + (8 \times 0.1)$ = 2.24. The corresponding MIPS rate is $(400 \times 10^6)/(2.24 \times 10^6) \approx 178$

THANK YOU!