COMPUTER SCIENCE

Computer Organization and Architecture

Introduction of COA

Lecture_02

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01 Instruction Cycle

02 System Bus

Computer Generation.

CA & CO.

Component of the Computer

1. CPU
2. Memory
3. I/O.

- PC
- AR / MAR
- DR / MBR / MDR
- IR
- AC
- SP
- PSW
- GPR

Instruction Cycle.

The Process Required for each Instruction Execution is called Instruction Cycle.

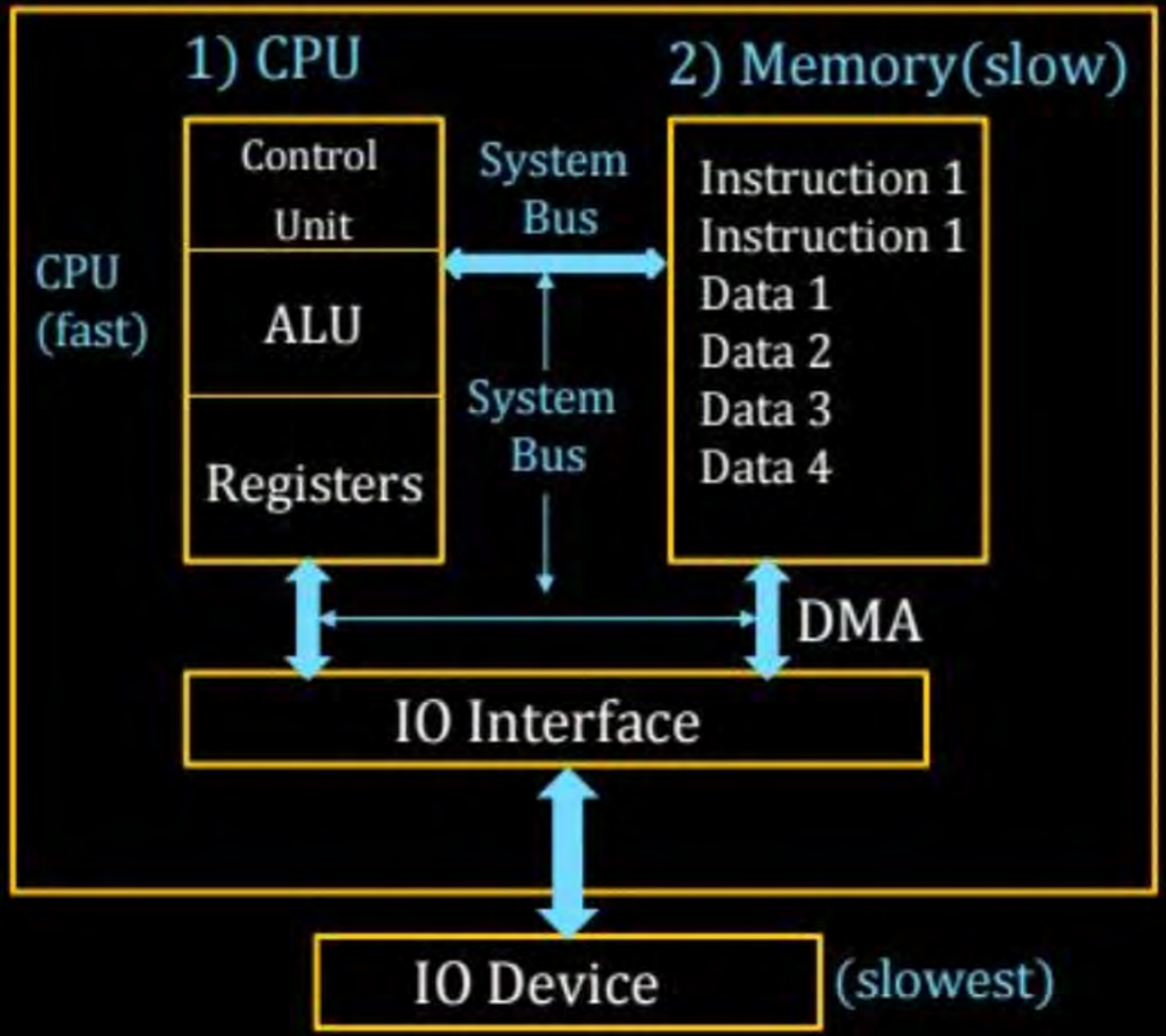
1. Fetch Cycle
2. Execute Cycle.

Component of Computer

(1) CPU

(2) Memory

(3) Input/output



Instruction Cycle

Instruction Cycle

① Fetch cycle

② Execute cycle

Instruction Cycle

① Fetch cycle : To Fetch (bring) the Instruction from Memory to CPU (IR).

At the end of Fetch Cycle. PC is updated (Increment). Now PC will Denote the Next Instruction Starting address.

Instruction Cycle

② Execute Cycle : The objective of Execute cycle is to Process the Fetch Instruction.

- Decode.
- Execute.

Instruction Cycle

The process required to execute the Instruction.

(or)

Instruction cycle describe the execution sequence of the instruction.

Instruction Cycle contain 2 sub cycle.

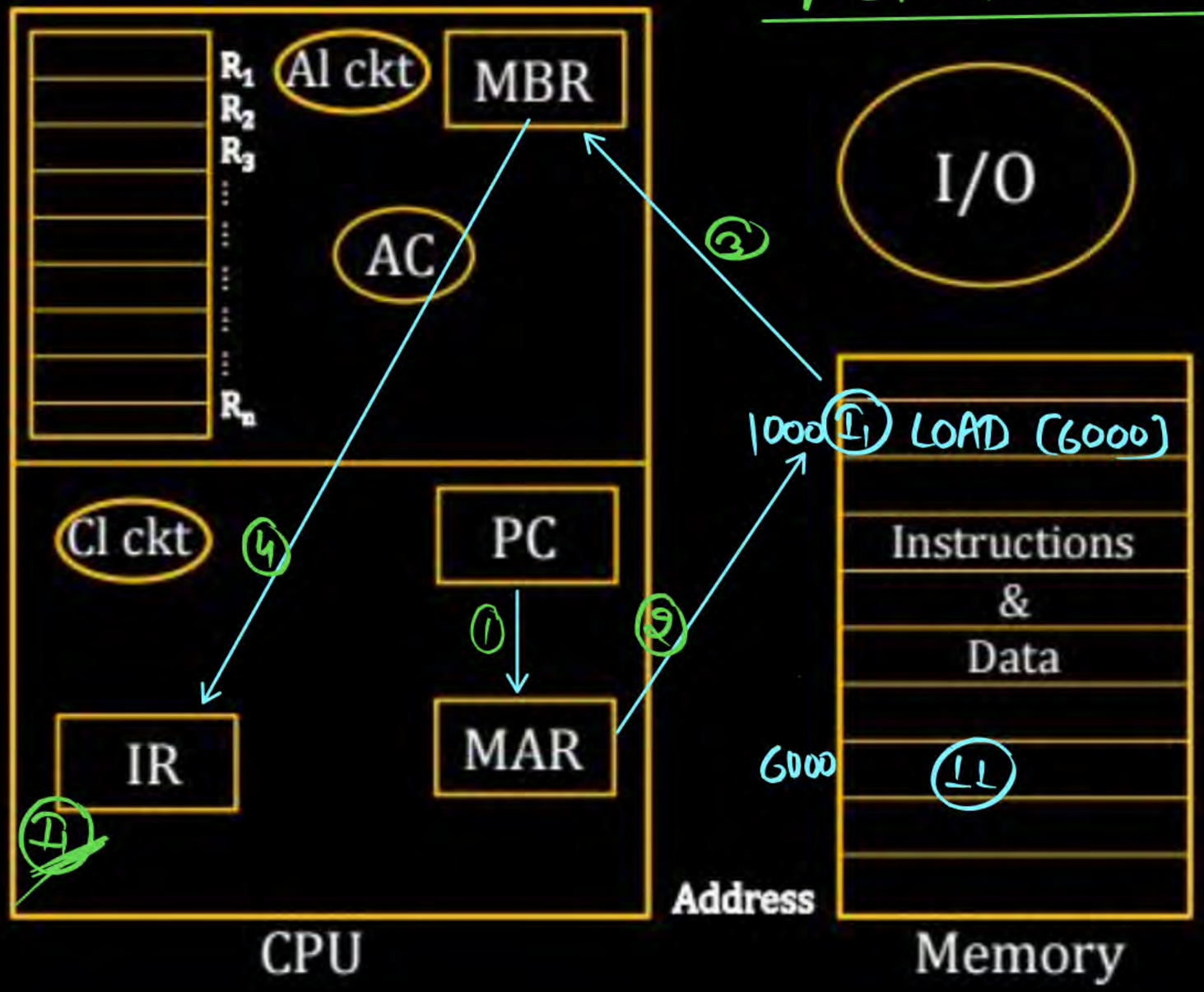
1) Fetch cycle
2) Execute cycle
   - Decode
   - Execute

Instruction Cycle

Steps in Fetch cycle.

Fetch cycle.

MEM to CPU (IR)

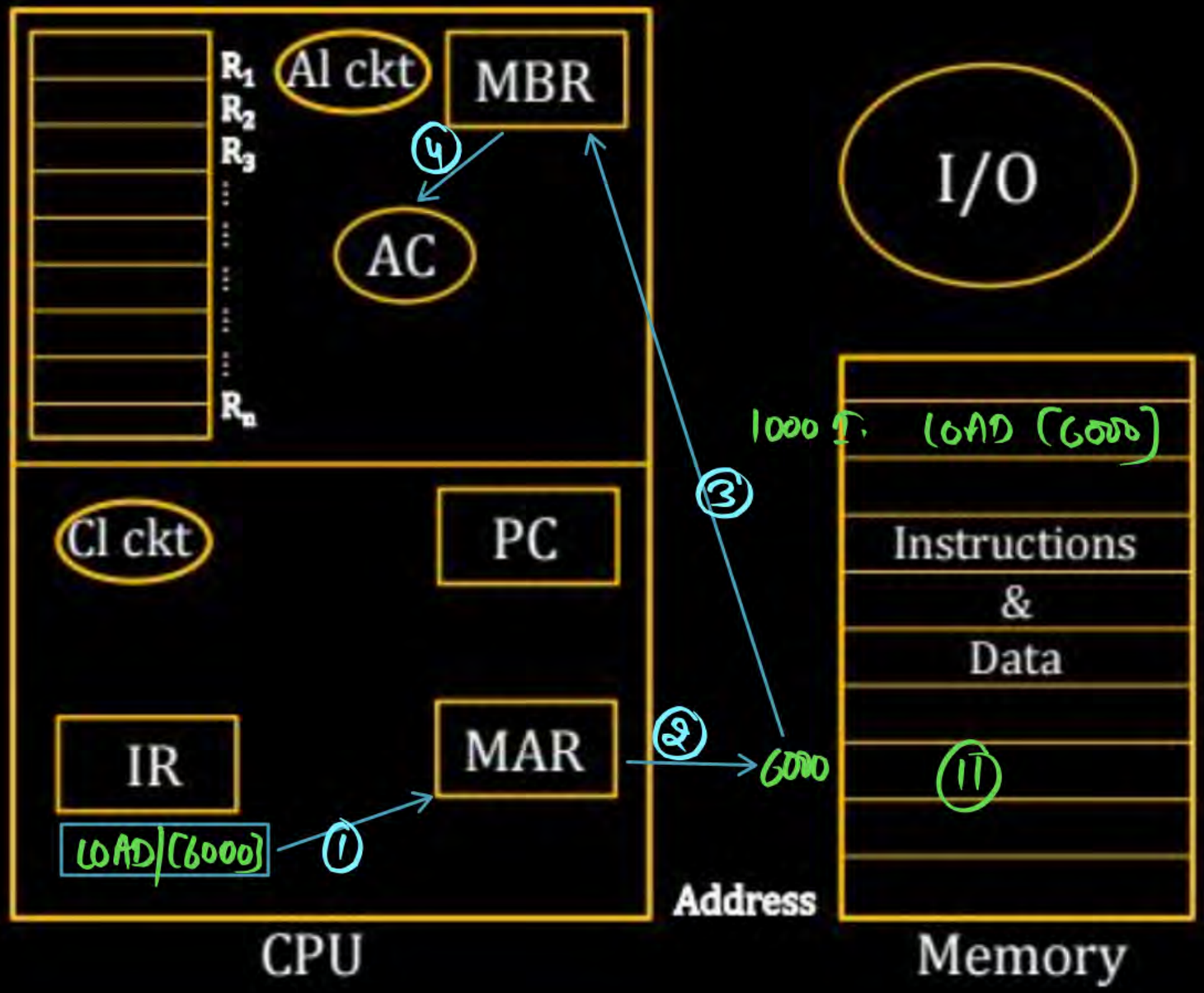


1000 I_1 : LOAD [6000]

AC ← M[6000]

[LD] LOAD: memory Read.

[ST] STORE: MEMOR write.



1000 : I1 LOAD [6000]

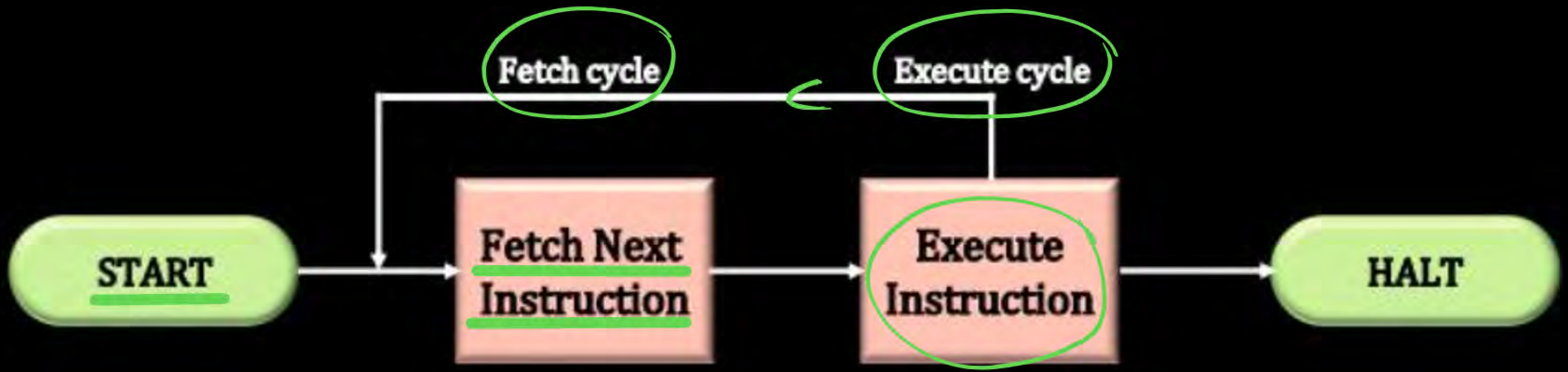
AC ← M[6000]

Steps in Instruction Cycle

- **Fetch cycle**
  1) IAC (Instruction Address Calculation) [MEM to CPU (IR)]
  2) IF (Instruction Fetch)
- **Execute cycle**
  - **Decode**
    3) Decoding (Analysis of Instruction
    (What opcode, how many operand,
    where operands are available))
    4) OAC (Operand Address Calculation)
    5) OF(Operand Fetch)
  - **Execute**
    6) DP (Data Processing)
    7) Result Storage

Fetch Cycle

- At the beginning of each instruction cycle the processor fetches an instruction form memory
- The program counter (PC) holds the address of the instruction to be fetched next
- The processor increments the PC after each instruction fetch so that it will fetch the next instruction in sequence
- The fetched instruction is loaded into the instruction register (IR)
- The processor interprets the instruction and performs the required action.



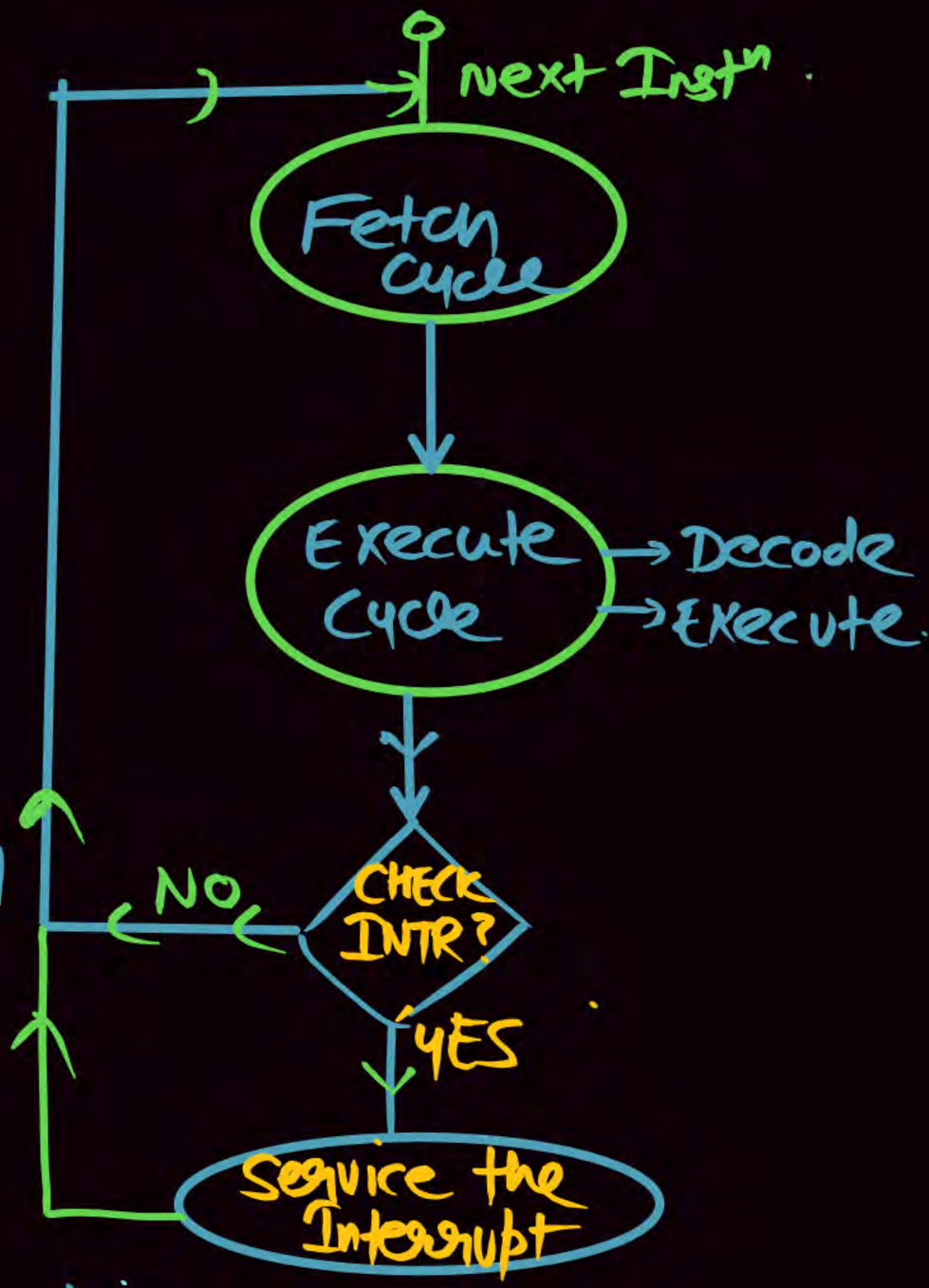
BASIC INSTRUCTION CYCLE

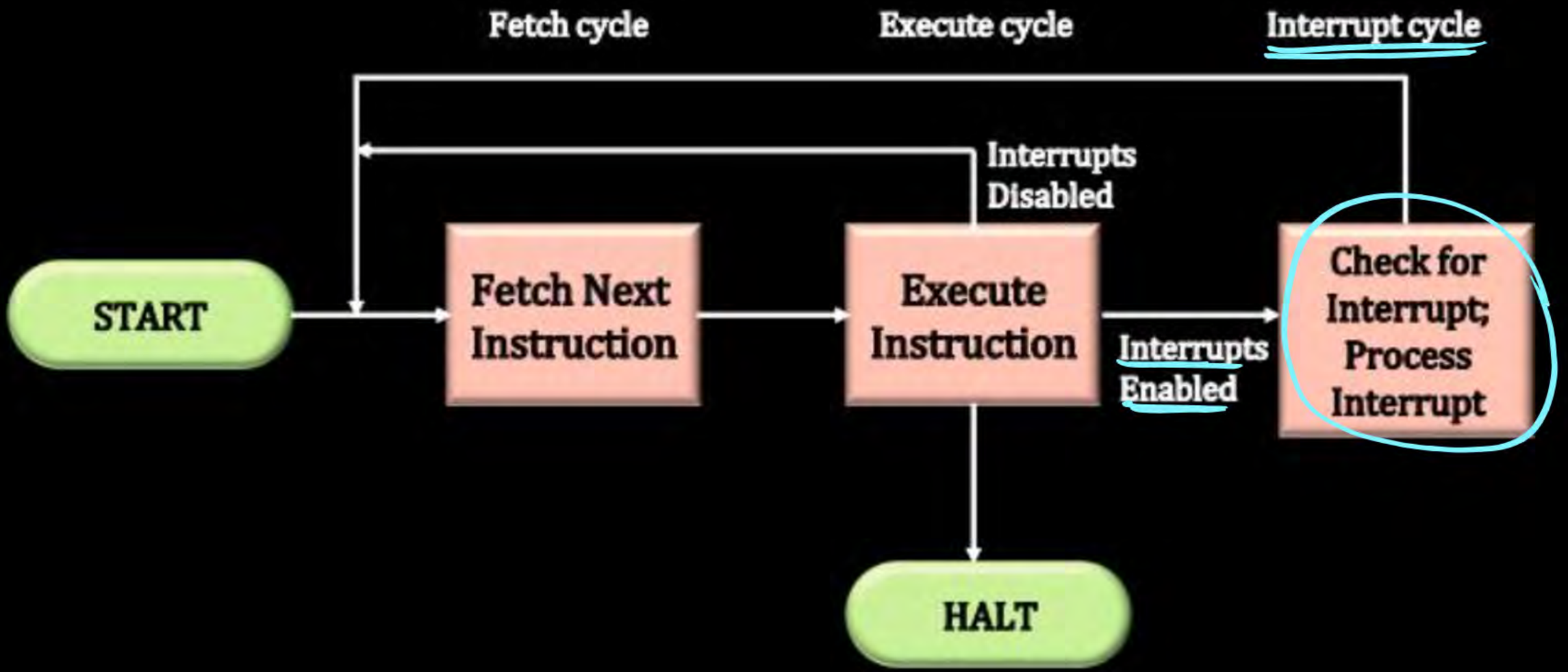
Instruction Cycle With Interrupt

1. Fetch cycle
2. Execute cycle
3. Interrupt cycle

Note

AFTER Completion of the Instruction Interrupt Will be Serviced.

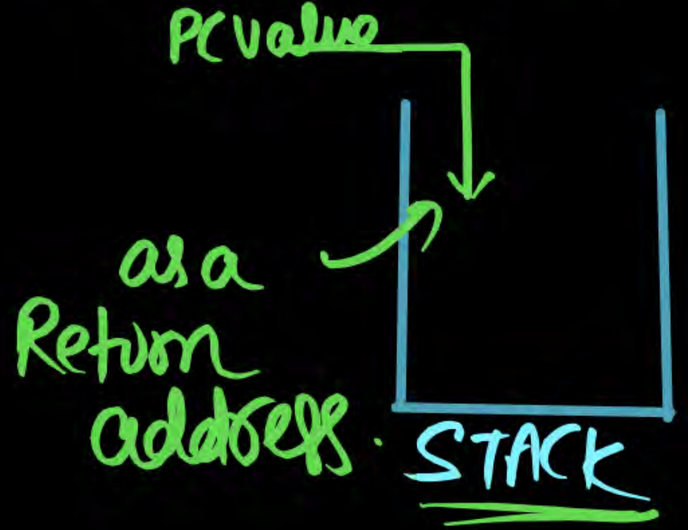




Instruction cycle with Interrupts

When Interrupt occur. then After Completion of current Instruction execution. interrupt will be serviced.

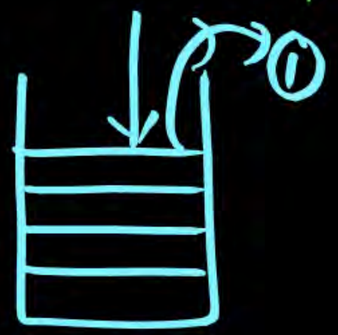
when Interrupt occur. it PUSH the PC Value into the Stack as a Return address & Controlled transfered to ISR (Interrupt Sub Routine)



& Controlled transferred to ISR.

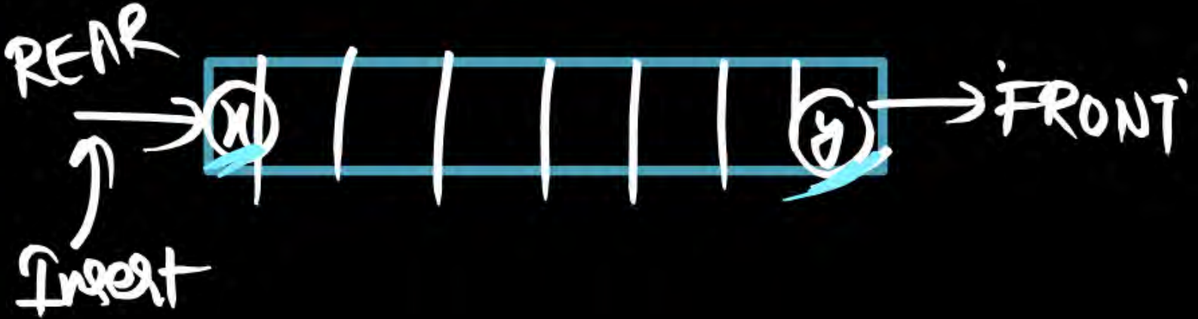
Q WHY in STACK ?

Soln LIFO [Last in First out]



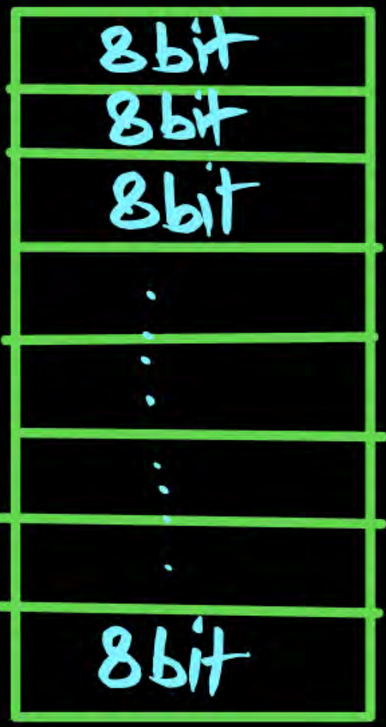
WHY Not in Queue.

FIFO



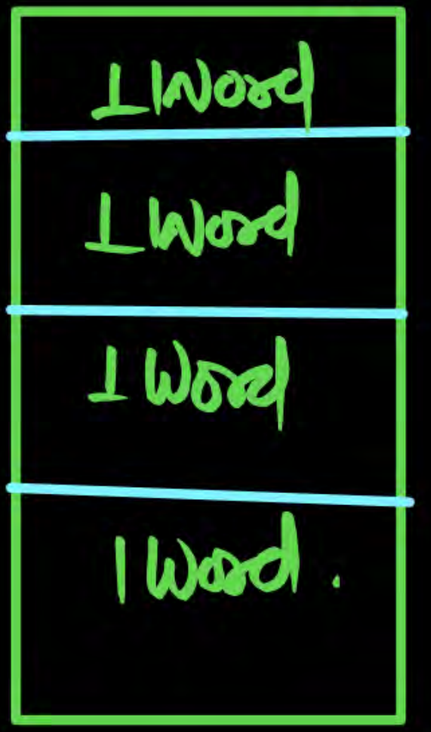
MEMORY

① Byte Addressable memory



1 cell = 1 Byte (8bit)

② Word Addressable memory



1 Cell = 1 Word

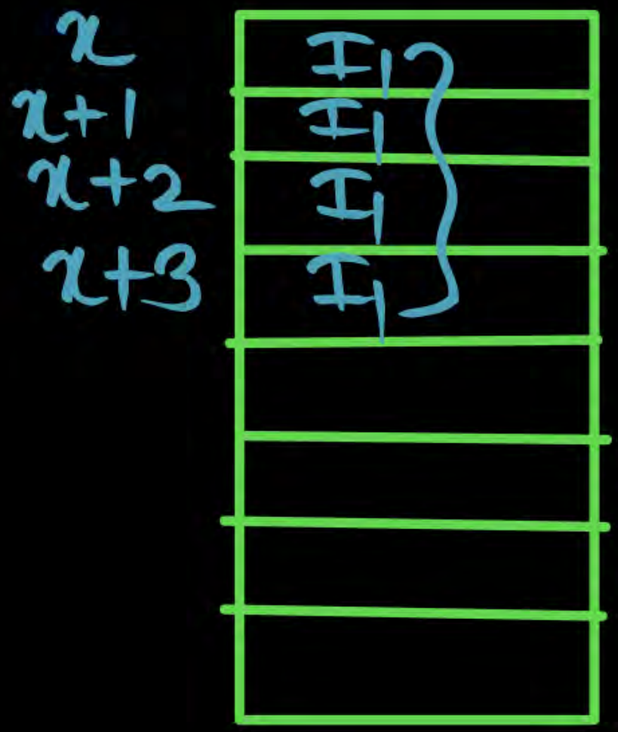
1 Word Size = 32 bit

1 Word = 4 Byte

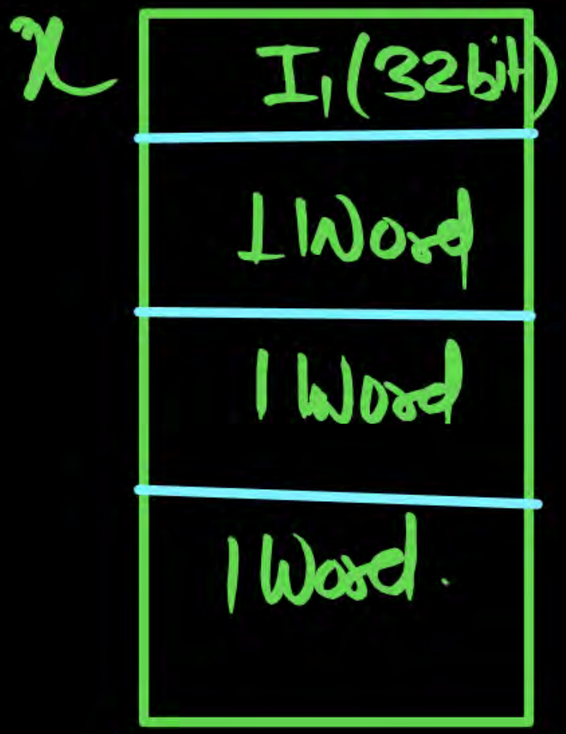
I_1 : 1 Word ≡ 4 Byte

MEMORY

① Byte Addressable memory



② Word Addressable memory.



1 Kilometer = 1000 meter.

1 Word = x bit

5.6 km ⇒ 5600 meter

5.6 X 1000 ⇒

5600 meter ⇒ 5600 / 1000 = 5.6 km

eg

1 Word = 32 bit ≒ 4 Byte

I_1 : 2 Word

✓ I_1 : 2 Word

⇒ 2 * 4 Byte

= 8 Byte

8 Byte Word ?

$\frac{8\ \text{Byte}}{4\ \text{Byte}}$ Words ⇒ 2 Words

Q.1 Consider the following program segment execute on Hypothetical processor. [4 Marks]

Assume that program is stored in the memory address 1000 (Decimal) onwards. During the execution of I_6 what could be value present in the Program counter. Assume that word size is 32 bit & memory is Byte Addressable?

1 Word = 32 bit = 4 Byte.

3w x 4B = 12 Byte

(32 bit)

1 Word = 4 Byte

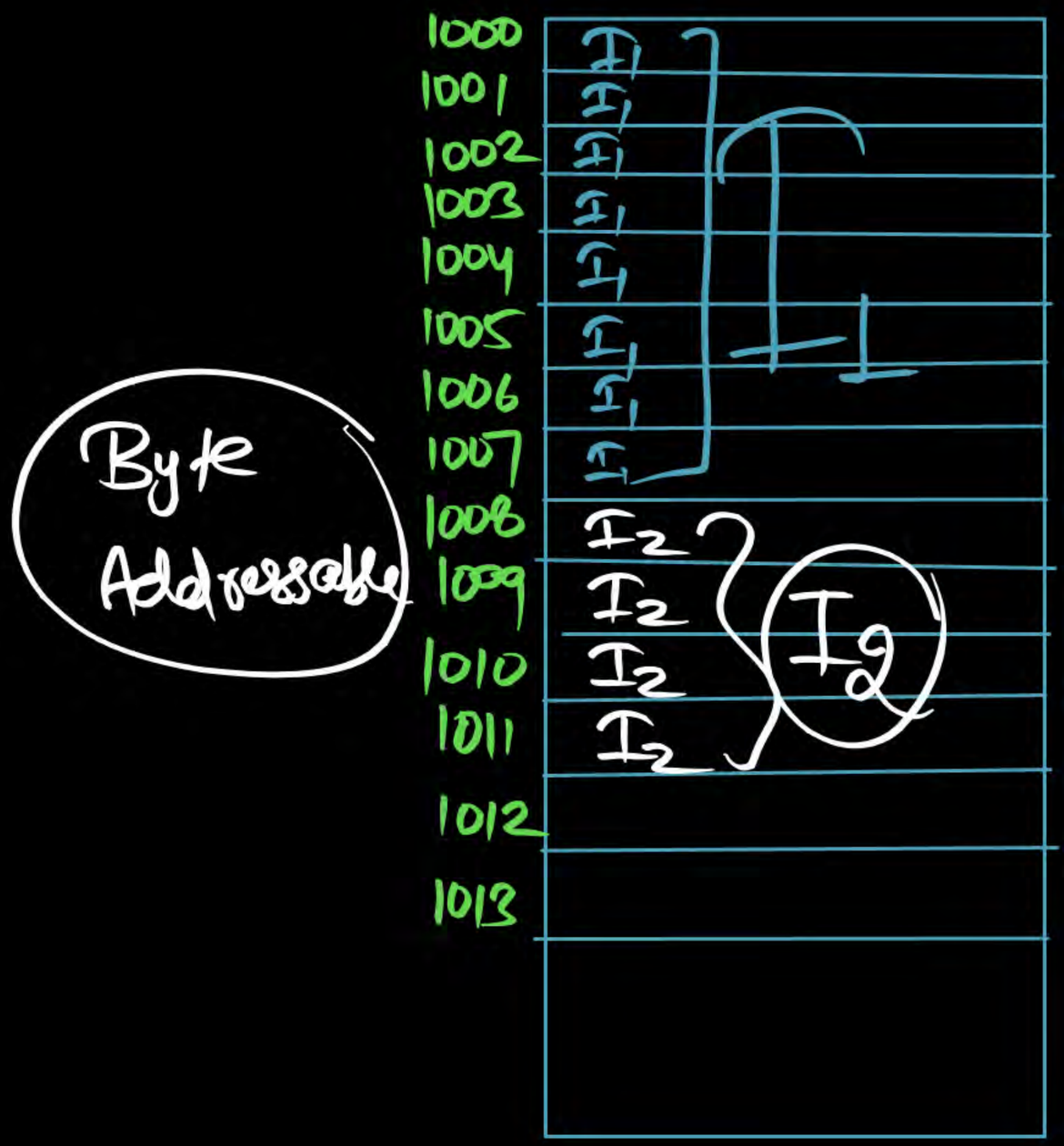
2 Word = 2 * 4B = 8 Byte.

1 Word = 1 x 4B = 4 Byte.

Byte Addressable

Instruction	Size (in words)	
I_1	2	1000 - 1007
I_2	1	1008 - 1011
I_3	1	1012 - 1015
I_4	3w	1016 - 1027
I_5	1	1028 - 1031
I_6	2	1032 - 1039
I_7	1	1040 - 1043.

Ans 1040.



Q During the execution of I_G What is PC Value?

Fetch

Execute.

PC Denote Next Instruction Starting Address.

Starting address of I_7.

Q.2 Consider the following program segment execute on Hypothetical processor. [4 Marks]

Assume that word size is 32 bit & memory is word addressable. The program is stored in the memory at address 1000 (Decimal) onwards. During the execution of I_5. What could be value present in the program counter?

Instruction	Size (in words)
I_1	2
I_2	1
I_3	1
I_4	3
I_5	1
I_6	2
I_7	1

Word Addressable.

1000 – 1001

1002

1003

1004, 5, 1006

1007

1008 – 1009

1010

Ans 2 1008

During Execution of I_5

If Interrupt occur During the execution of I_5 then what Return Address [value] Push into the Stack ?

Ans 1008

Q

I_5

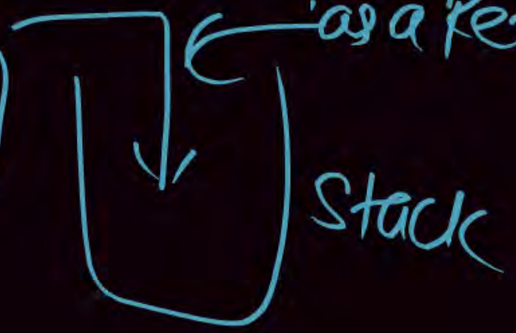
Interrupt occur

During execution of I_5

After I_5 Fetch PC Point (Denote) I_6 Starting address

But Now I_5 encounter Interrupt

So PC Value (I_6 Starting address) as a Return address

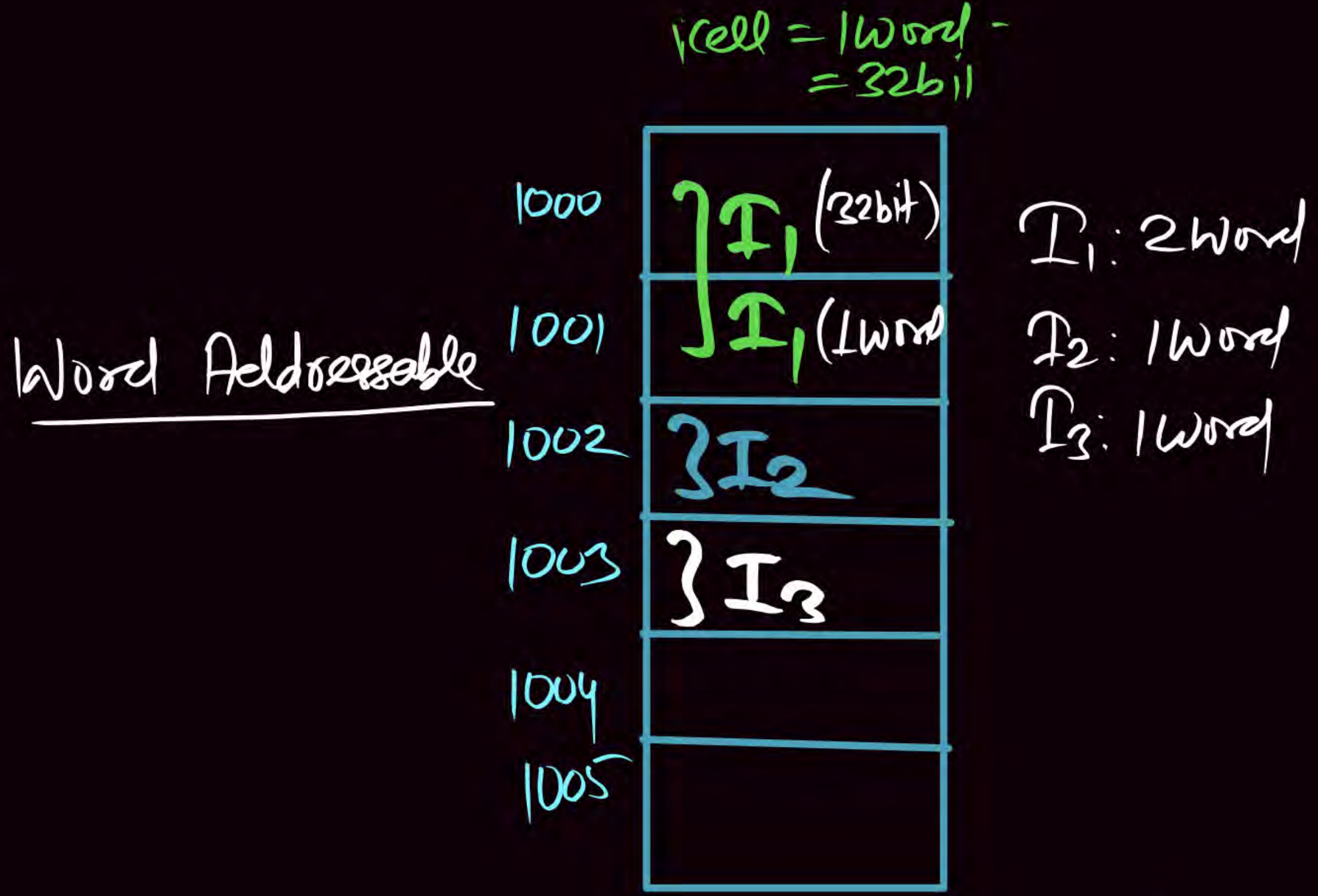


Fetch

Execute

Interrupt

(At the end of Fetch cycle) After Fetch PC Denote Next Instn Starting address.


1 cell = 1 word
= 32 bit
1000
1001
1002
1003
1004
1005
I1 (32bit)
I1 (1word
I2
I3
Word Addressable
I1 : 2 word
I2 : 1 word
I3 : 1 word

Q. Consider the following Program Segment for a hypothetical CN.

Instruction	Meaning	Instruction size (in words)
I_1 MOV r_0, 2000	$r_0 \leftarrow M[2000]$	3
I_2 MOV r_1, 3000	$r_1 \leftarrow M[3000]$	3
I_3 MUL r_0, r_1	$r_0 \leftarrow r_0 * r_1$	1
I_4 MOV 6000, r_0	$M[6000] \leftarrow r_0$	3
I_6 HALT	Machine Halt	1

51 cycle

Let the Clock Cycle required for various operation be as follows:
Instruction Fetch & Decode: 3 clock cycle per word
MUL with both operand & stored in register: 6 Clock Cycle.
Register to/from memory transfer: 4 clock cycle
The total number of clock cycle required to execute the program is____

Q. Consider the following program segment for a hypothetical CPU Having three users registers R1, R2 and R3. [GATE-2 Marks]

	Instruction	Operation	Instruction size (in words)	
I_1	MOV R1, 5000	R1 ← Memory[5000]	2	1000 – 1001
I_2	MOVR2, (R1)	R2 ← Memory[(R1)]	1	1002
I_3	ADD R2, R3	R2 ← R2 + R3	1	1003
I_4	MOV 6000, R2	Memory [6000] ← R2	2	1004 – 1005
I_5	HALT	Machine Halts	1	1006

Consider that the memory is word addressable with size 32 bits and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs during the ADD instruction, what will be the return address pushed on to the stack

(a) 1007 (b) 1004 (c) 1005 (d) 1016

ADD Instn (I_3) Fetch Cycle Done then PC Denote the Next Instn Starting address

PC Value → (Push into) Stack.

Q. Consider the following program segment for a hypothetical CPU Having three users registers R1, R2 and R3.

[GATE-2 Marks]

Instruction	Operation	Instruction size (in words)	
MOV R1, 5000	R1 ← Memory[5000]	2	1000 – 1007
MOVR2, (R1)	R2 ← Memory[(R1)]	1	1008 – 1011
ADD R2, R3	R2 ← R2 + R3	1	1012 – 1015
MOV 6000, R2	Memory [6000] ← R2	2	1016 – 1023
HALT	Machine Halts	1	1024 – 1027

I1 I2 I3 I4

Ans 1024

Consider that the memory is Byte addressable with size 32 bits and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the MOV 6000 R2 Instruction? the return address (in decimal) saved in the stack will be

(a) 1007 (b) 1020 (c) 1024 (d) 1028

! 1Word = 32bit

1Word = 4Byte.

I₁ : 2Word ⇒ 2×4 = 8Byte.

Q. Consider the following program segment for a hypothetical CPU Having three users registers R1, R2 and R3. [GATE- 2 Marks]

Instruction	Operation	Instruction size (in words)
MOV R1, 5000	R1 ← Memory[5000]	2
MOVR2, (R1)	R2 ←Memory [(R1)]	1
ADD R2, R3	R2 ← R2 + R3	1
MOV 6000, R2	Memory [6000] ← R2	2
HALT	Machine Halts	1

Let the clock cycles required for various operations be as follows:
Register to/from memory transfer:
3. Clock cycles.
ADD with both operand in register
1. Clock cycle
Instruction fetch and decode:
2. Clock cycles per word.
The total number of clock cycle required to execute the program is
(a) 29 (b) 24 (c) 23 (d) 20

COMMON DATA QUESTION (5 - 7)

Consider the following program segment, Here R1, R2 and R3 are the general purpose register.

Instruction	Operation	Instruction size (no. of words)
MOV R1, (3000)	R1←M[3000]	2
LOOP;		
MOV R2, M[R3] ADD R2, R1	R2←M[R3] R2←R1 + R2	1 1
MOV (R3), R2	M[R3] ←R2	1
INC R3	R3←R3+1	1
DEC R1	R1←R1-1	1
BNZ LOOP	Branch on not zero	2
HALT		Stop

Assume that the content of memory location 3000 is 10 and the content of the Register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the Numbers are in decimal.

Q.5 Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is

[2 marks]

(a) 10 (b) 11 (c) 20 (d) 21

COMMON DATA QUESTION (5 - 7)

Consider the following program segment, Here R1, R2 and R3 are the general purpose register.

Instruction	Operation	Instruction size (no. of words)
MOV R1, (3000)	R1←M[3000]	2
LOOP:		
MOV R2, M[R3] ADD R2, R1	R2←M[R3] R2←R1 + R2	1 1
MOV (R3), R2	M[R3] ←R2	1
INC R3	R3←R3 + 1	1
DEC R1	R1←R1 - 1	1
BNZ LOOP	Branch on not zero	2
HALT		Stop

Assume that the content of memory location 3000 is 10 and the content of the Register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the Numbers are in decimal.

Q.6 Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is

[2 marks]

(a) 100 (b) 101 (c) 102 (d) 110

COMMON DATA QUESTION (5 - 7)

Consider the following program segment, Here R1, R2 and R3 are the general purpose register.

Instruction	Operation	Instruction size (no. of words)
MOV R1, (3000)	R1←M[3000]	2
LOOP:		
MOV R2, M[R3] ADD R2, R1	R2←M[R3] R2←R1 + R2	1 1
MOV (R3), R2	M[R3] ←R2	1
INC R3	R3←R3+1	1
DEC R1	R1←R1-1	1
BNZ LOOP	Branch on not zero	2
HALT		Stop

Assume that the content of memory location 3000 is 10 and the content of the Register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the Numbers are in decimal.

Q.7 Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction "INC R3", what return address will be pushed on to the stack?

[2 marks]

(a) 1005 (b) 1020 (c) 1024 (d) 1040

THANK YOU!