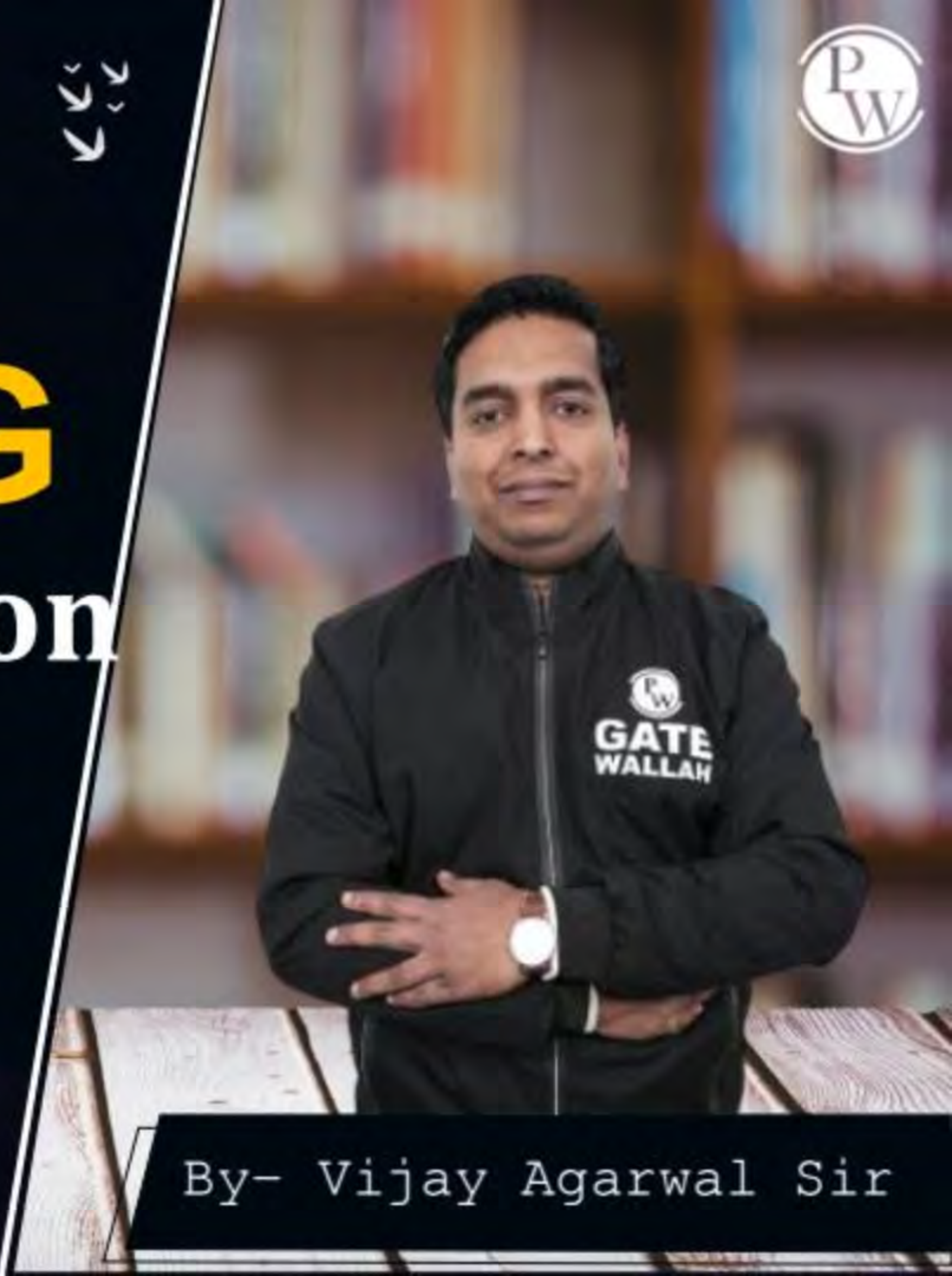
CS & IT ENGINEERING

Computer Organization & Architecture

Lecture No.- 01



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Recap of Previous Lecture

Topics to be Covered

- **Topic** Floating Point Representation
- **Topic** Memory Concept
- **Topic** Little Endian & Big Endian(Byte Ordering)
- **Topic** Clock Cycle Concept.

[MCQ]

#Q. 44FC6000H represents a floating point number in IEEE-754 single precision format. The value in decimal form is

bias = 127

A 2017

B 2018

C 2019

D 2020

$\boxed{\text{Ans [C].}}$

S	E(8bit)	M(23bit)
0	100 01001	11111 00 0110 0000 0000 0000

E = 10001001 = 137

$$(-1)^S \, 1.M \times 2^e \Rightarrow (-1)^S \, 1.M \times 2^{E-\text{bias}}$$

$$\Rightarrow (-1)^0 \, 1.11111000110000000000 \times 2^{137-127}$$

$$+1.11111000110000000000 \times 2^{+10}$$

$$+11111000011 \cdot 0000000$$

+(2019) Ans

[MCQ]

#Q. A number -1/8 is represented in IEEE 754 format as:

i)	1	01111100	00.....0
ii)	1	01111100	10.......0
iii)	1	01111111	0010......0
iv)	1	01111100	011.....1

Which of the following is TRUE?

A. i and ii

B. only i

C. i, ii, iii

D. i, iii, iv

Ans (B).

$$-\frac{1}{8} \Rightarrow -0.001 \times 2^{0}$$

$$\Rightarrow -1.0 \times 2^{-3}$$

$S = -ve$

$E = 124$

$E = 01111100$

1bit	8bit	23bit
S	E	M

1	01111100	0000000000000000

bias = 127

$e = -3$

$E = e + \text{bias}$

$= -3 + 127$

$$\boxed{E = 124}$$

[NAT]

#Q. 0x3F800000 represents a floating-point number in IEEE-754 single precision format. The value in decimal format is ______.

3F8 00000

$\boxed{\text{Ans}(1)}$

E = 8bit

0	0 1 1 1 1 1 1 1	0000 0000 0000 0000 0000 0000

Sign = 0   E = 127 , bias = 127 , M = 00000000000000000000000

$$(-1)^S \, 1.M \times 2^{E-\text{bias}}$$

$$(-1)^0 \, 1.000000000000 \times 2^{127-127}$$

$$+1.000000000 \times 2^0$$

$\Rightarrow +1$ Ans

[MCQ]

#Q. Which one of the following represents a denormal number in IEEE 754 single precision format?

A. 0xff800000

B. 0x7f7fffff

C. 0x00000001

D. 0x80000000

(a) | 1 | 11111111 | 000 0000 0000 0000 0000 0000 |

S=1 E=255, M=0 ⇒ $-\infty$

(b) | 0 | 11111110 | 111 1111 1111 1111 1111 1111 |

S=0 E=254 M: Any thing : Implicit Normalized.

[MCQ]

#Q. Which one of the following represents a denormal number in IEEE 754 single precision format?

A. 0xff800000

B. 0x7f7fffff

C. 0x00000001

D. 0x80000000

(c) | 0 | 000 0000 0 | 000 0000000 0 . - - - 1 |

S=0 E=0 M≠0 De Normalized Number.

(d) | 1 | 000 0000 0 | 0 0000 0 0000000000 |

S=1 E=0 M=0 ⇒ −0.

Topic : IEEE 754 Floating Point Representation

IEEE 754 Floating Point Representation

Single Precision
(32 bit)
Excess 127

S	E	M
1bit	8bit	23bit

32 bit

$$\text{bias} = 2^{K-1} - 1$$
$$= 2^{8} - 1$$
$$\text{Bias} = 127$$

Double Precision
(64 bit)
Excess 1023

S	E	M
1bit	11bit	52bit

64 bit

$$\text{bias} = 2^{11-1} - 1$$
$$\text{Bias} = 1023$$

Single Precision (32 bit)

S	E	M
1 bit	8 bit	23 bit

Sign(1 bit)	E(1 bit)	M(23 bit)	Value
0 or 1	00000000 E = 0	00000000000000000 0000000 M = 0	±0
0 or 1	11111111 E = 255	00000000000000000 0000000 M = 0	±∞
0 or 1	$1 \leq E \leq 254$	M = ...	Implicit Normalized form $(-1)^S \times 1.M \times 2^e$ $(-1)^S \times 1.M \times 2^{E-127 \text{ bias}}$
0 or 1	E = 0	$M \neq 0$	Denormalized number/Fractional form $(-1)^S \times 0.M \times 2^{E-127 \text{ bias}}$
0 or 1	E = 255	$M \neq 0$	Not a Number (NAN)

Topic : Double Precision

1-bit	11-bit	52-bit
S	E	M

Excess - 1023

Sign (1 bit)	E(11 bit)	M(52 bit)	Value
0 or 1	0000 0000 000 E = 0	00000000000.. M = 0	± 0
0 or 1	1111 1111 111 E = 2047	0000000000.. M = 0	$\pm \infty$
0 or 1	$1 \leq E \leq 2046$	M = __________	Implicit Normalization $(-1)^S \cdot M \times 2^e$ $(-1)^S \times 1 \cdot M \times 2^{E-1023}$
0 or 1	E = o	$M \neq 0$	Denormalized number/ Fractional Form $(-1)^S 0 \cdot M \times 2^{E-1023}$
	E = 2047	$M \neq 0$	Not a number

NOTE: When $E = 0$ then Value 0 $\begin{bmatrix} \text{when} \\ M = 0 \end{bmatrix}$ or fractional form $\begin{bmatrix} \text{when} \\ M \neq 0 \end{bmatrix}$

NOTE: When $E = 2047$

then Value ∞ $\begin{bmatrix} \text{when} \\ M = 0 \end{bmatrix}$ or Not a Number(NAN) $\begin{bmatrix} \text{when} \\ M \neq 0 \end{bmatrix}$

[MCQ]

#Q. Which of the given number has its IEEE-754 32-bit floating point representation as
(01000000110 0000 0000 0000 0000 0000)

A 2.5

$E = 128$

B 3.0

$\boxed{\text{Ans [C].}}$

C 3.5

D 4.5

$(-1)^S \, 1.M \times 2^{E - \text{bias}}$

$(-1)^0 \, 1.1100000000 \times 2^{128-127}$

$+1.110000 \times 2^{+1}$

$\Rightarrow 11.100 \Rightarrow +3.5$ Ans

[MCQ]

#Q. The range of representable normalized numbers in the floating point binary fractional representation in a 32-bit word with 1-bit sign, 8-bit excess 128 biased exponent and 23-bit mantissa is

A. 2^{-128} to $(2 - 2^{-23}) \times 2^{127}$

B. $(2 - 2^{-23}) \times 2^{-127}$ to 2^{128}

C. $(2 - 2^{-23}) \times 2^{-127}$ to 2^{23}

D. 2^{-129} to $(2 - 2^{-23}) \times 2^{127}$

| 0 | 00000000 | 00000000000000000 |

| 0 | 11111111 | 11111111111 . . . |

$\boxed{\text{Ans (A).}}$

M(23 bit)

0	00000000	00000000000000000000000

bias = 128.

$$(-1)^S \, 1.M \times 2^{E - bias}$$

$$(-1)^0 \, 1.000000000 \times 2^{0-128}$$

$$\Rightarrow +1.000000 \times 2^{-128} \Rightarrow \boxed{+1.0 \times 2^{-128}} \Rightarrow 2^{-128}$$

0	11111111	1111 1111 1111 1111 1111 111

S=0   E=255 , bias=128

$$(-1)^S \; 1.M \times 2^{E-\text{bias}}$$

$$\Rightarrow (-1)^0 \; 1.1111\,1111\,1111\,1111\,1111\,111 \times 2^{255-128}$$

$$\Rightarrow \boxed{+1.\underbrace{11111111111}_{23\text{ times}} \times 2^{+127}}$$

Right Shift 1 time

$$0.\underbrace{111111111}_{24\text{ times}} \times 2^{1} \times 2^{127}$$

$$(1-2^{-24}) \times 2 \times 2^{127}$$

$$(2-2^{-23}) \times 2^{127} \text{ Ans}$$

Left Shift 23 time.

$$\underbrace{1111111}_{24\ 1's} \times 2^{-23} \times 2^{127}$$

$$\Rightarrow (2-2^{-23}) \times 2^{127} \qquad (2^{24}-1) \times 2^{-23} \times 2^{127}$$

$$0111 = 1 - \frac{1}{2^3}$$

$$\left(1 - 2^{-3}\right)$$

[MCQ]

#Q. Consider IEEE 754 single precision floating point format

Sign	Exponent	Fraction
	8bits	23 bits

31 30 23 22 0

What is the maximum positive normal value represented by this format?

A 2^{127}

Ans (D).

B 2^{128}

C $(1 - 2^{24}).2^{127}$

D $(1 - 2^{24}).2^{128}$

0	111 1111 0	111 1111 1111 1111 1111 1111

$$(7\ F\ 7\ F\ F\ F\ F\ F)$$ **Ans**

0	11111110	1111 1111 1111 1111 1111 111

$$(-1)^S \; 1.M \times 2^{E-\text{bias}}$$

$E = 254$

$\text{bias} = 127$

$254 - 127$

$$(-1)^0 \; 1.\underbrace{11111111111111111111111}_{23 \text{ times}} \times 2$$

$$+1.\underbrace{1111\,11111\,1}_{23 \text{ Times}} \times 2^{127}$$

Right Shift 1 bit

$$0.\underbrace{111111111111111111111111}_{24 \text{ Times}} \times 2^{+1} \times 2^{127}$$

$$(1 - 2^{-24}) \times 2^{128}$$

Left Shift 23 bits.

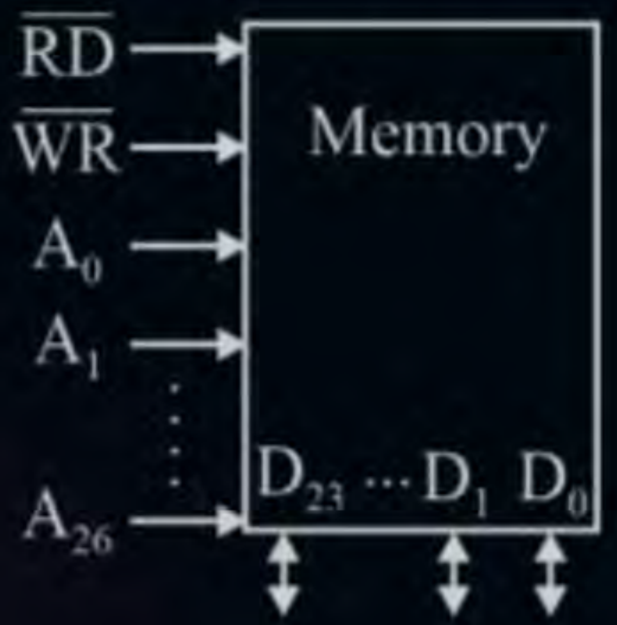
$$\underbrace{111111111111111111111111}_{24 \text{ times 1's}} \times 2^{-23} \times 2^{127}$$

$$[2^{24} - 1] \times 2^{-23} \times 2^{127}$$

$$(2^{1} - 2^{-23}) \times 2^{127} \Rightarrow (1 - 2^{-24}) \times 2^{128}$$

[NAT]

Consider the following memory design:



Address = 27

Data = 24 bits

$2^{27} \times 24$ bits $\Rightarrow \frac{2^{27} \times 24}{8}$ Byte

$\Rightarrow 2^{27} \times 3$ Byte

In above design A_0 to A_{26} are address pins and D_0 to D_{23} are data pins. The memory size in terms of byte is 384 MB.

$\Rightarrow$ 128 M × 3 Byte

$\Rightarrow$ 384 MByte

$\boxed{\text{Ans (384)}}$

[MCQ]

The memory size for P address lines and q data lines is given as:

(A) $2^P \times q$

(B) $2^q \times p$

(C) $2^{(P+q)}$

(D) $2^{(P-q)}$

$2^p \times q$

$\boxed{\text{Ans (A)}}$

[MCQ]

A processor has 51 distinct instructions and 50 general purpose register. System supports word addressable memory. Word size is 40 bits. One word instruction has an opcode, 3 register operands and memory operand. What is the size of main memory possible in the system?

(A) 64 kB

(B) 320 kw

(C) 320 kB

(D) None the these

51 Instn/operation ⇒ OPCODE = 6 bit   1 Word Size = 40 bit

50 Register ⇒ Reg AF = 6 bit

40 bit

OPCODE	Reg1	Reg2	Reg3	Mem AF
6 bit	6 bit	6 bit	6 bit	16 bit

Memory = 2^{16} Word

⇒ $2^{16} \times 40$ bits ⇒ $2^{16} \times 5$ Byte ⇒ 64K × 5 Byte

⇒ 320K Byte

$\boxed{\text{Ans (C)}}$

[MCQ]

The capacity of a memory unit is defined by the number of word multiplied by the number of bits/word. How many separate address and data lines are needed for a memory of ~~16~~ 32K × 16 ?

A. 8 address, 8 data line

B. 14 address, 8 data line

C. 15 address, 16 data line

D. 16 address, 16 data line

$\boxed{\text{Ans (C).}}$

$32K \times 16$

$2^5 \times 2^{10} \times 16$

$2^{15} \times 16$

15 bit Address

16 bit Dataline

[NAT]

Consider a computer system having 2 category of code module x & y with the following details.

Instruction type	CPI for this Instruction type
Type -1	1
Type -2	2
Type -3	3
Type -4	4

For the particular programing language statements, complier writer is considering 2 category of code module x & y with the following instruction count.

Code Module	Instructions Count. (IC) Instruction type			
	Type-1	Type-2	Type-3	Type-4
X	1	2	2	1
Y	4	2	1	1

$\boxed{\text{Ans } (4.375)}$

The CPI code module X is A & CPI for code module Y is B then the value of A + B is______.

CODE MODULE X = 1 + 2 + 2 + 1 = 6 Instn Total

CODE MODULE y = 4 + 2 + 1 + 1 = 8 Instn

$$\text{CPU Clock cycle} = \sum IC_i \times CPI_i$$

$$\text{MODULE X} = 1\times1 + 2\times2 + 2*3 + 1*4 = 1 + 4 + 6 + 4 = 15 \text{ Cycle Total}$$

$$\text{MODULE y} = 4\times1 + 2*2 + 1*3 + 1*4 = 4 + 4 + 3 + 4 = 15 \text{ Cycle}$$

$$\text{Avg } CPI_x = \frac{15}{6} = 2.5 \quad [A]$$

$$\text{Avg } CPI_y = \frac{15}{8} = 1.875 \quad [B]$$

$$A + B = 2.5 + 1.875 = \boxed{4.375} \text{ Ans}$$

Machine Instruction

& ADDRESSING MODE.

[MCQ]

Consider the following signed data and perform the addition operation

11010101

11010010

What is the status of carry, overflow, zero and sign flags after processing respectively?

(A) 1101

(B) 1011

(C) 1001

(D) 1100

Carry 1

$$
\begin{array}{r}
11010101 \\
+\ 11010010 \\
\hline
1\,10100111
\end{array}
$$

Carry = 1

Overflow = $1 \oplus 1$ = '0' (XOR)

zero = 0

Sign = 1

Ans (C).

$\frac{1}{\frac{0}{1}}$ $\frac{0}{\frac{1}{0}}$ $\frac{1}{\frac{1}{10}}$

$\frac{1}{\frac{1}{\frac{1}{11}}}$

Out of MSB	$\oplus$ (XOR)	MSB	
0		1	$\Rightarrow$ overflow = Set = 1
1		0	
0		0	Not overflow = Reset [0]
1		1	

[MCQ]

The unsigned integer can be written in 32bit- binary as
11110100 10011000 10110111 00001111
Putting it into four byte of memory beginning at address 100100 in big endian byte ordering scheme given in which picture?

$\boxed{\text{Ans(D)}}$

(A)

100100	100101	100102	100103
00001111	10110111	10011000	11110100

(B)

100100	100101	100102	100103
10110111	00001111	11110100	10011000

(C)

100100	100101	100102	100103
10011000	11110100	00001111	10110111

(D)

100100	100101	100102	100103
11110100	10011000	10110111	00001111

Little

100103	100102	100101	100100
11110100	10011000	1011 0111	00001111

Big Endian

100103	100102	100101	100100
00001111	10110111	10011000	11110100

[NAT]

If each address space represents one byte of storage space. The number of address lines needed to access the RAM CHIPS arranged in 4×8 array. Where size of each RAM CHIP 16K × 4 bits is_______ .

$\boxed{\text{Ans (18)}}$

$16K \times 4 \text{ bit} \Rightarrow 2^{14} \times 2^{2} \text{ bits} = 2^{16} \text{ bits}$.

Byte $\Rightarrow \dfrac{2^{16}}{8} \text{ Byte} \Rightarrow 2^{13} \text{ Byte}$.

To Represent 2^{13} Byte Memory $\quad$ 1RAM AF = 13 bits

Total RAM CHIP = 4X8 = 32 RAM CHIP = 5 bit Required to Represent these RAM Chip.

Total = 13 + 5

= 18 bits Ans

[MCQ]

Consider a 32 bit register which stores floating numbers in IEEE single precision format. What is the value of the number, if 32 bit are given below?

Sign(1bit)	Exponent (8bit)	Mantissa (23 bit)
0	10000011	1101 0000 0000 0000 0000 000

$E = 131$

$131 - 127$

$(-1)^0 \; 1.1101\,0000000 \times 2^{131-127}$

$+1.1101000000 \times 2^{+4}$

11101.00000

$+29$ Ans

(A) 48

(B) 50

(C) 56

(D) None of these

$\boxed{\text{Ans (D)}}$

2 mins Summary

Topic — Floating Point Representation

Topic — Memory Concept

Topic — Little Endian & Big Endian(Byte Ordering)

Topic — Clock Cycle Concept.

THANK - YOU