CS & IT ENGINEERING

Computer Organization & Architecture

1500 Series

Lecture No.- 04

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Recap of Previous Lecture

- Topic: Expand Opcode Techniue
- Topic: ALU Data Path
- Topic: Micro Operation & Micro Program
- Topic: Control Unit

Topics to be Covered

- Topic: Pipeline
- Topic: Pipeline Hazards

Min. 2 Marks
(3-4 Marks)

PIPELINE

- PIPELINE CONCEPT [ET, Speed up factors, efficiency, Throughput]
- Timing Diagram.
- PIPELINE HAZARDS.

PIPELINE HAZARDS

- (1) Structural Hazard
- (2) Data Hazards
- (3) Control Hazards.

[NAT]

1. A five-stage pipeline has stage delays of 100, 120, 125, 95 and 90 nanoseconds. The register that are used between the pipelined stages have a delay of 5 nano seconds. The total time to execute 500 independent instruction on this pipeline, assuming no pipeline stalls, is ___(nanoseconds, upto 1 decimal)

$k = 5$

$t_p = \max(\text{Stage Delay} + \text{Rubber Delay})$

$t_p = 130 \text{ nsec}$

$n = 500$.

$ET_{PIPE} = [k + (n-1)]\, t_p$

$\Rightarrow [5 + (500-1)] \times 125$

$= 504 \times 130$

$= 65,520 \text{ nsec}$ Ans

Ans (65,520)

[MSQ]

2 The performance of a pipelined processor has no effect if:

A The pipeline stages share hardware resources. ⇒ Structural Dep.

B The pipelined stages have different delays. ⇒ Control Dep.

C The consecutive instruction are dependent on one another. ⇒ Data Dependency

D None of these.

Ans (D)

The Performance of Pipeline effect Due to

1. Structural Hazard / Dependency ⇒ Resource Conflict
   Share the H/w Resource at same time.
2. Data Dependency ⇒ Consecutive Instⁿ Depend the Result of Previous
3. Control Dependency ⇒ Branch operation or Different Delay.

[NAT]

#Q. A 5-stage pipeline runs at 1 GHz. The pipeline can overlap all the instructions except branch instructions. Branch instructions incur 1 stall. If 25% instructions are branches, throughput of the system in MIPS (Million Instruction Per Second) is _____ 800ms.

Cycle time = $\frac{1}{1G}$ sec

Cycle time = 1nsec

Ans (800)

BIF = 25%

Stall = 1

#Stall/Instn = .25 × 1 = .25

Avg Instn ET = (1 + #Stalls/Instn) × Cycle time

$\Rightarrow (1 + .25) \times 1\text{nsec}$

ET	= 1.25 nsec

$\text{Throughput} = \frac{1}{ET} \Rightarrow \frac{1}{1.25} \times 10^9$

$= \frac{1000}{1.25} \times 10^6 = 800 \times 10^6$ Instn/sec

$\Rightarrow$ (800 MIPS) Ans

[MCQ]

#Q. The stage delay in a 5-stage pipeline is 400, 600, 500, 400, and 200 respectively in picoseconds. The second stage with delays 600 picoseconds in replaced with functionality equivalent design involving two stages 400 and 200 picoseconds. What is the percentage increase in throughput?

A 16.67

B 20

C 25

D 30

Ans (B)

OLD Design

$tp = \max(400, 600, 500, 400, 200)$

$\boxed{tp_{old} = 600}$

$\text{Throughput}_{old} = \frac{1}{600}$

New Design

$tp = \max(400, 400, 200, 500, 400, 200)$

$\boxed{tp_{new} = 500 \text{ nsec}}$

$\text{Throughput}_{new} = \frac{1}{500}$

$$\%\ \text{Increment in Throughput} = \frac{\text{New} - \text{OLD}}{\text{OLD}} \Rightarrow \frac{\frac{1}{500} - \frac{1}{600}}{\frac{1}{600}} = \frac{\frac{1}{5} - \frac{1}{6}}{\frac{1}{6}}$$

$$\Rightarrow \frac{6-5}{30} \times \frac{6}{1}$$

$$\Rightarrow \frac{6}{30} = \frac{1}{5} = 20\%$$ Ans

[MCQ]

#Q. A pipeline P operating at 400 MHz has a speed up factor of 6 and operating at 70% efficiency. How many stages are there in pipeline?

A 5

B 6

C 8

D 9

Ans (D).

$\eta = \frac{S}{K}$

$70\% = \frac{6}{K} \Rightarrow K = \frac{6}{70} \times 100 = \frac{60}{7} \Rightarrow \lceil 8.57 \rceil = 9$

[NAT]

#Q.6. An 8-stages perfectly balanced instruction pipeline has [illegible]-cycle-time overhead. If 35% of the instruction in 4 pipeline stall cycles, the speedup achieved with respect to non-piped execution when an application is executing on this 8-stage pipeline is _____ 3.33 Ans

Ans (3.33).

K = 8 Stage (Perfectly Balanced

B.I.F = 35%

Stall = 4 Stalls.

Stalls / Instn = .35 × 4 = 1.4

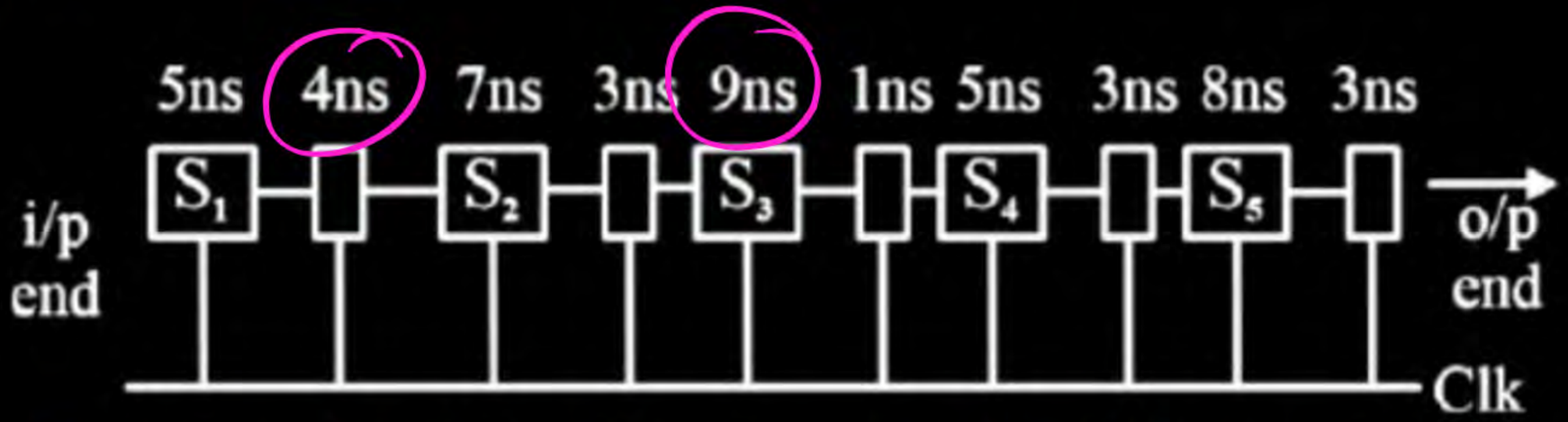
Avg Instn ET = (1 + # Stalls / Instn)

= (1 + 1.4) = 2.4

$$\text{Speed up Factor} = \frac{\#\text{ Stages (K)}}{(1 + \#\text{ Stalls / Instn})} \Rightarrow \frac{8}{(1+1.4)} = \frac{8}{2.4} = 3.33$$ Ans

[NAT]

7 Consider the following Pipeline used to execute the program which contain 700 Instructions.



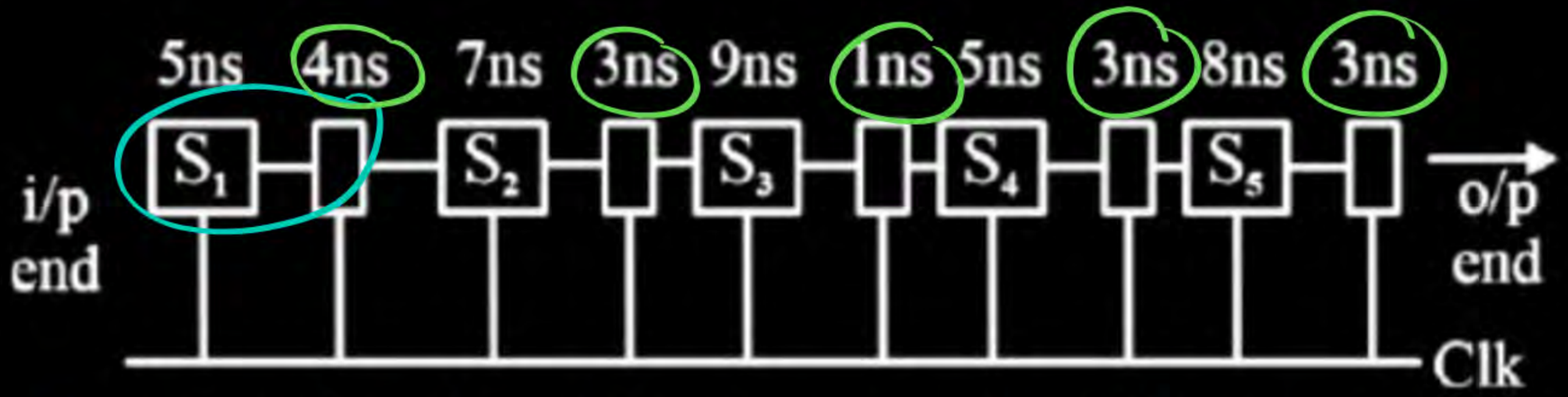
The execution time (in nano second) of the program is _____.

$t_p = 9 + 4$

$= 13$ nsec

[NAT]

Consider the following Pipeline used to execute the program which contain 700 Instructions.



The execution time (in nano second) of the program is 7744 Ans

$t_p = \max(\text{Stage Delay} + \text{Buffer Delay})$

$= \max(5+4, 7+3, 9+1, 5+3, 8+3)$

$\max(9, 10, 10, 8, 11)$

Ans (7744).

$t_p = 11 nsec$

$k = 5$

$n = 700$

$ET = [k + (n-1)] t_p$

$\Rightarrow [5 + (700-1)] \times 11$

$= 704 \times 11$

$\Rightarrow 7744 nsec$ Ans

[NAT]

#Q. (8) A pipelined processor uses a 4 stage instruction pipeline with the following stages: instruction fetch (IF) instruction decode (ID), execute (EX) and write back (WB). The arithmetic operation as well as the local and store operation are carried out in the EX-stage.

Consider the following sequence of instruction:

meaning

I_1:	ADD	R_4, R_0, R_1:	$R_4 \leftarrow R_0 + R_1$
I_2:	MUL	R_5, R_4, R_2:	$R_5 \leftarrow R_4 * R_2$
I_3:	ADD	R_7, R_4, R_5:	$R_7 \leftarrow R_4 + R_5$
I_4:	LOAD	$R_6, M(R_5)$:	$R_6 \leftarrow M(R_5)$
I_5:	MUL	R_4, R_7, R_7:	$R_4 \leftarrow R_7 * R_7$
I_6:	STORE	$M(R_6)\ R_4$;	$M[R_6] \leftarrow R_4$
I_7:	BNE	$R_4\ R_6\ I_2$;	If $(R_4 \neq R_6)$ then I_2

The number of read-after-write (RAW) dependencies in the sequence of instructions are ____ (9) Ans

[NAT]

#Q(8) A pipelined processor uses a 4 stage instruction pipeline with the following stages: instruction fetch (IF) instruction decode (ID), execute (EX) and write back (WB). The arithmetic operation as well as the local and store operation are carried out in the EX-stage.

Consider the following sequence of instruction:

I_1:	ADD	R_4, R_0, R_1;	$R_4 \leftarrow R_0 + R_1$
I_2:	MUL	R_5, R_4, R_2;	$R_5 \leftarrow R_4 * R_2$
I_3:	ADD	R_7, R_4, R_5;	$R_7 \leftarrow R_4 + R_5$
I_4:	LOAD	$R_6, M(R_5)$;	$R_6 \leftarrow M(R_5)$
I_5:	MUL	R_4, R_7, R_7;	$R_4 \leftarrow R_7 * R_7$
I_6:	STORE	$M(R_6)\ R_4$;	$M[R_6] \leftarrow R_4$
I_7:	BNE	$R_4\ R_6\ I_2$;	If $(R_4 \neq R_6)$ then I_2

meaning.

#RAW Dependency.

① $I_2 - I_1$
② $I_3 - I_2$
③ $I_3 - I_1$
④ $I_4 - I_2$
⑤ $I_5 - I_3$
⑥ $I_6 - I_5$
⑦ $I_6 - I_4$
⑧ $I_7 - I_6$
⑨ $I_7 - I_5$

⑨ Ans

The number of read-after-write (RAW) dependencies in the sequence of instructions are ___ ⑨ Ans

[NAT]

9 (11.W)

Consider a pipeline with IF, ID and WB stages taking 1 clock cycle each. The EX stage takes 2 clock cycle for any arithmetic operation and 3 clock cycle for store operation. Operand forwarding from the Ex to ID stage is used for the below set of instruction sequence.

ADD, $R_2 \leftarrow R_0, R_1$, $R_2 \leftarrow R_0 + R_1$,

MUL, $R_4 \leftarrow R_2, R_3$, $R_4 \leftarrow R_2 \times R_3$

SUB, $R_5 \leftarrow R_2, R_4$, $R_5 \leftarrow R_2 - R_4$

STORE R_5, x, store the content of M [X] to register R_5

The number of clock cycles required to complete the sequence of instruction is?

(1)

[NAT]

10 H.W

Consider a pipeline which is operating with a 1.8 GHz frequency contain 8 stages. Pipeline allow overlapping of all the instruction except branch instruction. Processor stop fetching of a sequential instruction after the branch instruction until the outcome is known. All the instruction output is available at the end of execution [Last Stage]. Program contain 40% branch instruction, among them 60% are conditional branch in which 40% instruction does not satisfy the condition (when condition is false) then the following instruction are overlapped then what is the average instruction execution time (in nano seconds) ____? (upto 2 decimal point)

2

[NAT]

(11)

The instruction pipeline of RISC processor has the following stages: Instruction fetch (IF), Instruction Decode(ID), Operand Fetch (OF), Perform Operation (PO), and Write Back (WB). The IF, ID, OF and WB stage takes 1 clock cycle each for every instruction. Consider a sequence of 100 instruction. In the PO stage 50 instruction takes 6 clock cycle each, 30 instruction takes 5 clock cycle and 20 instruction takes 3 clock cycle. Assume that there is no Data Hazard and no control Hazard. Then number of clock cycle required for completion of execution of the sequence of instruction is 514 Ans

Ans(514)

IF, ID, OF, PO, WB

$k = 5, \quad n = 100$

$ET_{PIPE} = [k + (n-1)]\,Cycle$

$\Rightarrow (5 + 100 - 1)$

$= 104\ Cycle$

$ET_{Total} = ET_{Normal} + Stalls$

$\Rightarrow 104 + 410$

$= 514$ Ans

Stage. CPI = 1

PO

		Extra Cycle
50	6 Cycle	5 Cycle
30	5	4 Cycle
20	3	2 Cycle

$Stalls = 50 \times 5 + 30 \times 4 + 20 \times 2$

$\Rightarrow 250 + 120 + 40$

$\Rightarrow 410$


OR

IF, ID, OF, PO, WB

$k=5, \quad n=100.$

Stage.

	PO
50	6
30	5
20	3

IF ID OF WB + PO

$\Rightarrow 1+1+1+1 \quad +(50\times6+30\times5+20\times3)$

$\Rightarrow 4+(300+150+60)$

$\Rightarrow 4+510$

$= 514$ nsec Ans

[MCQ]

H.W

Consider a hypothetical processor with five pipeline stages (IF, ID, EX, MEM, WB) perfectly balanced & clock cycle time 11 nsec. With the following branch frequencies:

Jump and calls-25%

Conditional branches -30%

Taken conditional branch – 60%

Un-conditional & conditional branches are resolved at the end of fifth and sixth stage respectively processor always executes the branch successor regradless of target and flushes the pipeline if branch is taken. What is the throughput (in million instructions per second) of the system?

(3)

A

B

C

D

[NAT]

We have two design D_1 and D_2 for a synchronous pipeline processor. D_1 has 6 pipeline stages with execution times of 5ns, 3ns, 6ns, 4ns, 5ns, and 2ns. While the design D_2 has 8 pipeline stage each with 3ns execution time. How much time can be saved using design D_2 over design D_1 for executing 200 instructions 609 Ans

$D_1 \Rightarrow k = 6$

$t_p = 6ns \quad n = 200$

$ET_{D_1} = [k + (n-1)]\, t_p$

$= [6 + (200-1)] \times 6$

$= 205 \times 6$

$= 1230 nsec$

Design D_2

$k = 8, \; t_p = 3nsec, \; n = 200$

$ET_{D_2} = [k + (n-1)] * t_p$

$= [8 + (200-1)] \times 3$

$= 207 \times 3$

$= 621 ns$

1230

621

609 Ans

[NAT] H.W

Q) Consider a 5-stage pipeline processor. The number of cycles needed by four instructions I_1, I_2, I_3, I_4 in stage S_1, S_2, S_3, S_4 and S_5 is shown below:

	S_1	S_2	S_3	S_4	S_5
I_1	2	2	1	2	3
I_2	1	1	2	1	2
I_3	1	3	1	1	1
I_4	1	1	1	1	1

What is the number of cycles needed to execute instruction i=1 completely for first iteration, for the below loop?

```
for(i = 1 to 2)
        {
                I1;
                I2;
                I3;
                I4;
        };
```

[NAT]

Consider a hypothetical 6 stage pipeline processor. Let P is the probability of an instruction being a branch. What must be value of p such that speed up factor is at least 5. Also assume each stage takes 1 cycle to perform its task and branch predicted on fifth stage of the pipeline is 0.05 (upto 2 decimal places)

Ans (0.05)

$B_p = 5 - 1 = 4$ $\quad B.P = P$

$$S = \frac{\text{PIPELINE Depth (\#Stages)}}{(1 + \text{\#Stalls/Instn})}$$

$$\frac{\text{\#stages}}{[1 + (B.I.F \times B.P)]}$$

$$= \frac{6}{1 + P \times 4} \geq 5$$

$$\Rightarrow \frac{6}{1+4P} \geq 5$$

$$\Rightarrow 6 \geq 5 + 20P$$

$$1 \geq 20P$$

$$P \leq 1/20 = 0.05 \text{ Ans}$$

2 mins Summary

Topic Pipeline

Topic Pipeline Hazards

THANK - YOU