CS & IT ENGINEERING

Computer Organization & Architecture

1500 Series

Lecture No.- 03

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Recap of Previous Lecture

Topic Clock Cycle Concept.

Topic Machine Instruction

Topic Expand Opcode Techniue

Topic Addressing Modes

Topics to be Covered

- Topic: Expand Opcode Techniue
- Topic: ALU Data Path
- Topic: Micro Operation & Micro Program
- Topic: Control Unit

[MCQ]

#Q. Consider the following assembly level program for a hypothetical processor.
R_1, R_2 and R_3
are 32-bit registers.

```
MOV R1, #0        ; R1 = 0
MOV R2, #1        ; R2 = 1
CMP R3, #0        ; Compare R3 with 0
BEQ DONE          ; Branch to DONE if zero flag is set
X:
ADD R2, R1, R2    ; R2 ← R1 + R2
SUB R1, R2, R1    ; R1 ← R2 – R1
SUB R3, R3, #1    ; R3 ← R3 – 1
BNE X             ; Jump to X if zero flag is not set.
DONE:
```

If the initial value of R_3 is 10, what will be the value of R_2 (in decimal)?

A 55

B 89

C 144

D None of these

Ans (B)

I_1: ADD $R_2 \leftarrow R_1 + R_2$

I_2: $R_1 \leftarrow R_2 - R_1$

I_3: SUB $R_3 \leftarrow R_3 - 1$

$R_1 = 0$

$R_2 = 1$

$R_3 = 10$

I_1: $R_2 = 0+1 = R_2 = 1$

I_2: $R_1 = 1-0 = R_1 = 1$

I_3: $R_3 = 10-1 = R_3 = 9$

I_1: $R_2 = 1+1 = R_2 = 2$

I_2: $R_1 = 2-1 = 1$

$R_3 = 9-1 = 8$

I_1: $R_2 = 1+2 = 3$

I_2: $R_1 = 3-1 = 2$

$R_3 = 8-1 = 7$

I_1: $R_2 = 2+3 = 5$

I_2: $5-2 = 3$

$R_3 = 7-1 = 6$

I_1: $3+5 = R_2 = 8$

I_2: $8-3 = 5$

I_3: $R_3 = 6-1 = 5$

R_2

1, 2, 3, 5, 8, 13, 21, 34, 55, 89

[MCQ]

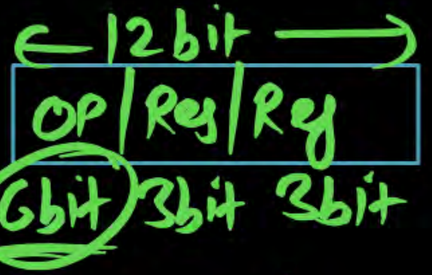
Consider a design will expand opcode technique with 12bit instructions, where a register operand requires 3 bits. There are 24 – 2 address instruction consisting of two register operands, and 5-one address instructions consisting of one memory operand of 8 bits. Then find the number of 0-address instruction in the system possible.

(a) 512

(b) 1024

(c) 2048

(d) ~~Not possible with the given instruction size.~~ None of these.



Derived

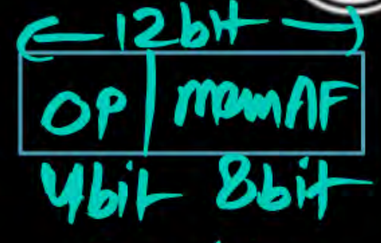
Total operation $= 11 \times 2^{6-4}$

$= 11 \times 4$

$\Rightarrow 44$

Given $= 24$

Free $= 24 - 24 = 20$

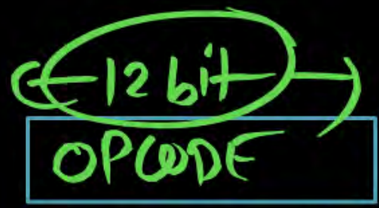


Primitive

Total # operation $= 2^4 = 16$

Given $= 5$

Free $= 16 - 5 = 11$



$20 \times 2^{12-6} \Rightarrow 20 \times 2^6$

$\Rightarrow 20 \times 64 = 1280$ Ans

[MCQ]

#Q. in $X = \frac{(M+N\times O)}{(P\times Q)}$, how many one-address instruction are required to evaluate it?

A 4

B 6

C 8

D 10

Ans (C)

I_1 : LOAD P : $AC \leftarrow M[P]$

I_2 MUL Q : $AC \leftarrow AC * Q$

I_3 STORE T; $M[T] \leftarrow AC$

I_4 LOAD N $AC \leftarrow M[N]$

I_5 MUL O $AC \leftarrow N * O$

I_6 ADD M $AC \leftarrow M + (N*O)$

I_7 DIV T $AC \leftarrow AC / M[T]$

I_8 STORE X $M[X] = \frac{M+N\times O}{P\times Q}$

8 Instn.

[MCQ]

#Q. A computer supports 32-bit wide instructions and 8-bit wide addresses. If it supports x 3 –address instructions, y 2-address instructions, how many 1-address instructions can be supported? x, $y \neq 0$

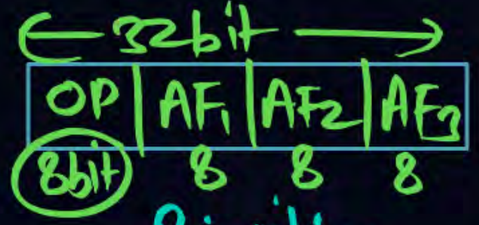
A 2^{24}

B $((2^{16}-x) - y) * 2^8$

C $((2^8 - x)-y) * 2^8$

D $((2^{16} - x.2^8) - y) * 2^8)$

Ans (D)

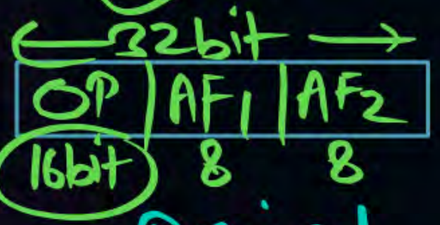


Primitive

Total operation = 2^8

Given = x

Free = $(2^8 - x)$



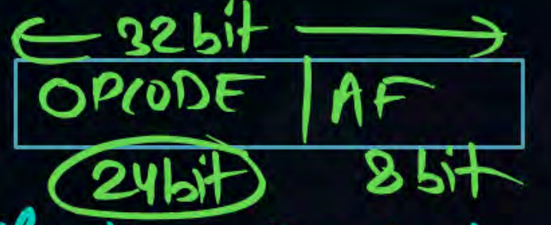
Derived

Total operation = $(2^8 - x) \times 2^{(16-8)}$

Given = y

$(2^{16} - x \cdot 2^8)$

Free = $(2^{16} - x \cdot 2^8) - y$



further Devied.

Total = $\left[(2^{16} - x.2^8) - y\right] \times 2^{(24-16)}$ Ans

[MCQ]

T.I

#Q. Consider a hypothetical control unit which supports:

4 control signals $\{S_0, S_1, S_2, S_3\}$

3 instruction $\{I_1, I_2, I_3\}$

Each instruction takes 4 μ-instructor $\{T_1, T_2, T_3, T_4\}$ to complete the execution.

The following table shows the control signals request for each μ-operator for each instructor the control operator for S_0 and S_3?

μ – Op ↓ inst →	I_1	I_2	I_3
T_1	S_0, S_2	S_1, S_3, S_2	S_0, S_3, S_1
T_2	S_0, S_3, S_2	S_1, S_0, S_3	S_0, S_2, S_1
T_3	S_1, S_0, S_2	S_1, S_2, S_3	S_1, S_2
T_4	S_1, S_2, S_3	S_0, S_3	S_1, S_2

$S_0 = T_1(I_1+I_2) + T_2(I_1+I_2+I_3) + T_3 I_1 + T_4 I_2$

$S_0 = T_1(I_1+I_2) + T_2 + T_3 I_1 + T_4 I_2$ Ans

$S_3 = T_1(I_2+I_3) + T_2(I_1+I_2) + T_3 I_2 + T_4(I_1+I_2)$

Continues ...

A

$S_0 = T_1 (I_1 + I_3) + T_2 + T_3 I_1 + T_4 I_2$

$S_3 = T_1 (I_2 + I_3) + T_2 (I_1 + I_2) + T_3 I_2$
$T_4 (I_1 + I_2)$

Ans (a)

B

$S_0 = T_1 (I_1 + I_3) + T_2 (I_1 + I_3) + T_3 I_1 + T_4 I_2$

$S_3 = T_1 (I_2 + I_3) + T_2 (I_1 + I_2) + T_3 I_2 + T_4 (I_1 + I_2)$

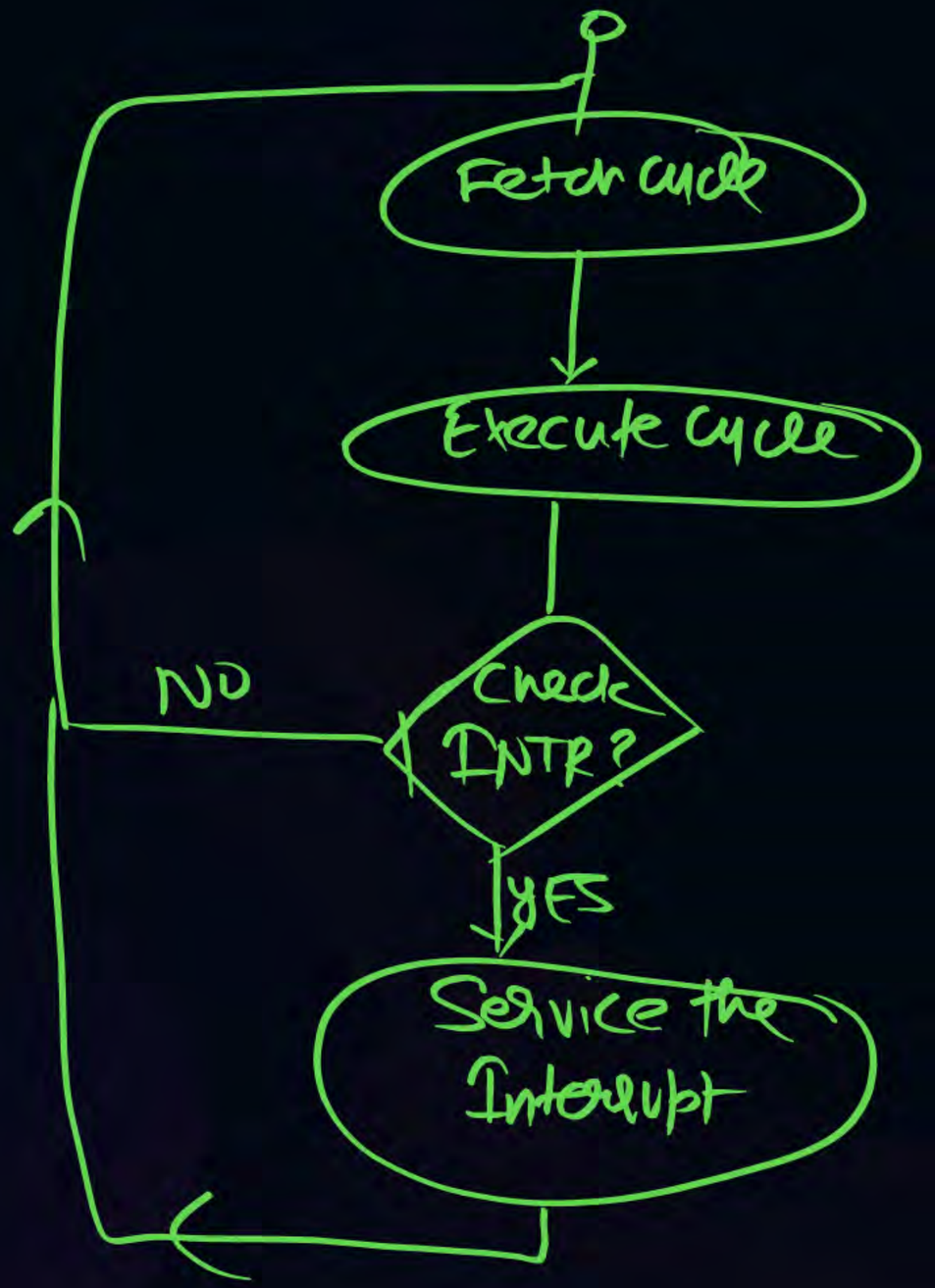
C

$S_0 = T_1 (I_1 + I_3) + T_2 + T_3 I_1 + T_4 I_2$

$S_3 = T_1 (I_1 + I_3) + T_2 (I_1 + I_2) + T_3 I_3 + T_4 (I_1 + I_2)$

D

None


Fetch cycle
Execute cycle
Check INTR?
NO
YES
Service the Interrupt

[MCQ]

Consider the following micro-operations about instruction fetch (IF):
(i) The content of the MDR are loaded into the IR.
(ii) The result of a memory read operation, the instruction is loaded in to the MDR.
(iii) The content of the program counter is loaded into the MAR.
Which of the following is correct sequence of instructions fetch in micro program?

(iii) PC → MAR
(ii) Mem → MBR/MDR
(i) MBR → IR.

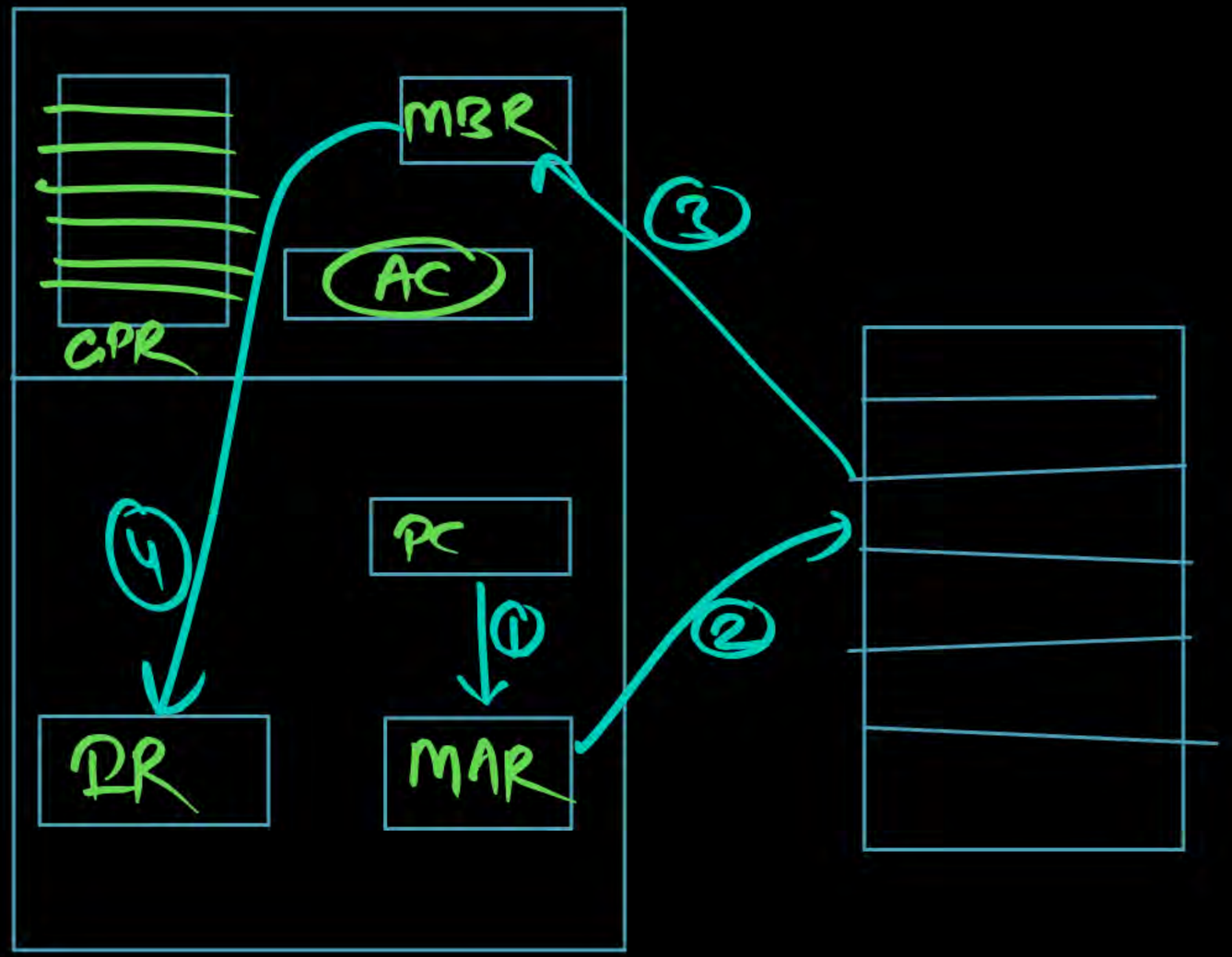
A (iii), (ii), (i)

B (i), (iii), (ii)

C (i), (ii), (iii)

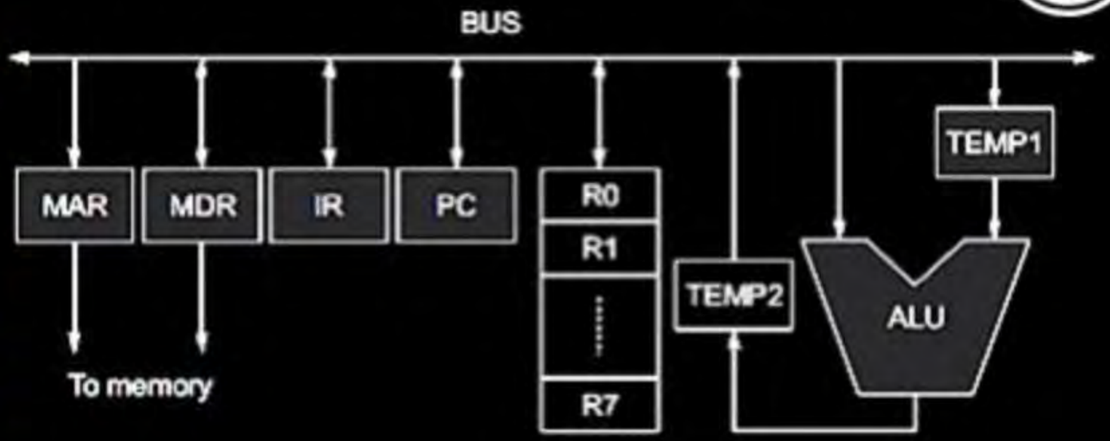
D (ii), (iii), (i)

Ans (A)


MBR
AC
GPR
PC
IR
MAR
1
2
3
4

MCQ

Consider the following data path diagram



Consider an instruction: R0←R1+R2. The following steps are used to execute it over the given data path. Assume that PC is incremented appropriately. The subscripts r and w indicate read and write operations, respectively.

1. $R2_r$ $TEMP1_R$, ALU_{add}, $TEMP2_W$
2. $R1_r$ $TEMP1_W$,
3. PC_r, MAR_W, MEM_r
4. $TEMP2_R$,RO_W
5. MDR_r, IR_W

Which one of the following is the correct order of execution of the above steps?

A. 3, 5, 1, 2, 4

B. 2, 1, 4, 5, 3

C. 3, 5, 2, 1, 4

D. 1, 2, 4, 3, 5

[MSQ]

Which of the following is/are INCORRECT about micro instruction?

A. Individual bits in horizontal micro instructions correspond to individual control lines. → CORRECT

B. Vertical micro instructions are much shorter than horizontal ones. Correct

C. Vertical micro instructions are allowed maximum parallelism. low Degree of parallelism

D. Decoding is necessary in both micro instructions, horizontal as well as vertical. No

Ans (C) & (D)

NAT

Consider a CPU where all the instructions require 9 clock cycles to complete execution. There are 200 instructions in the instruction set. It is found that 130 control signals are needed to be generated by the control unit. While designing the horizontal micro-programmed control unit, single address field format is used for branch control logic. What is the minimum size of the control word and control address register?

Total #Instn = 200

#cycle/Instn = 9

Total #uopern = 200 × 9 = 1800 uopn/CW

Control Memory = 1800 CW

CAR | AF = 11 bit

Horizontal

C.S = 130 ⇒ CF = 130 bit

CF	AF
130	11

141, 11 Ans

MCQ

Consider the following sequence of micro -operations.

MBR ← PC

MAR ← X (SP/TOS)

PC ← Y (ISR)

Memory (TOS(SP)) ← MBR

Which one of the following is a possible operation performed by this sequence

A Instruction fetch

B operand fetch

C Conditional branch

D Initiation of interrupt service

Ans (D)

(a) Instr Fetch

PC → MAR → Mem → MBR → IR

(b) Operand Fetch

IR(AF) → MAR → MEM → MBR → AC/ALU.

[NAT]

Consider a CPU where all instruction takes 11 cycles to complete execution. There are total 290 instructions in a instruction set. In this 3190 control signals are needed to be generated by control unit while single address field format is used for designing the vertical micro-programmed control unit. Then the size of control memory (in byte)is 9570 Ans

Total μ operation = 290 × 11 = 3190 μOperⁿ/CW

Control Memory = 3190 CW ⇒ 2^{12}

AF/CAR/NIA = 12 bit

Vertical

C.S = 3190 ⇒ CF = 12 bit

12	12
CF	AF

⇒ 1CW = 24 bit

CM = 3190 CW

⇒ 3190 × 24 bit

⇒ 3190 × 3 Byte

= 9570 Ans

24/8 = 3 Byte

[MCQ]

Consider the following microprogram to fetch the data from the memory to CPU register (r_1) using the indirect addressing mode:

T_1: P → MAR

T_2: Memory → MBR

T_3: MBR → Q

T_4: Memory → MBR

T_5: Memory → R

What are the registers used in the place of P, Q and R variables respectively?

A r_1, PC, MAR

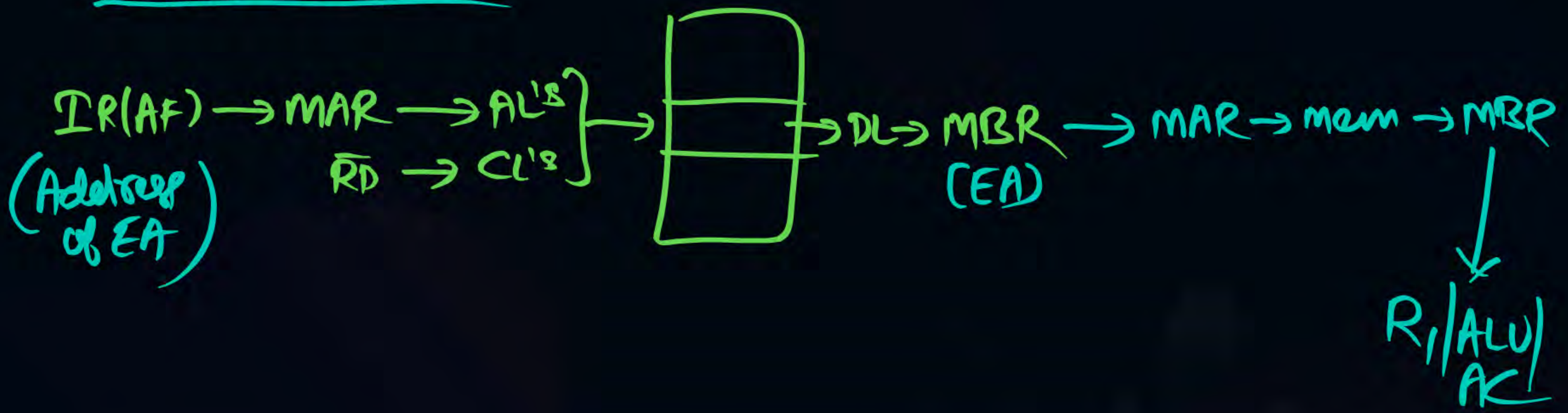
B IR, MAR, r_1

C r_1, MAR, IR

D None of these

Ans (B)

Indirect AM

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[MSQ]

Which of the following characteristics are correct about the design of RISC processor?

A. It support more number of registers

B. It support less number of addressing modes

C. It uses micro programmed control unit

D. It support smaller instruction set

RISC ⇒ Hardwired CU.

Ans (A)(B) & (D)

[MSQ]

#Q. Consider a hypothetical control unit that support 9 groups of mutually exclusive control signals. Also assume that group-1, group-2, group-3 and group-4 are using horizontal micro-programming where as group-5, group-6, group-7, group-8, and group-9 are using vertical microprogramming. Identify which of the following is/are in correct?

Groups	G_1	G_2	G_3	G_4	G_5	G_6	G_7	G_8	G_9
Control Signal	8	9	10	11	19	31	40	51	74

A. Total bits for groups (G_5 G_6 G_7 G_8 G_9) is 29 bits and Total bits for control word is 42.

B. Total bits for Group (G_1 G_2 G_3 G_4) is 38 bits and total bits for control word is 43.

C. Total bits for control word is 67 bits. → correct

D. Total bits for control word is 46 bits

Ans (A) (B) & (D)

Horizontal

G_1	G_2	G_3	G_4
8	9	10	11

bit = 8 + 9 + 10 + 11

⇒ 38 bit

Vertical

G_5	G_6	G_7	G_8	G_9
19	31	40	51	74
⇓	⇓	⇓	⇓	⇓
5	5	6	6	7

$\left(\log_2 \frac{19}{27} \approx 0\right)$

bits = 5 + 5 + 6 + 6 + 7 = 29 bit

CW = 38 + 29

= 67 bits

2 mins Summary

- Topic: Expand Opcode Techniue
- Topic: ALU Data Path
- Topic: Micro Operation & Micro Program
- Topic: Control Unit

THANK - YOU