Memory management techniques

Part 01

Lecture no -03

1-memory management techniques

PAGING ;

L.A.S = 8KB ; P.A.S = 4KB ; P.S = 1KB ;

VAS

d = 10 bits

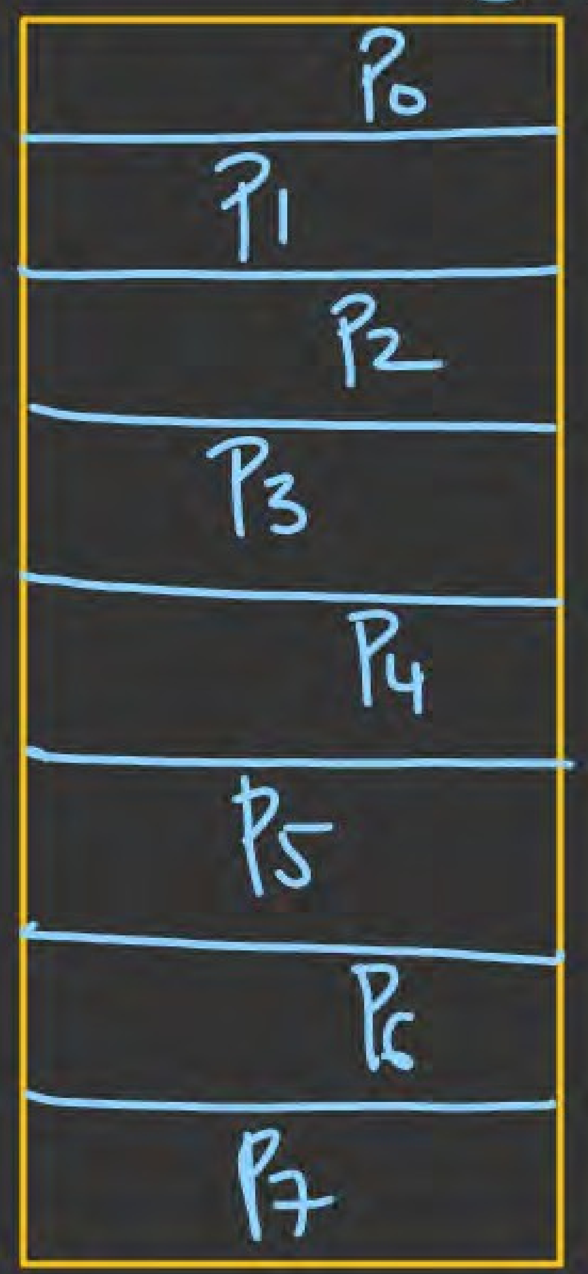
P.S = F.S

L.A = 13 bit ; P.A = 12 bit

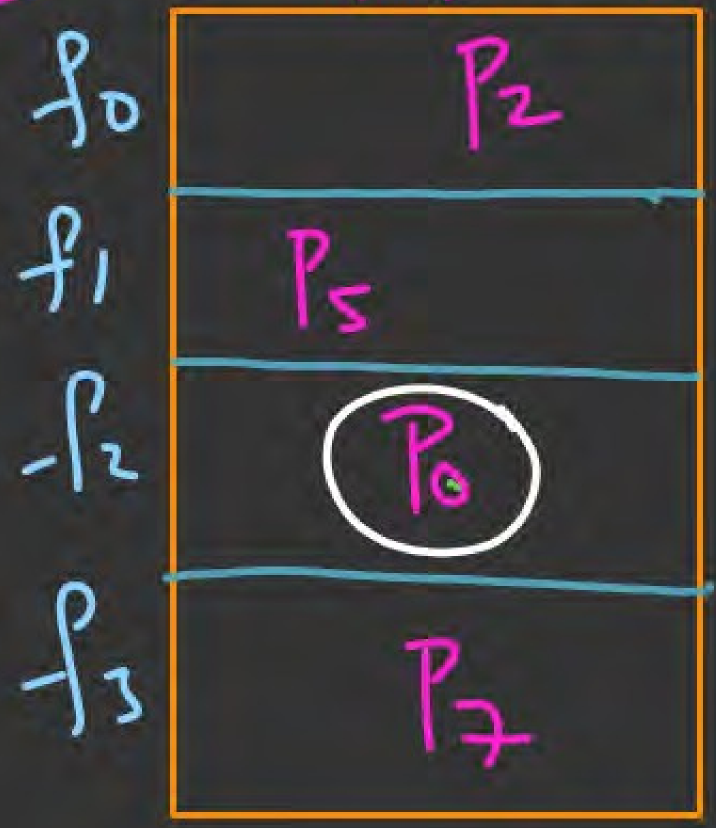
f = 2 bits

P = 3 bits

① 8KB



② P.A.S : 4KB



③ organization of M.M.U

→ Page Table (PT)

(Page Map Table)

(Address Translation Table)

3) Orgn. of M.M.U (P.T)

- → Each Process has its own P.T
- → P.Ts of Processes are Stored in Memory;
- → P.T is organized as a series of entries (P.T entries / PTE)

* Such that No. of Entries = No. of Pages in Address Space.

- → No. of entries in P.T = P.T. Size
- → P.T. Entry contains the frame No in which the referred Page is present;
- → P.T. Entry Size = 'e' ≥ 1 Bytes;
- → $\boxed{\text{P.T-Size in Bytes} = N_{pages} * e}$

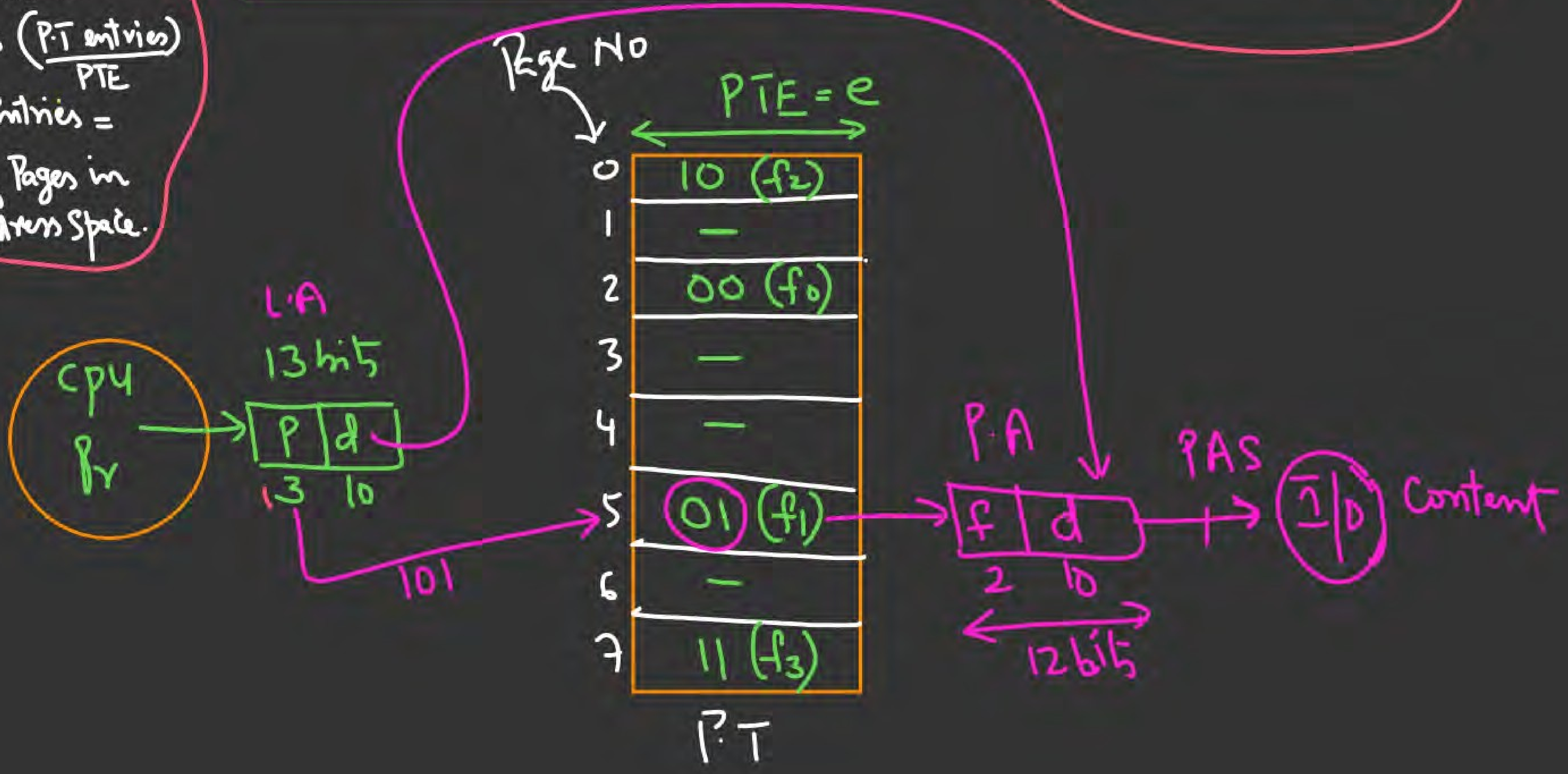
L.A.S = 8KB

LA = 13 bits

PAS = 4KB

PA = 12 bits

Simple Paging



Q) Consider a System with a V.A = 25 bits

P.A = 20 bits ; d = 12 bits; P.S = 2^{12} = 4KB

$N = 2^{25}/2^{12} = 2^{13} = \underline{\underline{8K}}$

$M = 2^{20}/2^{12} = 2^{8} = \underline{256}$ ✓

$LAS = 2^{25} = 32MB$

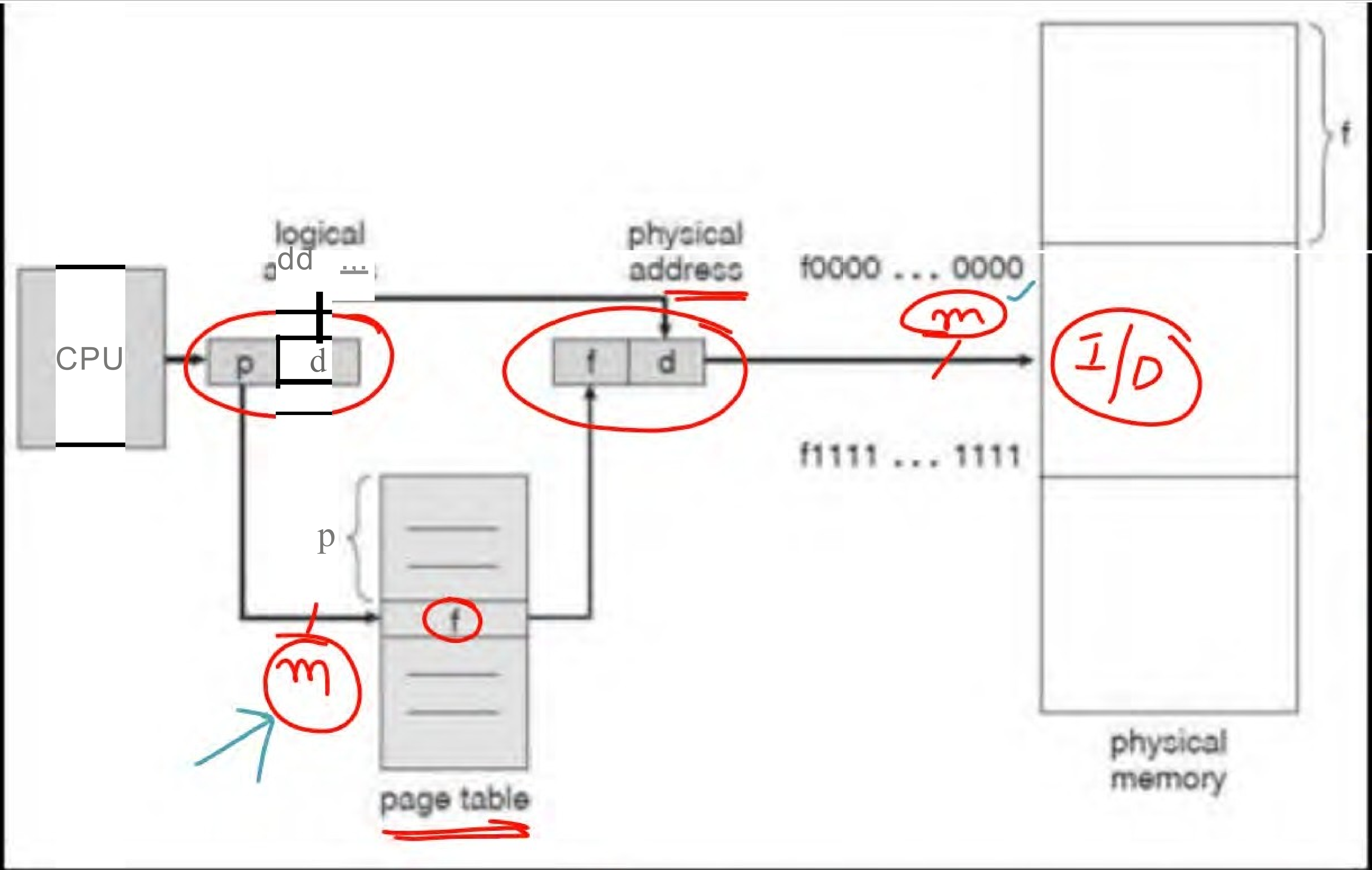
$PAS = 2^{20} = 1MB$

$P = 13$ bits

$f = 8$ bits

$\underline{\underline{e}}$ = PTE = f = 8 bits = 1B

PT Size = N * e = 8K * 1B = $\underline{\underline{8KB}}$ ✓



→ Main Memory

Access Time = 'm' units

→ Paged Memory access

(Effective Memory Access Time = '2 m'

EMAT Paging)

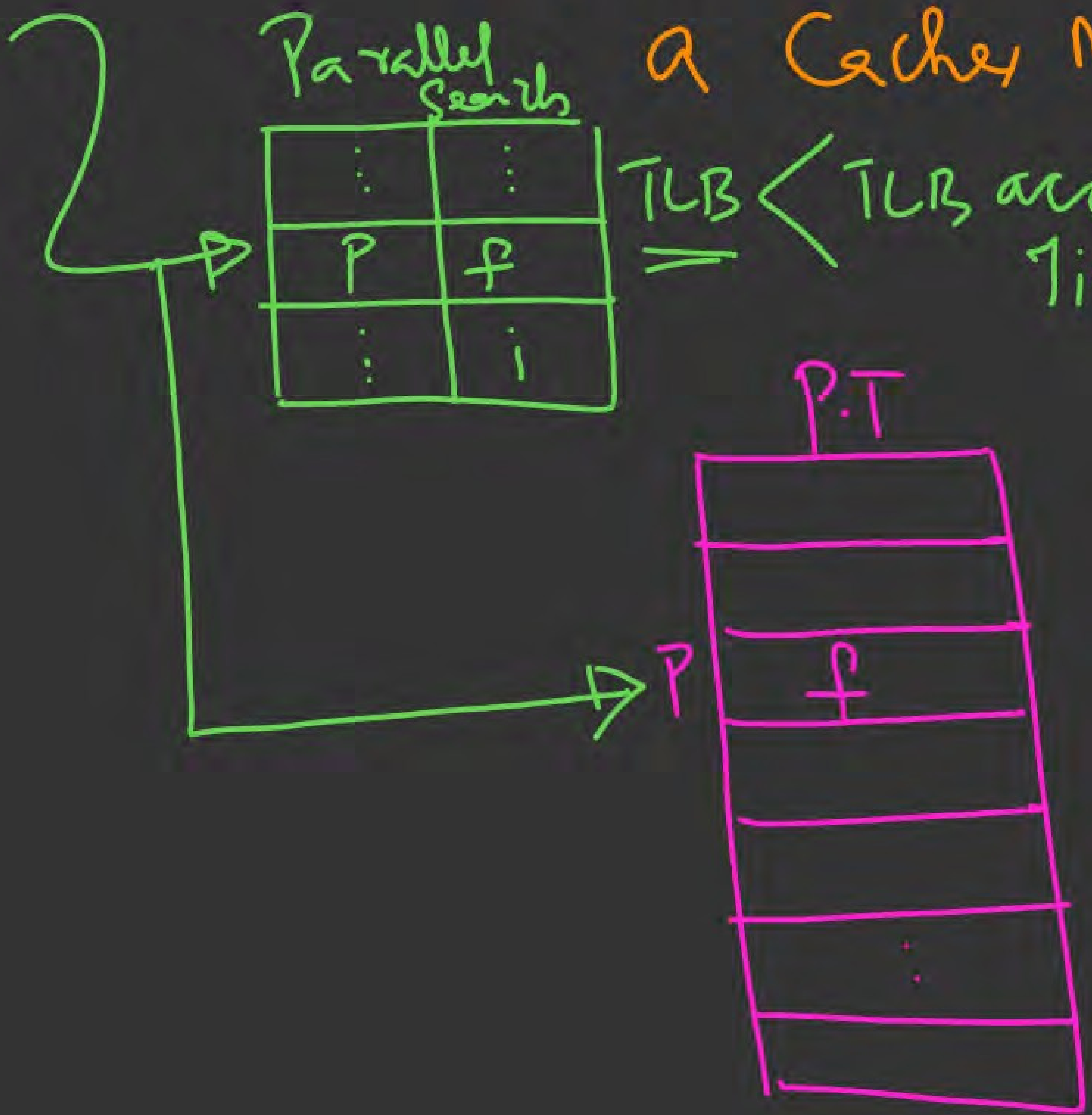
(m+m)

Address Transl. (PT)

Content Access

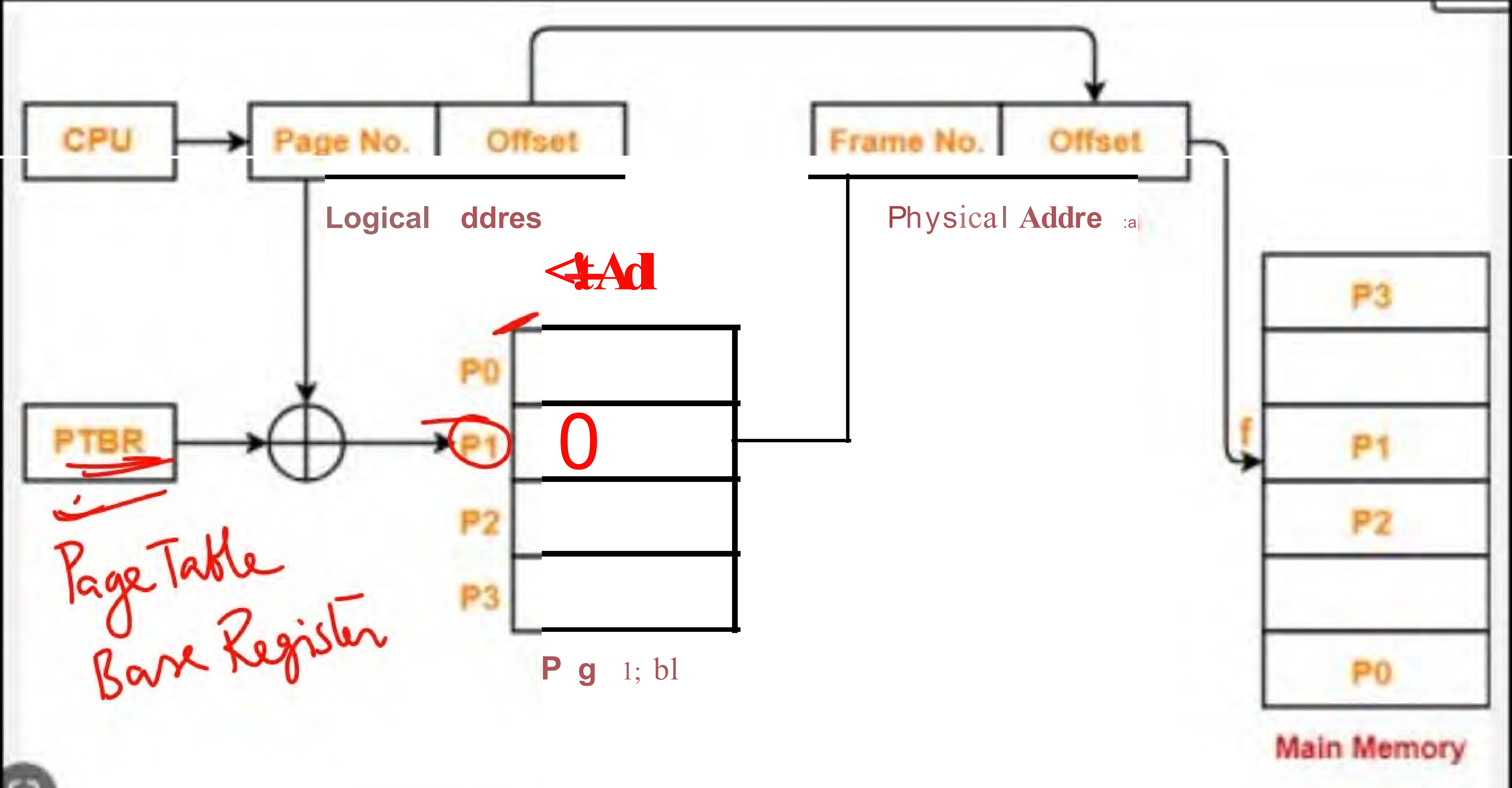
Paged Memory access is increasing Prog. execution Time objective is to Reduce EMAT from '2m' & bring it closer to 'm'

→ we can reduce the P.T Acc time by using a Cache Memory (T.L.B) → Translation look Aside Buffer.



TLB < TLB access time = 'c' >

"$c << m$"



Translating Logical Address into Physical Address

Performance of Paging

(i) Timing Issue / Temporal:

→ TLB Acc. Time = 'c'

→ MMAT = 'm'

→ $\boxed{EMAT_{TLB} = x(c+m) + (1-x)(c+2m)}$

→ TLB Hit ratio = 'x' $\langle 0 \le x \le 1 \rangle$ $= \frac{\text{No. of hits}}{\text{Total Refs}}$

→ Miss ratio = $1-x$

$m = 100\,ns$

$c = 20\,ns$

① Paged Mem. Access = 200 ns (2m)

② EMAT if $x = 90\%$

$= 0.9(120\,ns) +$
$0.1(220\,ns)$

$= 9 \times 12 + 22 = 130\,ns$

③ if $x = 10\%$

$EMAT = 0.1(120) + 0.9(220)$

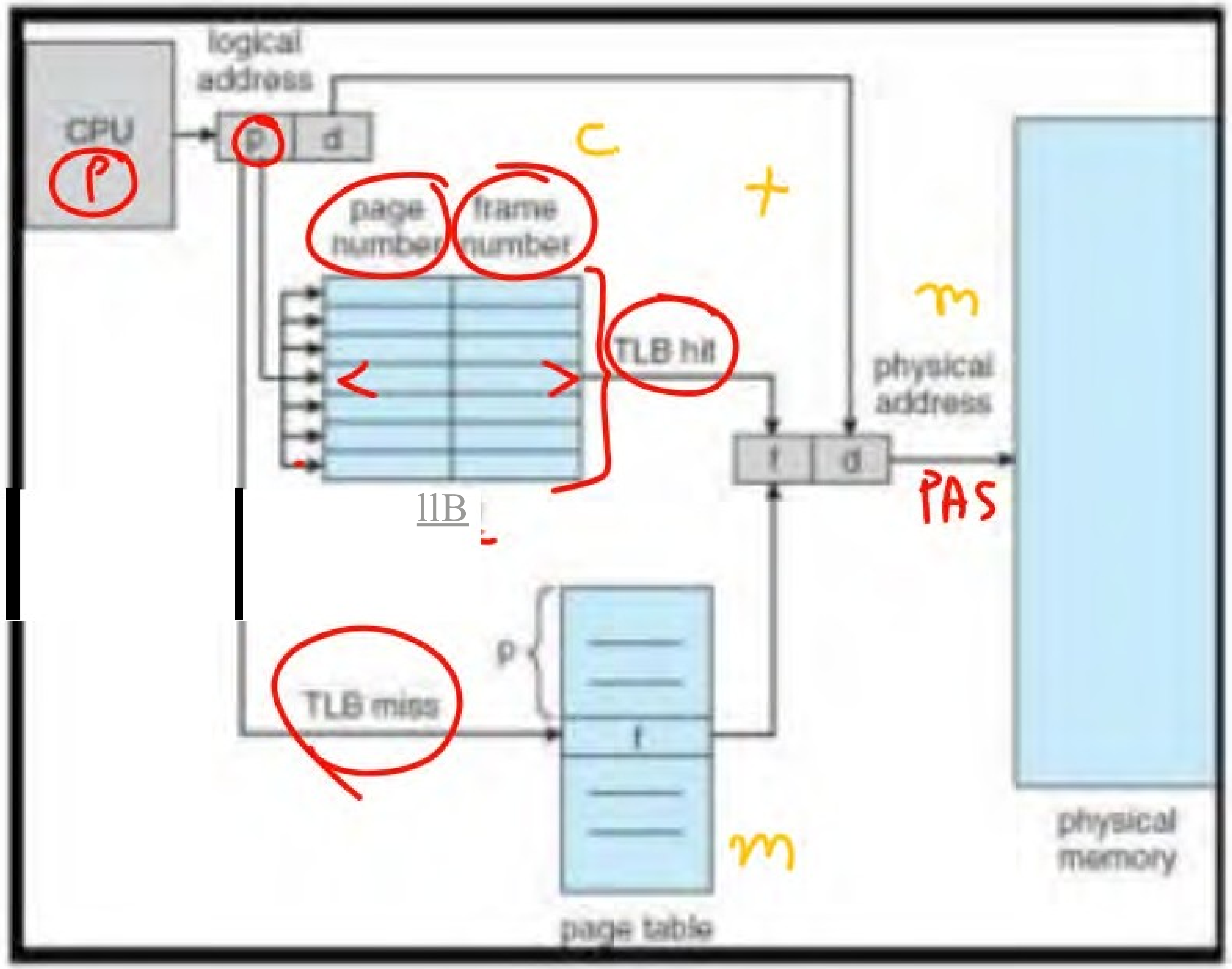
$= 12 + 9 \times 22 = 210\,ns$

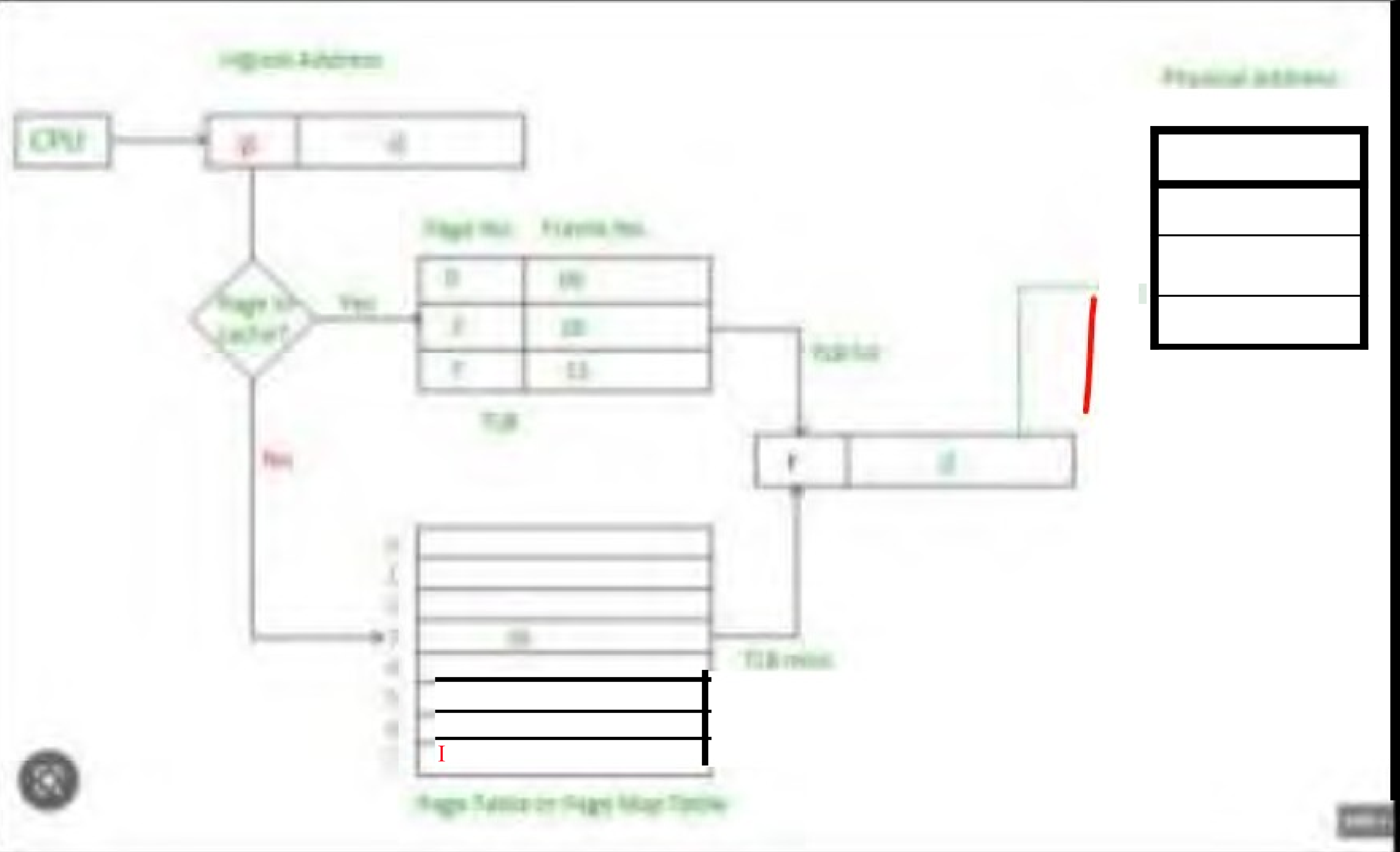
Conclusion:

The deployment of TLB in Paging is justified only if Hit ratio is high

Paging Hardware With TLB

Paging with TLB
<Reduce EMAT>





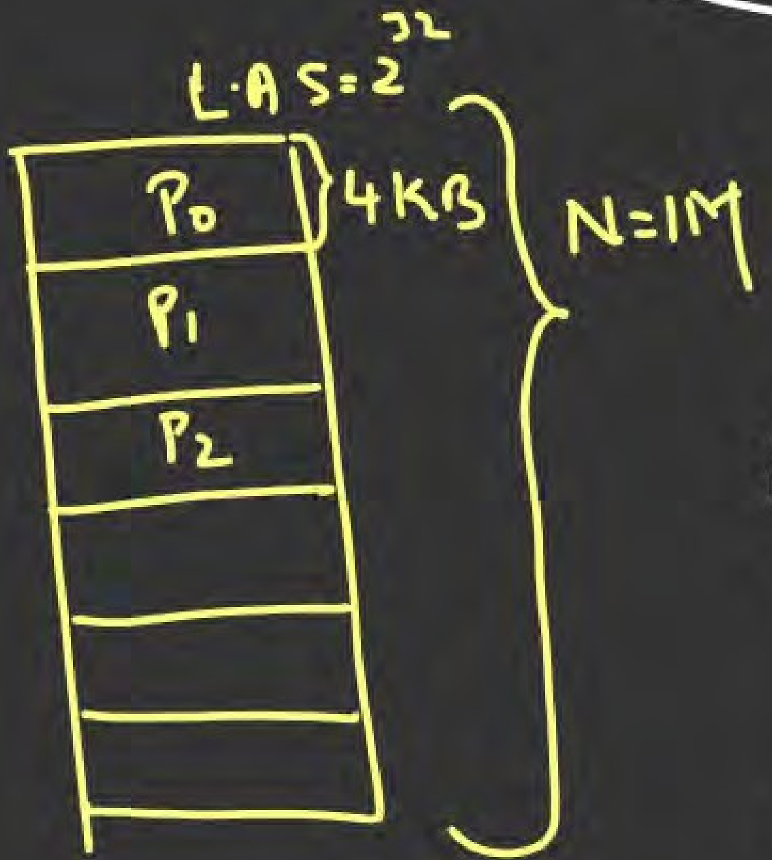
Performance of Paging w.r.to Space (Spatial Issue)

1) L.A = 32 bits ; P.S = 4KB ; $N = \frac{2^{32}}{2^{12}} = 2^{20} = 1M$

What is P.T. Size = $N * e$

$\boxed{P.T.S \propto N}$

P.T



P.T. Size = 1M entries

assume = e = 4B

∴ P.T.S = 1M × 4B
= 4MB ✓

Each Process will have its own P.T of 4MB

100 process

Total mem = 100 × 4MB = 400MB

objective :

Reduce P.T. Size of Process

Associate a Smaller P.T with the Process

How to Reduce P.T. Size?

$P.T.S \propto N \propto \frac{1}{PS}$

$N = \frac{LAS}{PS}$ ∴ $N \propto \frac{1}{PS}$

$PTS \propto \frac{1}{PS}$

(i) Reduce P.T.S by Increasing P.S

$P.T.S \propto N \propto \frac{1}{PS}$

$\therefore PTS \propto \frac{1}{PS}$

$LA = 32$ bits

$PS = 4KB$

$N = \frac{2^{32}}{2^{12}} = 2^{20} = 1M$

$PTS \propto N = 1M$

$LA = 32$ bits

$PS = 8KB$

$N = \frac{2^{32}}{2^{13}} = 2^{19}$

$= 512K$

$PTS \propto N = 512K$

Inc. P.S has a Sideffect of Producing More Internal Frag.

Prog-Size = 1026 By.

P.S

(Small) 2B

(i) $N = \frac{1026}{2}$

= 513 Pages

$PT = 513$ ✓

$I.F = 0$ By

513

(large) 1024B (1KB)

$N = \frac{1026}{1024} = (1 + 1)$

= 2 pages ✓

$PTS = 2$ ✓

2

$IF = 1022B$ ✓

P_1: 1024 B

P_2: 2B, IF

P.S $\propto$ Impact
① P.T.S $\propto N \propto \frac{1}{PS}$
② IF $\propto$ P.S

'IF' always occur in Last Page of the Process.

(What must Ideal P.S such that both P.T.S & I.Frag are kept Minimum)

Optimal Page Size?

Consider a System of LAS = 'S' Bytes
Page Size = 'P' Bytes = ?
PTE = 'e' Bytes

$$I.F = \frac{P}{2}$$

Assuming that 1/2 of last Page is I.F

$$P.T.S = N * e$$

$$= \left(\frac{S}{P} * e\right) \text{Bytes}$$

What must be optimal value of 'P' S.T (PTS + IF) is Kept Minimum?

$$\frac{d}{dp}\left(\frac{S}{P} \times e + \frac{P}{2}\right) \simeq 0$$

$$-\frac{Se}{P^2} + \frac{1}{2} = 0$$

$$P^2 = 2Se$$

$$\boxed{P = \sqrt{2 \cdot S \cdot e}}$$

② Paging with Hashing (Hashed Page Table)

$f(\text{Key}) = \text{index} \rightarrow$ H.T for getting the value;

$f = (\% 10) = 10$

Hashing : Collission

$f(x_1) = f(x_2) = i$

Collission

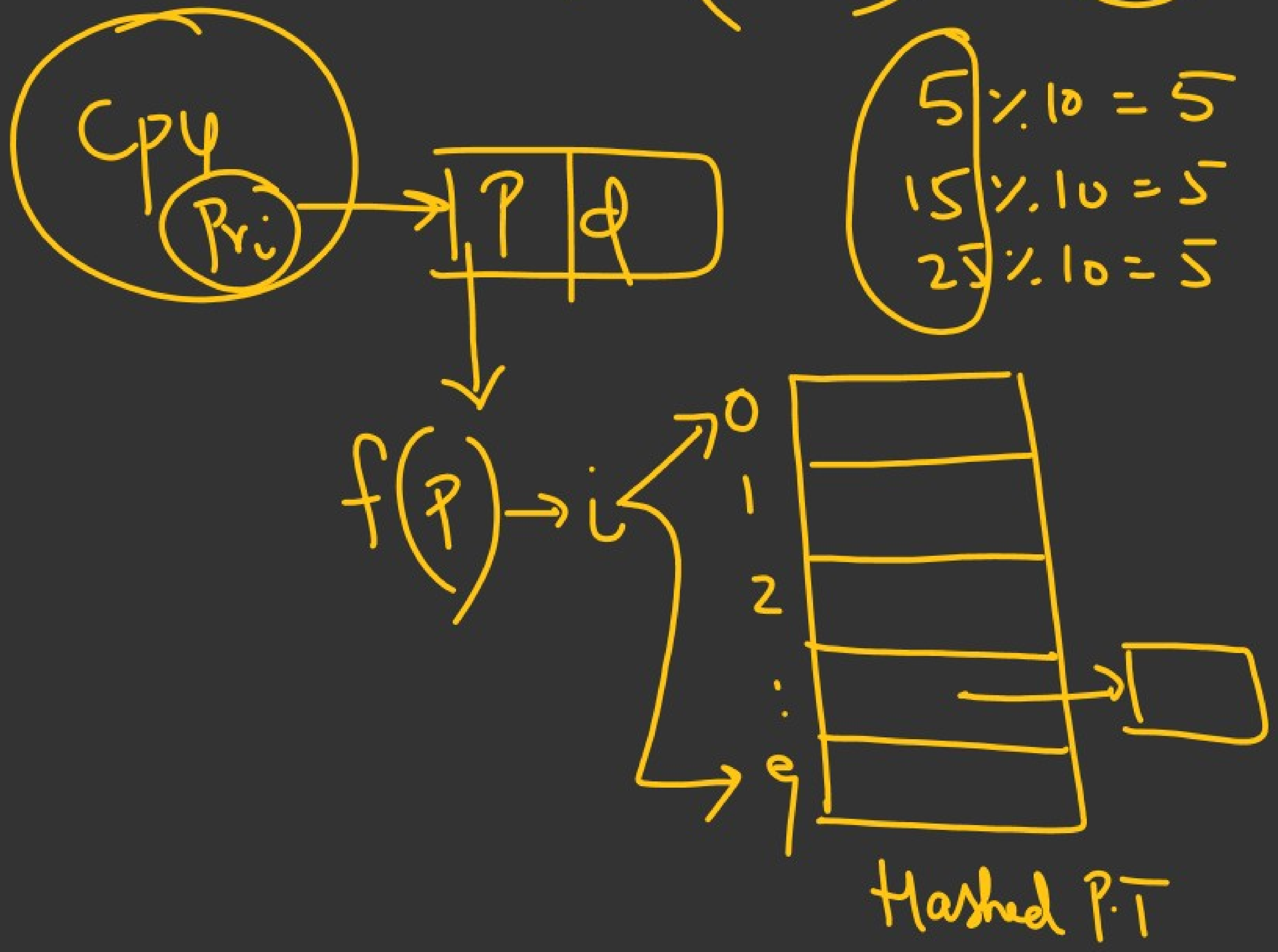
↓

Probing | Chaining ✓

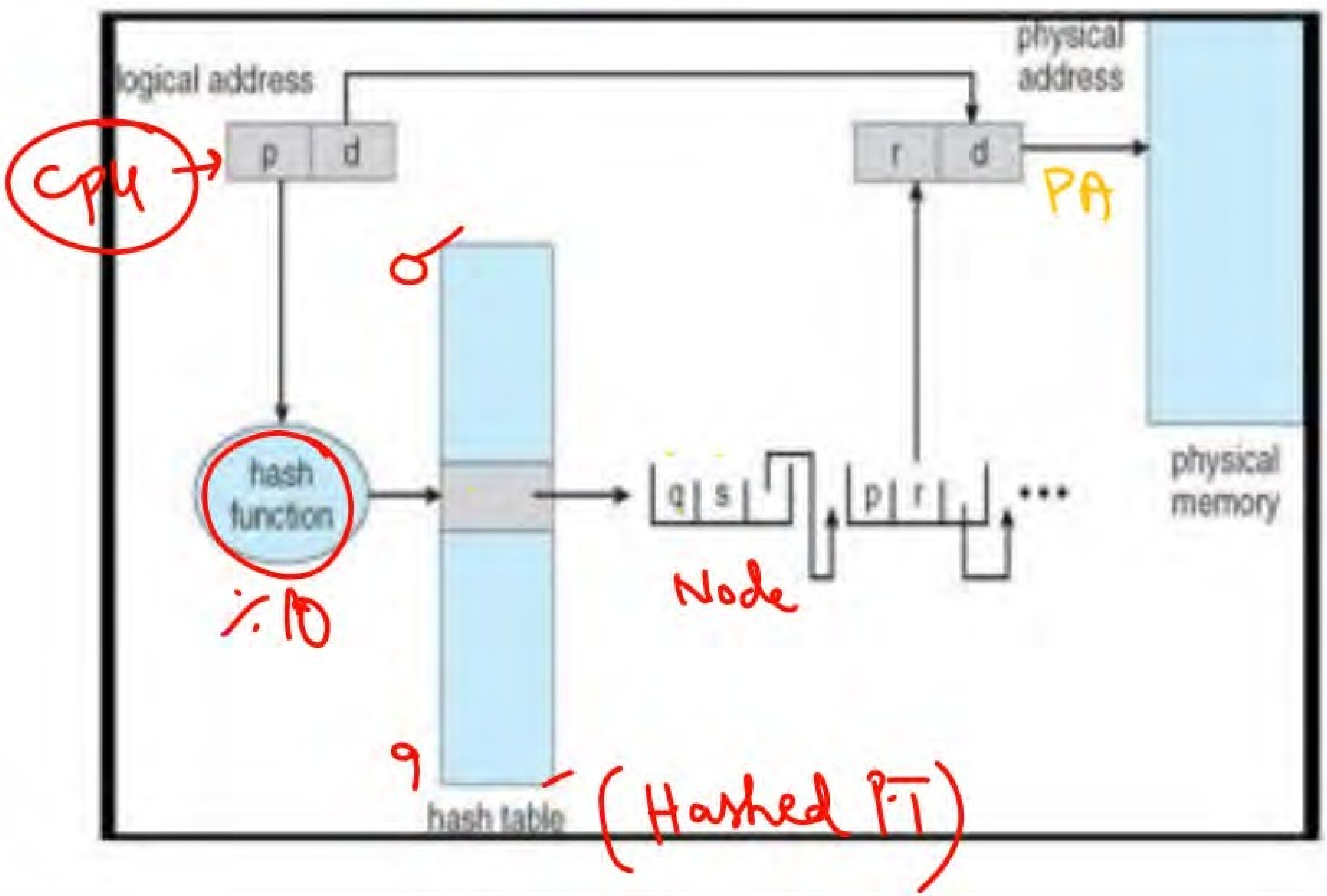
$5 \% 10 = 5$

$15 \% 10 = 5$

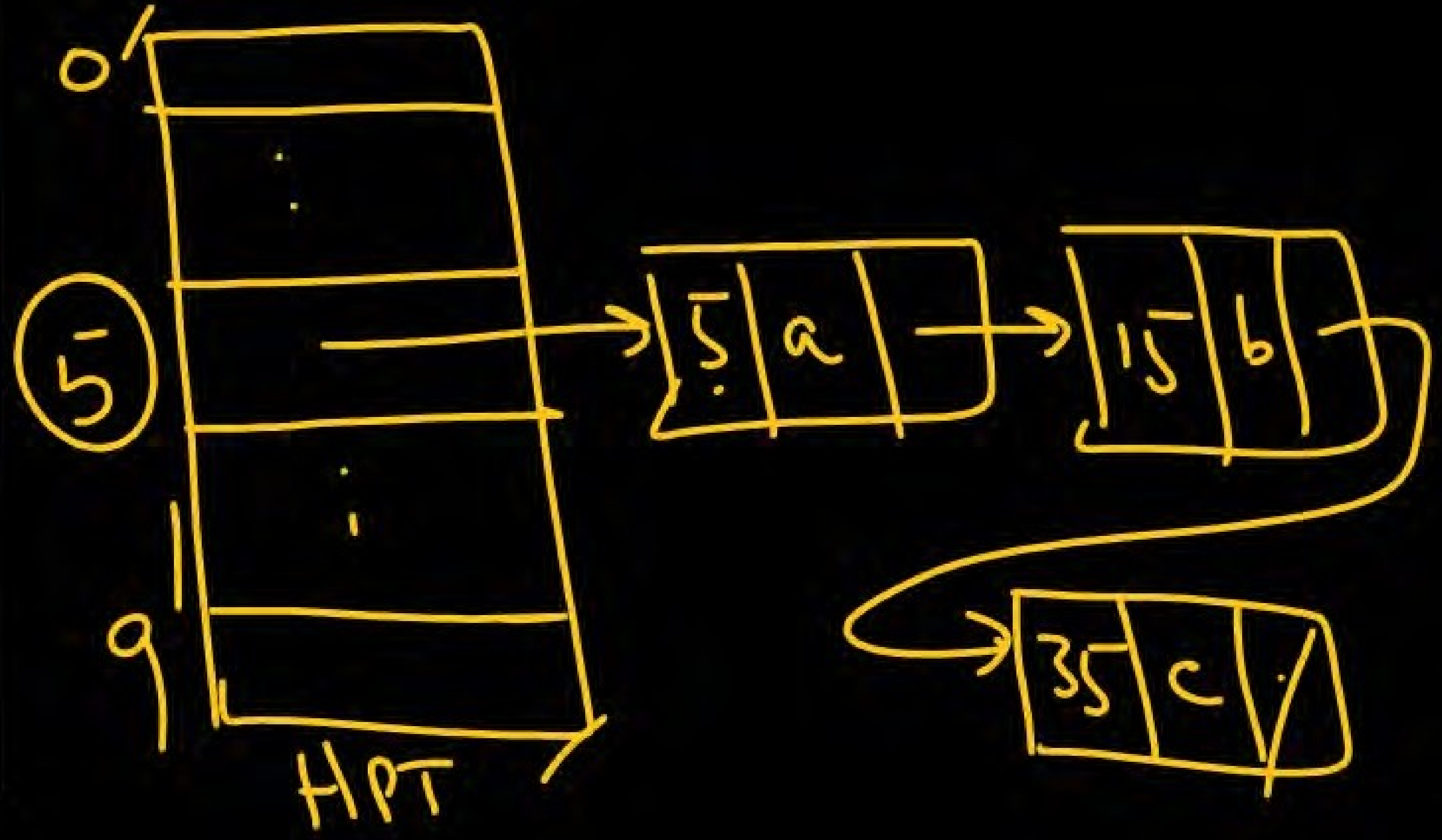
$25 \% 10 = 5$



Hashed Page Tables



Hashed P.Ts relatively has less No. of entries in comparison to original (Traditional) P.Ts



Q.1

A Computer System using **Paging Technique** implements an 8KB Page with a **Page Table of Size** 24MB. The Page Table Entry is 24 bits. What is the **length of Virtual Address** in this System?

$P.S = 8KB ; \Rightarrow d = 13$ bits

$PTS = 24 MB ;$

$PTE = 24$ bits $= 3$ By

$PTS = N * e$

$24 MB = N * 3 B$

$N = \frac{24 MB}{3 B} = \underline{\underline{8M}}$ pages

$P = 23$ bits

V.A:

P	d
23	13

$\longleftrightarrow$ 36 bits ✓

Q.2

A Computer System using Paging technique has a Virtual Address of length 'l'. The Number of Pages in the Address Space are 'Z'. There are 'H' Frames in PAS. Calculate the number of bits in Page Offset and the size of PAS

'l'

VA	P	d

$\log Z$

$N = 'Z'$

$P = \log_2 Z$

$\therefore d = l - \log_2 Z$

$M = H$

$f = \log_2 H$ bits

P.A	f	d

$(\log H + l - \log_2 Z)$

$P.A.S = 2^{\log H + l - \log Z}$

$= 2^{l + \log_2 \frac{H}{Z}}$

$= 2^l * 2^{\log \frac{H}{Z}} = \left(\frac{H}{Z}\right) \cdot 2^l$ Bytes

PAS

$PAS = 2^{P.A}$

$\log A - \log B = \log \frac{A}{B}$

$2^{a+b} = 2^a \cdot 2^b$

Q.3

Consider a System using **Simple Paging Technique** with Logical Address (LA) of 32 bits. Page Table Entry (PTE) of 32 bits. What must be the Page Size in bytes, such that the Page Table of the Process Exactly fits in one Frame of Memory (PAS)?

$L.A = 32$ bits

$PTE = 32$ bits $= 4B$

$P.S = ?$

$F.S = P.S = 2^x$

P.T.S exactly fits in one frame

Let $P.S = 2^x$ Bytes ? $\Rightarrow P.S = 2^{17} = 128KB$

$P.T.S = N * e$

$= \left(\frac{2^{32}}{2^x}\right) * 4B = 2^{34-x}$ Bytes

$\therefore \boxed{2^{34-x} = 2^x}$

$\therefore 34 - x = x$

$\therefore 2x = 34$

$x = 17$

Consider a System with a L.A of 32 bits; PAS = 64MB; Page Size = 4KB; Calculate the approximate P.T-Size in Bytes;

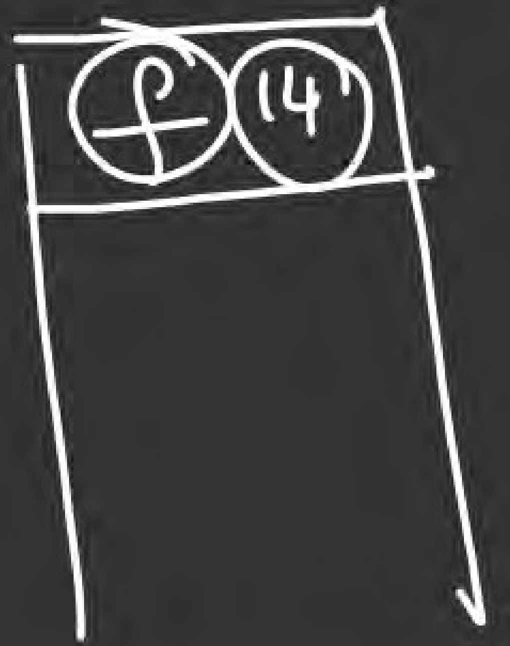
$$P.T.S = N * e$$
$$= 1M * 2B = 2MB$$

$$N = \frac{2^{32}}{2^{12}} = 2^{20} = 1M$$

$$e \sim f$$

$$M = \frac{2^{26}}{2^{12}} = 2^{14}$$

$$e \sim f = 14 \text{ bits} = 2B$$



Q.4 Consider a System using Paging with TLB. What Hit Ratio is required to reduce the EMAT from 'D' ns to 'Z' ns using TLB. Assume that TLB access time is 'K' ns.

$$EMAT_{TLB} = x(c+m) + (1-x)(c+2m)$$

$$EMAT_{TLB} = 'Z'$$

$$EMAT_{\text{without TLB}} = 'D' = 2m$$

$$\therefore m = \frac{D}{2}$$

hit ratio = 'x'

$$'Z' = x\left(K+\frac{D}{2}\right)+(1-x)(K+D)$$

$$x =$$

Q.6

Consider a System using Paging technique with an Address Space of 65,536 Bytes. The Page Size in this System is 4096 Bytes. The Program Consists of Text, Data and Stack Sections as per the specifications given below:

PG

$N_{pages} = \frac{65536}{4096} = 16$

2) $P.S = 4B$

$N_{pages} = \frac{65536}{4} = 16384$

(yes) ✓

Code		
8192	Text:	32,768 Bytes
4097	Data:	16,386 Bytes
3968	Stack:	15,870 Bytes

$= 16257$ ✓

$N_{Text} = \frac{32768}{4096} = 8$

$N_{Data} = \frac{16386}{4096} = 4.00048 = 5$

$N_{Stack} = \frac{15870}{4096} = 3.87 = 4$

A Page of the program contains portion of only one section i.e either Text or Data or Stack.

17 Pages

(a) Does the Program Fit in the given Address Space? NO

(b) What is the Maximum Page Size in Bytes such that the Program Fits in the Given Address Space?

Challenge H/W

" Smaller Pages utilize Mem effectively "

$\frac{5}{10}$ = remainder

M.L Paging

$$10 \overline{)\,5\,}\ \text{quotient } 0,\quad 5 - 0 = 5 \text{ remainder}$$

$$10 \overline{)\,15\,}\ \text{quotient } 1,\quad 15 - 10 = 5$$

11:45am

$5 \% 10 = 5$

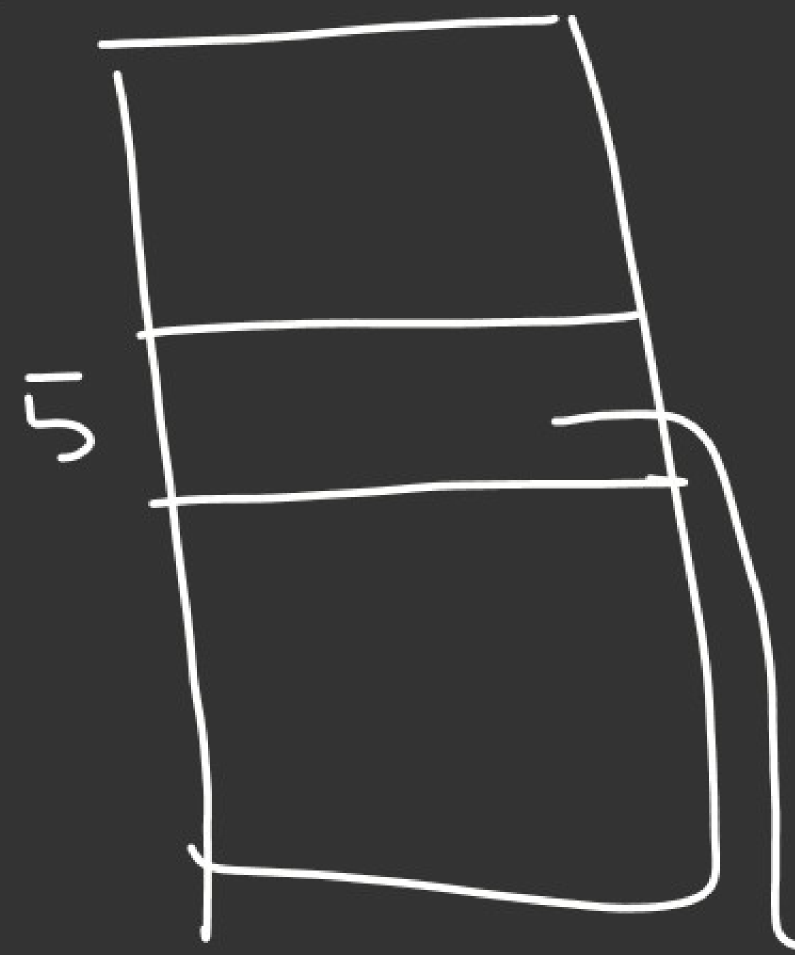
$15 \% 10 = 5$

$35 \% 10 = 5$

Collission

Pages

5



$$f(I_1) = f(I_2) = x$$

Collission

THANK YOU!