

CS & IT ENGINEERING

Operating System

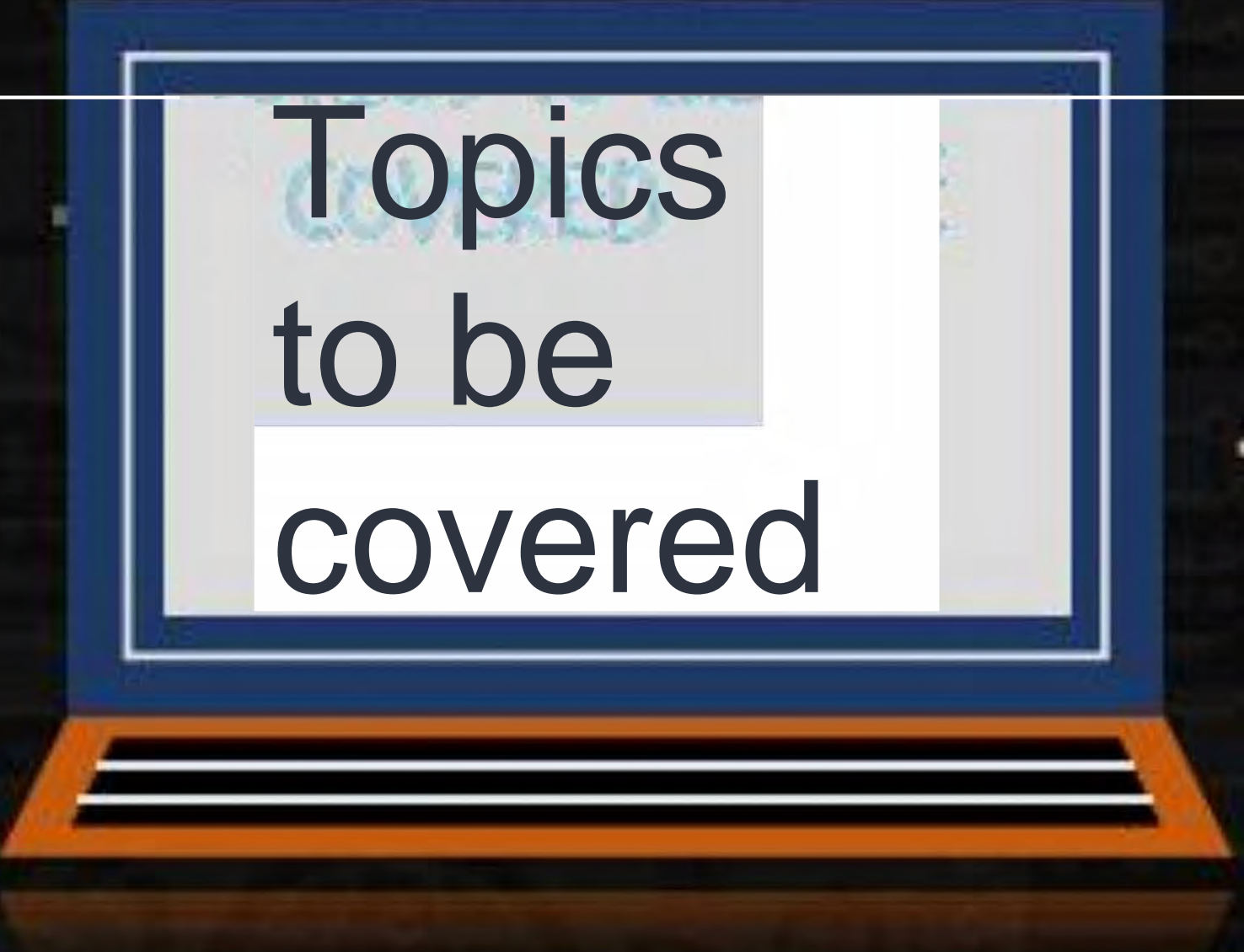


Inverted Paging, Monitors and Shared Pages

Lecture no:01



By- Dr. Khaleel Khan sir

A stylized illustration of a laptop with a blue frame and an orange base. The screen is white and displays the text 'Topics to be covered'.

Topics
to be
covered

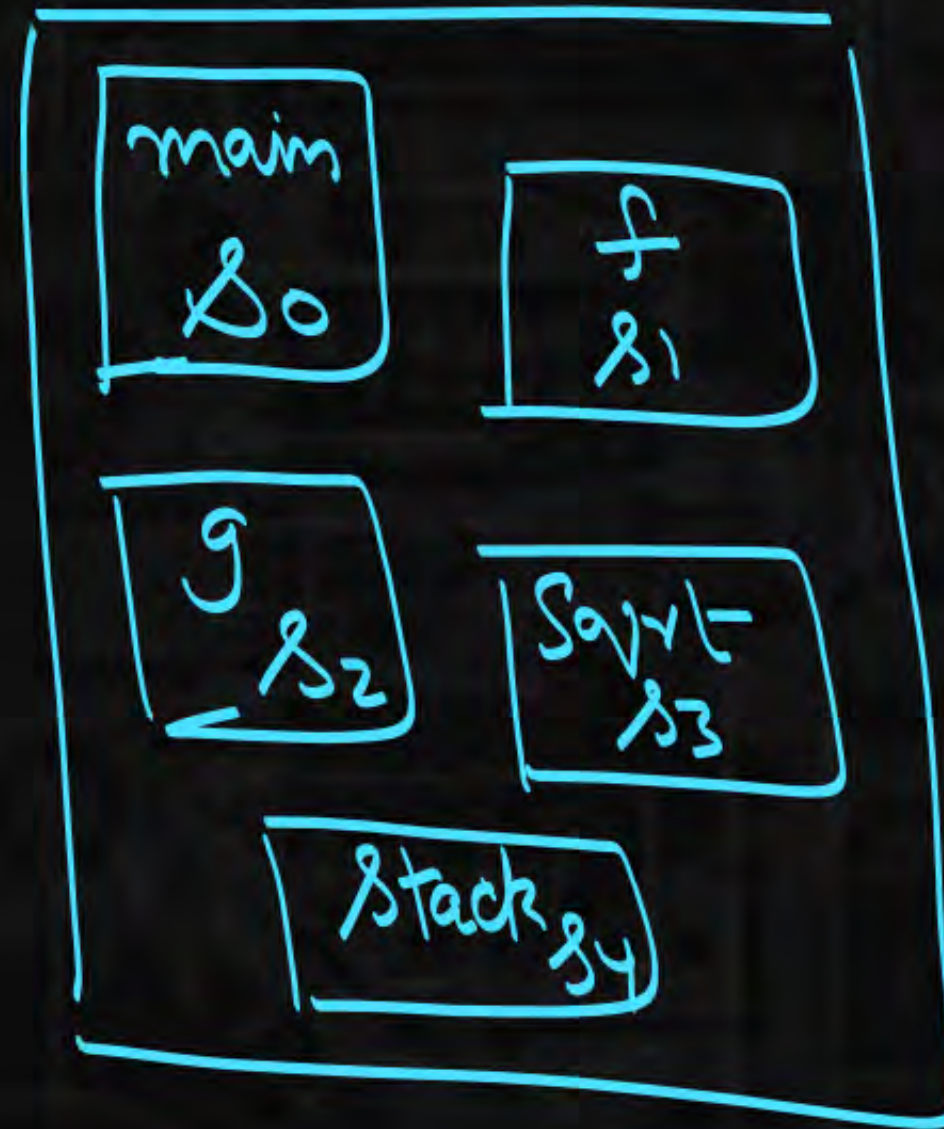
Inverted Paging, Monitors
and Shared Pages

Segmented Paging Architecture



Segmentation

→ to guarantee (Preserve) user's view of Mem. alloc. to Programs;



	Paging	Segmentation
Int. Frag.	✓ Last Page	✗
Ext. Frag.	✗	✓ P.A.S

→ Paging

< Segmented-Paging >

Segment

S.T

→ (If Segment Table becomes large)

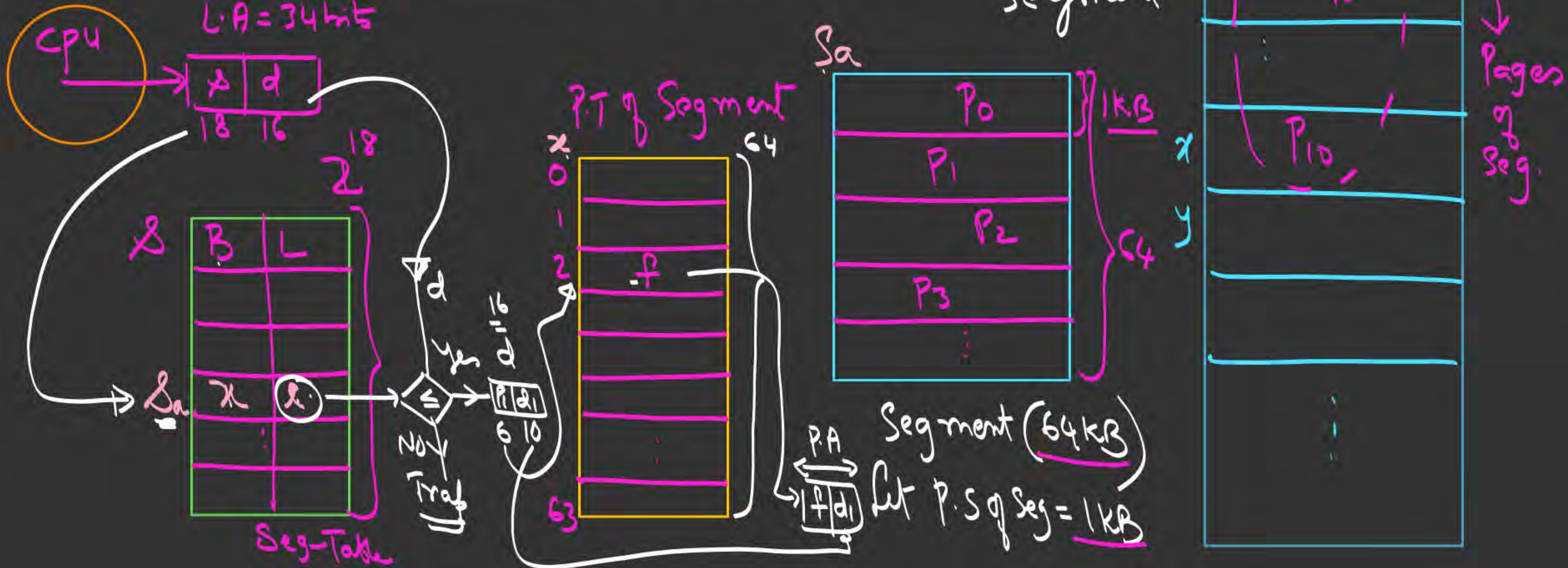
Segmented - Paging:

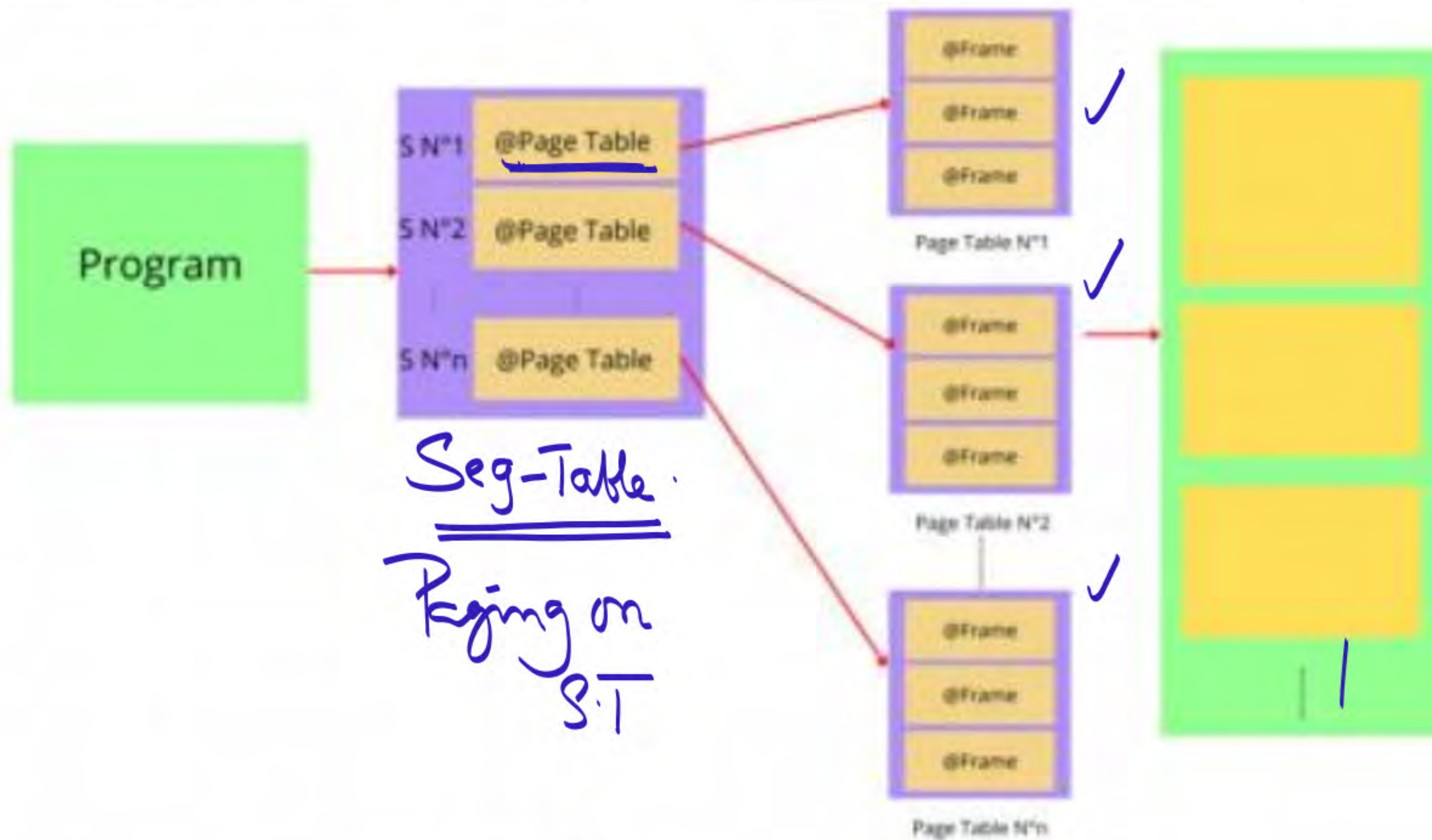
L.A = 34 bits

No. of Seg's = 2^{18}

$\langle s, d \rangle = \langle 18, 16 \rangle \Rightarrow$ Max. Seg. Size = $2^{16} = 64 \text{ KB}$

B = Address of P.T of the Seg. Apply Paging on Segment





Program divided into Segments → Segment Table with Page Tables Addresses → Page Tables with frames addresses → Main Memory

Virtual Address :

Segment Number

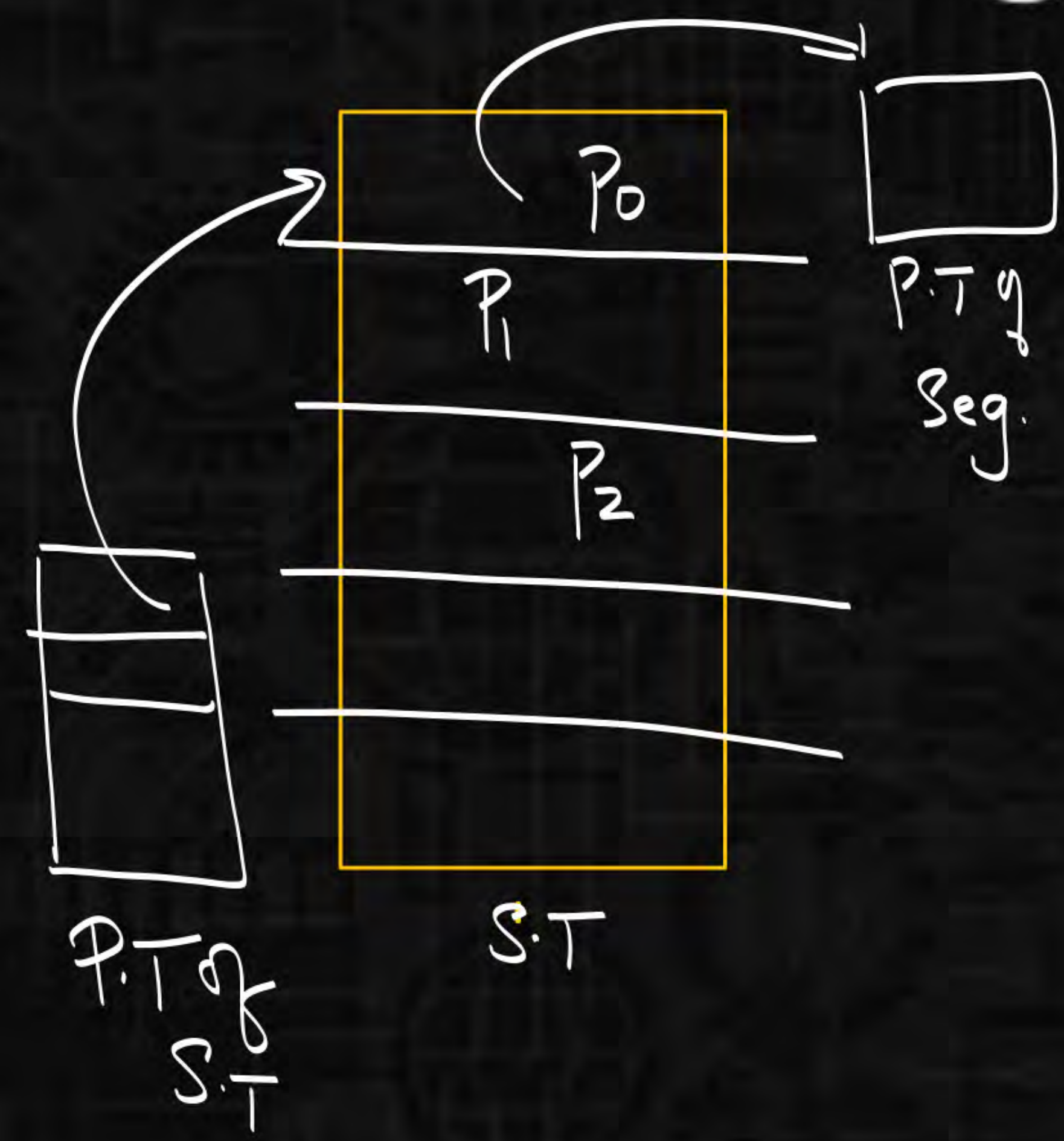
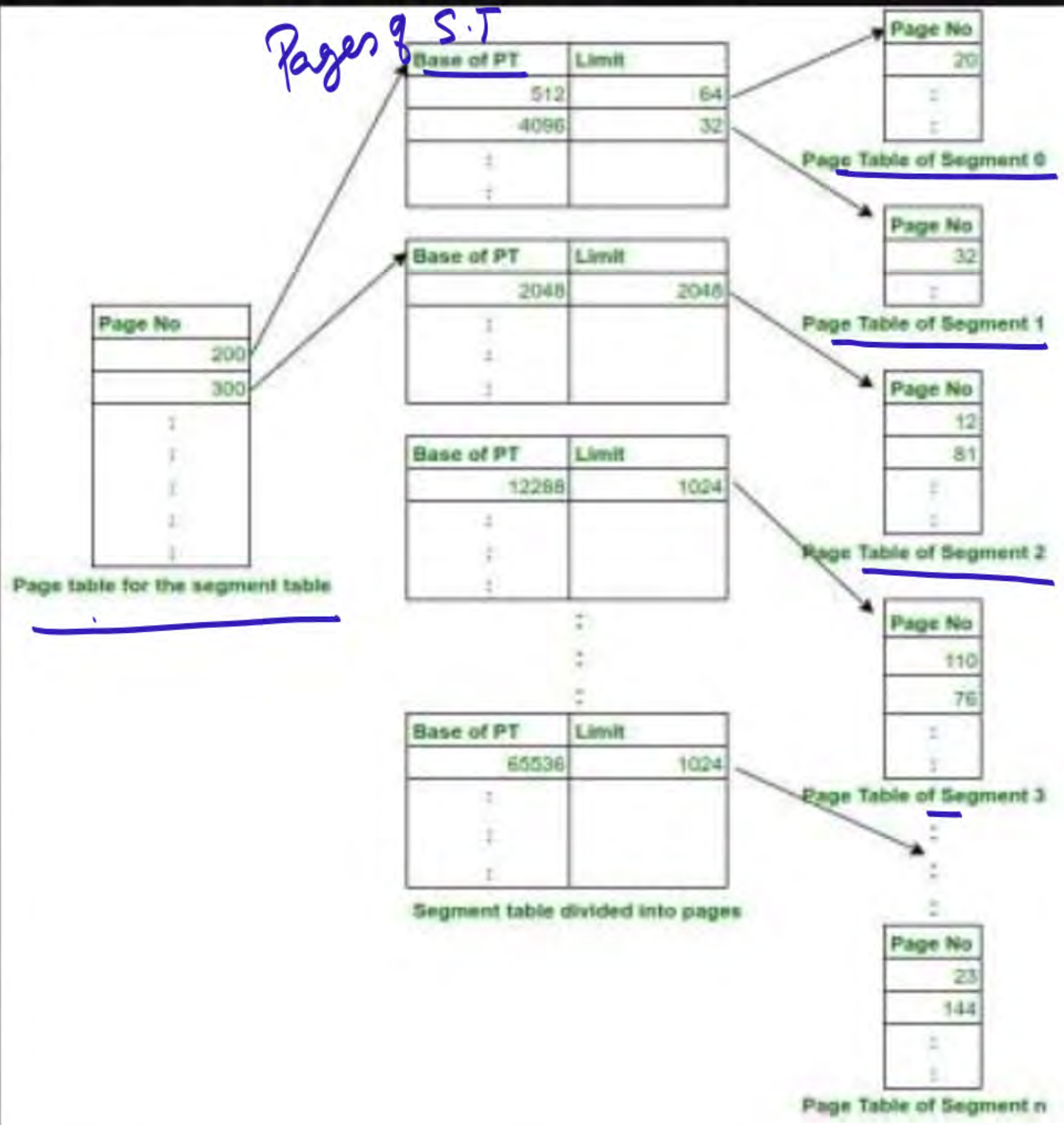
+

Page Number

+

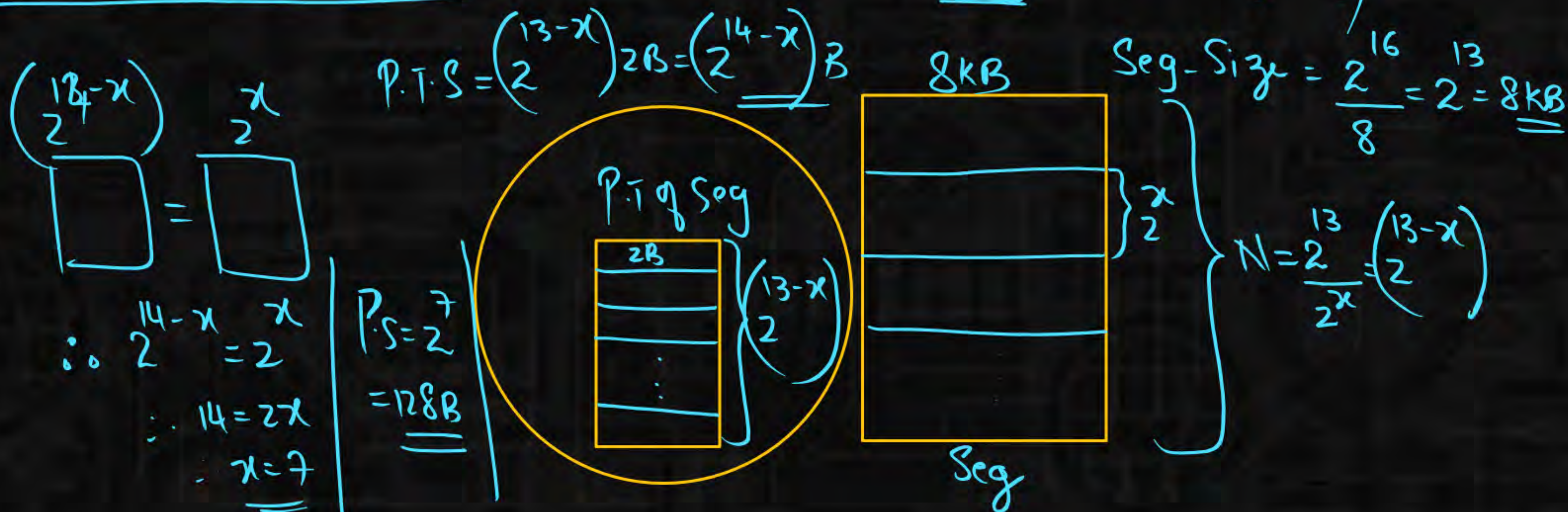
Offset

Pages of S.T



Q.1

Consider a System using Segmented-Paging Architecture with $V.A.S = P.A.S = 2^{16}$ Bytes. The VAS is divided into 8 equal sized nonoverlapping Segments. Paging is applied on Segment, with a Page size being a power of 2 in Bytes. The Page Table Entry size of the Page Tables of the Segment is 16 bits. What must be the Page Size of the Segment such that the Page Table of the Segment exactly fits in one frame of Memory. Let $P.S = 2^x$ By $V.A.S = 2^{16}$ By



Q.2



Calculate

Seg 256

$$\overline{e_2}$$

ImB

8KB	P ₀
8KB	P ₁
8KB	P ₂₅₅

4GB (a) Size of Virtual Address Space

S.T + P.T)

85kB (b) Address Translation Space Overhead in Bytes.

(c) The number of levels of Memory accesses required for Address Translation.

$$\begin{aligned} \text{S.T. Size} &= 2K * 4B \\ &= \underline{8KB} \checkmark \end{aligned}$$

$$\begin{aligned} \text{P.T. Size} &= 256 * 2B \\ &= 512B \end{aligned}$$

ss Translation.

$\therefore \text{Seg-Size} = 256 \times 8 \text{KB}$

$= 2^8 \times 2^{13}$

$= 2^{21} = \underline{\underline{2 \text{MB}}}$

2K Seg's

V.A.S = No. of Seg's * Seg-Size

$= 2\text{K} * 2\text{MB} = \underline{\underline{4 \text{GB}}}$ ✓

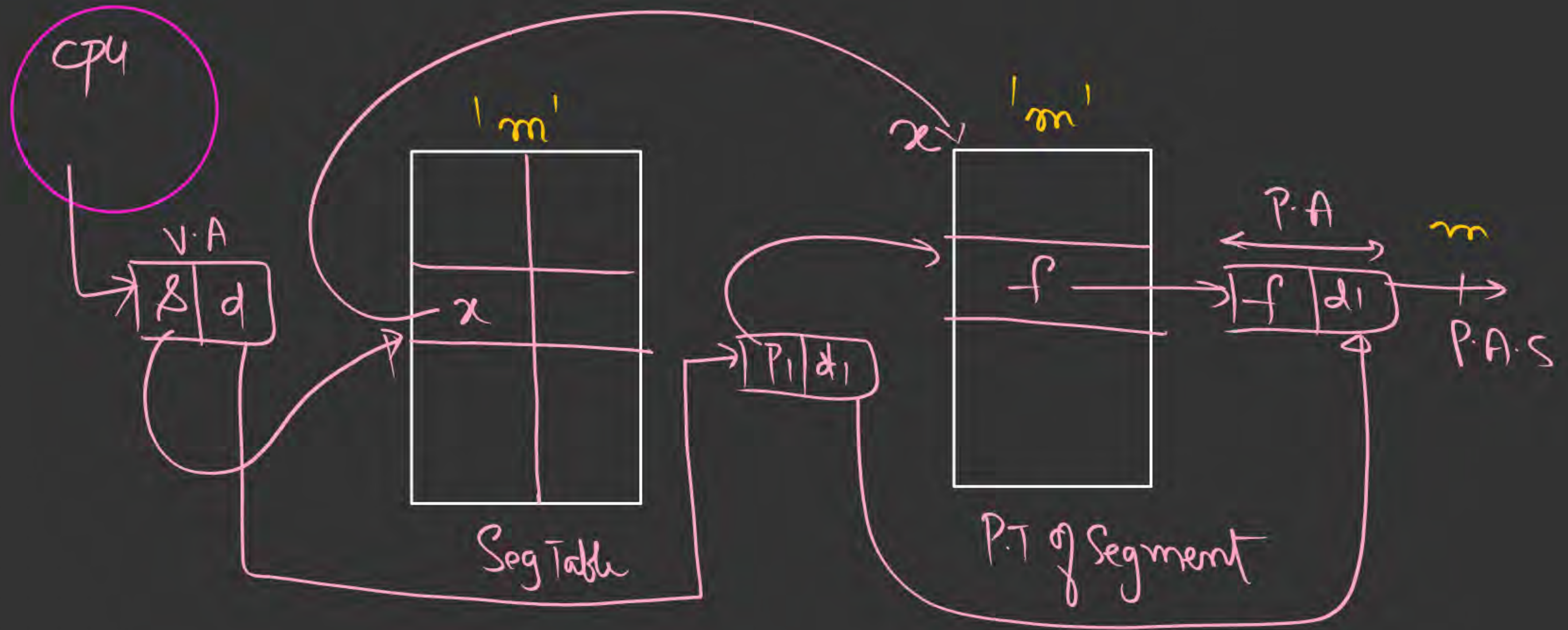
$$= 2^8 \cdot 2^{13} = 2^{21} = 2 \text{ MB}$$

\therefore 256 Pages
in Seg.

P.T of seg.

$$M.M.A.T = 'm'$$

$$E.M.A.T = \underline{\underline{3m}}$$



Q.3

Which one of the following statements is FALSE?



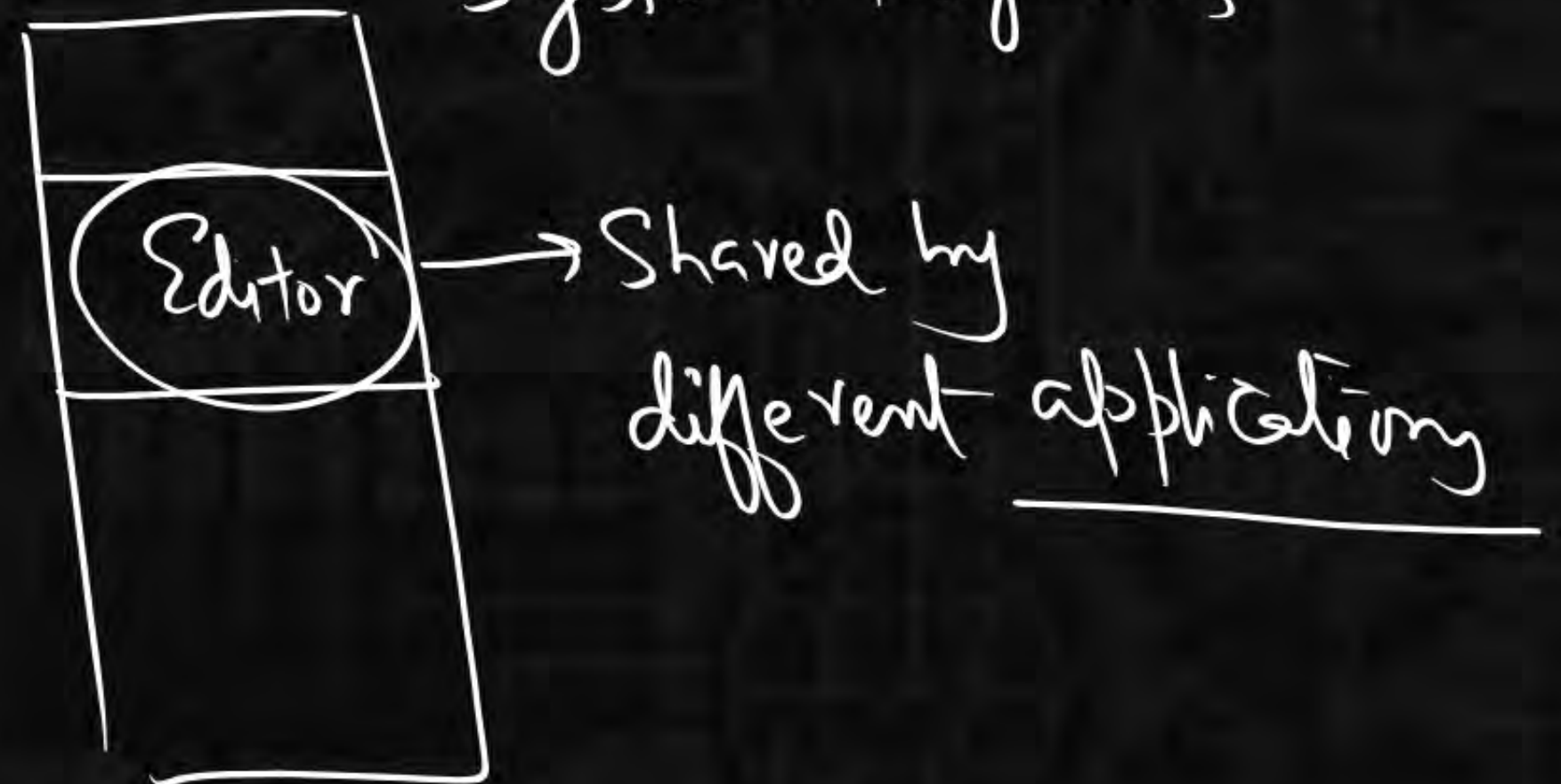
- A** The TLB performs an associative search in parallel on all its valid entries using page number of incoming virtual address. ✓
- B** If the virtual address of a word given by CPU has a TLB hit, but the subsequent search for the word results in a cache miss, then the word will always be present in the main memory. ✓
- C** The memory access time using a given inverted page table is always same for all incoming virtual addresses. ✗
- D** In a system that uses hashed page tables, if two distinct virtual addresses V1 and V2 map to the same value while hashing, then the memory access time of these addresses will not be the same. ✓

Shared Pages



Many a Times in a Multiprogrammed environment applications need to access common Routines
Programs

like Editors & other
System Programs



Shared Pages



Shared code

One copy of read-only (reentrant) code shared among processes (i.e., text editors, compilers, window systems).

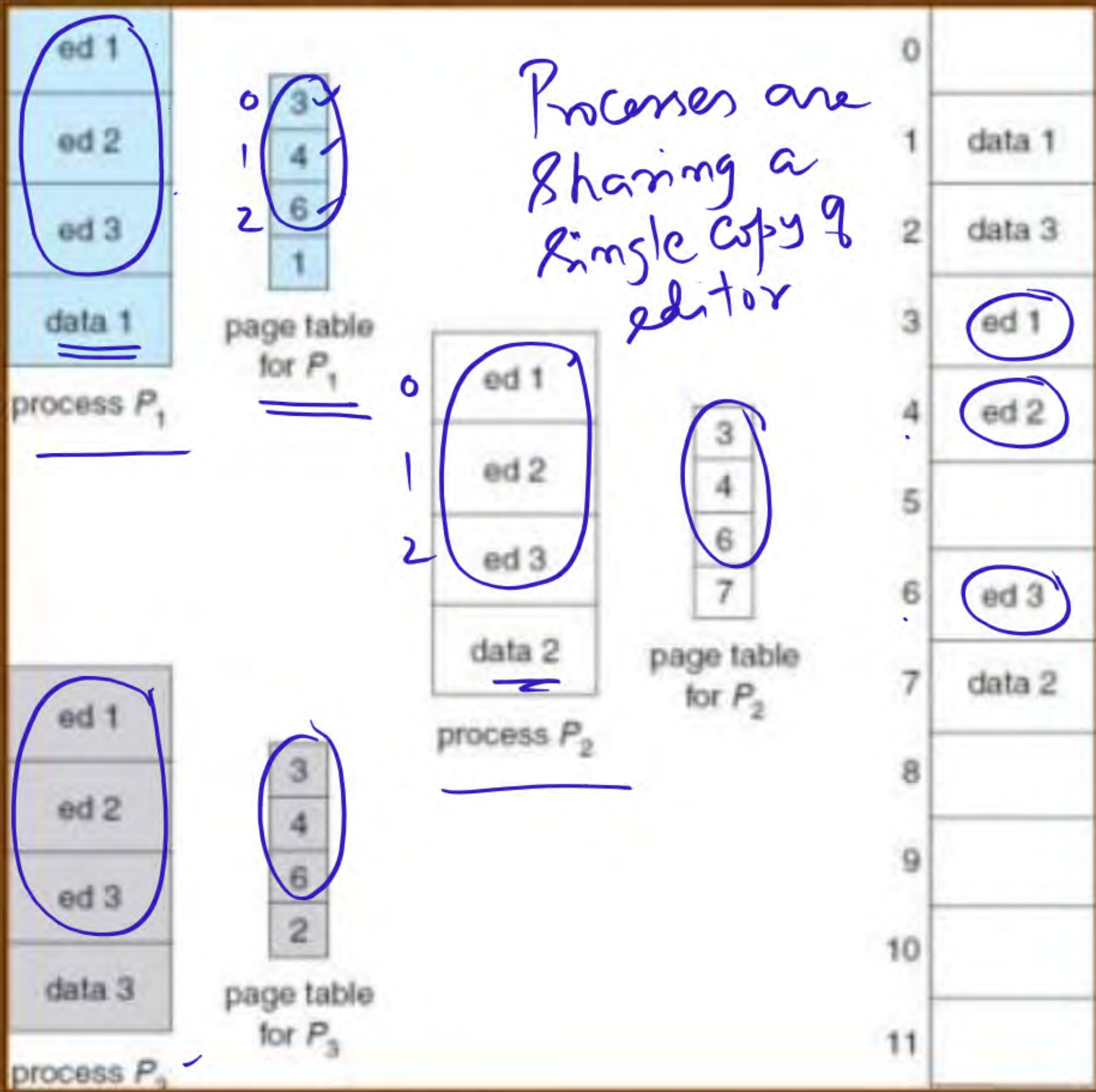
Shared code must appear in same location in the logical address space of all processes

Private code and data

Each process keeps a separate copy of the code and data

The pages for the private code and data can appear anywhere in the logical address space

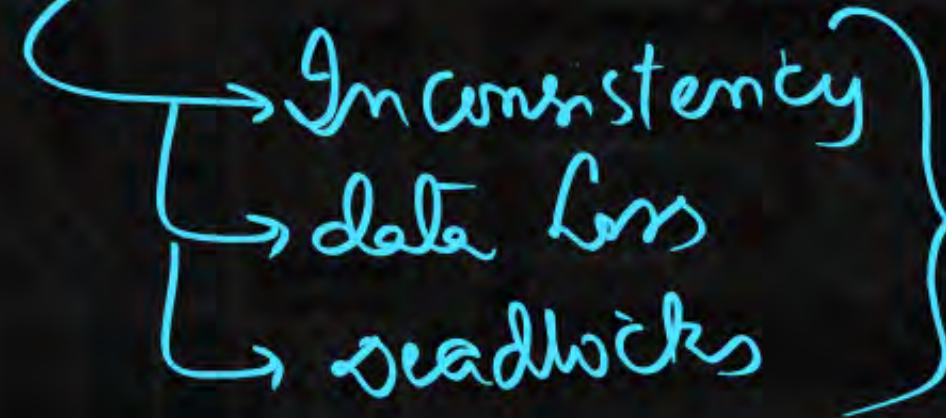
Shared Pages Example



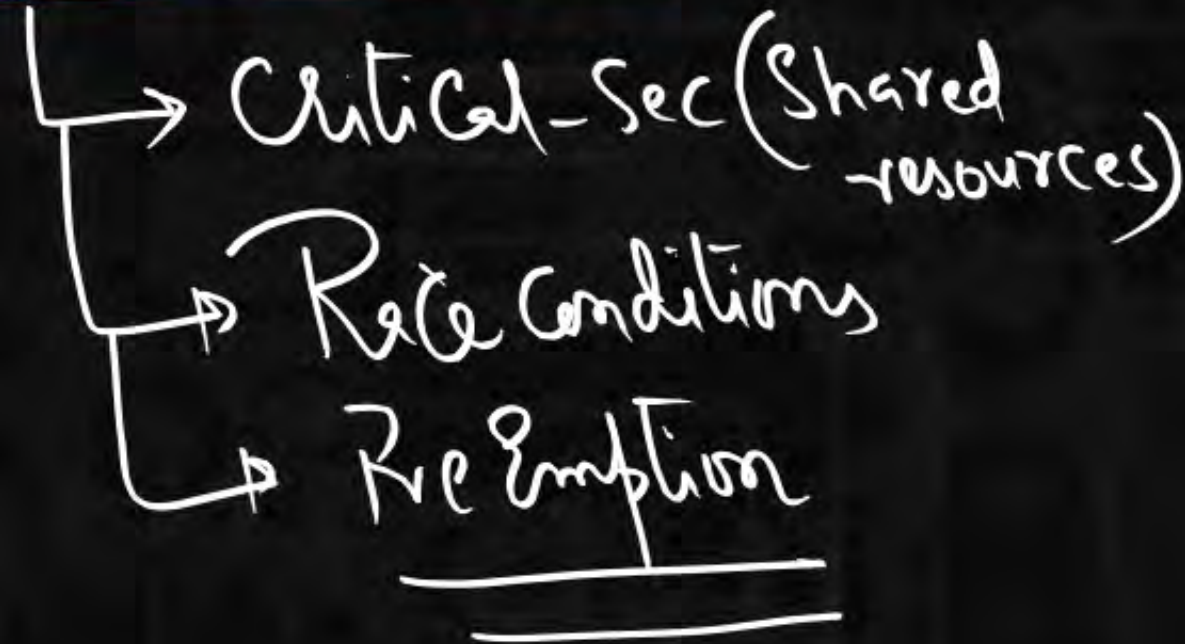
Monitors



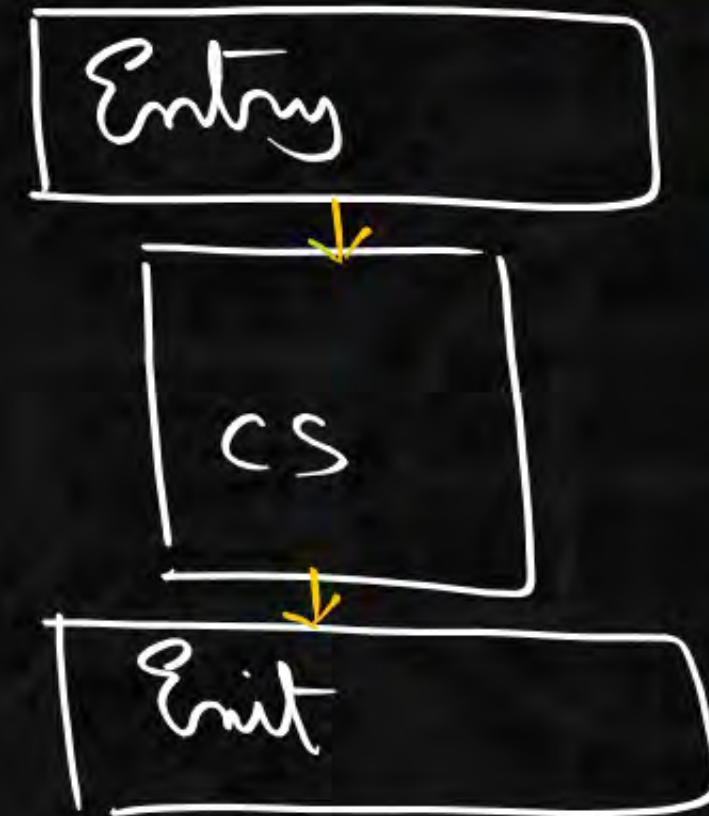
Synchronization



Nec Conditions:



CS-Problem



Requirements

- Mut Exclusion
- Progress
- Boundedwait

Wastage of
CPU time

Synch. Mech's

S/w um (Busy-waiting)

- ① Lock variable
- ② Strict Alternation
- ③ Peterson soln
- ④ Dekker's Algo

H/w (a) TLS } Lock based
(b) SWAP }

Priority
Inversion

Blocking/N.B.W

→ Sleep() & wakeup() : Deadlock

→ Semaphore < Counting Binary

→ Monitors

Monitors:

↳ (B. Hansen)

: is a collection of Procedures, variables and data structures that are all grouped together in a special kind of Module/Package, $\langle \text{class} = \text{Abstraction} + \text{Encapsulation} \rangle$

→ Procedures that run outside the monitor cannot access Monitor's internal variables and data structures, however they can activate only member functions, $\langle \text{Private} \rangle$

→ Monitor include special condition variables, that support 'P' & 'V' ops;

→ Monitors have an important Property that only one Process will be active in the Monitor at any time;


```

monitor monitor name
{
    /* shared variable declarations */ ✓

    function P1 ( . . . ) {
        . . .
    }

    function P2 ( . . . ) {
        . . .
    }

    .
    .
    .
    function Pn ( . . . ) {
        . . .
    }

    initialization_code ( . . . ) {
        . . .
    }
}

```

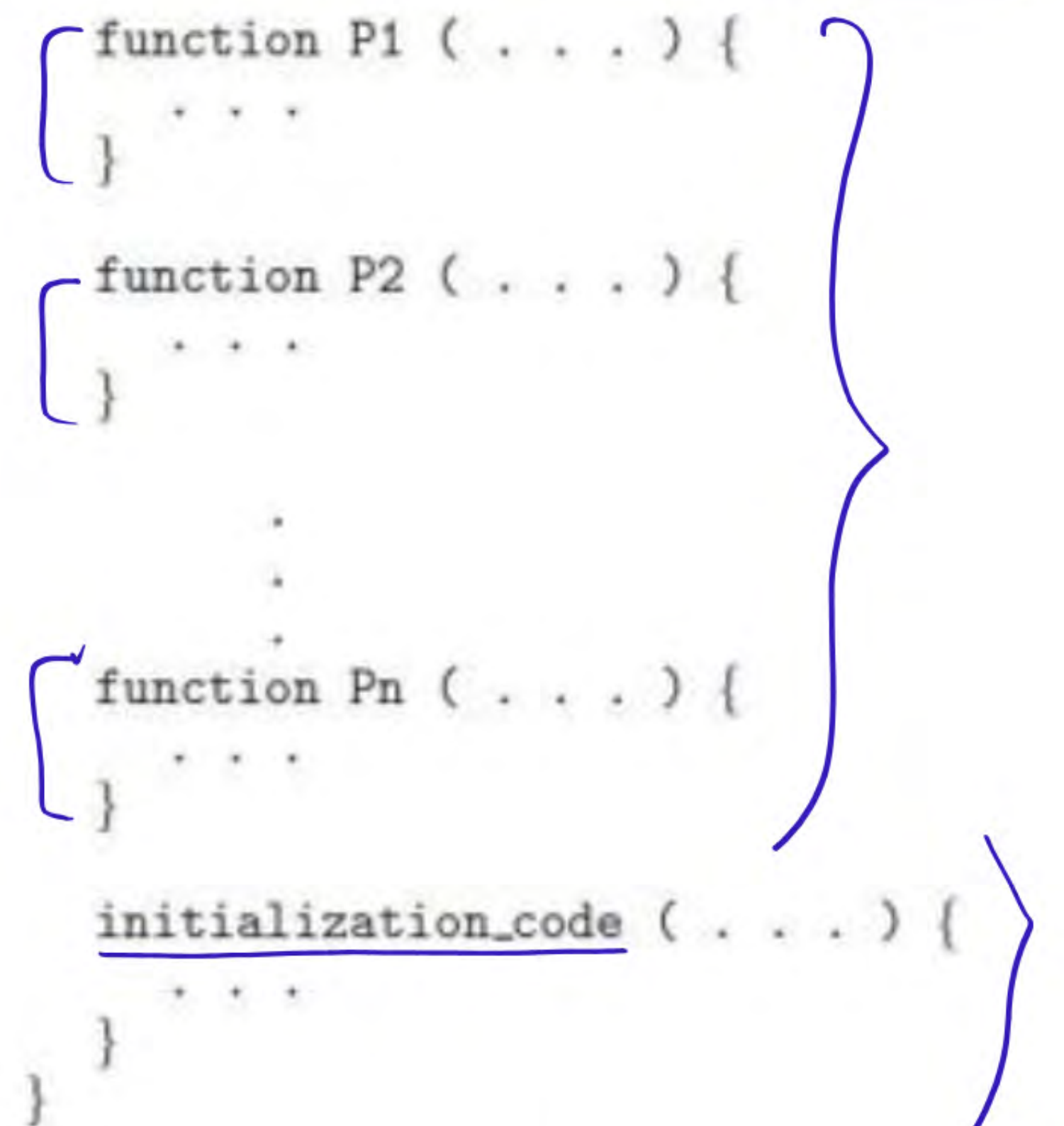


Figure 5.15 Syntax of a monitor.

Constructor

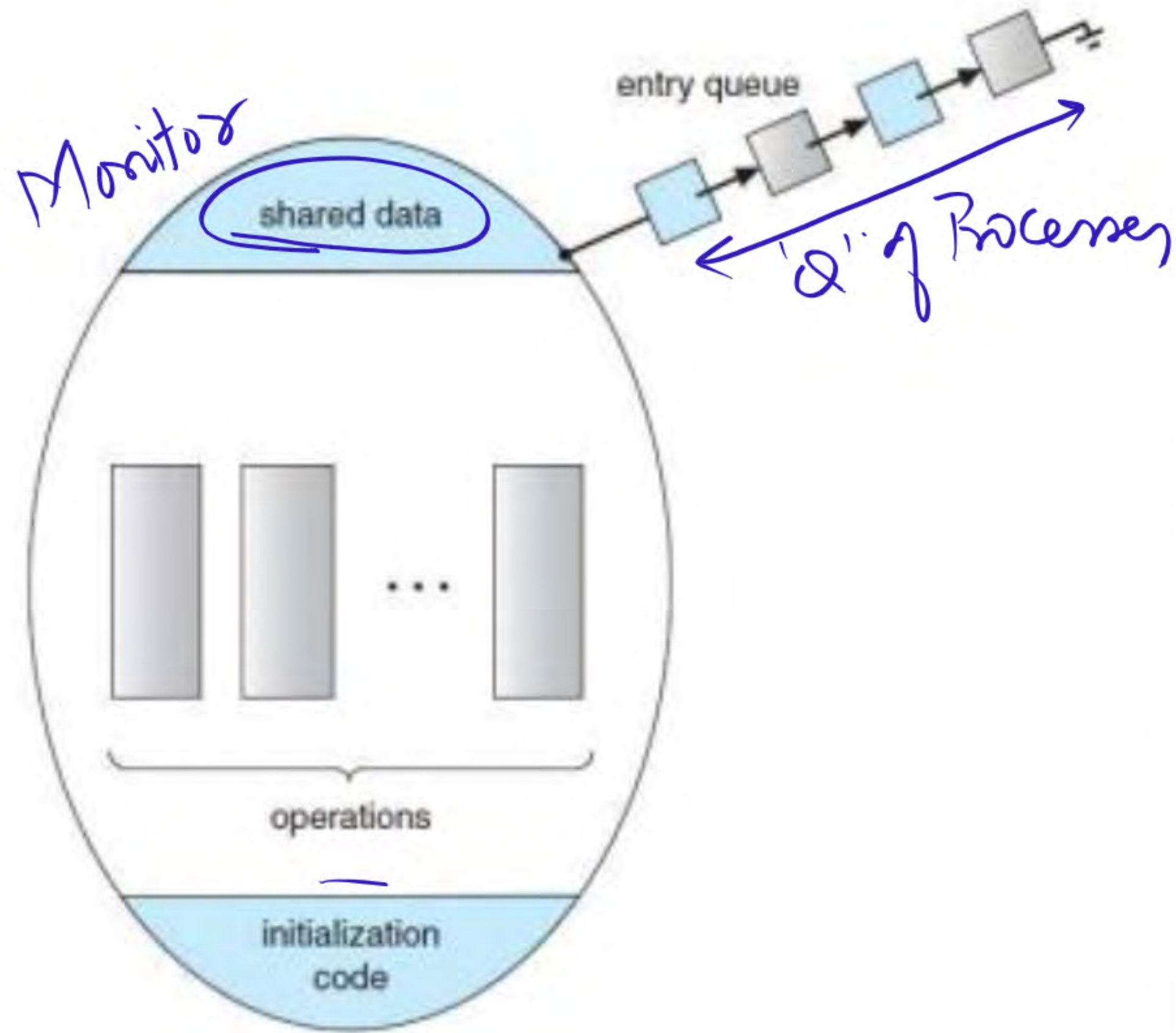


Figure 5.16 Schematic view of a monitor.

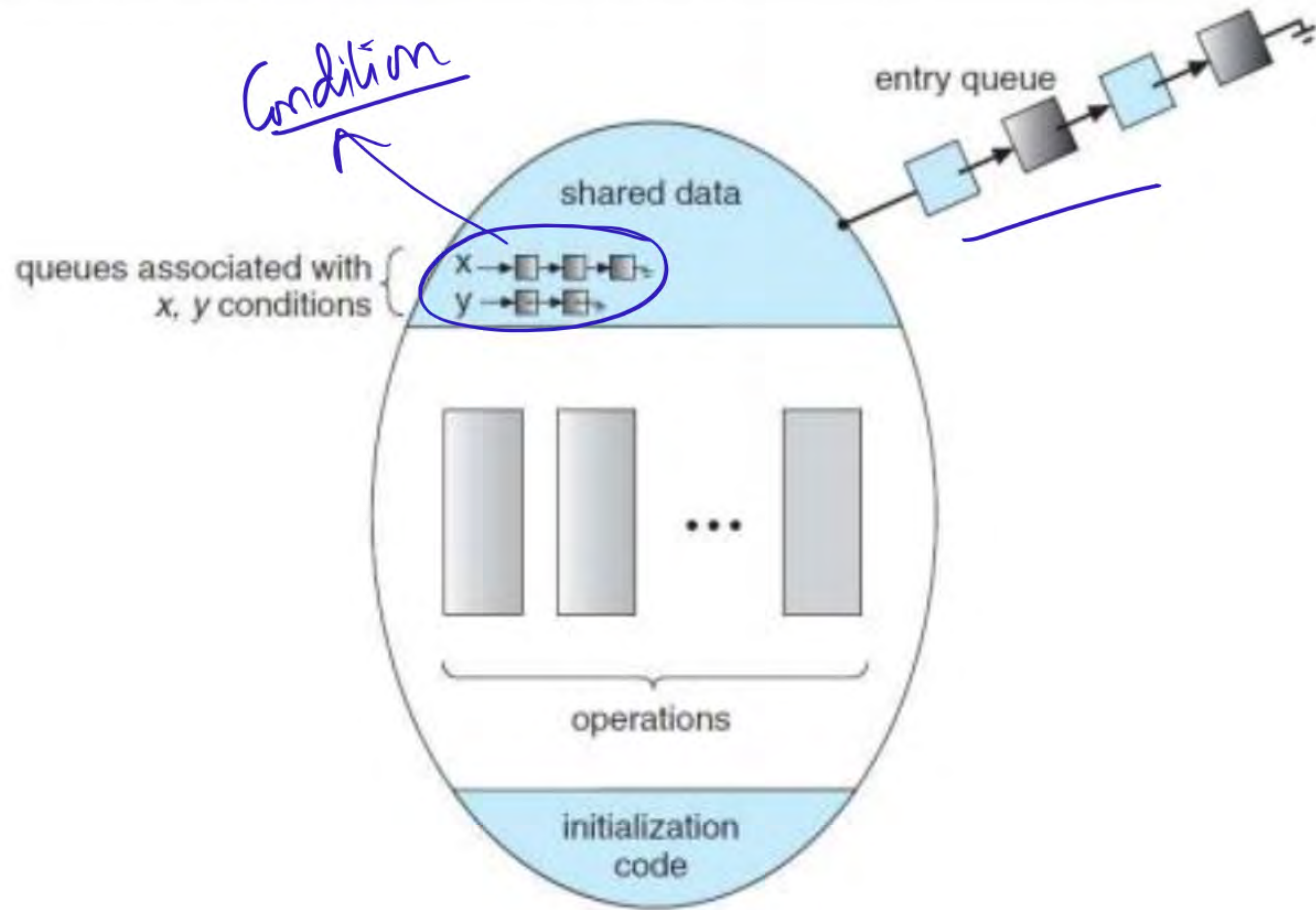


Figure 5.17 Monitor with condition variables.


```

monitor DiningPhilosophers
{
    enum {THINKING, HUNGRY, EATING} state[5];
    condition self[5];

    void pickup(int i) {
        state[i] = HUNGRY;
        test(i);
        if (state[i] != EATING)
            self[i].wait();
    }

    void putdown(int i) {
        state[i] = THINKING;
        test((i + 4) % 5);
        test((i + 1) % 5);
    }

    void test(int i) {
        if ((state[(i + 4) % 5] != EATING) &&
            (state[i] == HUNGRY) &&
            (state[(i + 1) % 5] != EATING)) {
                state[i] = EATING;
                self[i].signal();
            }
    }

    initialization_code() {
        for (int i = 0; i < 5; i++)
            state[i] = THINKING;
    }
}

```

Take-forks

Blocked

L

R

enum {THINKING, HUNGRY, EATING} state[5];

condition self[5];

Implementation of
Dining Philosopher
Problem using Monitors



Semaphore
~ Monitors

Figure 5.18 A monitor solution to the dining-philosopher problem.

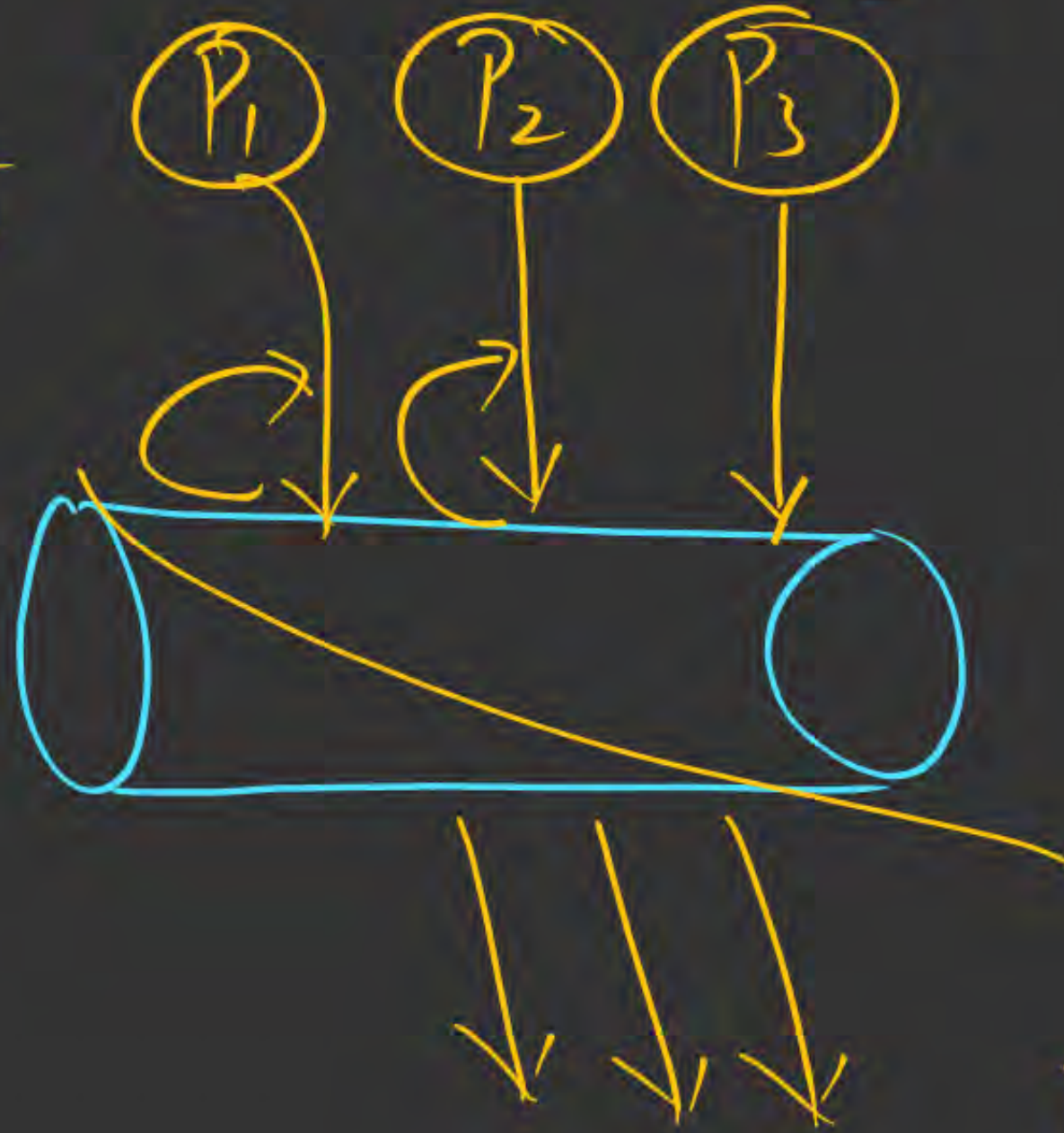
Regular Revision

Barrier Synchronization

40%

Practice (PYQ's +
+ Enc exercises ISRO +
BARC +
TIFR)

Test Series
→ (Time Mgmt
→ Syllabus
Coverage)



Recorded
videos for
unsolved (H/W)
Questions of
the Handout

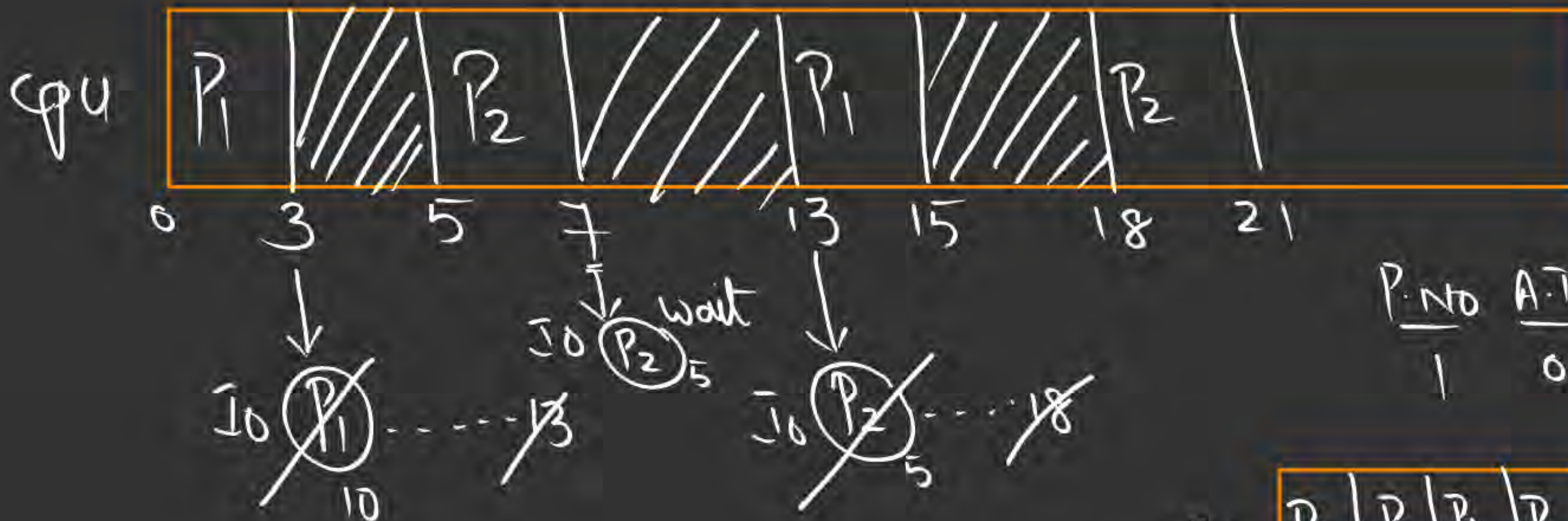
Platform
60% + 40%

FCFS with non-Conc. IO

<u>P.No</u>	<u>A.T</u>	<u><BT; IOBT; B.T></u>
1	0	<3; 10; 2>
2	5	<2; 5; 3>

$$TAT(P_1) = 15 - 0 = 15$$

$$TAT(P_2) = 21 - 5 = 16$$



<u>P.No</u>	<u>A.T</u>	<u>B.T</u>
1	0	10

