



DIGITAL LOGIC

Sequential circuit

Lecture No. 4



By- CHANDAN SIR



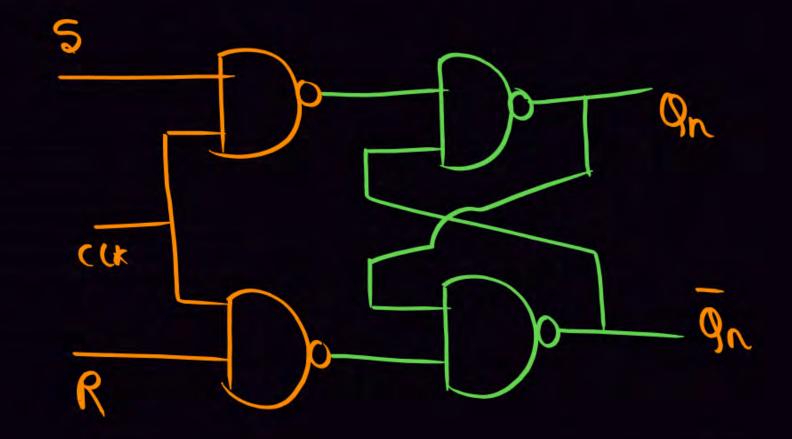
TOPICS TO BE COVERED 01 D, T Flip Flop

02 DESIGNING of Flip Flop

03 Discussion



S-R FF



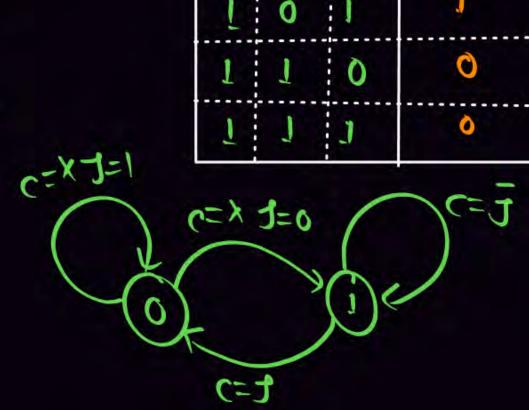


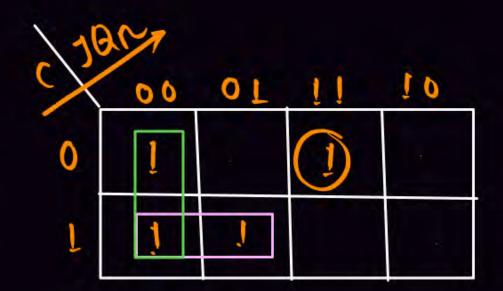
Q_n	Bn+1	L	K
0	0	Ò	×
0	1	1	×
1	0	X	1
1	1	×	0

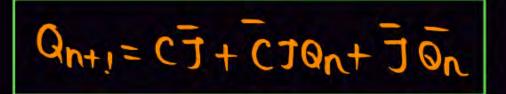
C	J	G _{r+1}
0	0	<u>On</u>
0	1	On
1	0	7
ι	1	0

Write characteristic table characteristic Equation characteristic Equation Excitation table & state Diagram.

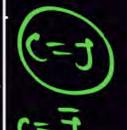
C	t	On	OM 1
0	0	0	1
0	0	J	0
	1	0	0
0	1	1	1
1	0	0	J
L	0	1	J
1	1	0	0
1	J	J	0







Qn	Qnti	0	t
0	C	×	1
0	1	×	0
1	0	0/1	0/1
1	1	0/1	1/0



D-FLIP-FLOP



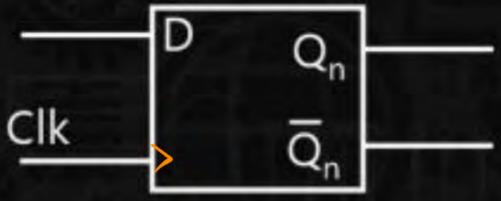
(i) It is known as Delay FF or Transparent FF.

Roda FF

(ii) In the D FF what ever the input is applied it will directly come to the

output along with the clock.

1. Symbol



2. Truth Table

D	Q _{n+1}
0	0
1	1

D-FLIP-FLOP



3. Characteristic table

D	Qn	Q _{n+1}
0.	0	0
0	1	0
1	0	1
1	1	1

$$Q_{n+1} = D \overline{Q}_n + D Q_n = D (\overline{Q}_n + Q_n) = \overline{M}$$

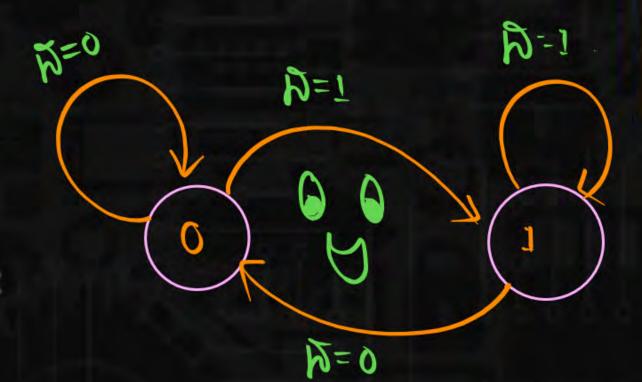
4. Characteristic Equation

$$Q_{n+1} = 10$$

D-FLIP-FLOP

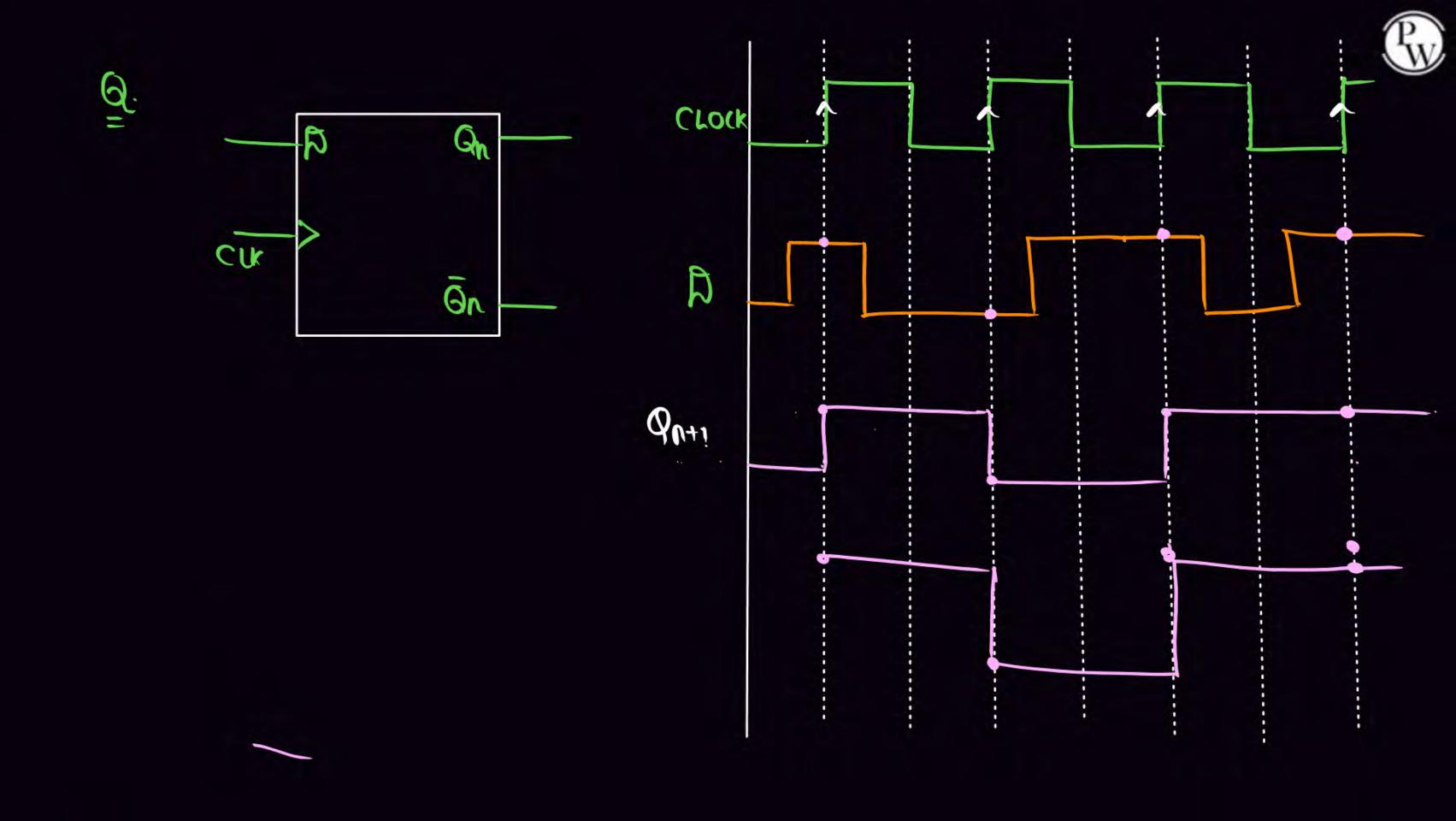


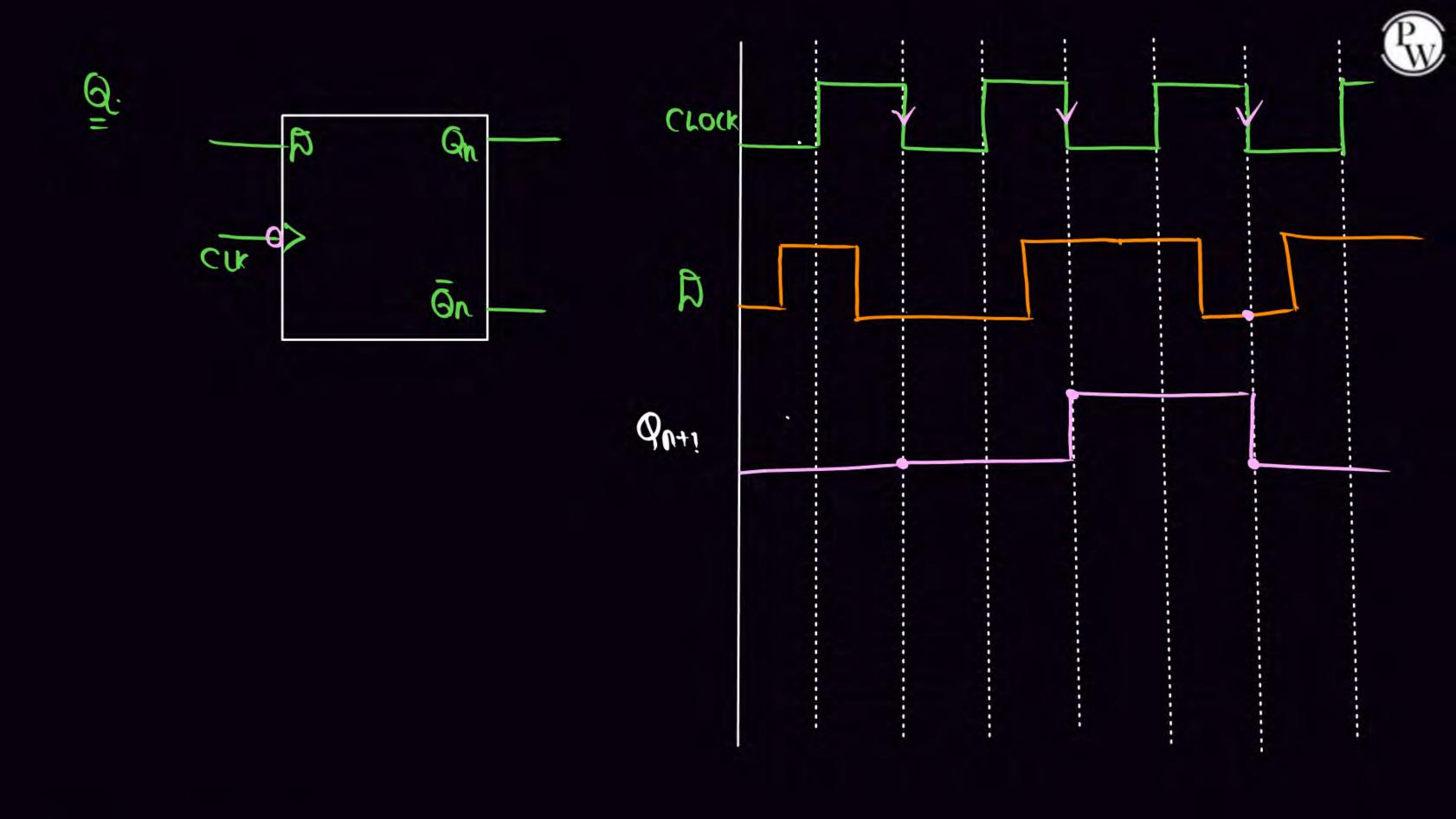
5. Excitation table:



Qn	Q _{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

6. State diagram:

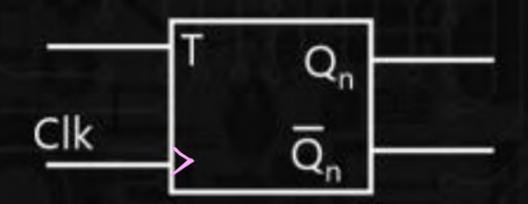




T-FLIP FLOP (TOGGLE FLIP-FLOP)



1. Symbol



2. Truth Table

T	Q _{n+1}
0	Qn
1	-Qr

T-FLIP FLOP (TOGGLE FLIP-FLOP)



3. Characteristic table

T	Q _n	Q _{n+1}
0	0	0
0	1	J
1	0	1
1	1	0

4. Characteristic Equation

$$Q_{n+1} = \overline{7}q_n + 7\overline{q}_n$$

$$Q_{n+1} = T \oplus Q_n$$

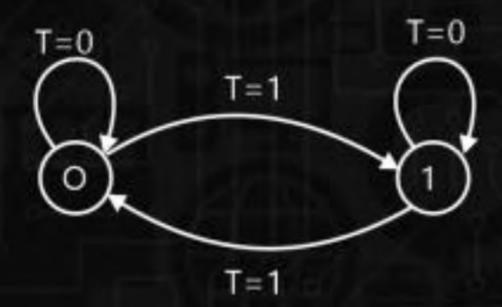
T-FLIP FLOP (TOGGLE FLIP-FLOP)

Pw

5. Excitation table:

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

6. State diagram:



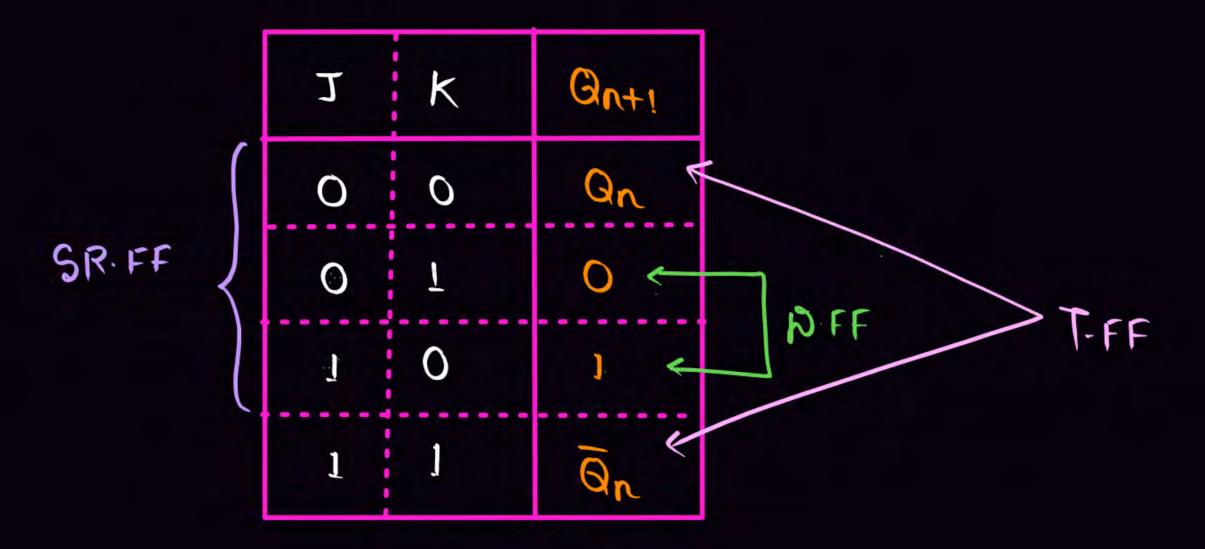
Excitation Table.

5	7
·,	7
N	U
	N

Qn	Qn+1	Ş	R	ナ	K	D	T
0	0	0	×	0	X	0	0
0	1	1	0]	X	1	1
1	0	O]	×	1	0	1
1	1	×	0	×	Ò]	0



(JK.FF) -> universal FF





-> Resired

→ avaliable.

Step (1): Write the characteristic table of desired Flip Flop.

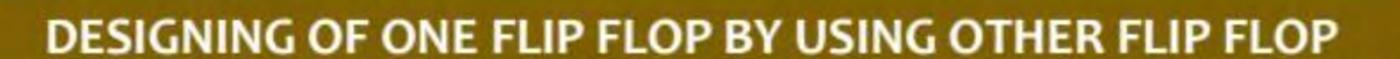
Step (2): Write the excitation table of available Flip Flop.

Step (3): Write the logical expression.

Step (4): Minimize the logical expression.

Step (5): Hardware implementation.

Characteristic Be





Ex. 1. Design a D FF by using T FF?

Step (1) Desired

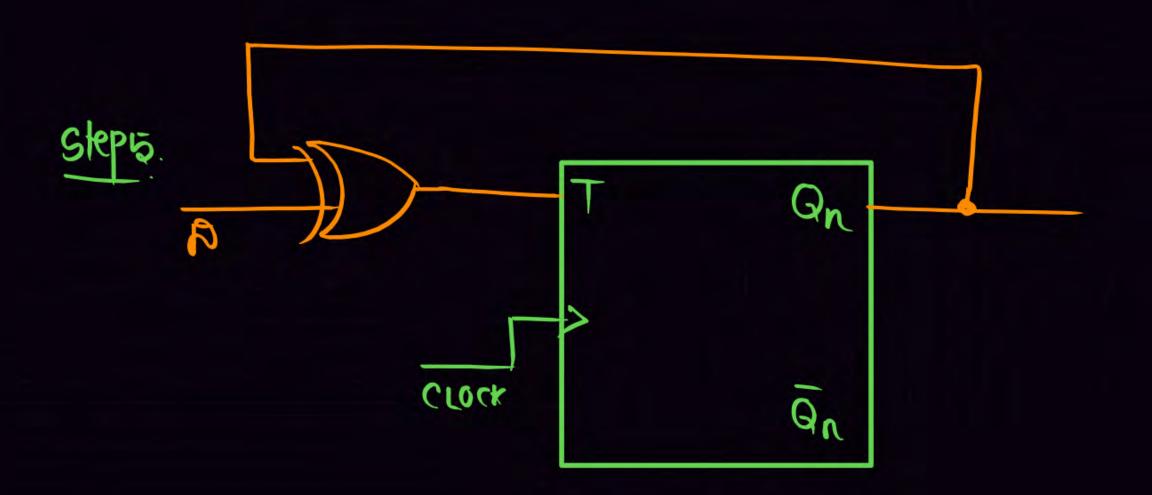
and Step (2)

D	Qn	Q _{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Step (3):- Logical Expression

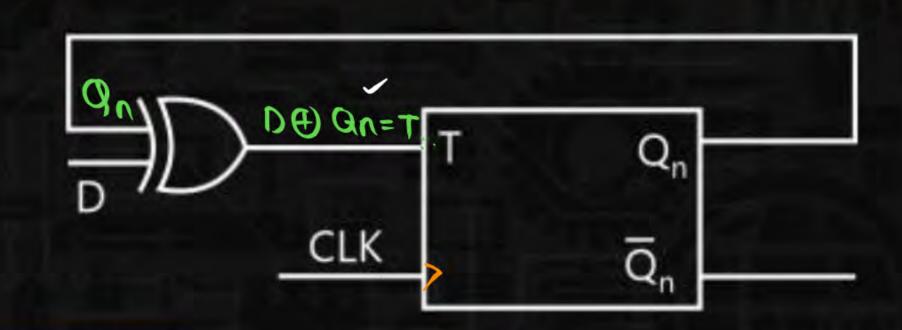
$$7 = \overline{D}Q_n + \overline{D}Q_n$$

Step (4):- No minimization









Justification

Method	D	Qn	Q _{n+1}
	0	0	0
L	0	1	0
L	1	0	1
	1	1	1

Method (2)
$$Q_{n+1} = T \oplus Q_n$$

$$= R \oplus Q_n \oplus Q_n$$

= 1



Design a J K FF by using SR FF.

Step (1) Resided.
and Step (2)

		1		
9n	Omti	5	R	2
O	6	0	X	3.
0	1	1	0	4
1	0	0	1	5
L	1	X	9	0
			1	6

Step (3):

					✓	
	J.	K	Q _n	Q _{n+1}	S	R
	0	0	0	0	0	X
	0	0	1	1	X	0
	0	1	0	0	0	X
	0	1	1	0	0	ţ
	1	0	0	Ī	1	0
	1	0	1	1	X	O
Г	1	1	0	1	L	0
	1	1	1	Ò	0	1

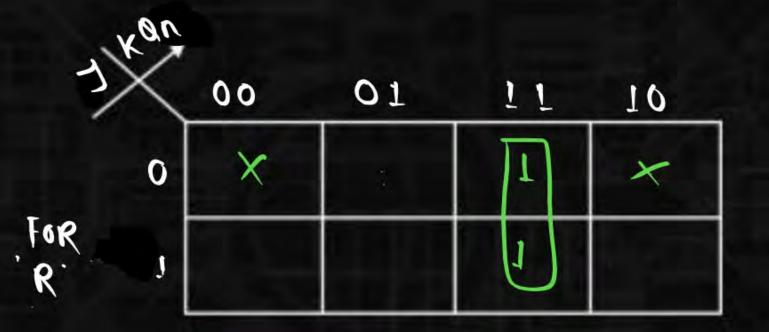
Pw

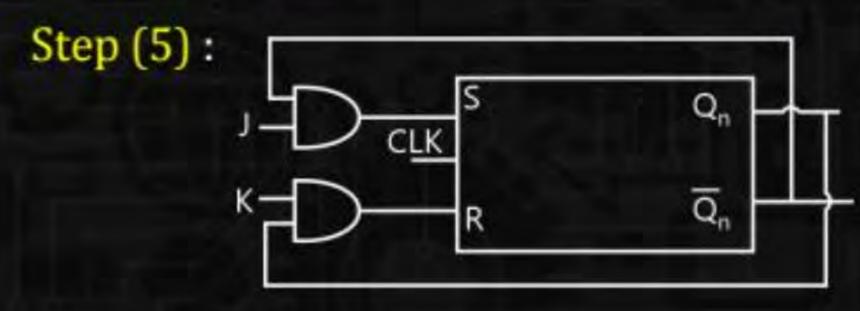
DESIGNING OF ONE FLIP FLOP BY USING OTHER FLIP FLOP

 $R(J, K, Qn) = \sum m(3,7) + \sum d(0,2)$

Step (4) Minimization.

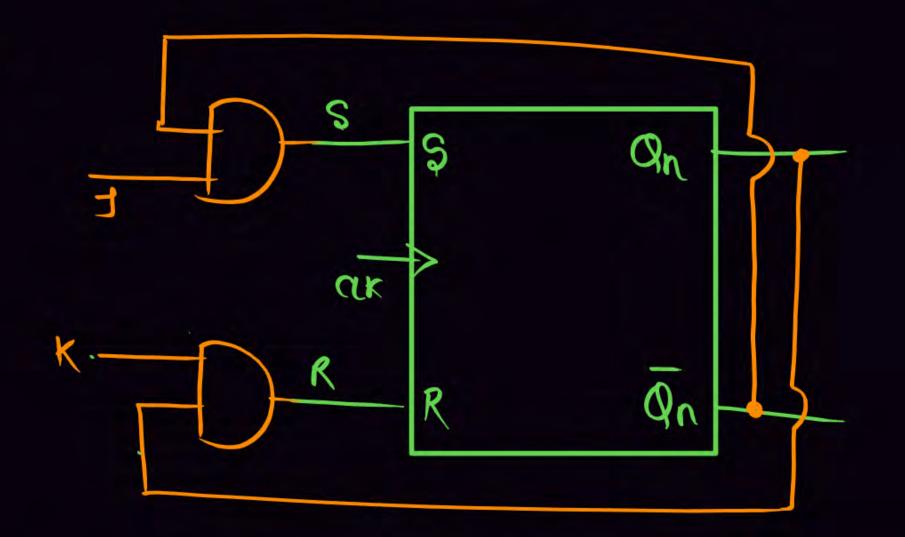






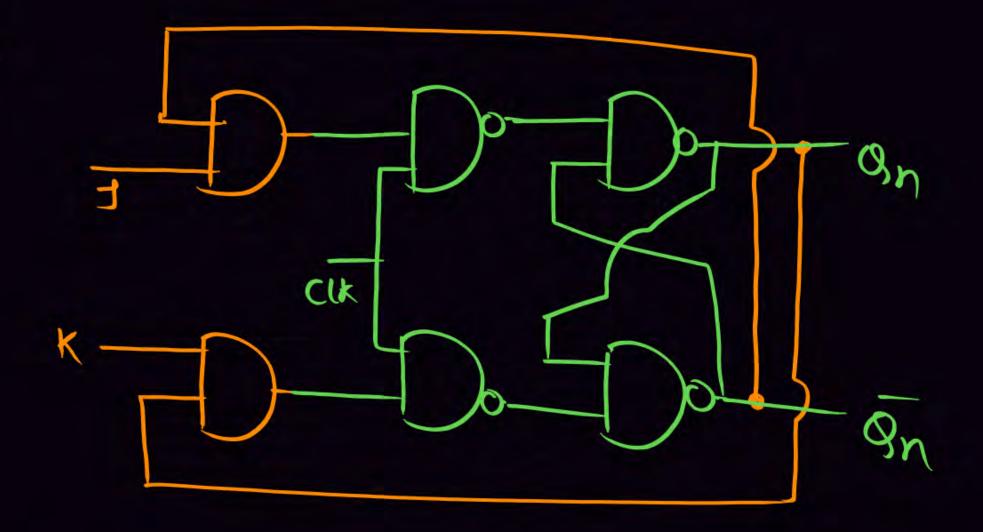


Step 5



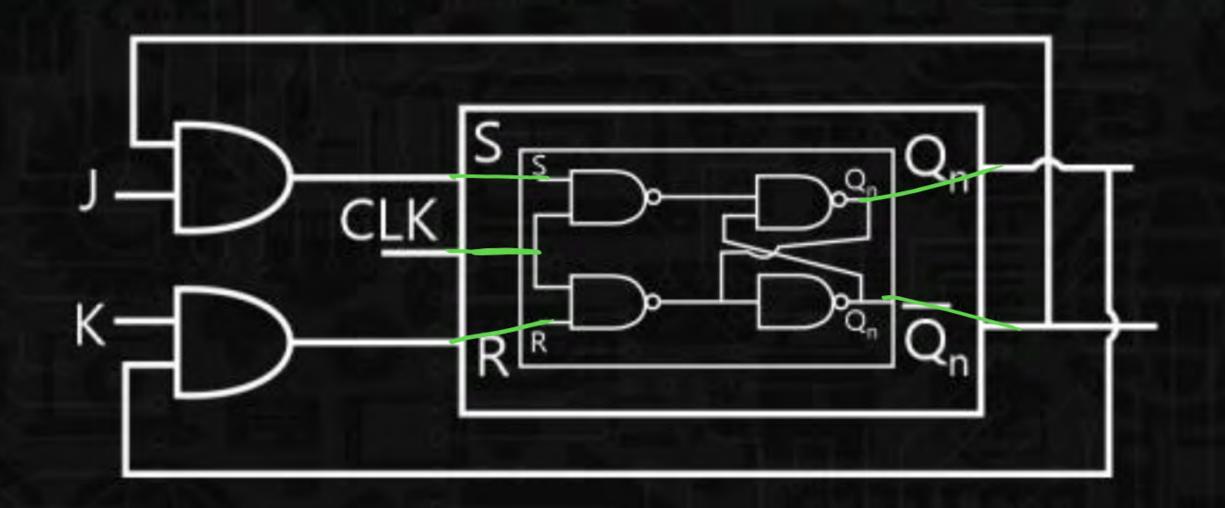


Step 5



(Pv

DESIGNING OF ONE FLIP FLOP BY USING OTHER FLIP FLOP





Desired. Desired.

@ Design a TFF by using S-R FF.

Step3 Estep4

FOR

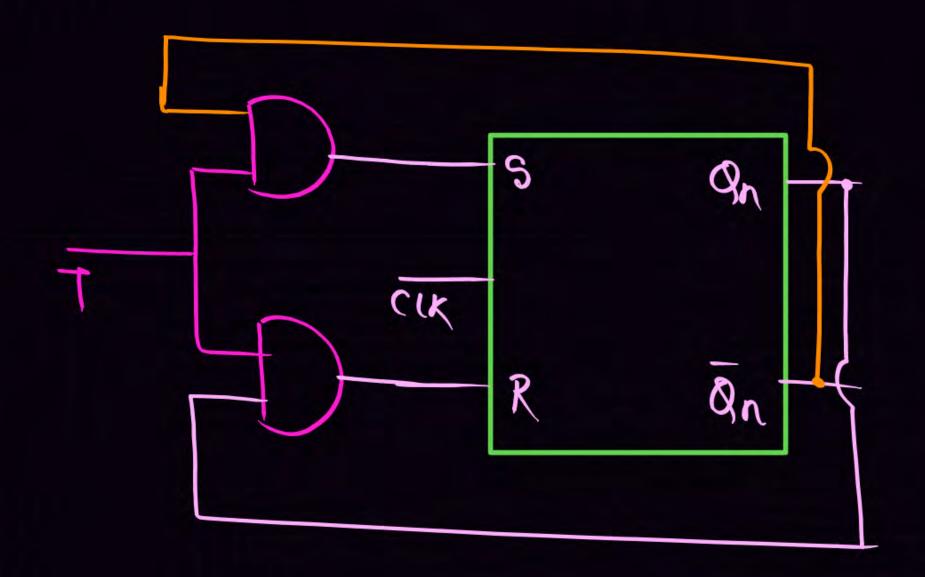
Step (1) T O. O. 1

and Step (2)

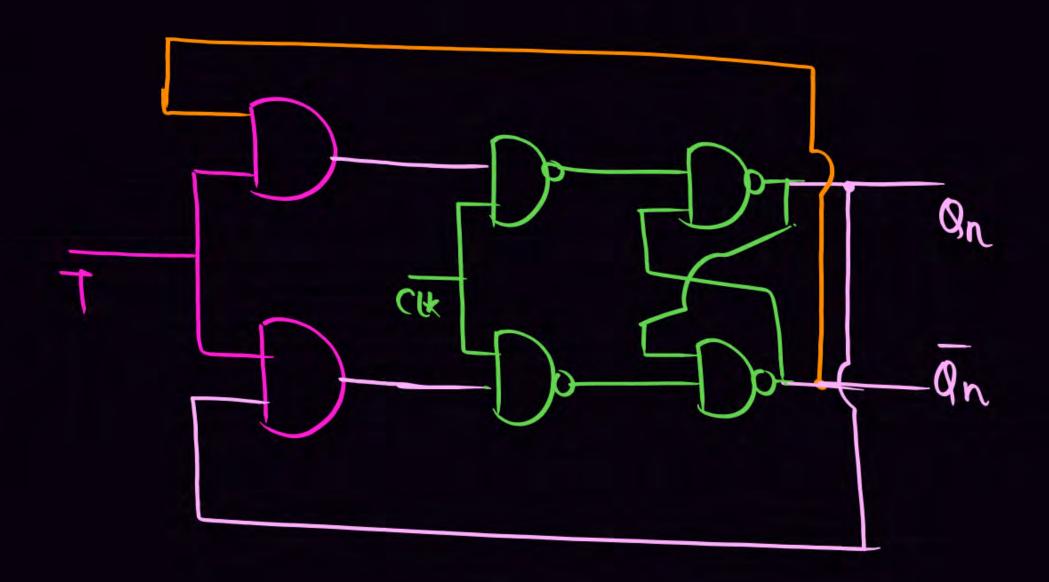
T	Q _n	Q _{n+1}	S	R
0	0	0	0	X
0	1	1	×	0
1	0	1	J	0
1	1	0	0	1

X









Q Besign a POFF by using SR FF?

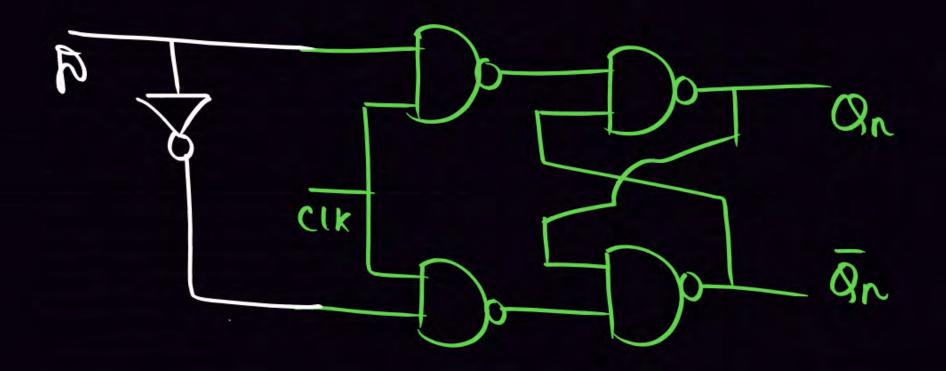


Step 1

e estes 3

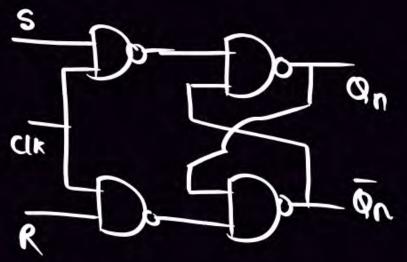
B	On	Qn+i	Ş	R
0	0	0	0	X
	1	0	0	1
	0	1	1	0
1	Ţ	.]	×	0

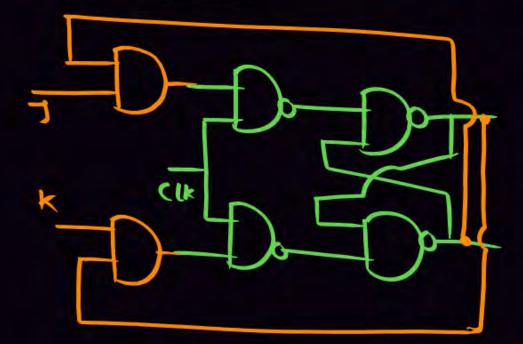


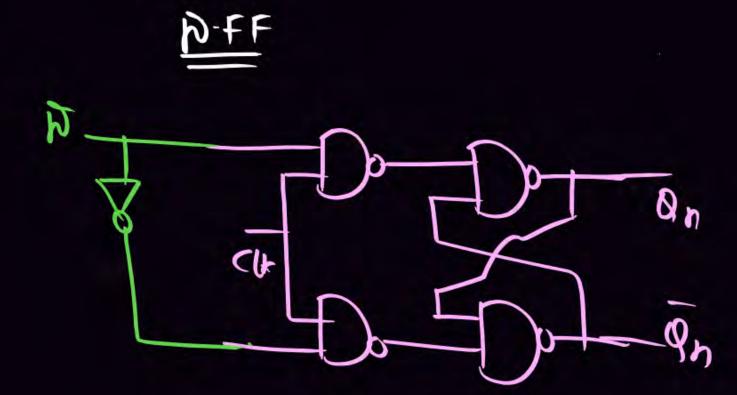


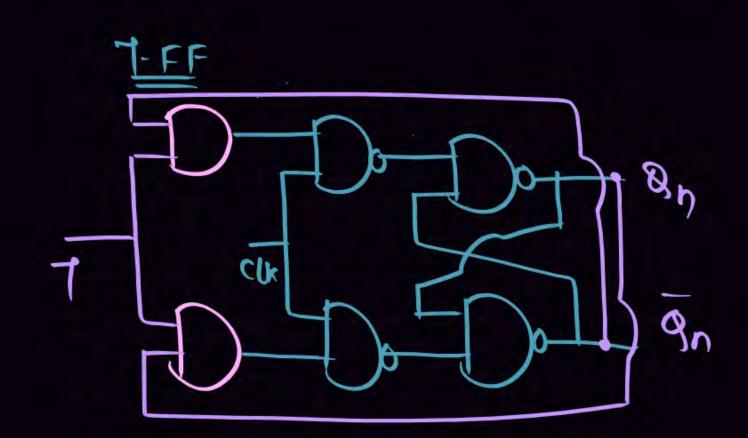












Q.

Desired

ovaliable

Design a C J FF by using S-R FF.

С	J	Q _{n+1}
0	0	Qn
0	1	Q _V
1	0	7
1	1	O





Design a T FF by using S-R FF.

Step (1)

and Step (2)

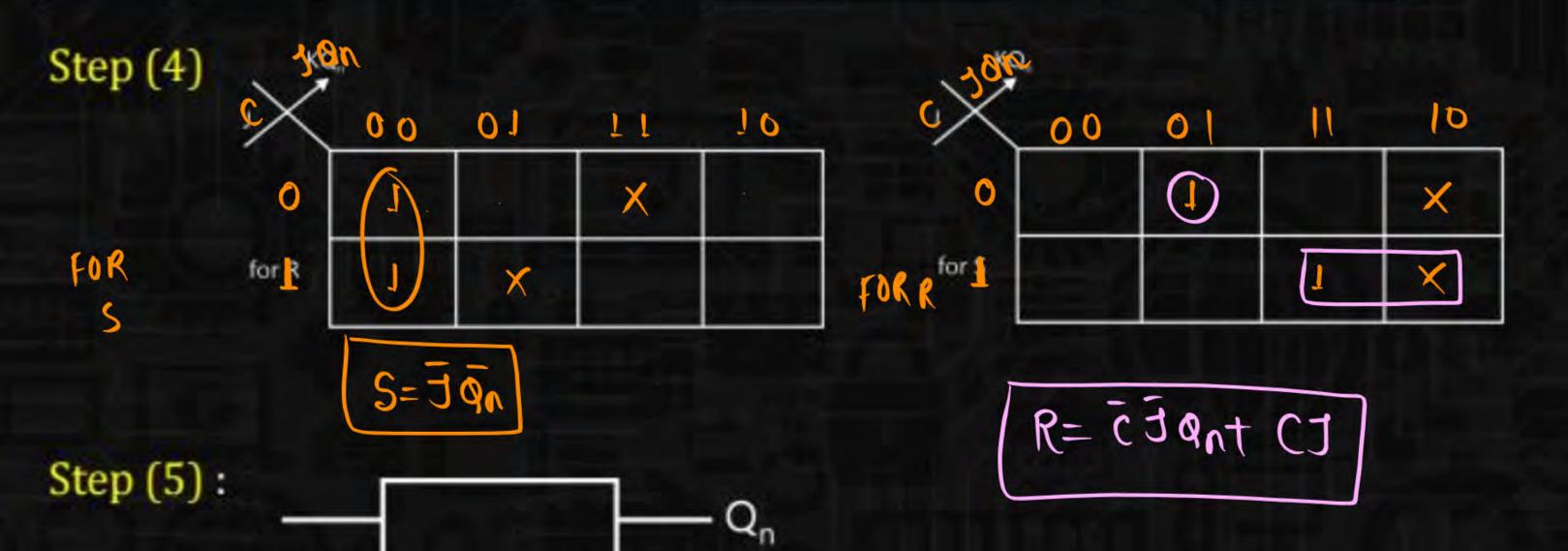
Step (3) \$	(4,0) m3 = (np,t,)	+Ed(3,5)
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Step (4)
$$R(c,1,0) = Em(1,7) + Ed(2,6)$$

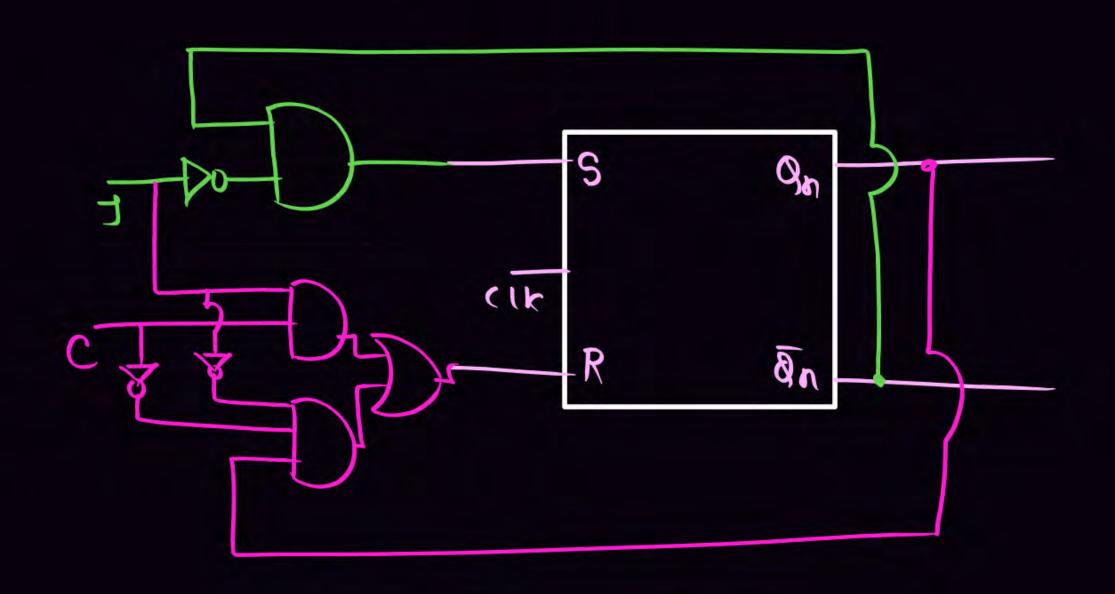
Step (5)

C	J	Q _n	Q _{n+1}	S	R
0	0	0	1	1	0
0	0	1	0	0	J
0	1	0	0	0	×
0	1	1	1	X	0
1	0	0	1	1	0
1	0	1	4	X	Ò
1	1	0	0	0	X
1	1	1	0	0	1



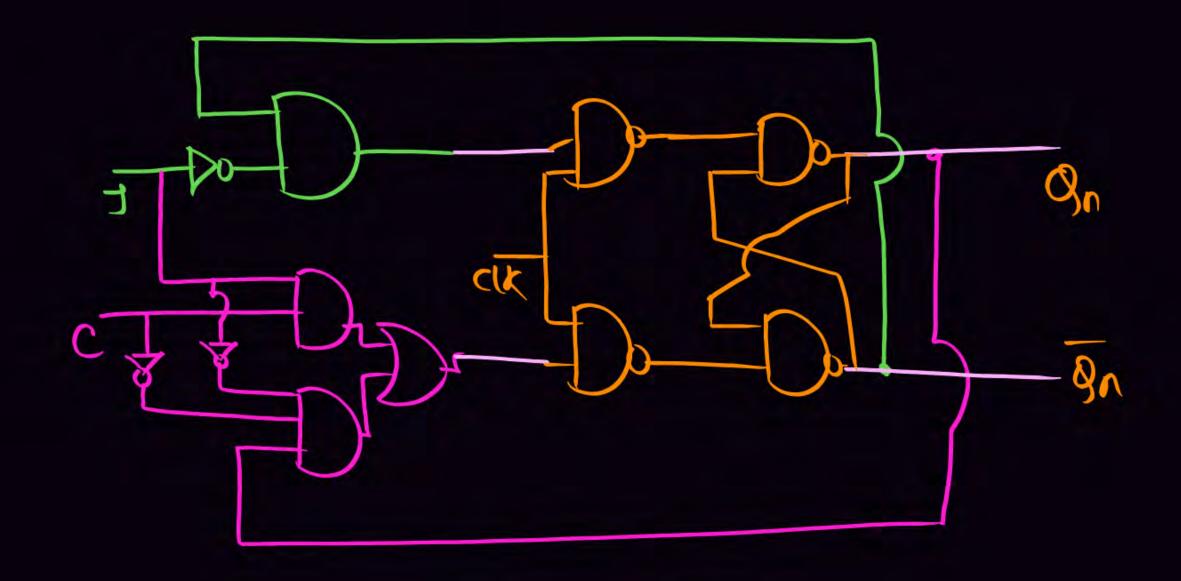






$$R = CJ + \bar{C} \bar{J} gn$$







Hive Design a VN FF by using 7-FF7.



V	N	gnti
0	0	0
0	1	1
1.	0	an
L]	1



