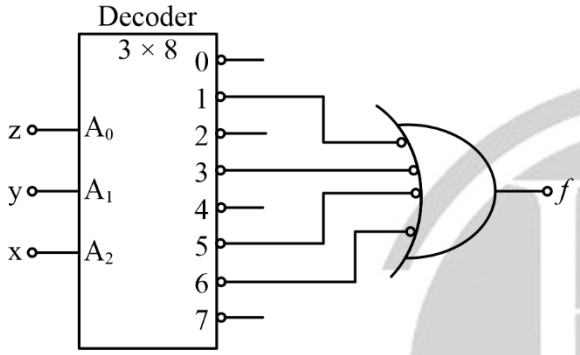
# CS & IT

## Digital Logic

**DPP-03**

### HA, FA, HS, FS

**1.** A 3 line to 8 line decoder with active low outputs, is used to realize Boolean function involving three variables x, y and z (x is MSB and z is LSB) as shown below.




The minimized Boolean function $f(x, y, z)$ in POS format, will be

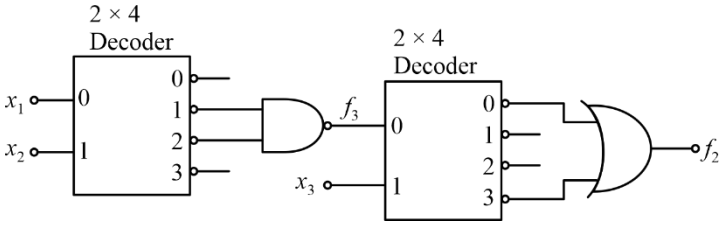
(a) $(\bar{x}+\bar{y}+\bar{z})(x+y+z)(x+\bar{y}+\bar{z})(\bar{x}+y+\bar{z})$

(b) $(\bar{x}+\bar{y}+z)(\bar{x}+y+z)(x+\bar{y}+z)(x+y+\bar{z})$

(c) $(x+z)(y+z)(\bar{x}+\bar{y}+\bar{z})$

(d) $(\bar{x}+\bar{z})(\bar{y}+\bar{z})(x+y+z)$

**2.** Two 2 × 4 decoders one with active low outputs and another with active high outputs are interconnected as shown below. The output function $f_2(x_3, x_2, x_1)$ will be




(a) $f_2 = (x_1 \oplus x_2) \odot x_3$

(b) $f_2 = (x_1 \odot_2) \odot x_3$

(c) $f_2 = (x_1 \oplus x_2) \oplus x_3$

(d) $f_2 = (x_1 \oplus x_2) \oplus x_3$

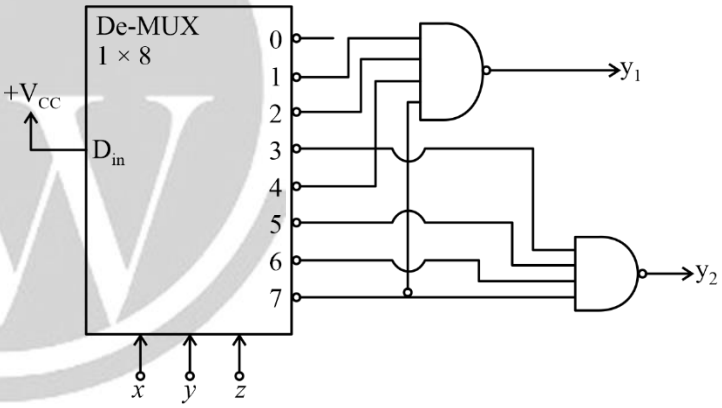
**3.** A designer has sufficient number of units of decoder with enable input of size $4 \times 2^4$ and a decoder of size $8 \times 2^8$ is to be realized. The number of units of $4 \times 2^4$ decoders, required will be

(a) 17 (b) 12

(c) 8 (d) 16

**Common date for Q.No.-4 & 5**

A demultiplexer of size 1 × 8 with active low outputs, is programmed as shown below. The circuit has three inputs x, y, z and generates to outputs $y_1$, $y_2$.




**4.** What is this circuit?

(a) Half subtractor (b) Full subtractor

(c) Half adder (d) Full adder

**5.** If de-multiplexer has active high outputs instead of active low outputs, then in order that outputs do not change

(a) NAND gates should be replaced by NOR gates

(b) NAND gates should be replaced by OR gates

(c) NAND gates should be replaced by AND gates

(d) the inputs x, y, z should be inverted

**6.** Consider the following statements.

**I.** A 2 × 4 decoder with enable input can also be used as a 1 × 4 de-multiplexer.

**II.** In order to use d-multiplexer as decoder, the select lines of de-multiplexer should be used as input lines of decoder and input line of de-multiplexer as enable input of decoder.

**III.** The de-multiplexer does many to one data operation.

Of these, the INCORRECT statements is (are)

(a) only I (b) only II

(c) only III (d) I and II

**7.** Not withstanding overflow, the addition/subtraction of k bit signed binary numbers can be realized by using k full adders and

(a) k 2-input AND (b) k 2-input OR

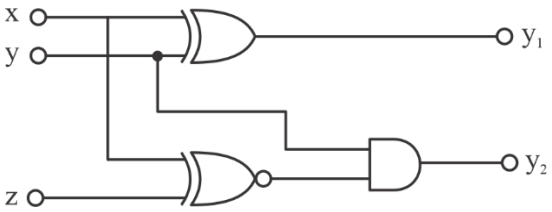
(c) k 2-input X-OR (d) k 2-input NOR

**8.** How many half adders, will be required to add two k bit numbers?

(a) 2k + 1 (b) 2k – 1

(c) 2k (d) 2(k + 1)

**9.** The circuit shown below, is a controlled half adder/ half subtractor. The inputs to half adder/ half subtractor are x and y while z is a control. The outputs are y1 and $y_2$.



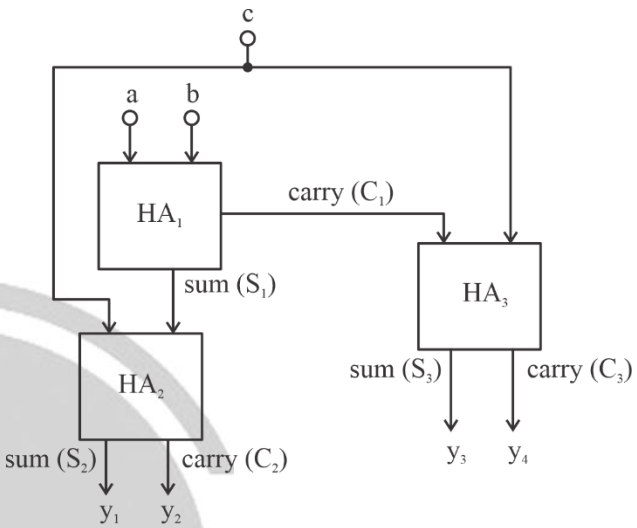

(a) Half adder for z = 0

(b) Half subtractor for z = 1

(c) Half adder for z = 1 and half subtractor for z = 0

(d) Half adder regardless of whether z = 0 or z = 1 due to design defect.

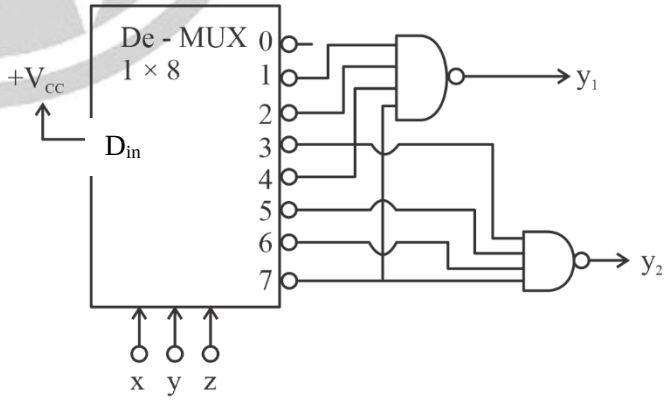
**10.** Three half adders $HA_1$, $HA_2$ and $HA_3$ are inter-coupled as shown below. The four output functions $y_1$, $y_2$, $y_1$ and y4 are expressed in terms of inputs a, b and c. Which one of the following output expressions, is correct?




(a) $y_1 = (a \oplus b)c$ (b) $y_2 = (a \oplus b) \oplus c$

(c) $y_3 = ab \oplus c$ (d) $y_4 = a(b \oplus c)$

**11.** A demultiplexer of size 1×8 with active low outputs, is programmed as shown below. The circuit has three inputs $x_4$ y, z and generates two outputs $y_1$, $y_2$.

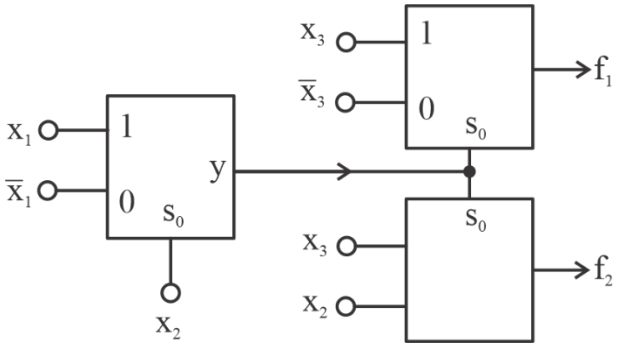



What is circuit?

(a) Half subtracter (b) Full subtractor

(c) Half adder (d) Full adder

**Statement for question 12 & 13.**




**12.** The function $f_1$ and $f_2$ are

(a) $f_1 = (x_1 \oplus x_2)x_3$ and $f_2 = x_1\bar{x}_2 + x_1\bar{x}_3 + x_2x_3$

(b) $f_1 = x_1 \oplus x_2 \oplus x_3$ and $f_2 = \overline{x_1}x_2 + \overline{x_1}x_3 + x_2x_3$

(c) $f_1 = \overline{(x_1 \oplus x_2 \oplus x_3)}$ and $f_2 = x_1x_2 + x_1x_3 + x_2x_3$

(d) $f_1 = x_1(x_2 \oplus x_3)$ and $f_2 = x_1x_2 + x_1x_3 + \overline{x_2}\,\overline{x_3}$

**13.** What is this circuit?

(a) Full adder

(b) Full subtractor

(c) Magnitude comparator

(d) Priority encoder

**14.** Minimum number of NAND gate required to implements half subtractor?

**15.** Minimum number of NAND gate required to implements full subtractor?

# Answer Key

1. (c)
2. (a)
3. (a)
4. (d)
5. (b)
6. (c)
7. (c)
8. (b)
9. (c)
10. (c)
11. (d)
12. (b)
13. (b)
14. (5)
15. (9)

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