CS & IT ENGINEERING

DIGITAL LOGIC

HA, FA,HS,FS

Lecture No. 03

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01 HA FA

02 QUESTION PRACTICE

03 HS FS

04 QUESTION PRACTICE

05 DISCUSSION

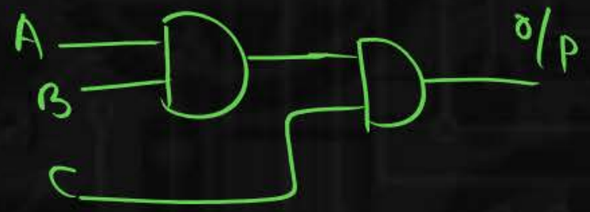
Combinational Circuit

↳ A circuit without memory or feedback.

↳ Combinational circuit is a circuit in which o/p will depends only on present state of input.

↳ Static circuit.

Ex.



Combinational Circuit

Designing of Combinational circuit

- Step 1 : Find the number of i/ps and o/ps.
- Step 2: Write the truth table.
- Step 3: Write the Logical expression.
- Step 4: Minimization
- Step 5: Hardware Implementation.

Q Design a Half adder ?

Two bit adder

0	0	1	1
+ 0	+ 1	+ 0	+ 1
0 0	0 1	0 1	1 0

Carry Sum

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HALF ADDER

0	0	1	1
+0	+1	+0	+1
00	01	01	10

- Two bit adder are known as half adder.

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HALF ADDER

Step 1: Number of inputs and O/ps.

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HALF ADDER

Step 2: Truth Table.

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$Sum = \bar{A}B + A\bar{B}$

$= A \oplus B$

$Carry = A \cdot B$ ✓

HA, FA, HS, FS

HALF ADDER

Step 3: Logical expression

$$\text{sum} = \overline{A}B + A\overline{B} = A \oplus B$$

$$\text{carry} = AB$$

Step 4: Minimization

→ Already minimized

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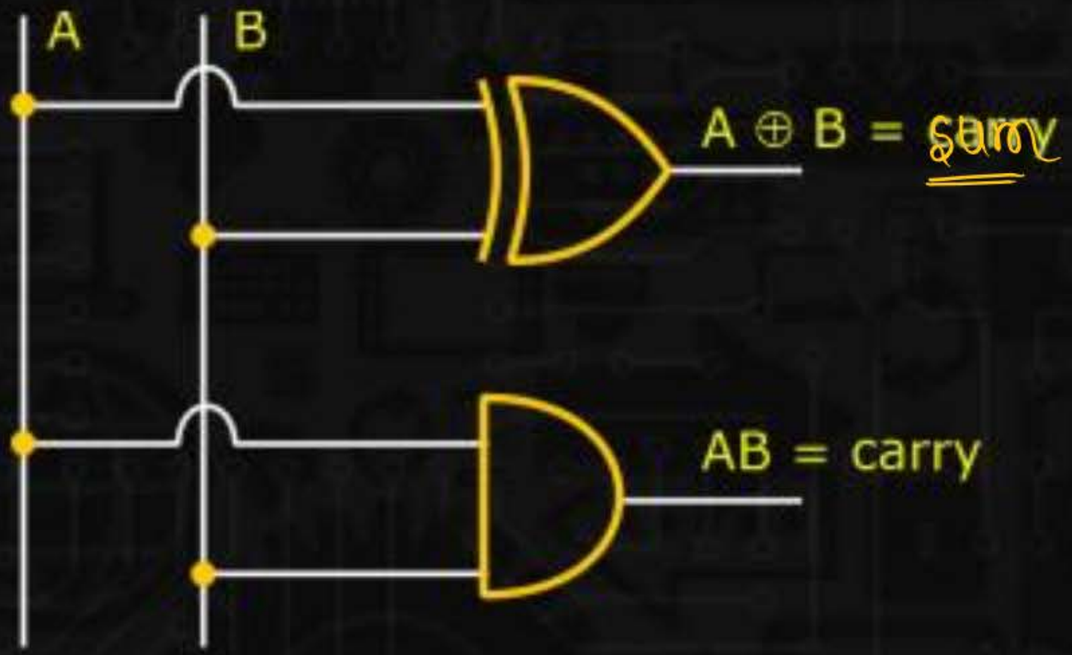
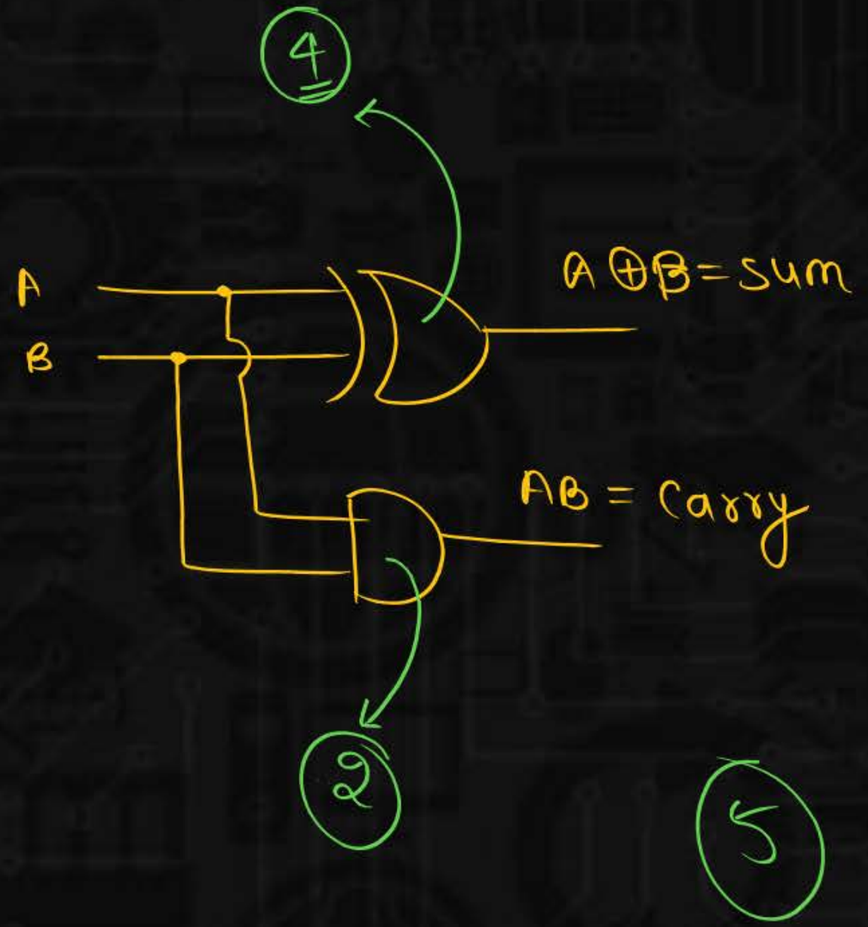
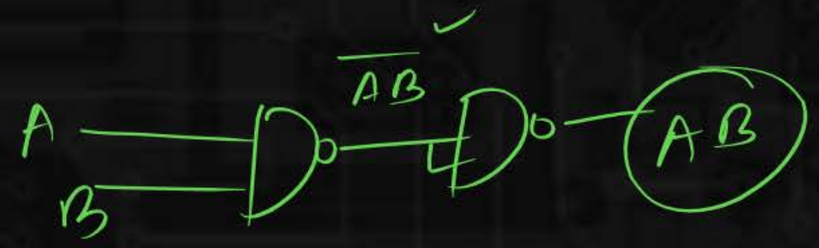
HALF ADDER

Step 5: Hardware Implementation

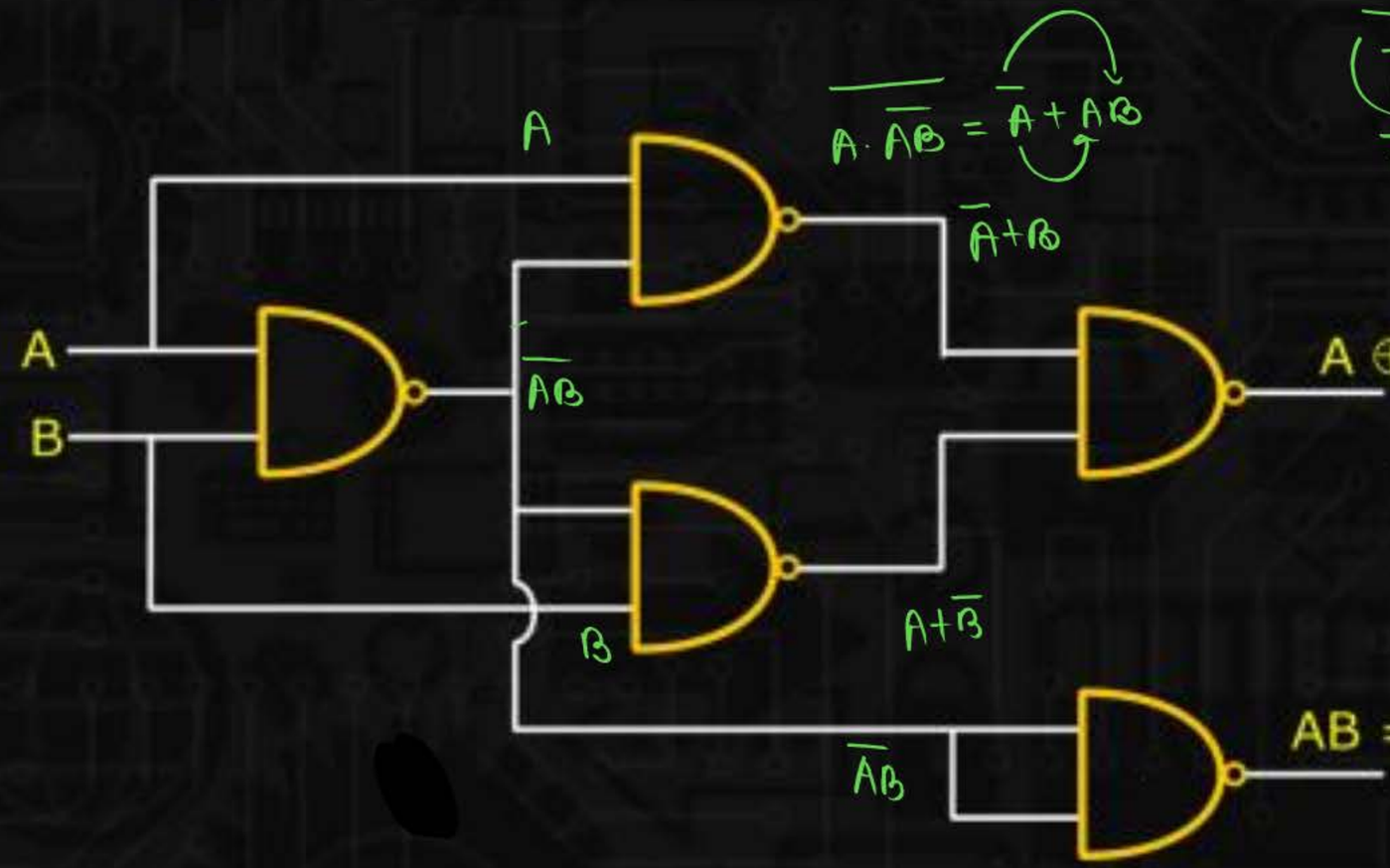




HA, FA, HS, FS



By NAND GATE



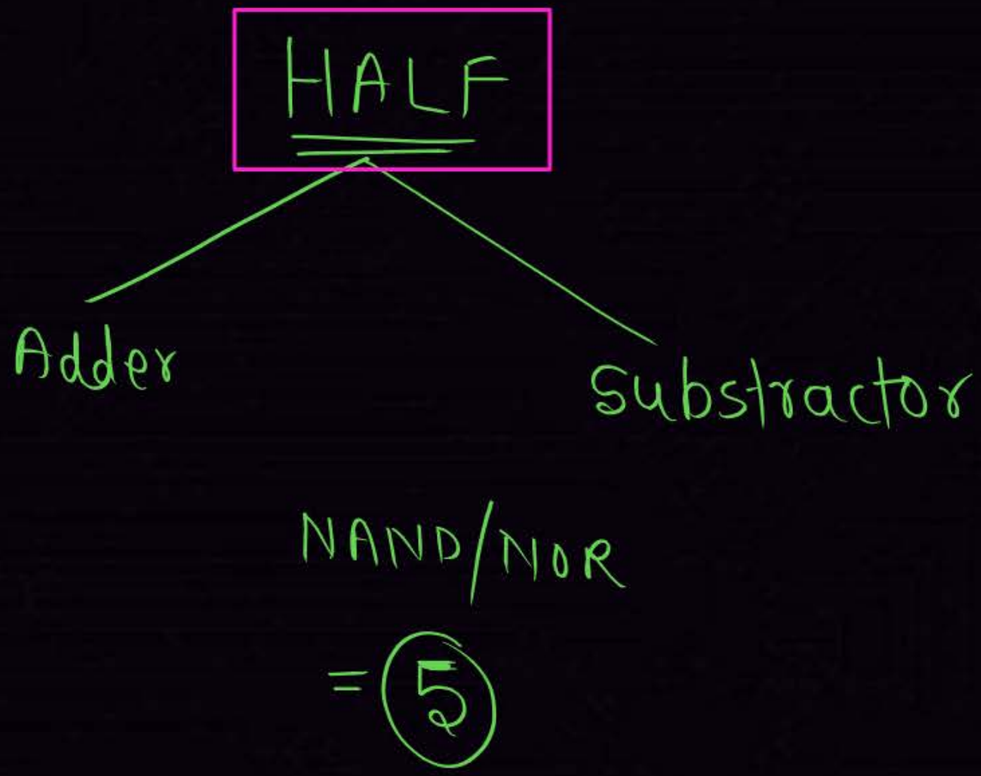
$\overline{A \cdot \overline{AB}} = \overline{A} + AB$

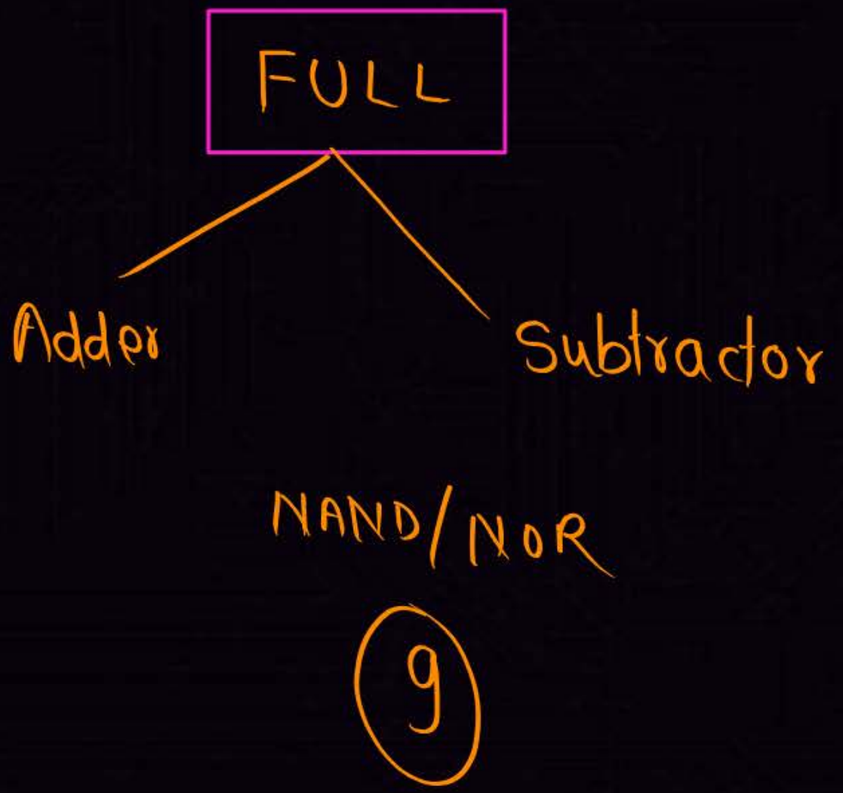
$\overline{(\overline{A}+B)\cdot(A+\overline{B})}$

$\overline{\overline{A}+B} + \overline{A+\overline{B}}$

$A\overline{B} + \overline{A}B = A \oplus B = \text{Sum}$

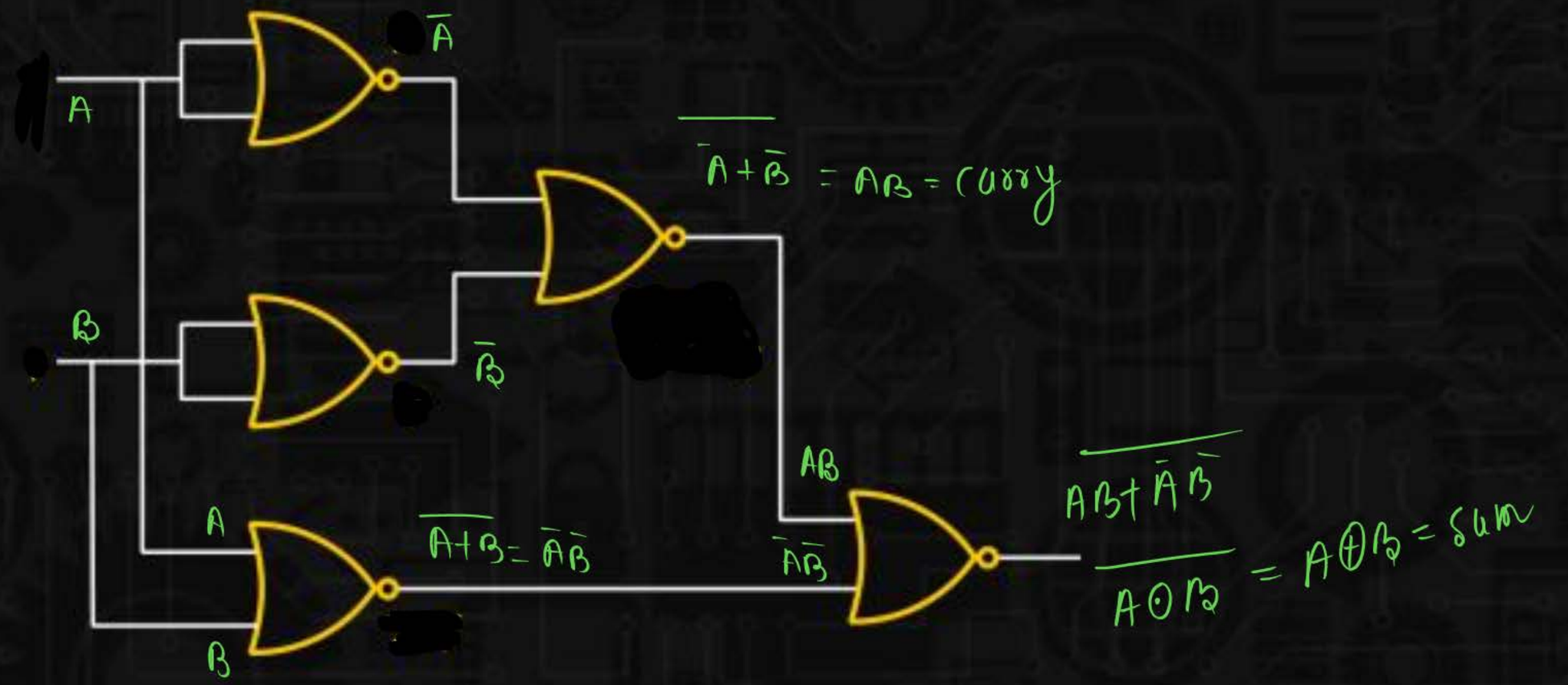
NOTE


HALF
Adder
Substractor
NAND/NOR
= 5


FULL
Adder
Subtractor
NAND/NOR
9

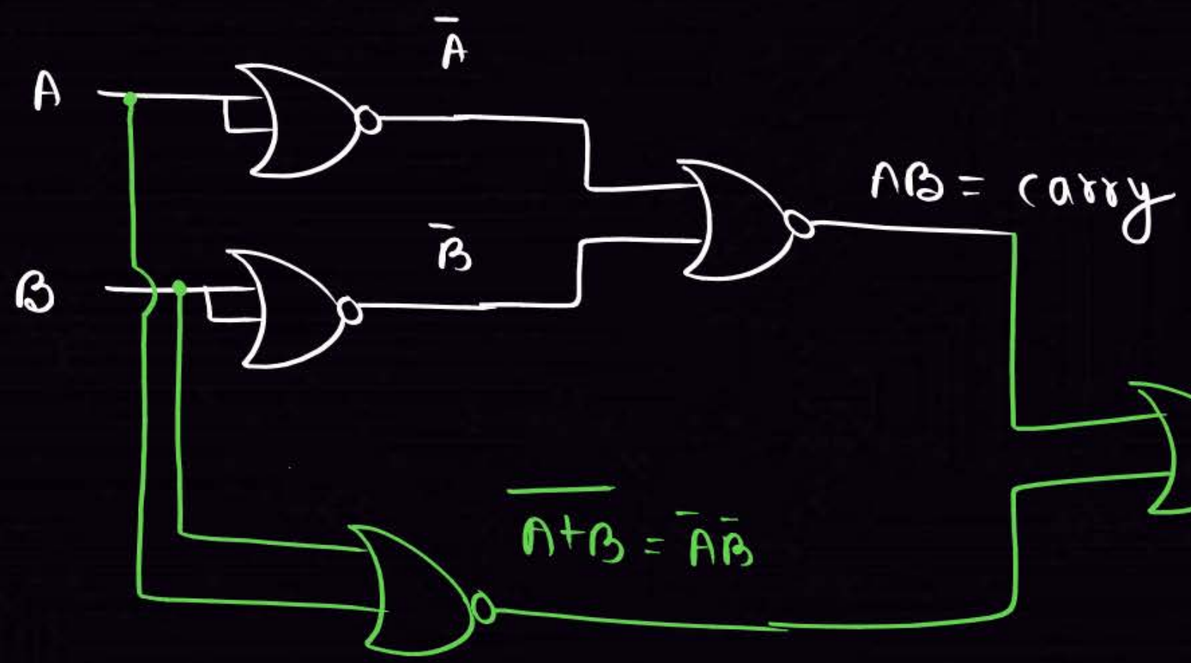
HA, FA, HS, FS

By NOR GATE



Sum = $A \oplus B$

Carry = AB

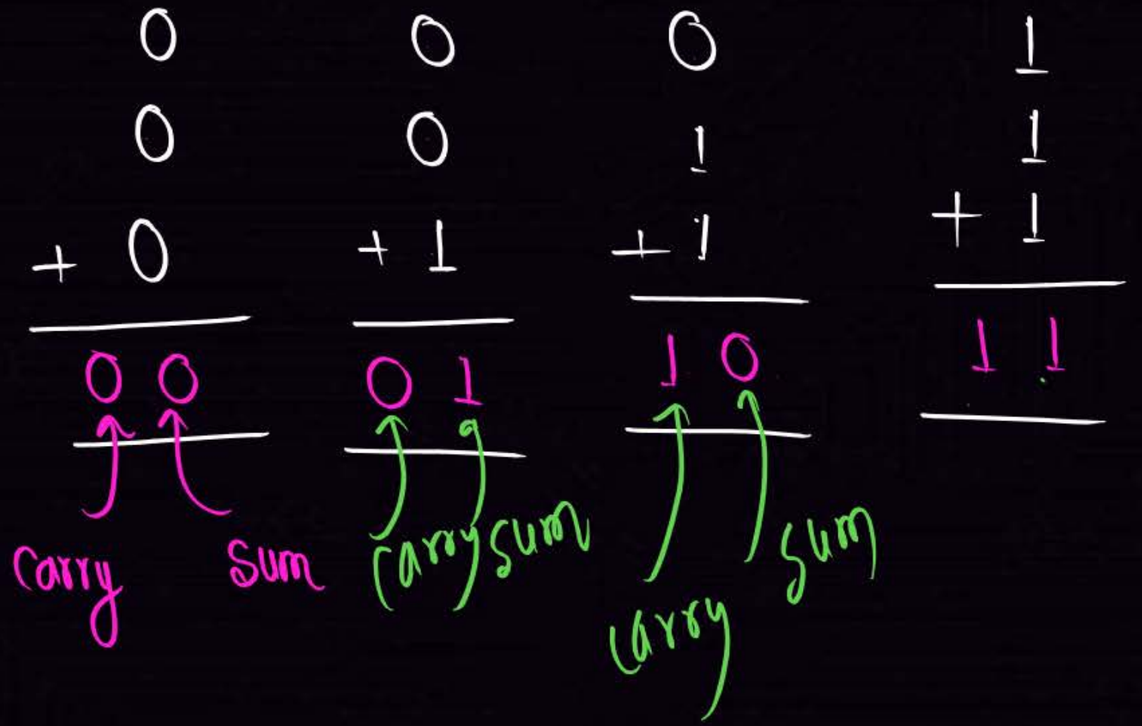


(5) ✓

$\overline{AB+\bar{A}\bar{B}} = \overline{A \odot B} = A \oplus B$

= sum

Full adder



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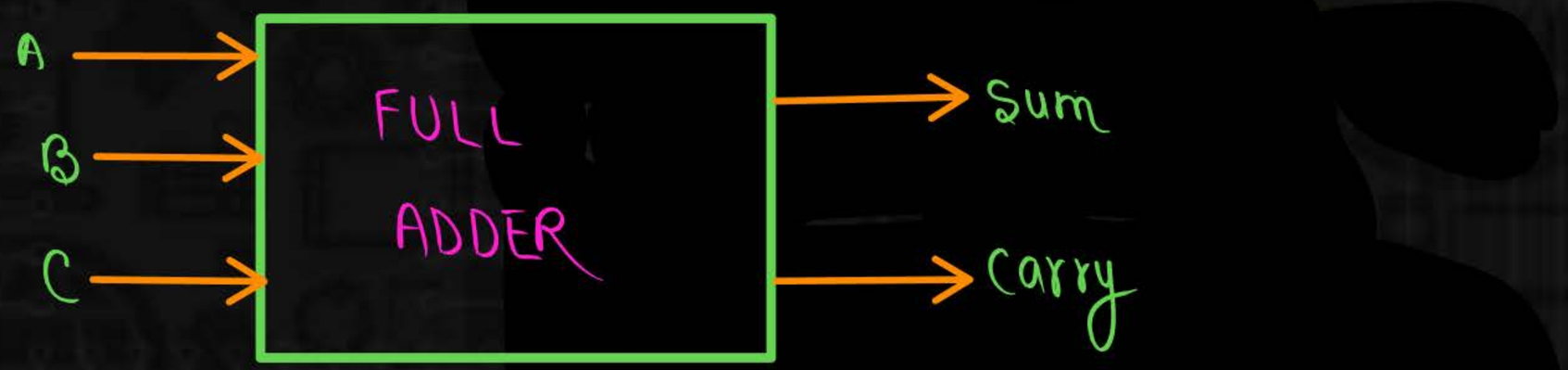
FULL ADDER

Three bit adder are known as full adder

Step 1:



HA, FA, HS, FS

majority high logic

Step 2:

Decimal	A	B	C	Sum	Carry
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

HA, FA, HS, FS

FULL ADDER

Step 3: Sum (A, B, C) = $\Sigma m(1,2,4,7)$

$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= A \oplus B \oplus C$

Carry (A, B, C) = $\Sigma m(3,5,6,7)$

$= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$

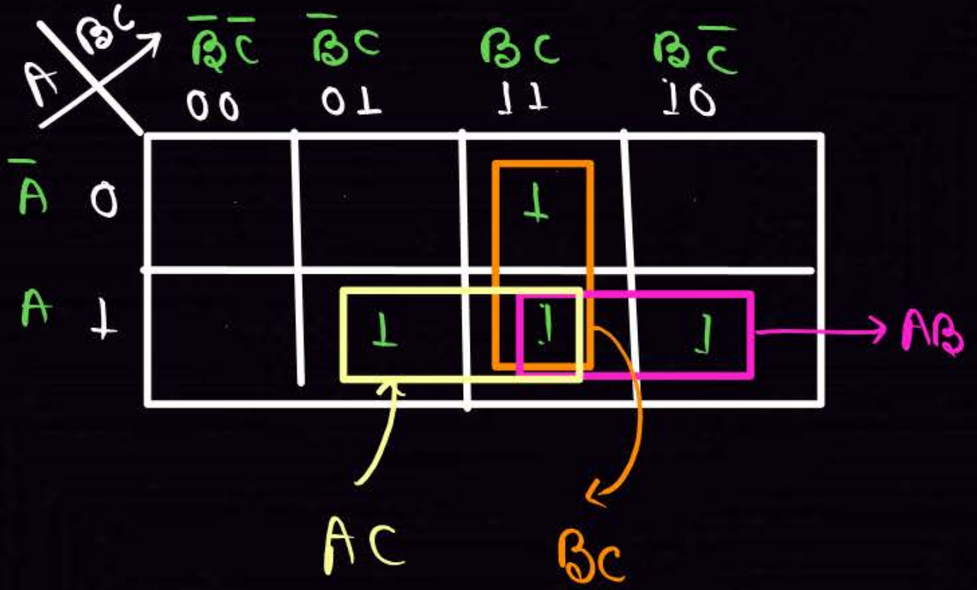
$= (\bar{A}B + A\bar{B})C + AB(\bar{C} + C)$

$= (A \oplus B)C + AB$

Step 4 :→ Minimization

$$Sum = A \oplus B \oplus C$$

$$Carry = \Sigma m(3,5,6,7)$$



$$Carry = AB + BC + AC$$

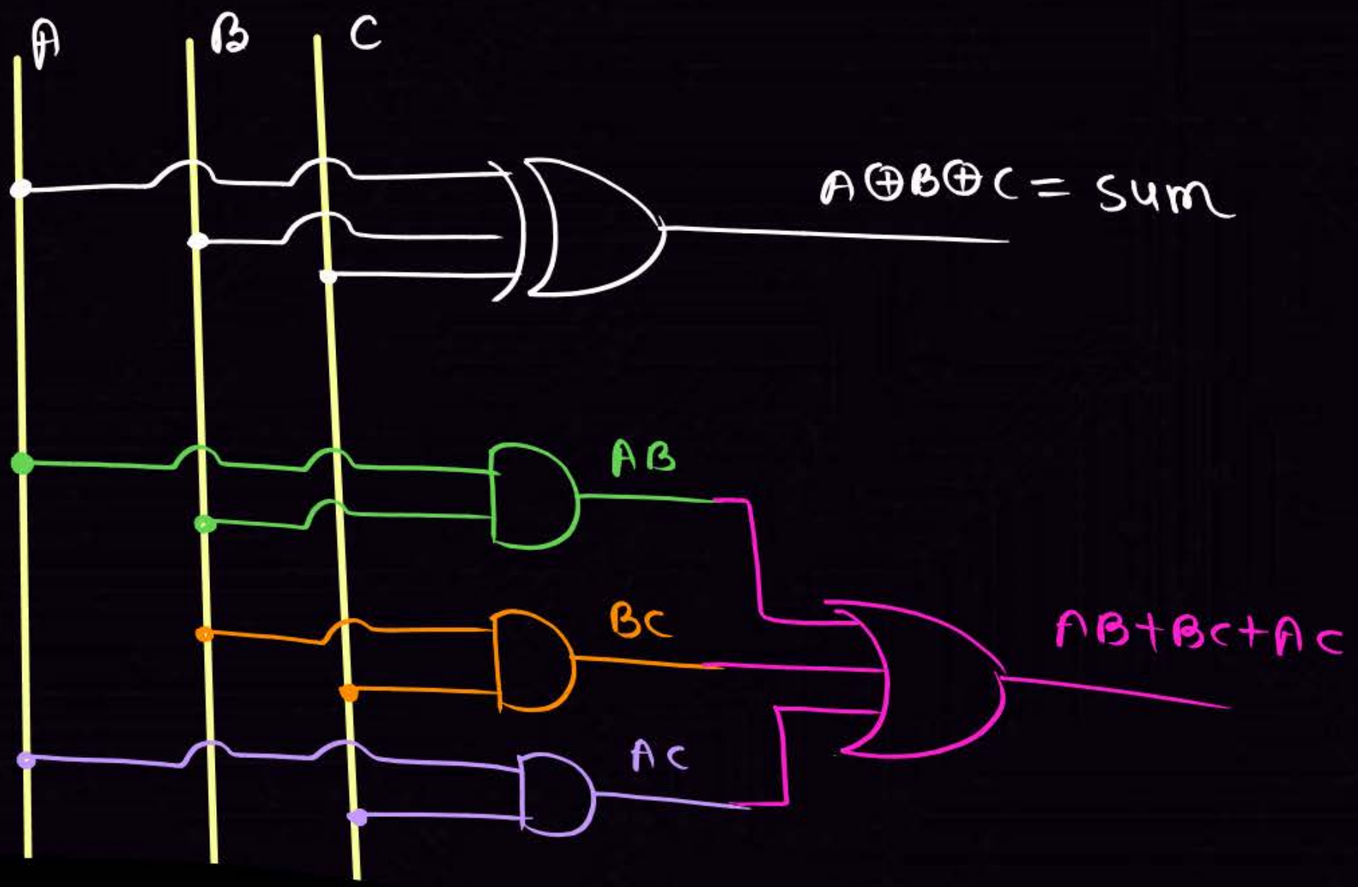
$$\text{Sum} = A \oplus B \oplus C = \Sigma m(1,2,4,7) = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

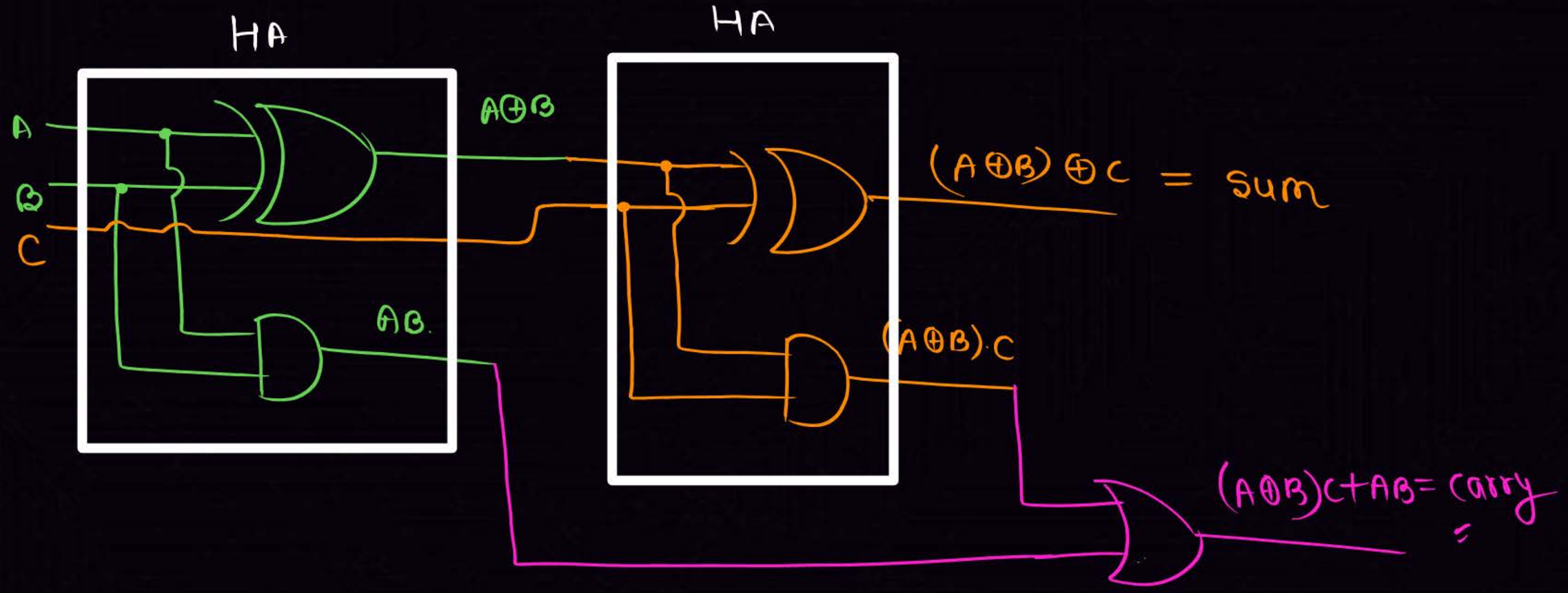
$$\text{Carry} = \Sigma m(3,5,6,7)$$

$$= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC \leftarrow \text{non minimized}$$

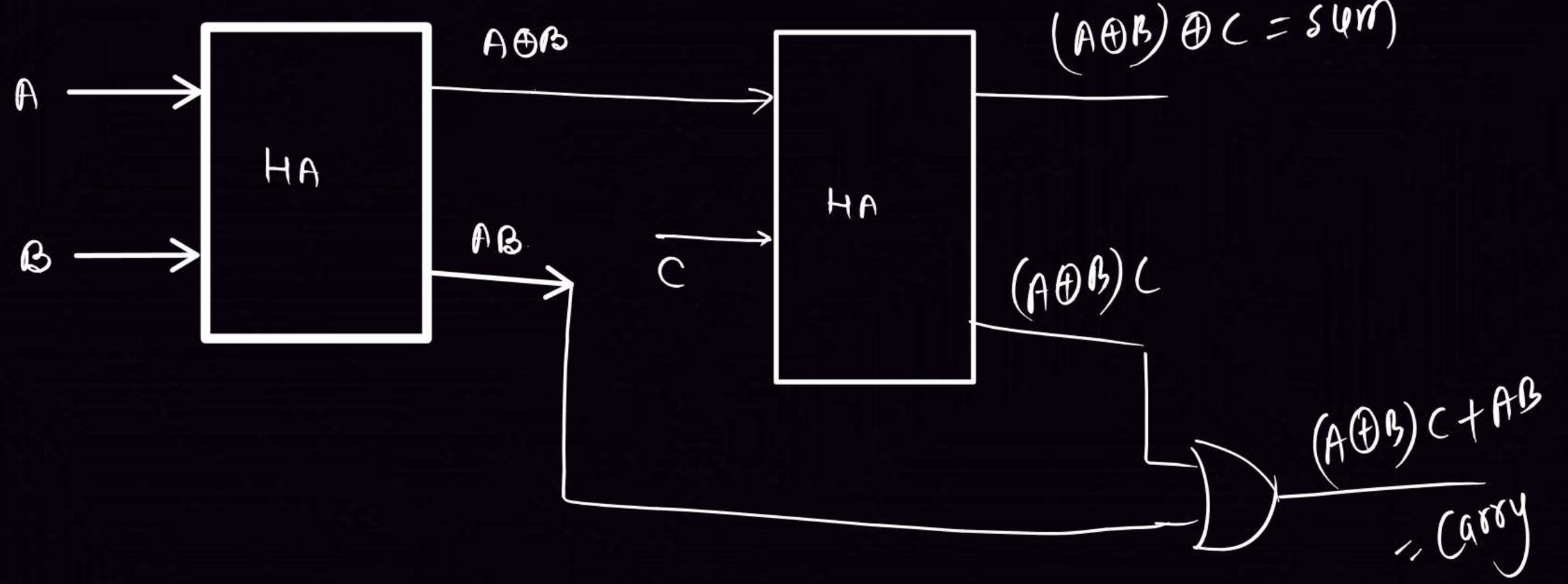
$$= (A \oplus B)C + AB \longrightarrow \text{Semiminimized}$$

$$= AB + BC + AC \longrightarrow \text{minimized}$$


A
B
C
A⊕B⊕C = sum
AB
BC
AC
AB+Bc+Ac



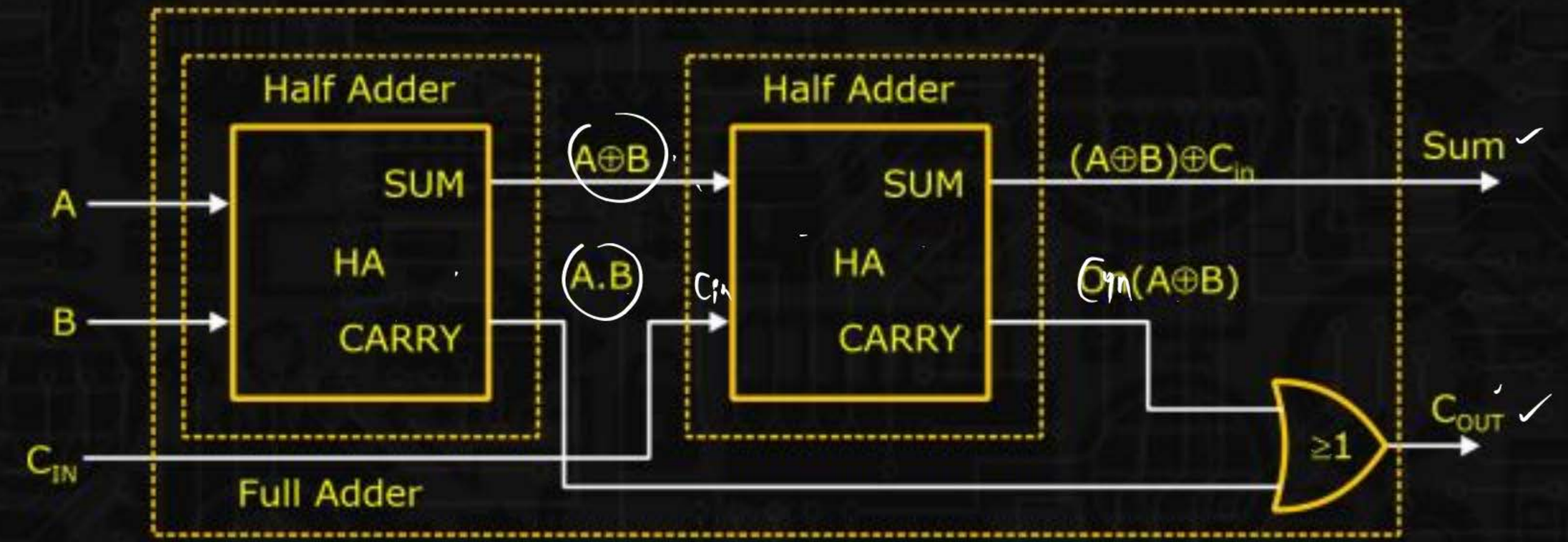
1 Full Adder = 2 HA + 1 OR


A
B
HA
A⊕B
AB
C
HA
(A⊕B)⊕C = sum
(A⊕B)C
(A⊕B)C+AB
= Carry

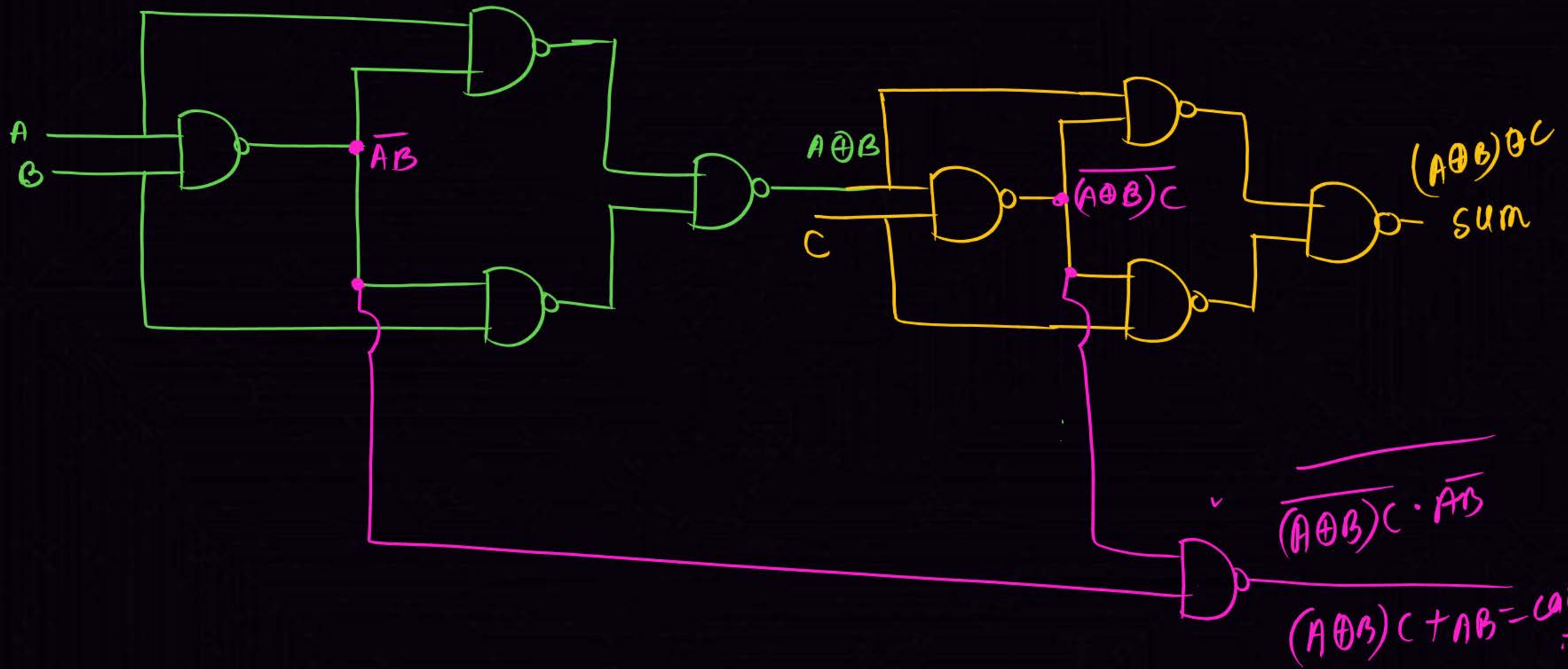
HA, FA, HS, FS

FULL ADDER

Step 5:



By NAND GATE


A
B
$\overline{AB}$
$A \oplus B$
C
$\overline{(A \oplus B)C}$
$(A \oplus B) \oplus C$
SUM
$\overline{\overline{(A \oplus B)C} \cdot \overline{AB}}$
$(A \oplus B)C + AB$ = carry

Full ADDER

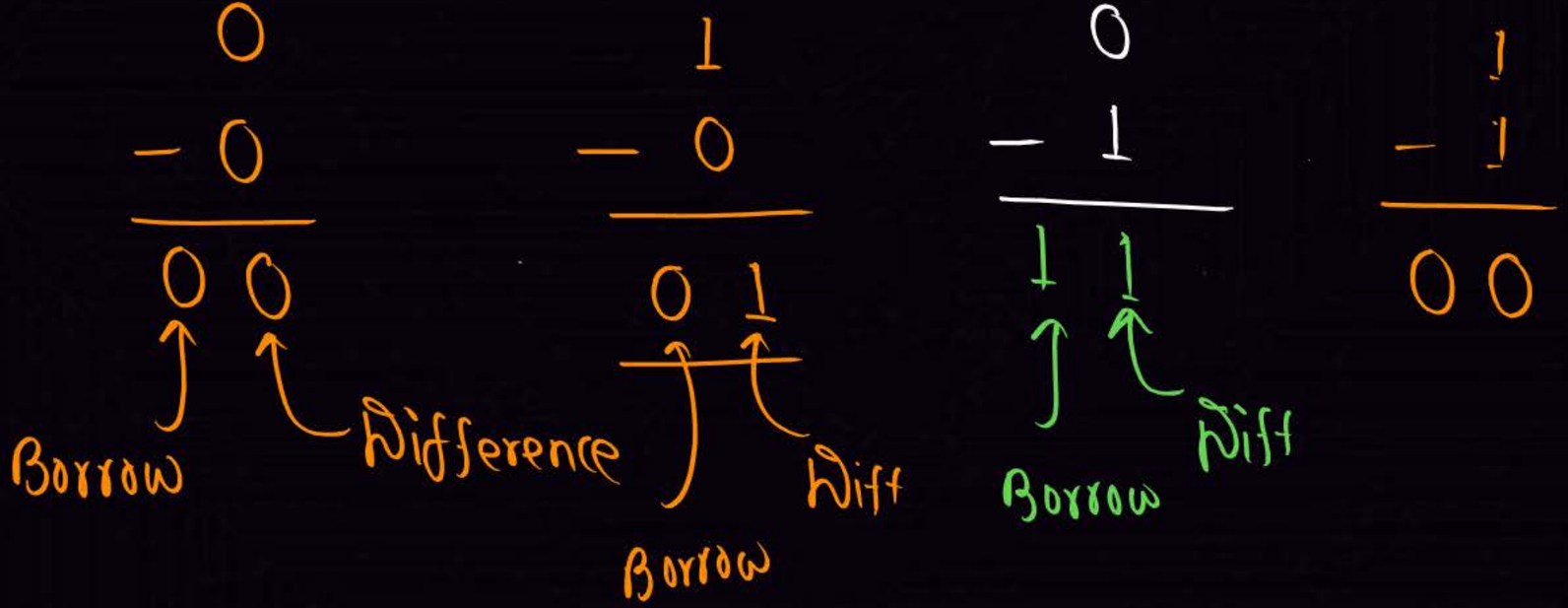
→ (9) NOR GATE

minimum

→ H.W.

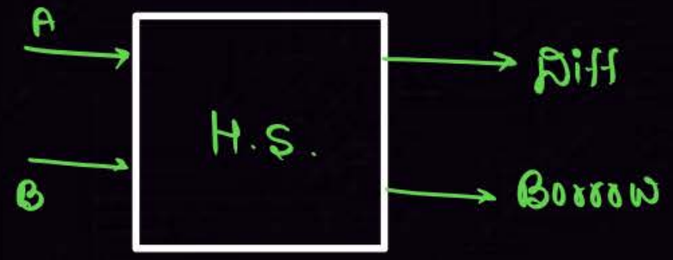
HALF SUBTRACTOR :→

↳ Two bit subtractor



HALF SUBTRACTOR :→

Step 1.



Step 2.

A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

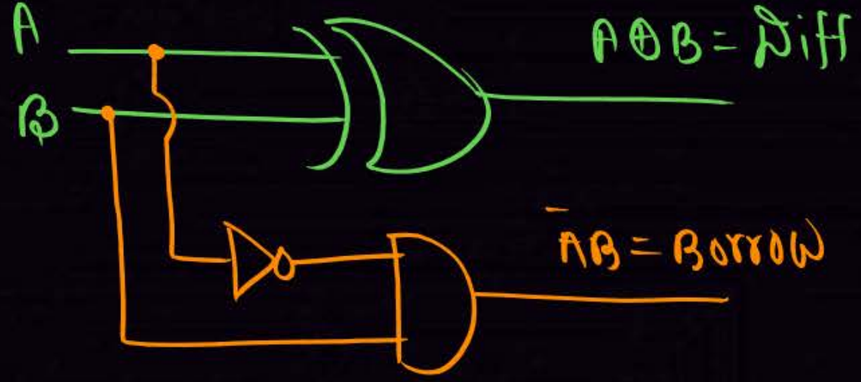
Step 3.: $Diff = \bar{A}B + A\bar{B}$

$= A \oplus B$

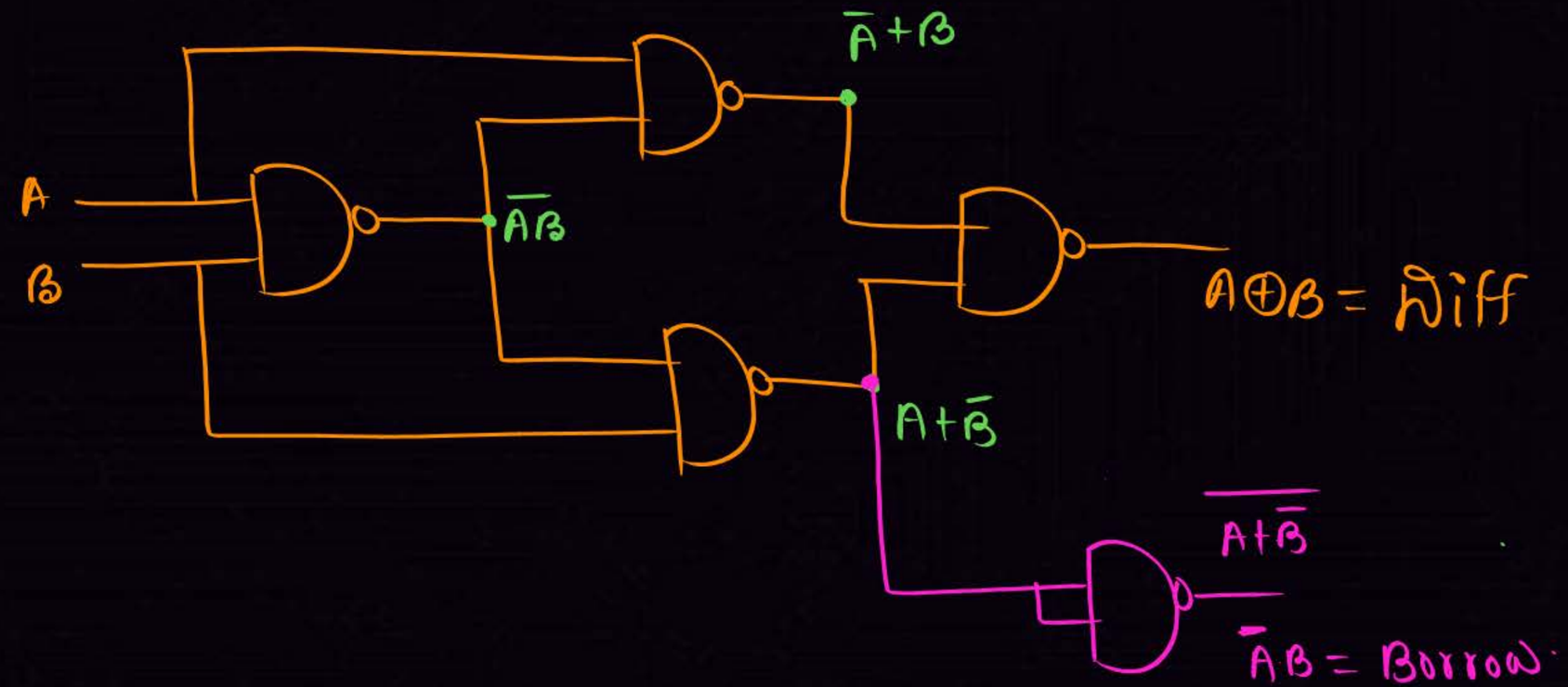
$Borrow = \bar{A}B$

Step 4 Minimization.

Step 5: Hardware Implementation

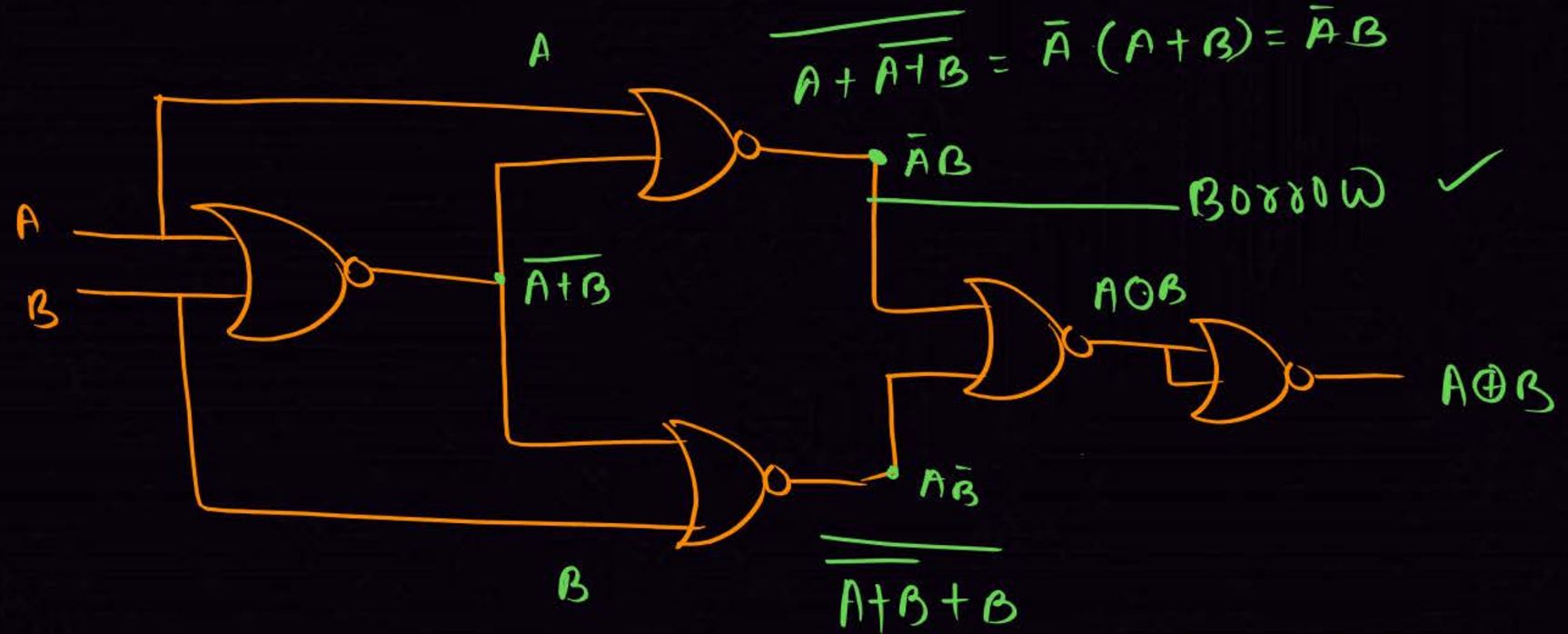


By NAND GATE :→


A
B
$\bar{A}B$
$\bar{A}+B$
$A+\bar{B}$
$A \oplus B$ = Diff
$\overline{A+\bar{B}}$
$\bar{A}B$ = Borrow

HW.

By NOR = ?


A
B
A
B
$\overline{A+B}$
$\overline{A+\bar{A}B} = \bar{A}(A+B) = \bar{A}B$
$\bar{A}B$
Borrow
$A \odot B$
$A \oplus B$
$A\bar{B}$
$\overline{\overline{A+B}+B}$


THANK YOU GW
SOLDIERS !