CS & IT ENGINEERING

DIGITAL LOGIC

Sequential circuit

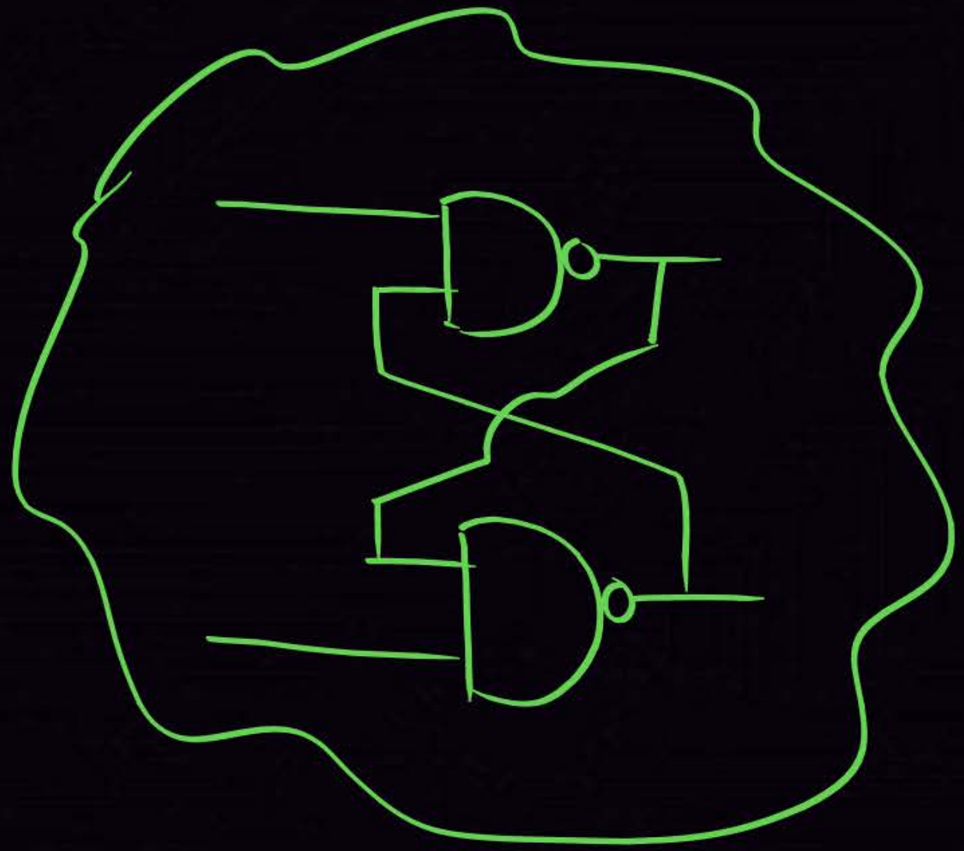
Lecture No. 3

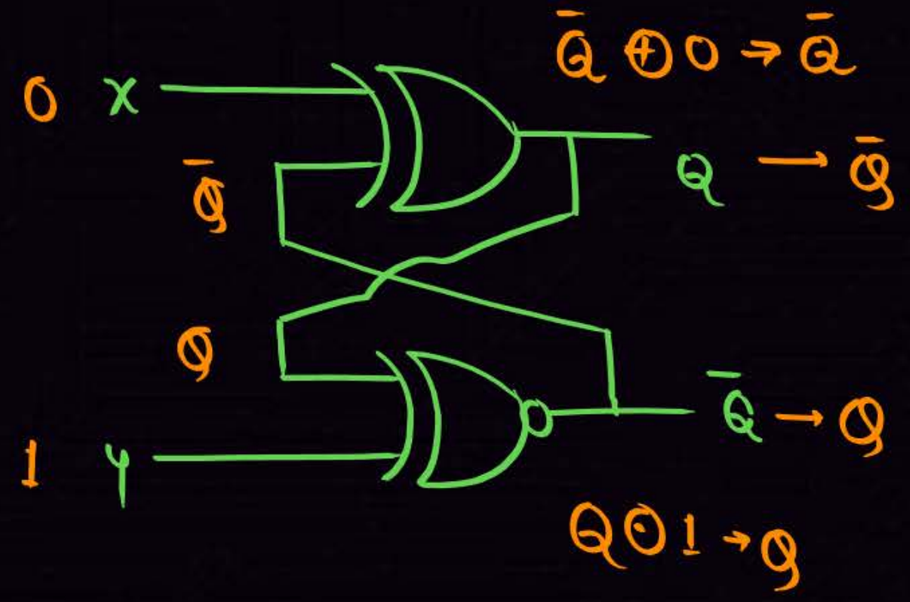
By- CHANDAN SIR

01 FFs

02 Practice

03 Discussion





X	Y	Q	$\bar{Q}$	
0	0	$\bar{Q}$	$\bar{Q}$	→ Invalid condition.
0	1	$\bar{Q}$	Q	→ Toggle
1	0	Q	$\bar{Q}$	→ HOLD / MEMOR / Previous state.
1	1	Q	Q	→ Invalid forbidden don't care.

X-OR

$Q \oplus Q = 0$

$Q \oplus 0 = Q$

$\bar{Q} \oplus 0 = \bar{Q}$

$Q \oplus \bar{Q} = 1$

$Q \oplus 1 = \bar{Q}$

$\bar{Q} \oplus 1 = Q$

X-NOR

$Q \odot Q = 1$

$Q \odot 1 = Q$

$\bar{Q} \odot 1 = \bar{Q}$

$Q \odot \bar{Q} = 0$

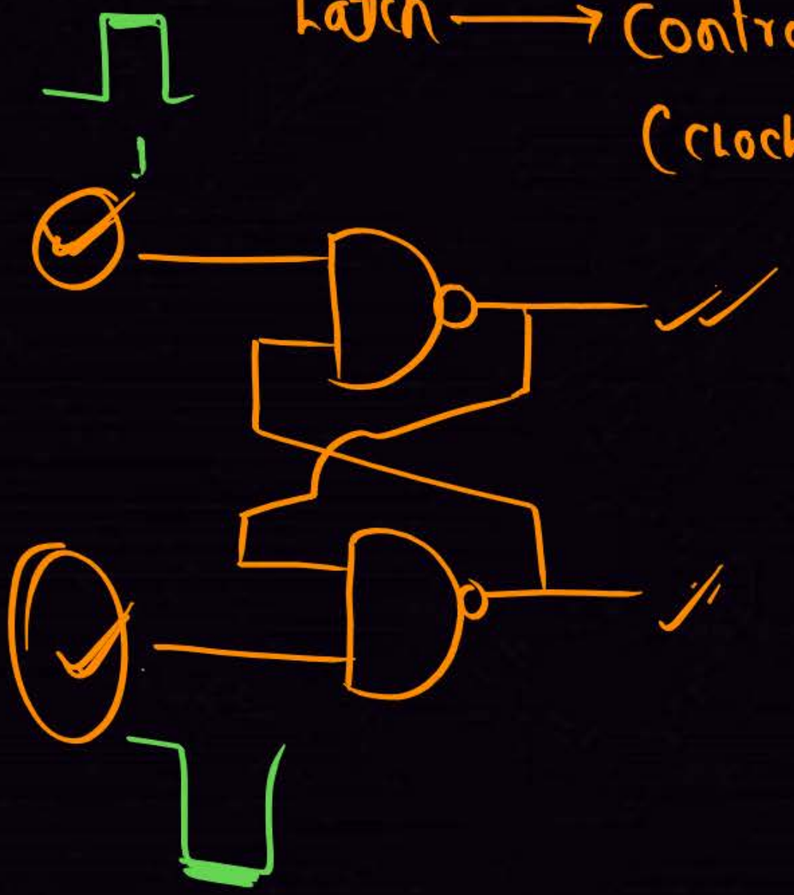
$Q \odot 0 = \bar{Q}$

$\bar{Q} \odot 0 = Q$

Level sensitive.

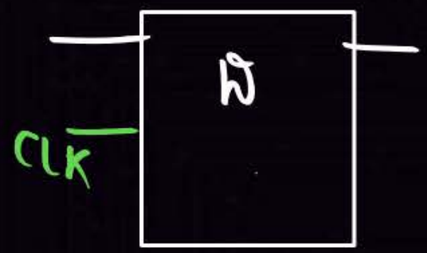
Latch ⟶ Control (clock) ⟶ Flip-Flop

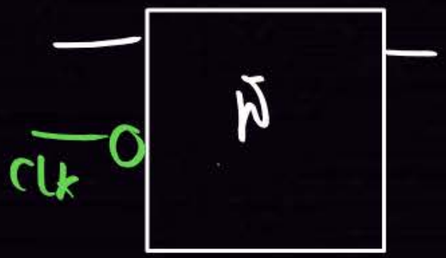
Edge sensitive.

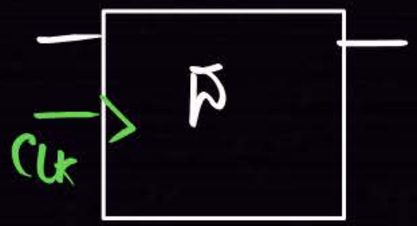


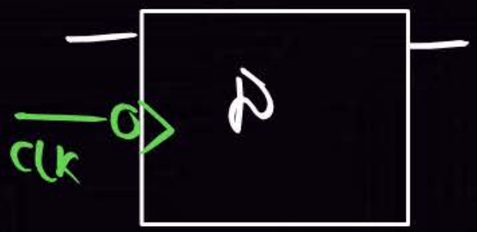
Triggering

- Level triggered
  - +ve Level
    - "1"
  - -ve Level
    - "0"
- Edge triggered
  - +ve edge
    - 0→1
  - -ve edge
    - 1→0



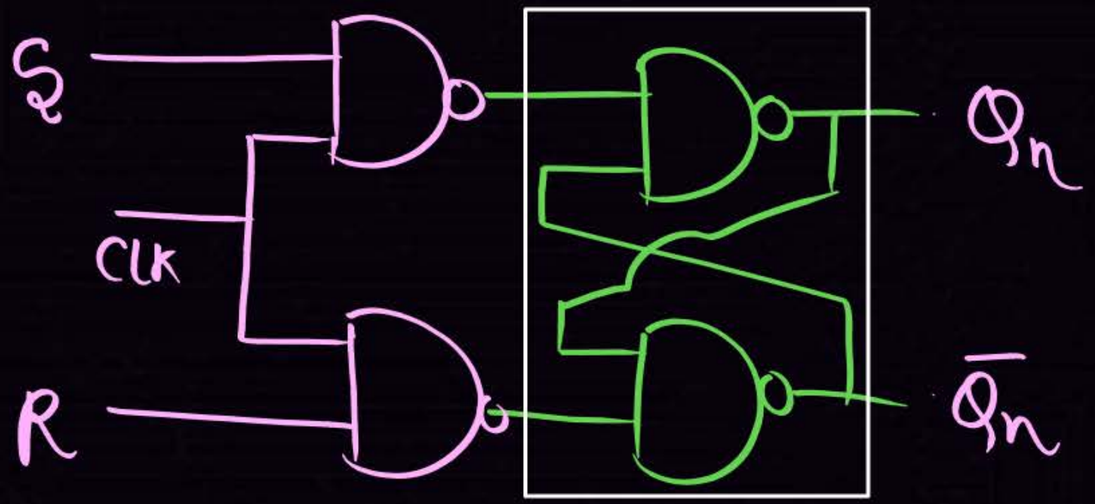


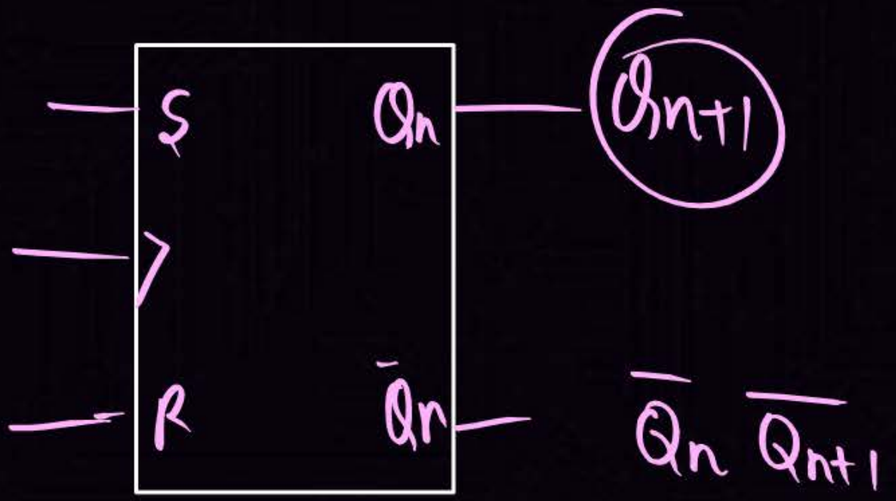


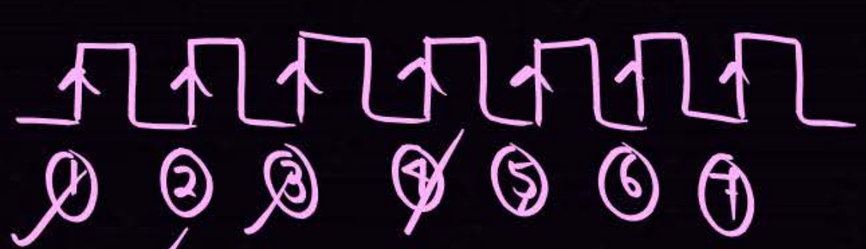


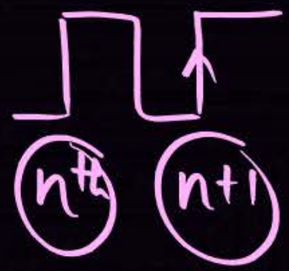
S R · Flip · Flop

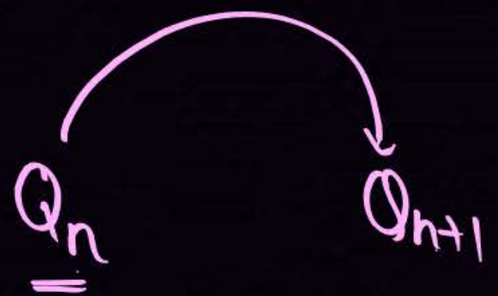
Q_1 Q_2 Q_3 Q_4 ..... Q_n Q_{n+1}










Q_n
Q_{n+1}

① Circuit Diagram / Symbol

② Truth Table.

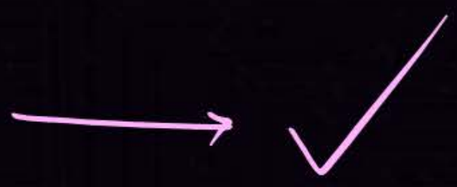
③ Characteristic Table.

④ Characteristic Equation

⑤ Excitation Table.

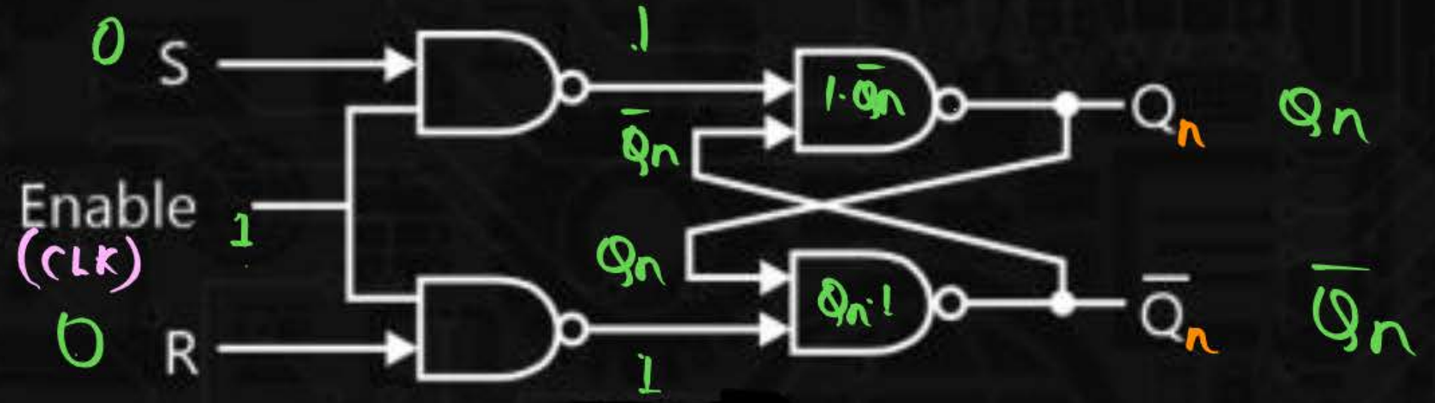
⑥ State Diagram

SR FF
JK FF
D FF
T FF



(1) SR FLIP-FLOP [SET RESET FF]

(i) Circuit Diagram :



(ii) Truth Table :

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	
0	0	Q_n	$\bar{Q}_n$	→ HOLD
0	1	0	1	RESET.
1	0	1	0	SET.
1	1	X	X	InValid

SR FLIP-FLOP [SET RESET FF]

$Q_{n+1}(S,R,Q_n) = \Sigma m(1,4,5) + \Sigma d(6,7)$

(iii) Characteristic Table:

	S	R	Q_n	Q_{n+1}
0→	0	0	0	0
1→	0	0	1	1
2→	0	1	0	0
3→	0	1	1	0
4→	1	0	0	1
5→	1	0	1	1
6→	1	1	0	X
7→	1	1	1	X

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

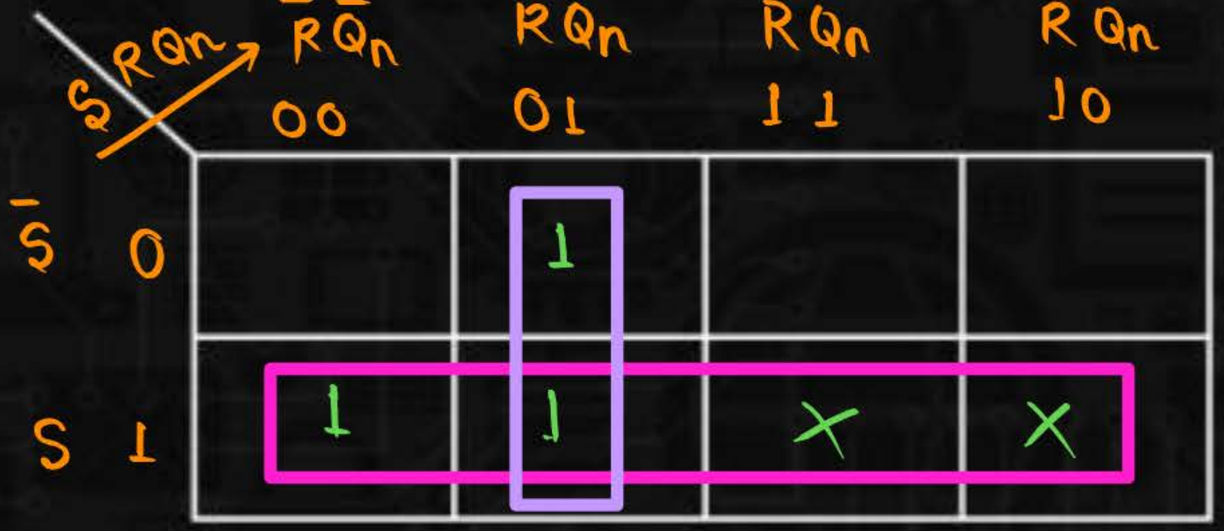
S=0, R=0 } $Q_{n+1} = Q_n$

S=0, R=1 } $Q_{n+1} = 0$

S=1, R=0 } $Q_{n+1} = 1$

SR FLIP-FLOP [SET RESET FF]

(iv) Characteristic equations



$$Q_{n+1} = S + \bar{R}Q_n$$

SR FLIP-FLOP [SET RESET FF]

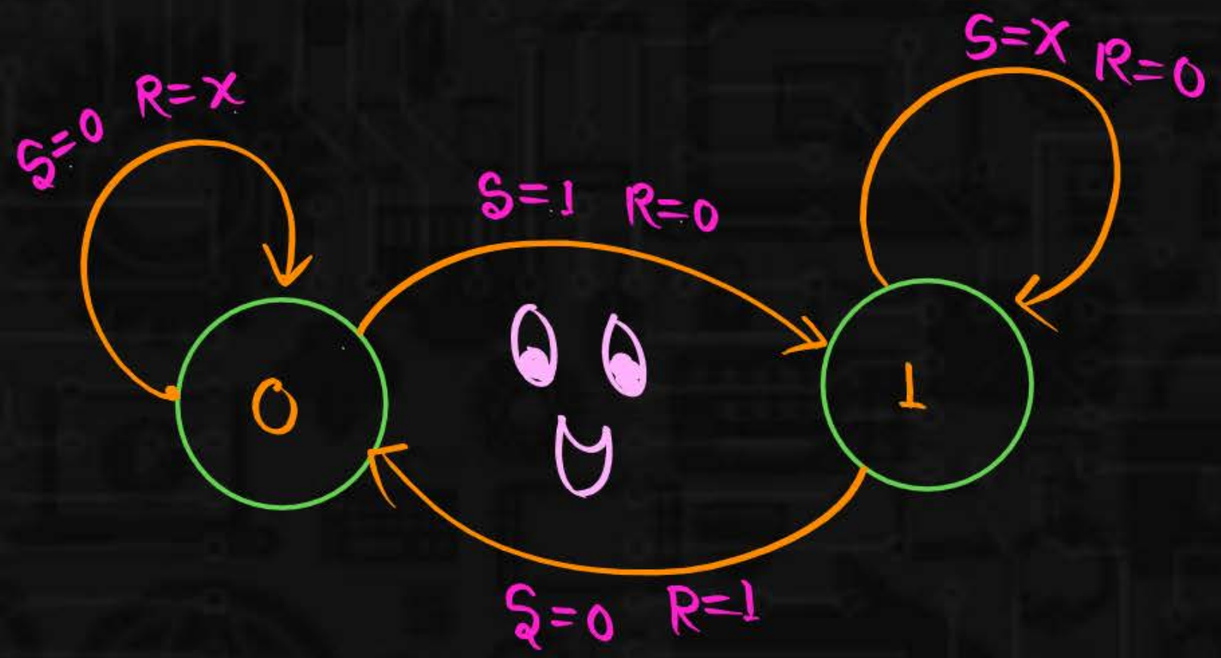
(v) Excitation Table

Qn	Qn+1	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

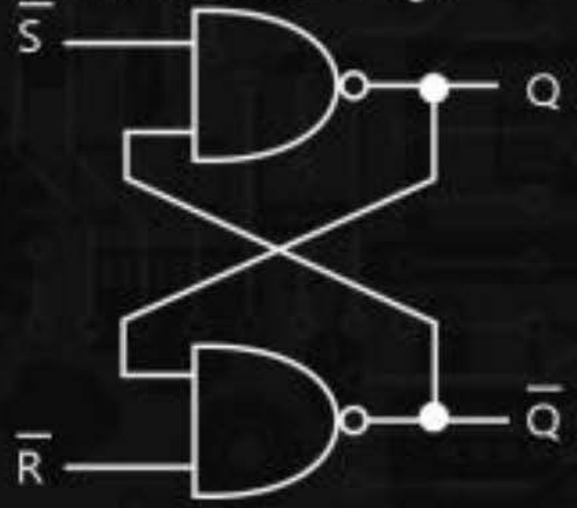
SR FLIP-FLOP [SET RESET FF]

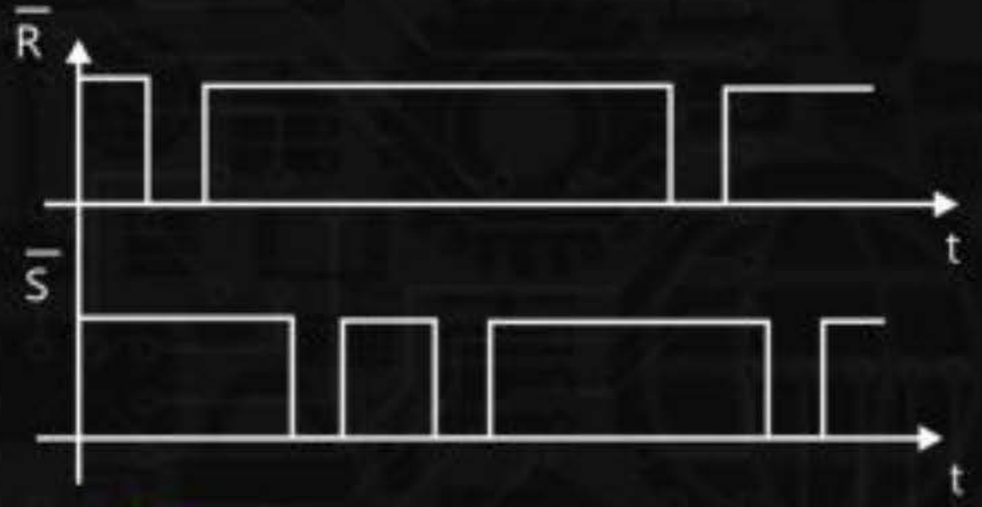
(vi) State Diagram :



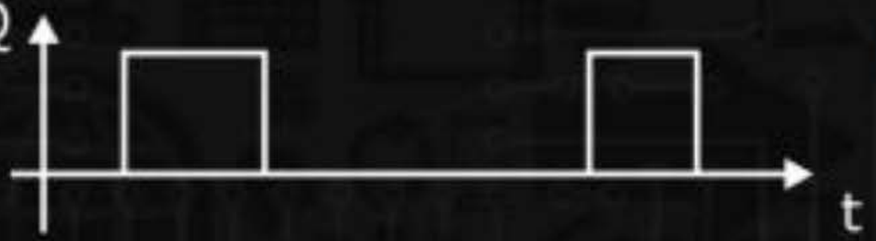
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Q. The $\bar{S}$ and $\bar{R}$ inputs shown in the figure are applied toa NAND latch. Assuming the Q is 0 initially, which plot gives correct waveform for Q?

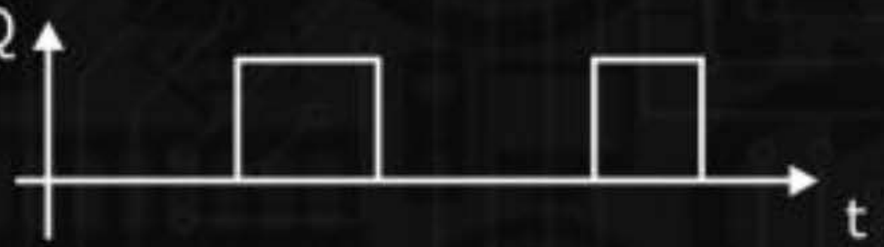




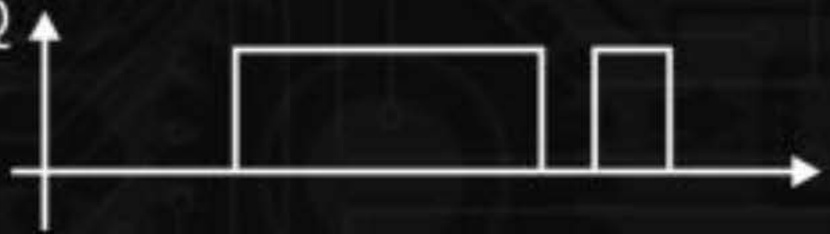
A.



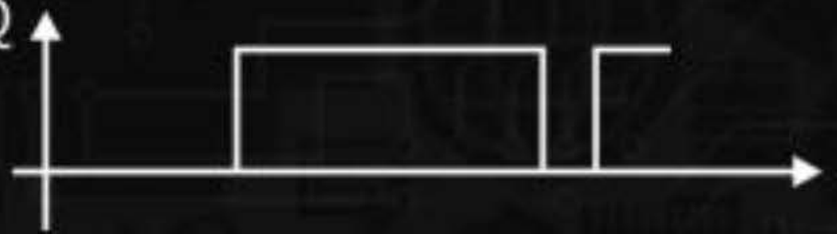
B.



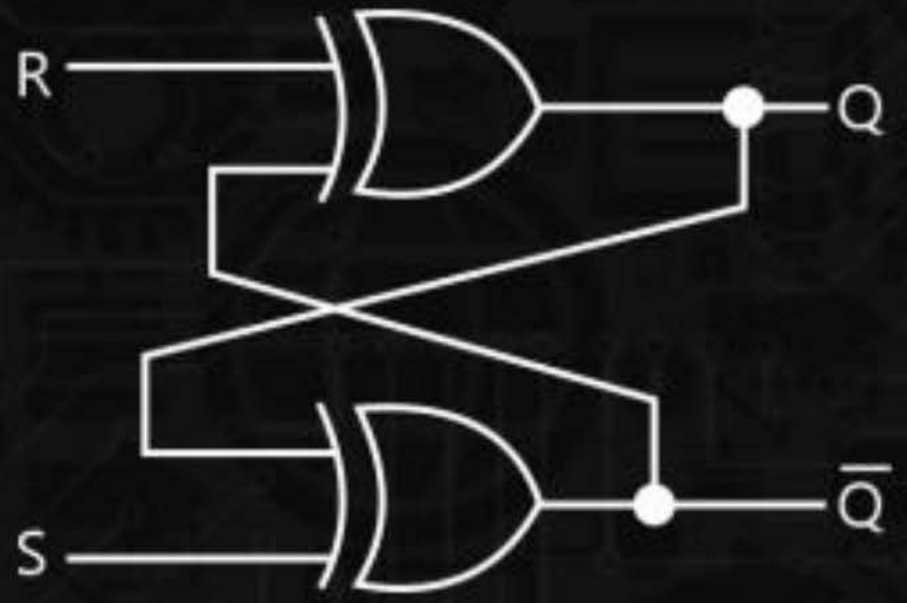
C.



D.



Q. Which of the following will be correct for the given sequential circuit?



A. The circuit would hold the previous state for S=0, R=0

B. The circuit would hold the previous state for S=0, R=1

C. The circuit would hold the previous state for S=1, R=1

D. The circuit would never be able to hold the previous state under any condition

JK FLIP FLOP

(1) Symbol

Figure 8: JK Flip-Flop

(2) Truth Table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$ → Toggle

JK FLIP FLOP

(3) Characteristic Table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

	J	K	Q_n	Q_{n+1}
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	0
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

JK FLIP FLOP

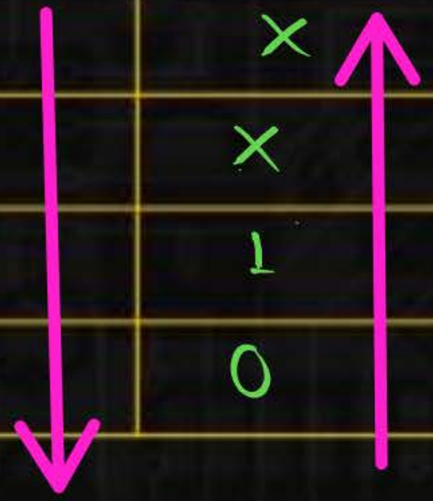
(4) Characteristic Equation

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

JK FLIP FLOP

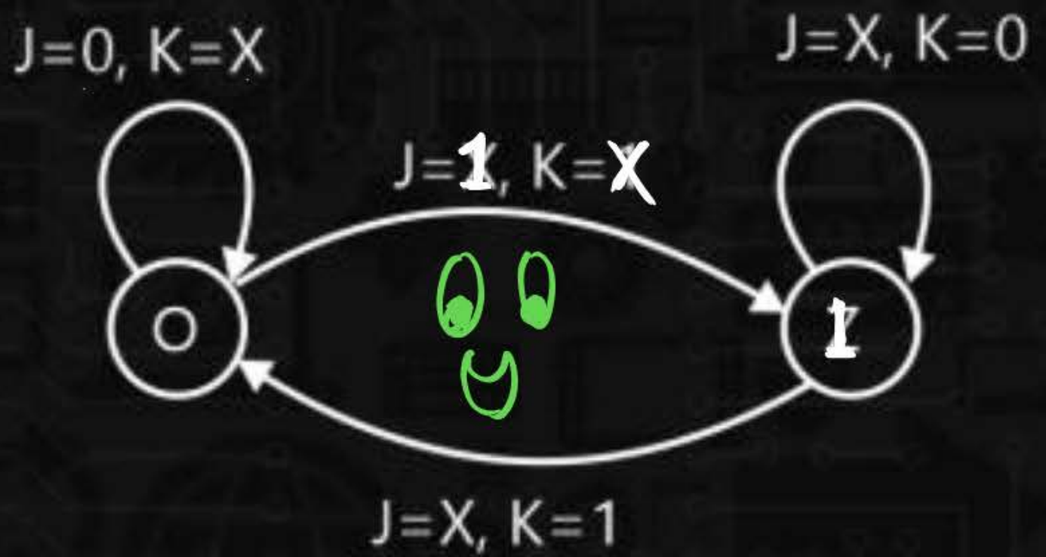
(5) Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



JK FLIP FLOP

(6) State Diagram



Q_n	Q_{n+1}	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0


THANK YOU GW
SOLDIERS !