CS & IT ENGINEERING

DIGITAL LOGIC

(Sequential Circuit)

Latches, SR FF

Lecture No. 1

By- CHANDAN SIR

01 Latches, SR FF

02 Practice

03 Discussion

Recape

Basics.

Minimization
- Boolean algebra
- K-MAP ✓

Combinational Circuit.

HA, FA, H.S., F.S.

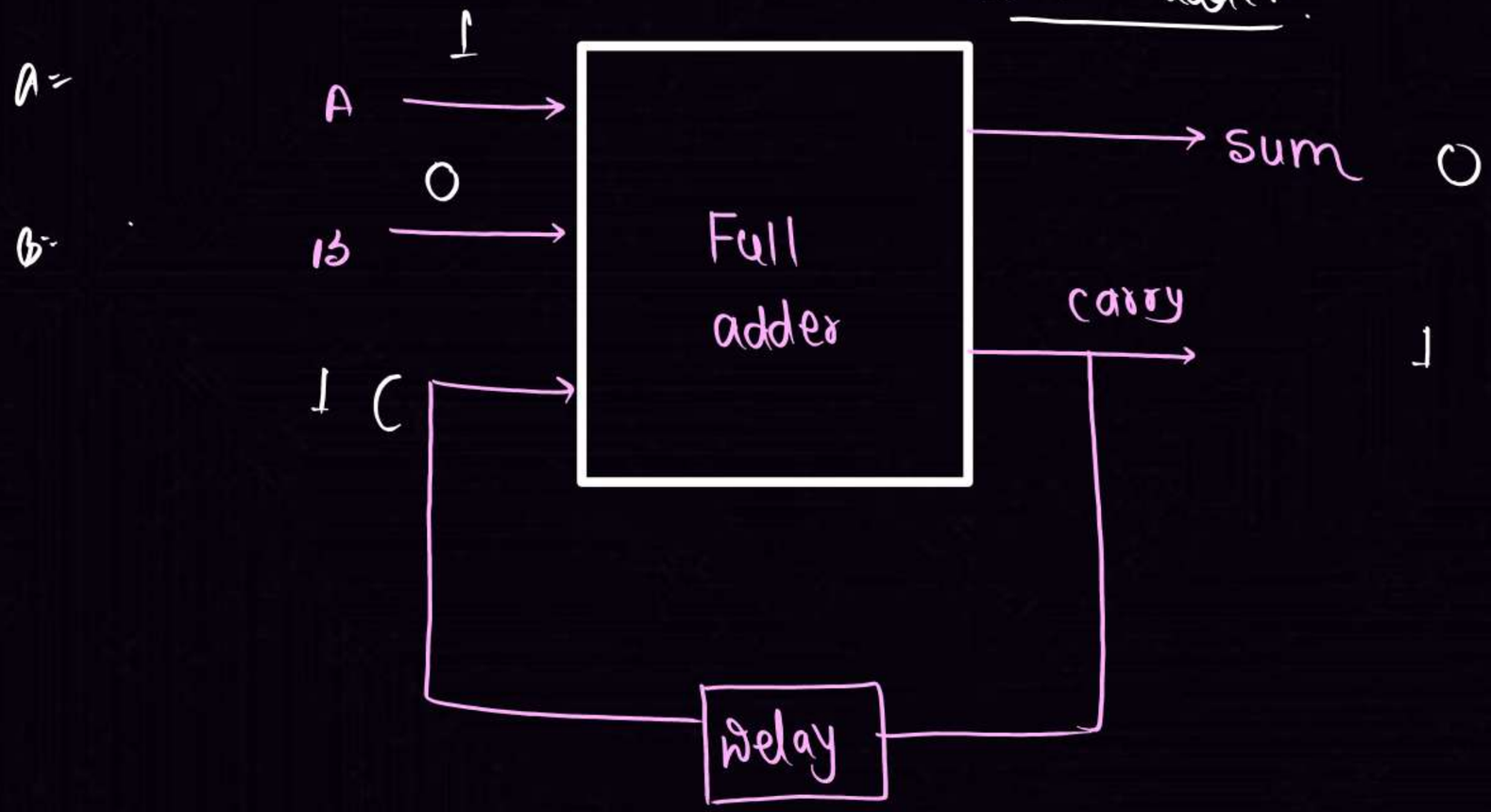
Comparator, MUX, DEMUX, Encoder, Decoder, Parallel adder

Delay

LACA

SERIAL ADDER

→ Slowest adder among all the adder.



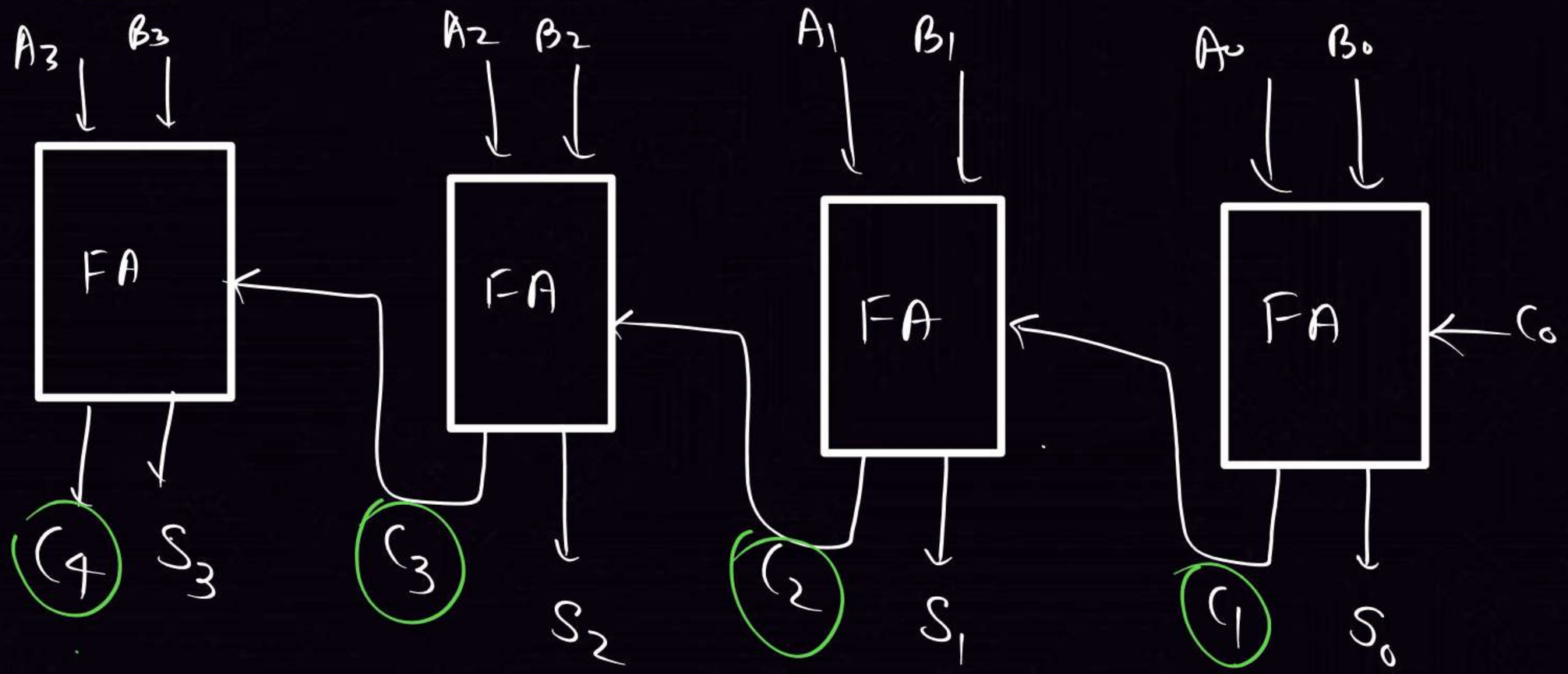
1 0 0 0

= 1

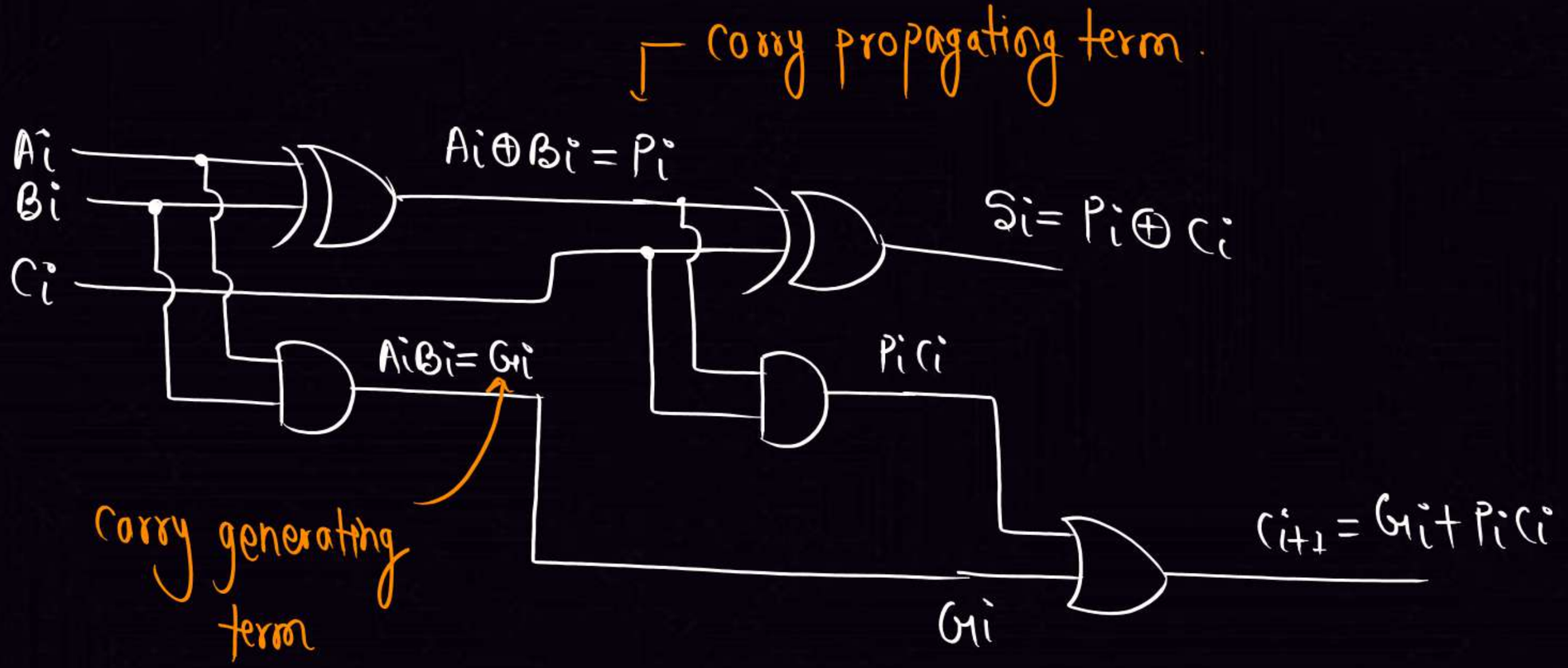
final carry

$T = (n-1)T_{carry} + Max\{T_{sum}, T_{carry}\}$

Parallel adder [Ripple carry adder]



LOOK AHEAD CARRY ADDER :→



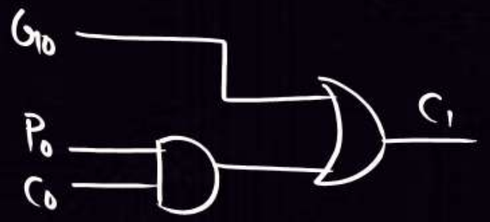
$P_i = A_i \oplus B_i$ $\quad G_i = A_i B_i$ $\quad S_i = P_i \oplus C_i$ $\quad C_{i+1} = G_i + P_i C_i$

$P_0 = A_0 \oplus B_0$ $\quad G_0 = A_0 B_0$ $\quad S_0 = P_0 \oplus C_0$

$P_1 = A_1 \oplus B_1$ $\quad G_1 = A_1 B_1$ $\quad S_1 = P_1 \oplus C_1$

$P_2 = A_2 \oplus B_2$ $\quad G_2 = A_2 B_2$ $\quad S_2 = P_2 \oplus C_2$

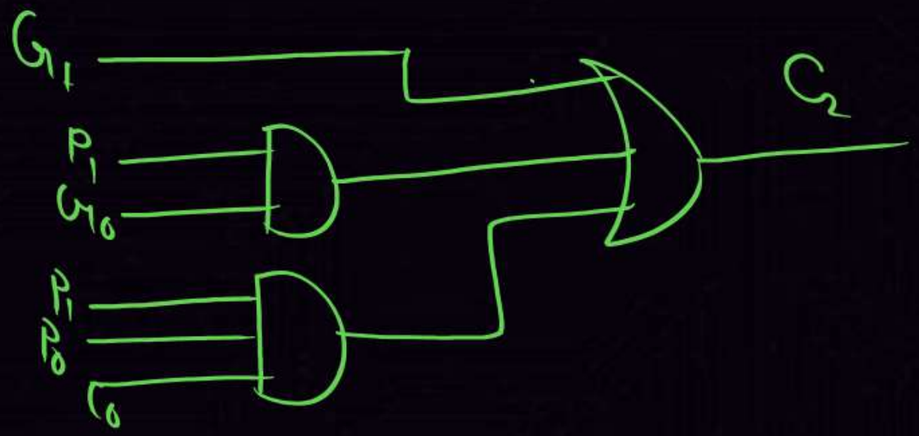
$$\boxed{C_1 = G_0 + P_0 C_0} \checkmark$$



$$C_2 = G_1 + P_1 C_1$$

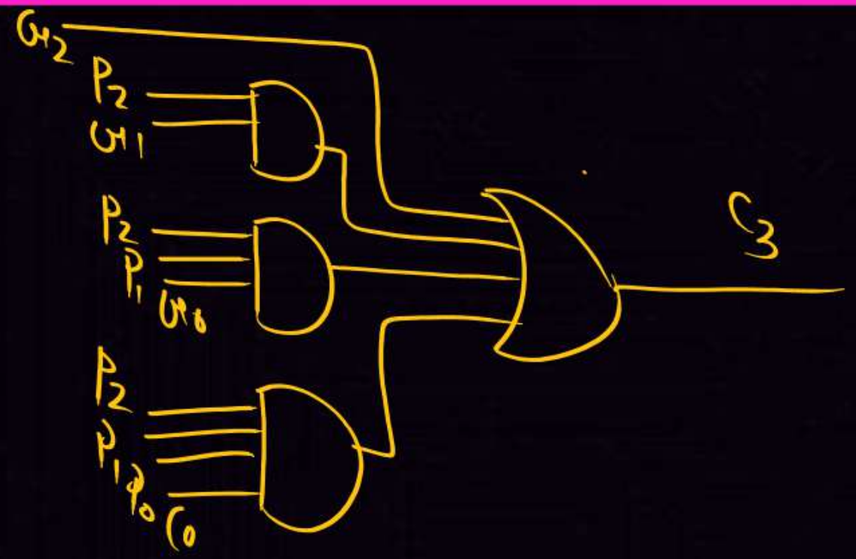
$$C_2 = G_1 + P_1 [G_0 + P_0 C_0]$$

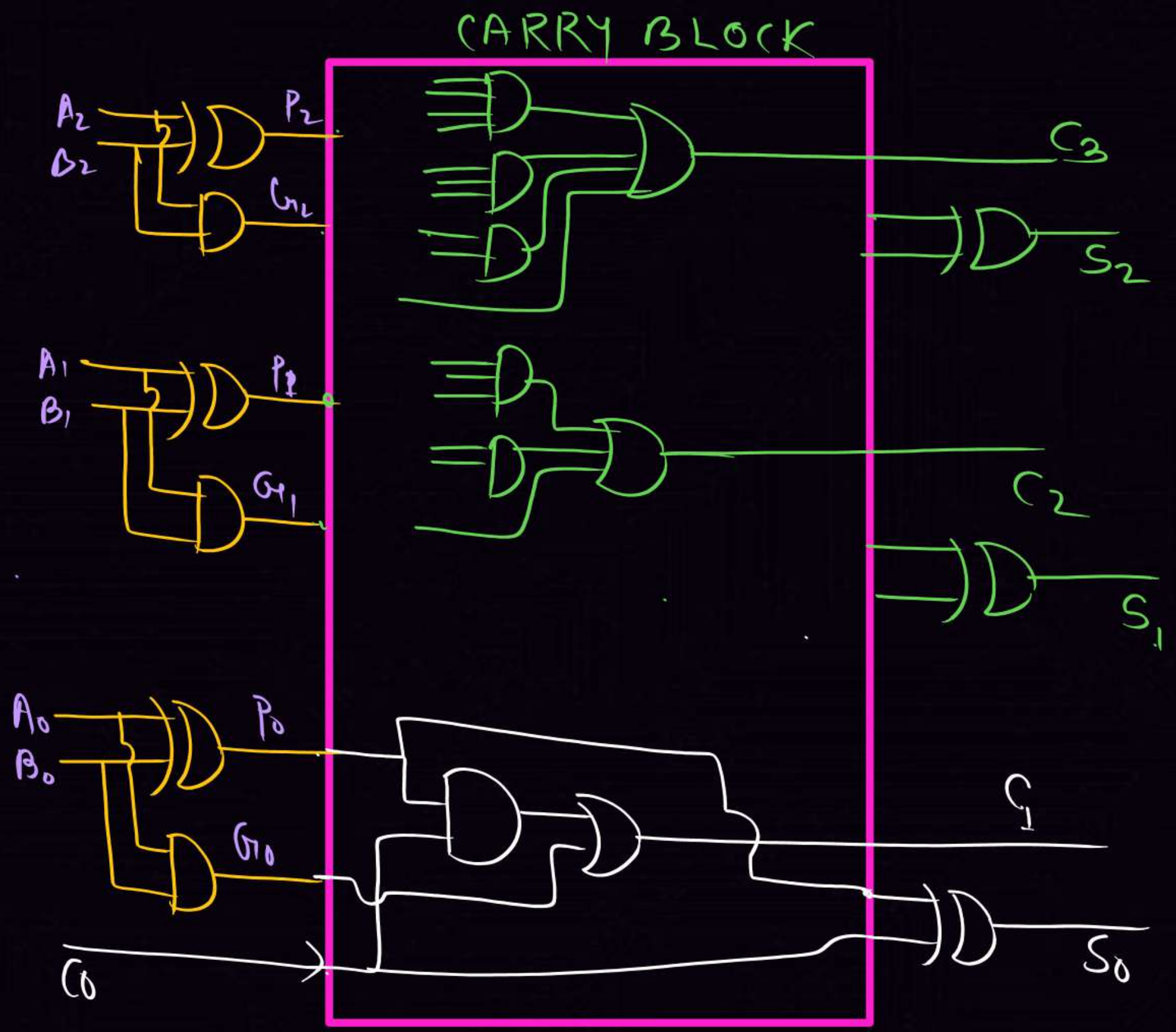
$$\boxed{C_2 = G_1 + P_1 G_0 + P_1 P_0 C_0}$$



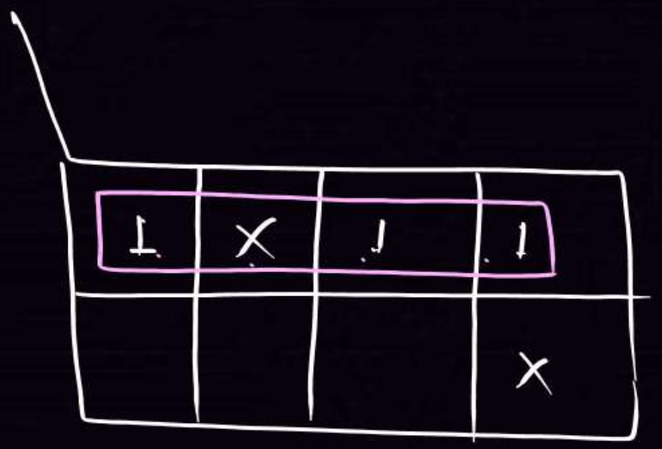
$$C_3 = G_2 + P_2 C_2$$

$$\boxed{C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0}$$




CARRY BLOCK
A2
B2
P2
G2
C3
S2
A1
B1
P1
G1
C2
S1
A0
B0
P0
G0
C1
S0
C0

Ex.



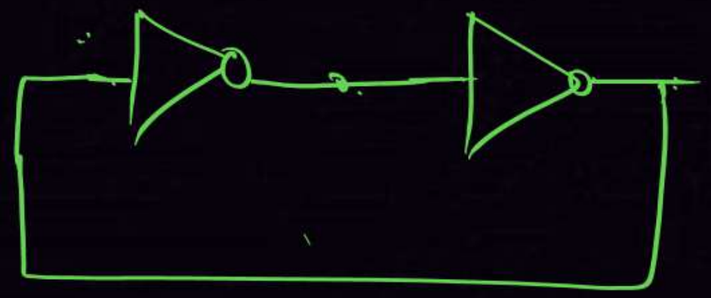
I = 4

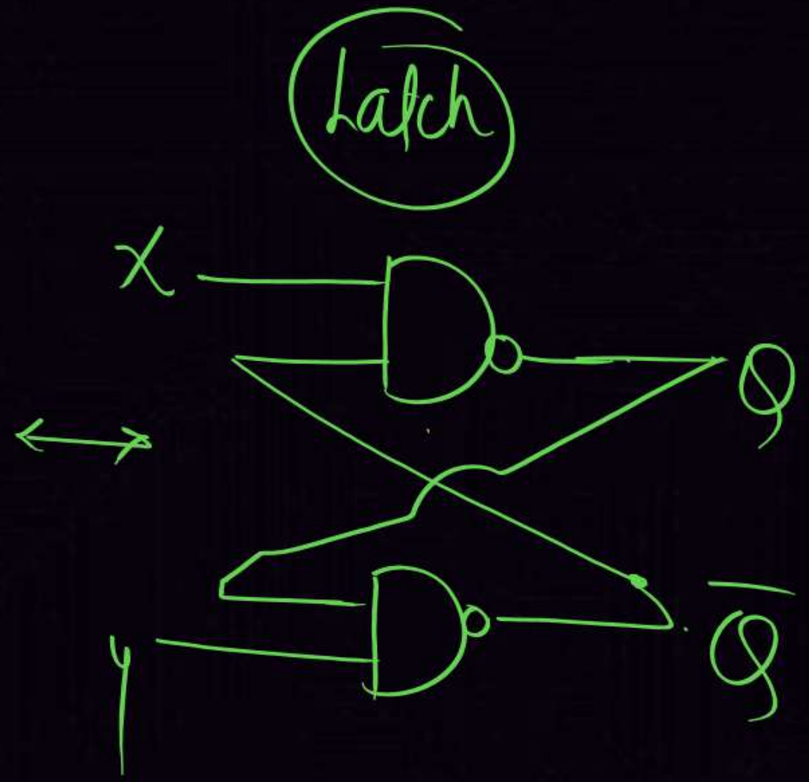
Sequential circuit

SEQUENTIAL CIRCUIT

1. A circuit with feedback and memory are called sequential circuit.
2. Output of the sequential circuit depends on previous output as well as present state of input.

Dynamic circuit

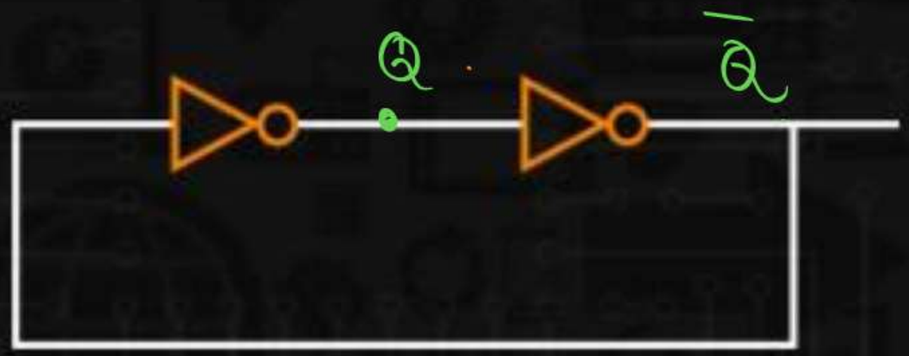


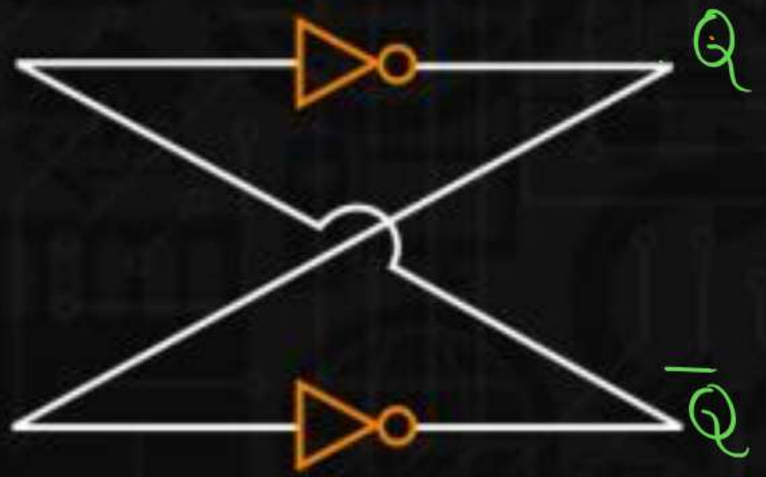


Basic memory element

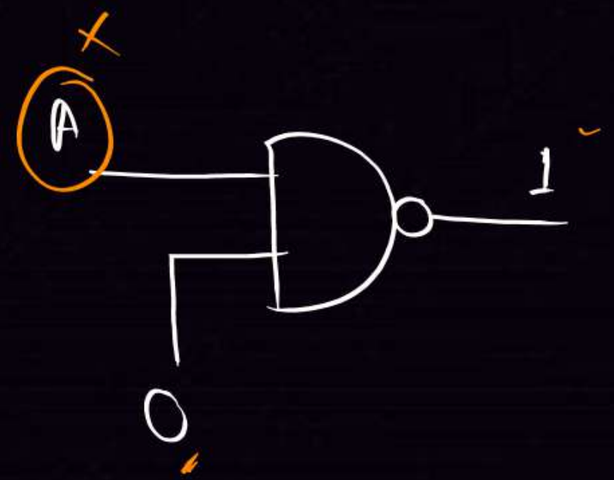
LATCHES

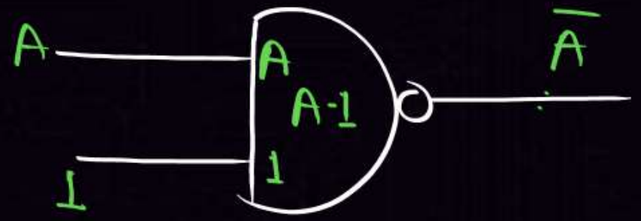
- ✓ Basic memory element
- [redacted]
- ✓ Latches are level triggered
- ✓ Latches has two output which is complement of each other





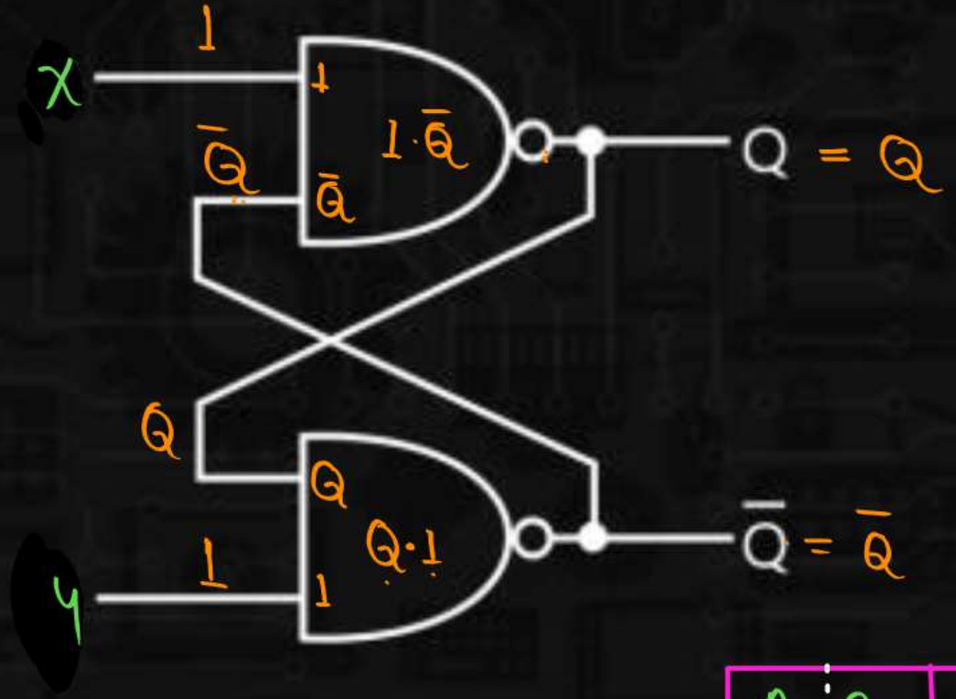
$A \cdot 1 = A$





LATCHES

$1 \cdot \bar{Q} = \bar{Q}$



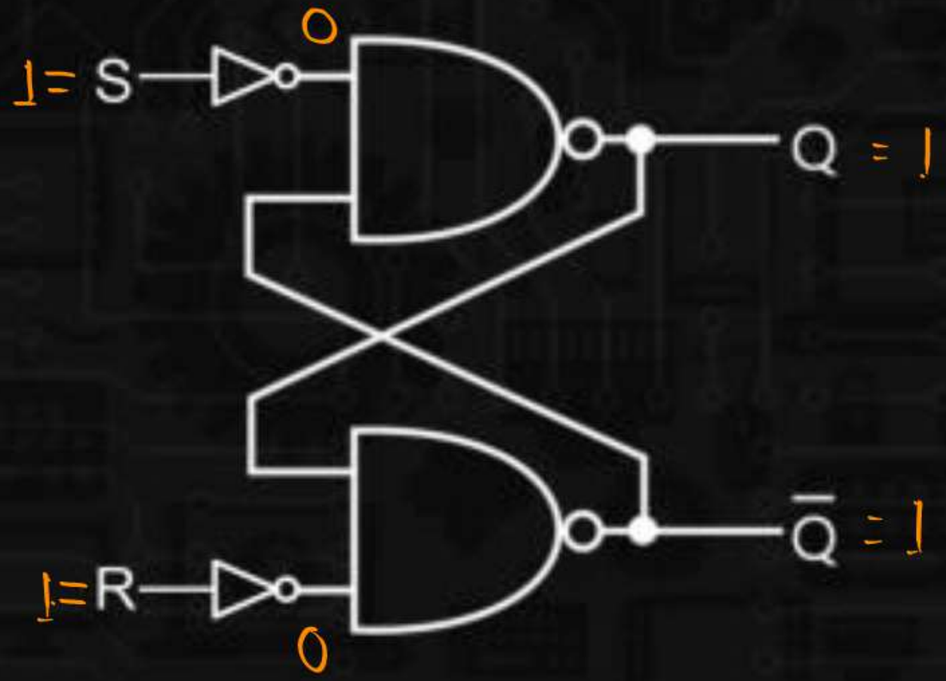
X	Y	Q	$\bar{Q}$	
0	0	1	1	Invalid
0	1	1	0	
1	0	0	1	
1	1	Q	$\bar{Q}$	→ HOLD

NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

LATCHES

SR latch

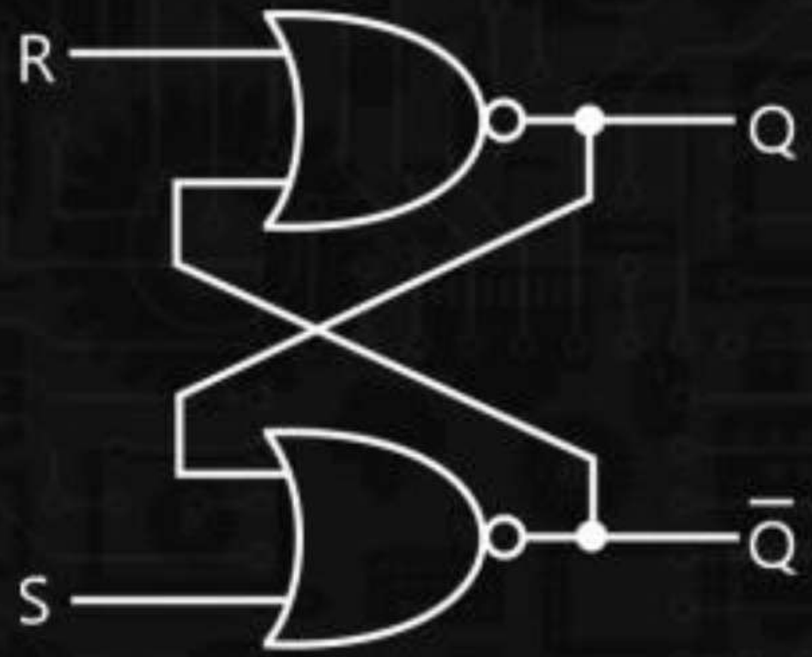


S	R	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$ (HOLD)
0	1	0	1
1	0	1	0
1	1	1	1 (inValid)

LATCHES

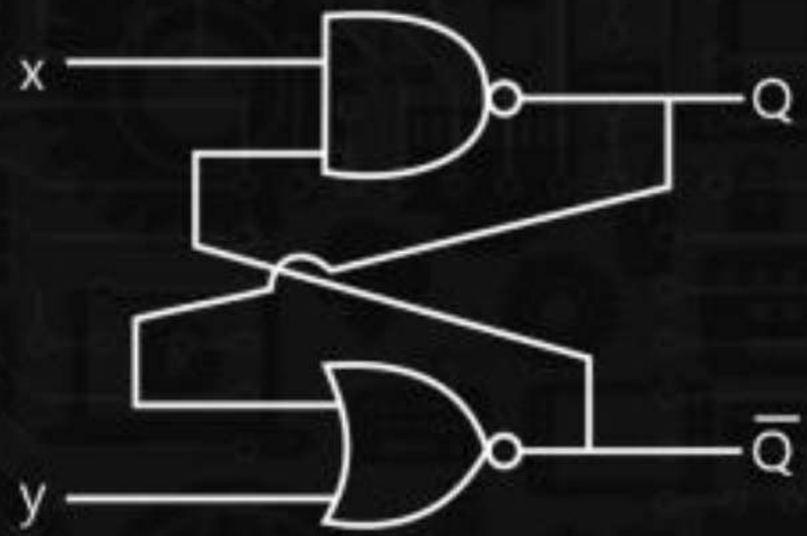
Note : Whenever S = R = 1 is applied and invalid condition occurs than a NAND having lower propagation delay first change its output and other remain on its previous state are called racing problem or raising problem.

LATCHES



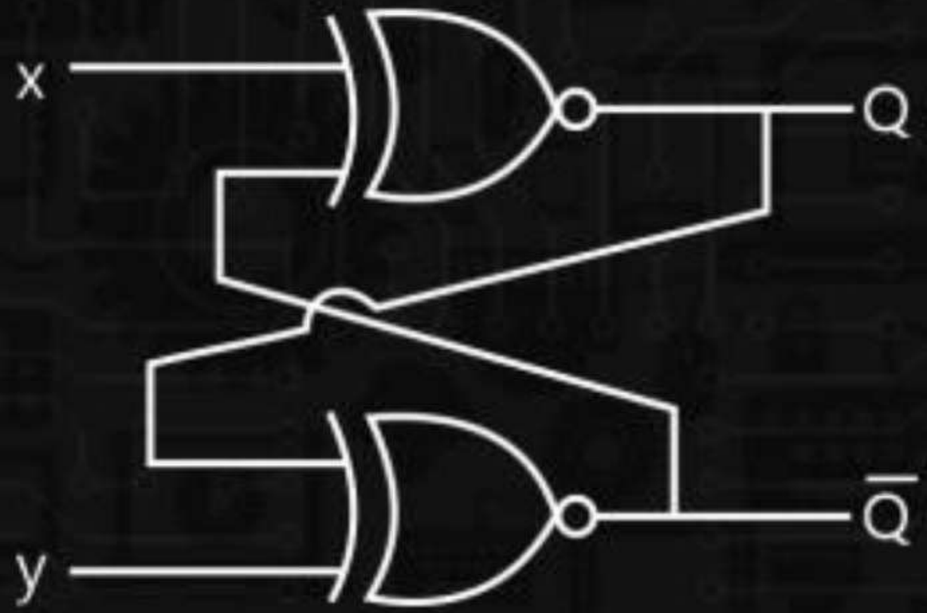
S	R	Q	
0	0		
0	1		
1	0		
1	1		

LATCHES



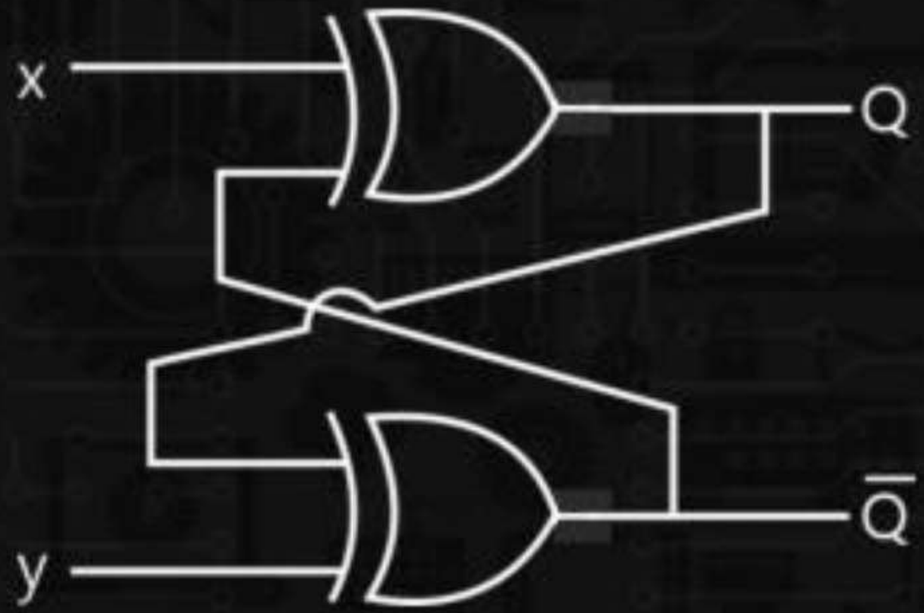
X	Y	Q	
0	0		
0	1		
1	0		
1	1		

LATCHES



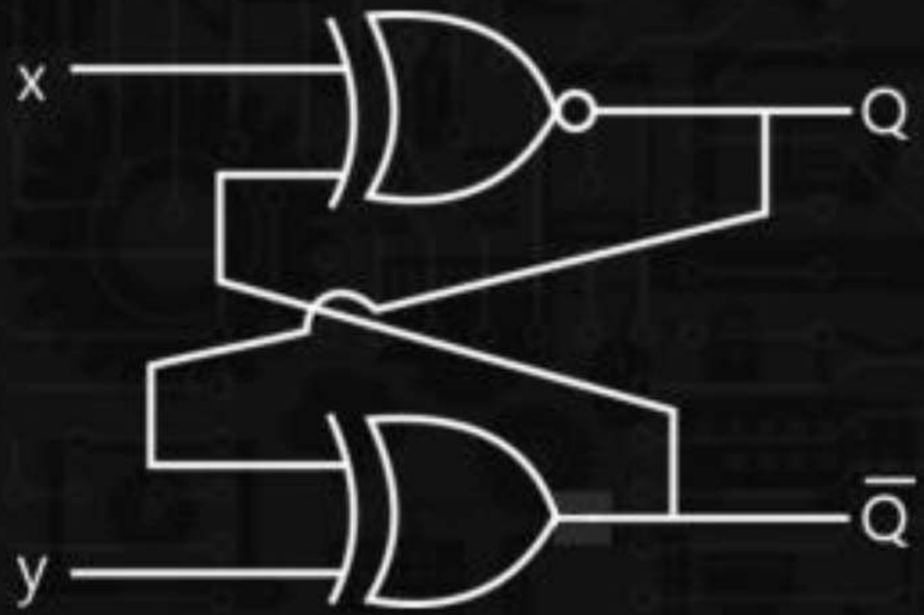
X	Y	Q	
0	0		
0	1		
1	0		
1	1		

LATCHES



X	Y	Q	
0	0		
0	1		
1	0		
1	1		

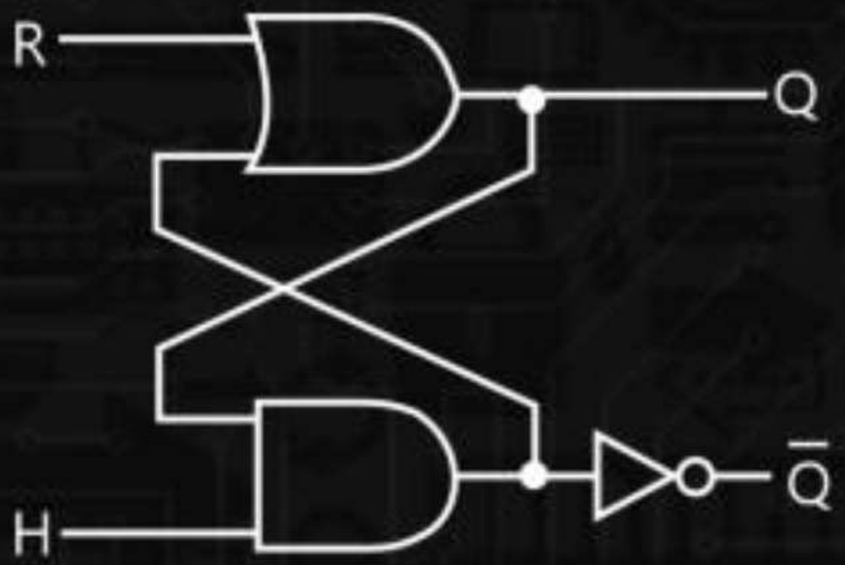
LATCHES



X	Y	Q	
0	0		
0	1		
1	0		
1	1		

LATCHES

Q.1 Consider a latch circuit shown in figure below. Which of the following set of input is invalid for circuit?



A. R = 0, H = 0

B. R = 0, H = 1

C. R = 1, H = 1

D. R = 1, H = 0

LATCHES

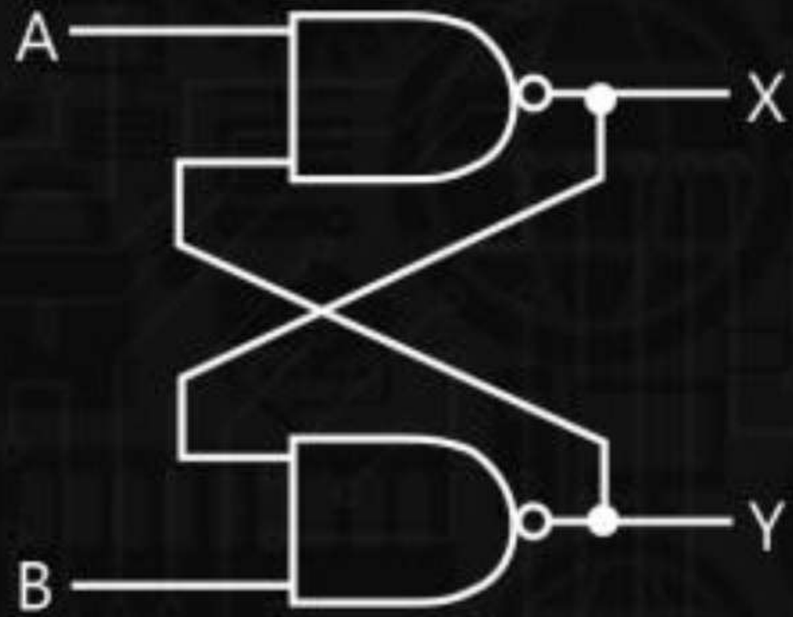
Q.2 In the circuit shown below, initially A = 1 and B = 1. The input B is now replaced by a sequence 101010 ..... the outputs X and Y will be

A. Fixed at 0 and 1, respectively

B. Fixed at 1 and 0, respectively

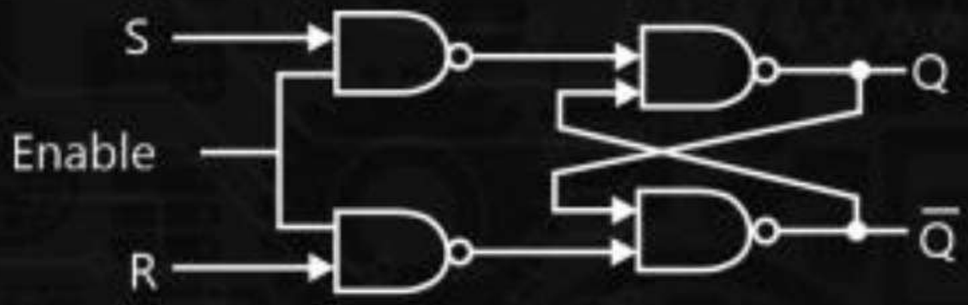
C. X = 1010..... while Y = 1010....

D. X = 1010 ..... while Y = 0101 .....



(1) SR FLIP-FLOP [SET RESET FF]

(i) Circuit Diagram :



SR Latch

(ii) Truth Table :

X	Y	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

SR FLIP-FLOP [SET RESET FF]

(iii) Characteristic Table:

S	R	Q_n	Q_{n+1}
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

SR FLIP-FLOP [SET RESET FF]

(iv) Characteristic equations

SR FLIP-FLOP [SET RESET FF]

(v) Excitation Table

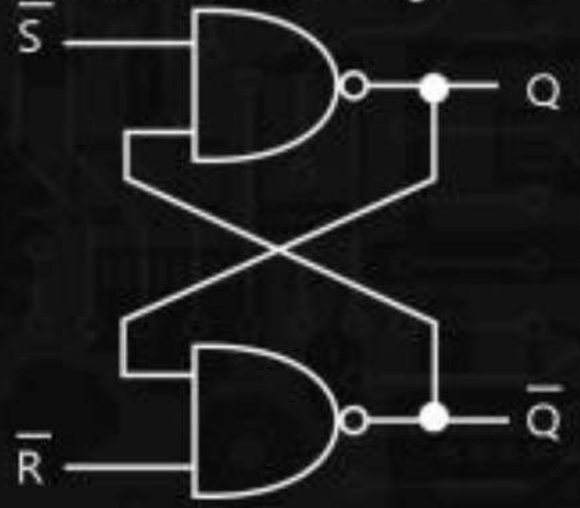
Qn	Qn+1	S	R
0	0		
0	1		
1	0		
1	1		

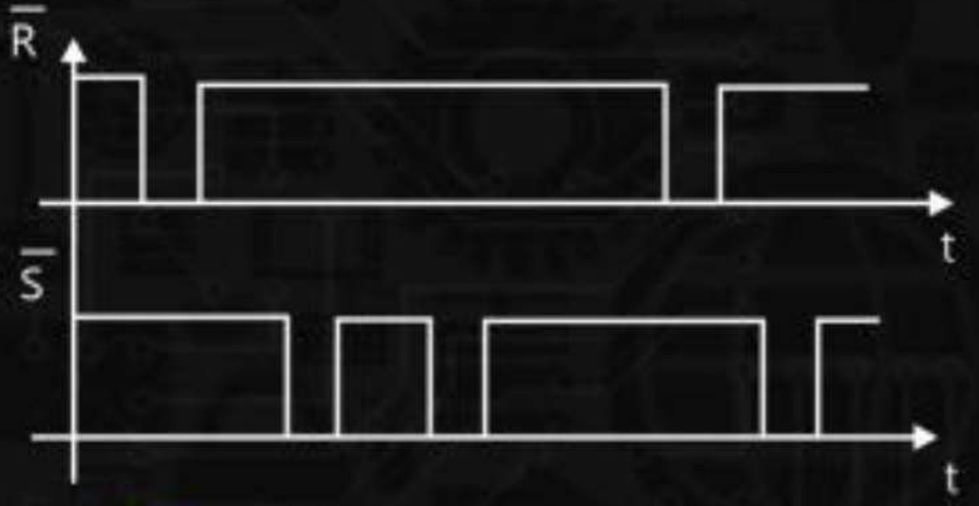
S	R	Q_n	Q_{n+1}
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

SR FLIP-FLOP [SET RESET FF]

(vi) State Diagram :

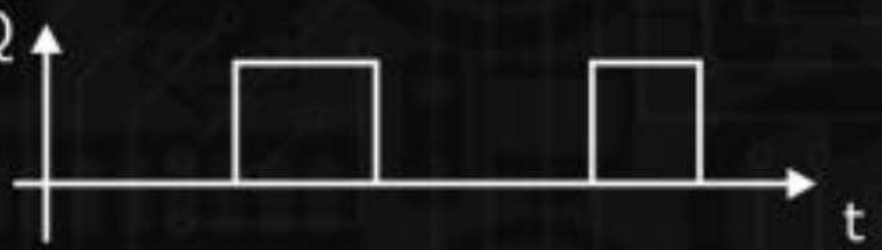
Q. The $\bar{S}$ and $\bar{R}$ inputs shown in the figure are applied toa NAND latch. Assuming the Q is 0 initially, which plot gives correct waveform for Q?





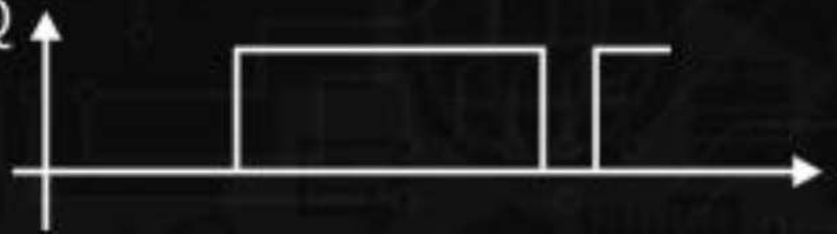
A.

B.



C.

D.



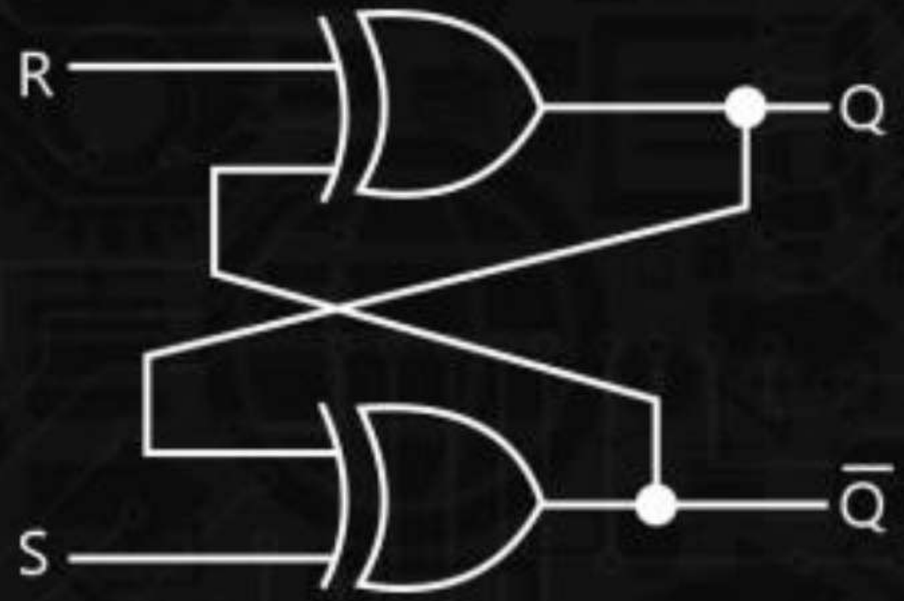
Q. Which of the following will be correct for the given sequential circuit?

A. The circuit would hold the previous state for S=0, R=0

B. The circuit would hold the previous state for S=0, R=1

C. The circuit would hold the previous state for S=1, R=1

D. The circuit would never be able to hold the previous state under any condition



Q. Find the characteristics equation of following excitation table?

A. $X\,Q(t)' + Y'\,Q(t)$

B. $X + Y'\,Q(t)$

C. $X\,Q(t) + Y'\,Q(t)'$

D. $X + Y'\,Q(t)'$

X	Y	Q(t)	Q(t+1)
0	×	0	0
1	0	0	1
0	1	1	0
×	0	1	1

X	Y	Q_n	Q_{n+1}
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

S	R	Q_n	Q_{n+1}
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

S	R	Q_{n+1}	
0	0		
0	1		
1	0		
1	1		

Q_n	Q_{n+1}	S	R
0	0		
0	1		
1	0		
1	1		


THANK YOU GW
SOLDIERS !