CS & IT ENGINEERING

DIGITAL ELECTRONICS

Combinational circuit

Lecture No. 9

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01 Parallel Adder

02 Question Practice

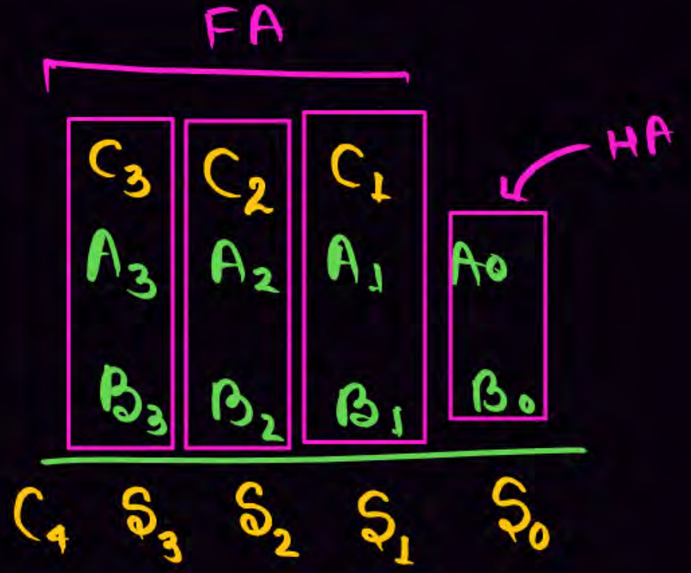
03 Discussion

combinational circuit

- Designing
  - HA, FA, H.S, F.S.
  - MUX DEMUX
  - Encoder, Decoder
  - comparator

PARALLEL ADDER

4 bit



$(n-1)[2HA+1OR]+1HA$

$(2n-2)HA+(n-1)OR+1HA$

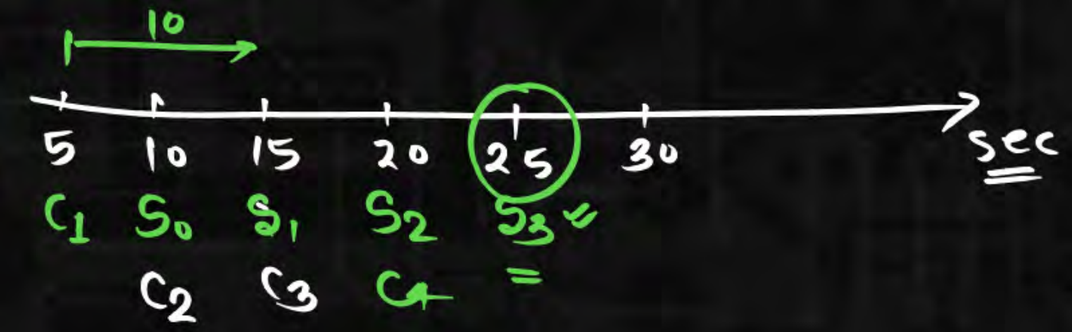
$(2n-1)HA+(n-1)OR$

n bit parallel adder

1. $(n-1)$ FA + 1 H.A
2. n FA
3. $(2n-1)$ HA + $(n-1)$ OR GATE

Parallel Adder

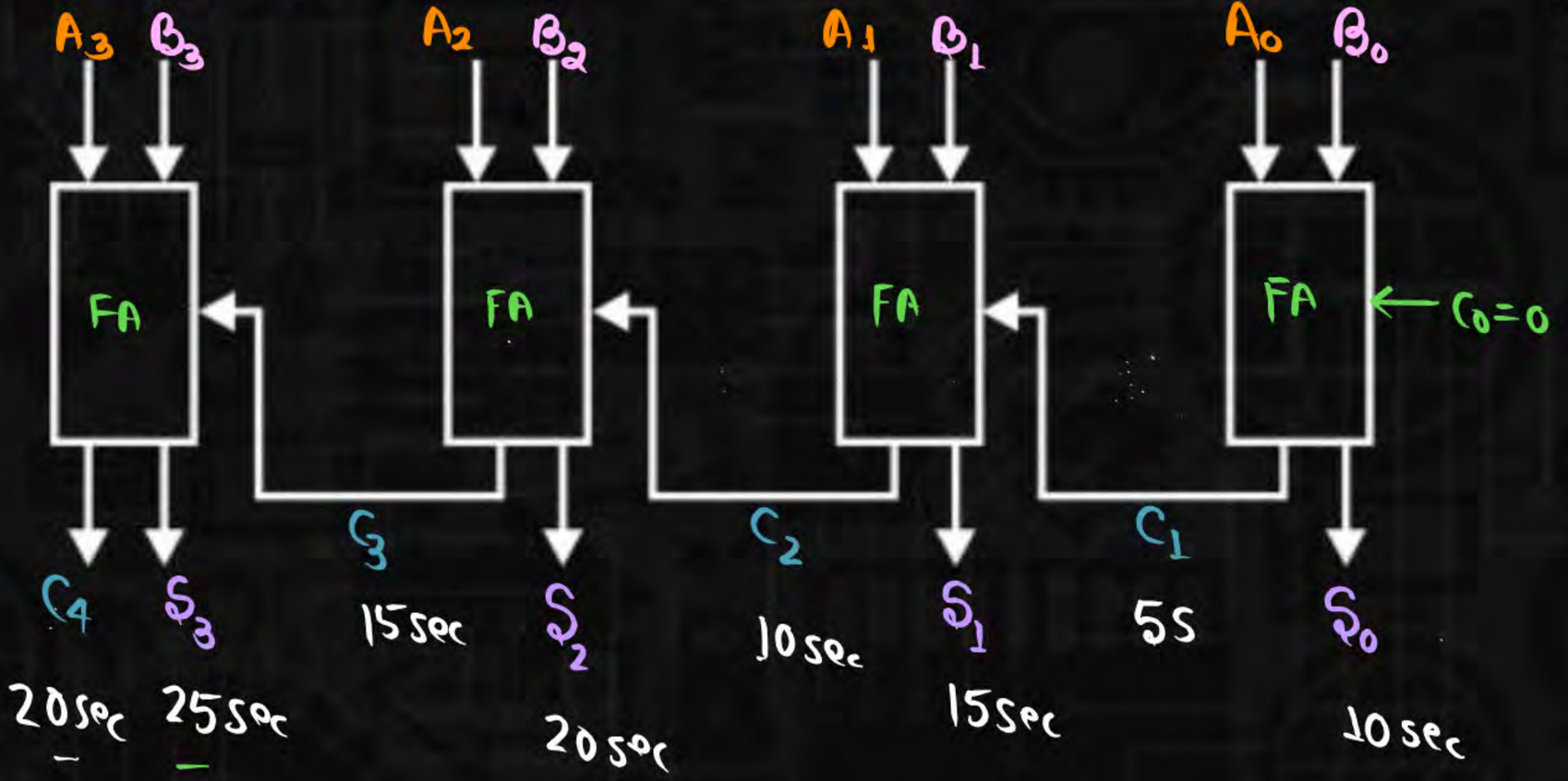
{RIPPLE CARRY ADDER}



$T_{sum} = 10$ sec

$T_{carry} = 5$ sec

PARALLEL ADDER



"n" bit parallel adder

Delay

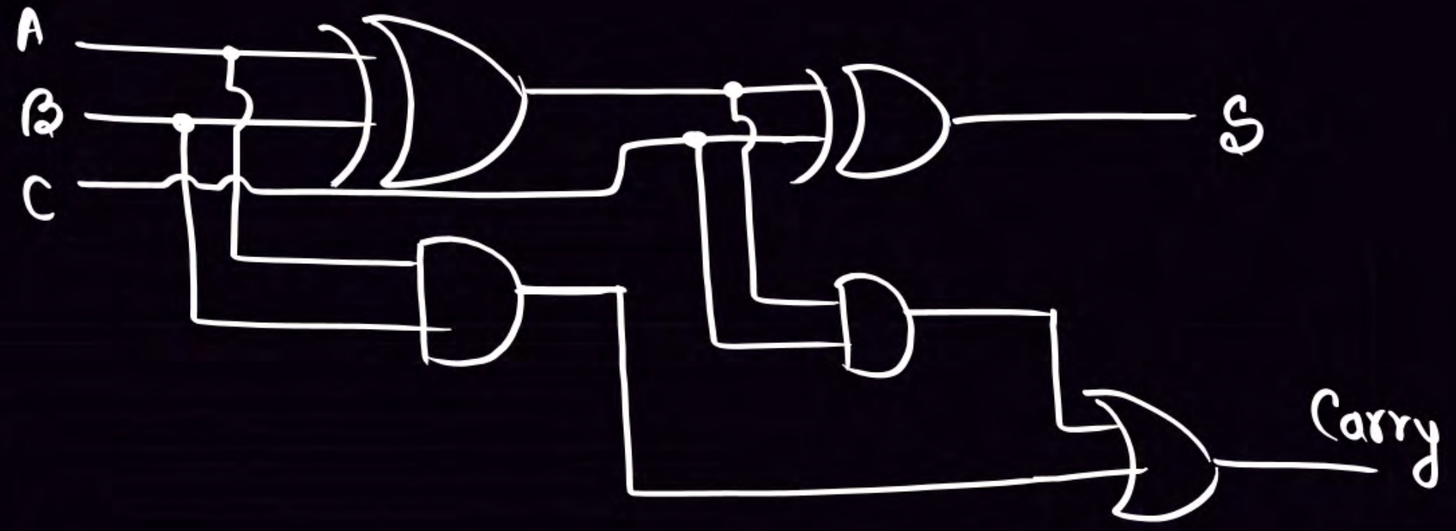
$$T = (n-1)T_{carry} + Max\{T_{sum}, T_{carry}\}$$

Ex $T_{sum} = 10s$ $n = 4$

$T_{carry} = 5s$

$T = (4-1)5 + Max\{10, 5\}$

$T = 3 \times 5 + 10 = 25$ sec

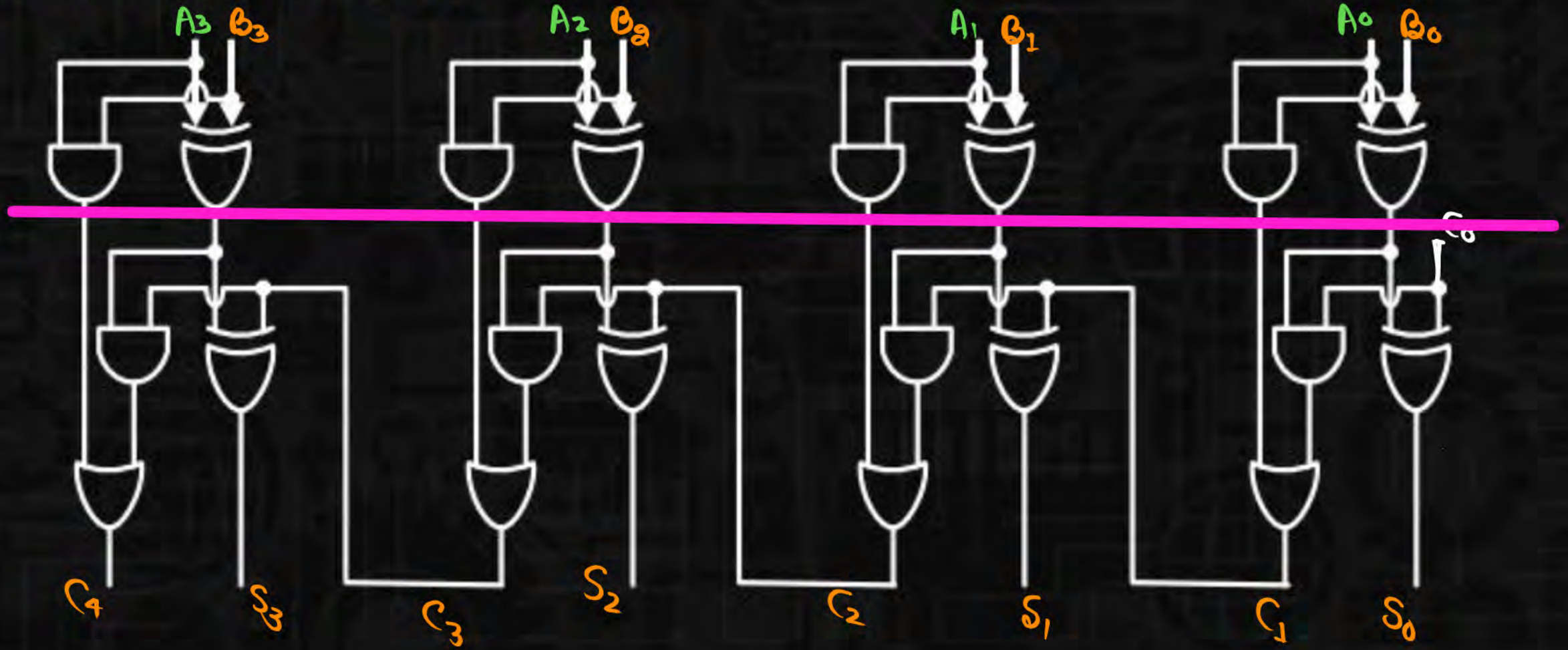

A
B
C
S
Carry

Parallel Adder

$$T = (n-1)\{T_{AND} + T_{OR}\} + \text{Max}\{T_{sum}, T_{carry}\}$$

$2T_{XOR}$ $\quad$ $T_{XOR} + T_{AND} + T_{OR}$

PARALLEL ADDER



Parallel Adder

$T_{carry} = 12\,ns$ $T_{sum} = 15\,ns$ $n = 16$

Q.1 A 16-bit ripple carry adder is realized using 16 identical full adders. The carry propagation delay of each full adder is 12 ns and the sum propagation delay of each full adder is 15 ns. The worst case delay of this 16 bit adder will be ____ ?

$T = (n-1)T_{carry} + Max\{T_{sum}, T_{carry}\}$

$T = (16-1)\,12ns + Max\{15ns, 12ns\}$

$T = 15 \times 12 + 15\,ns$

$T = 195\,ns$

addition per second $= \frac{1}{T}$

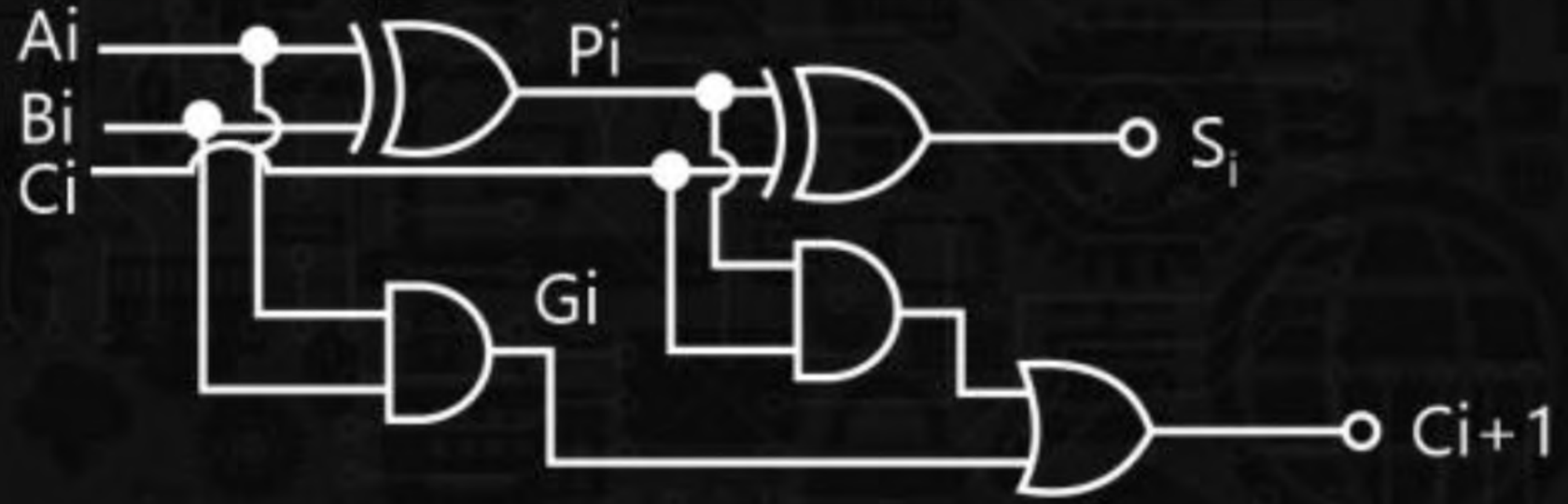
A. 195 ns

B. 220 ns

C. 250 ns

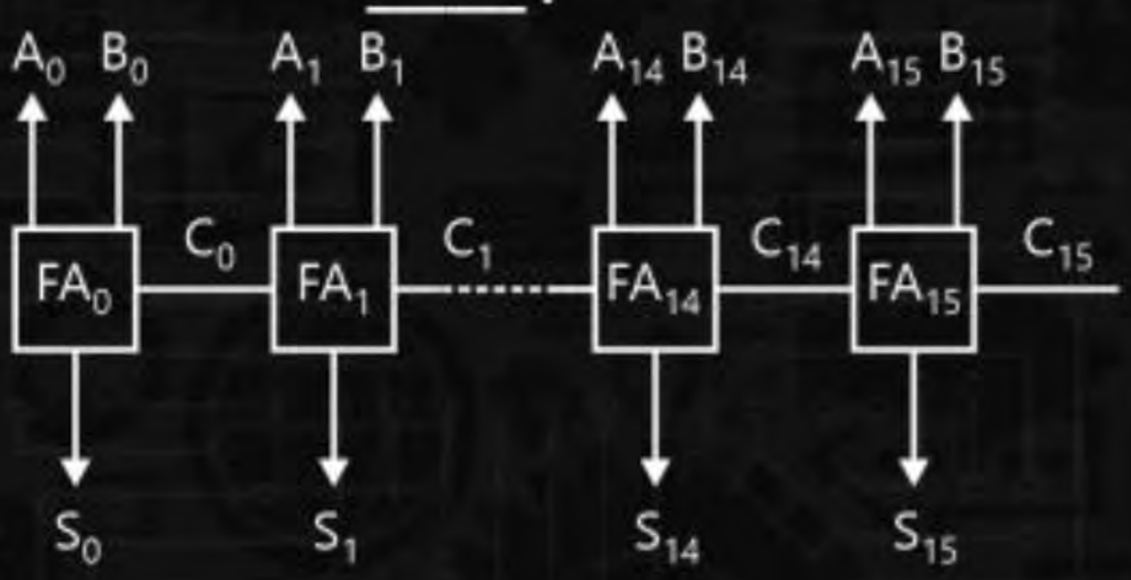
D. 300 ns

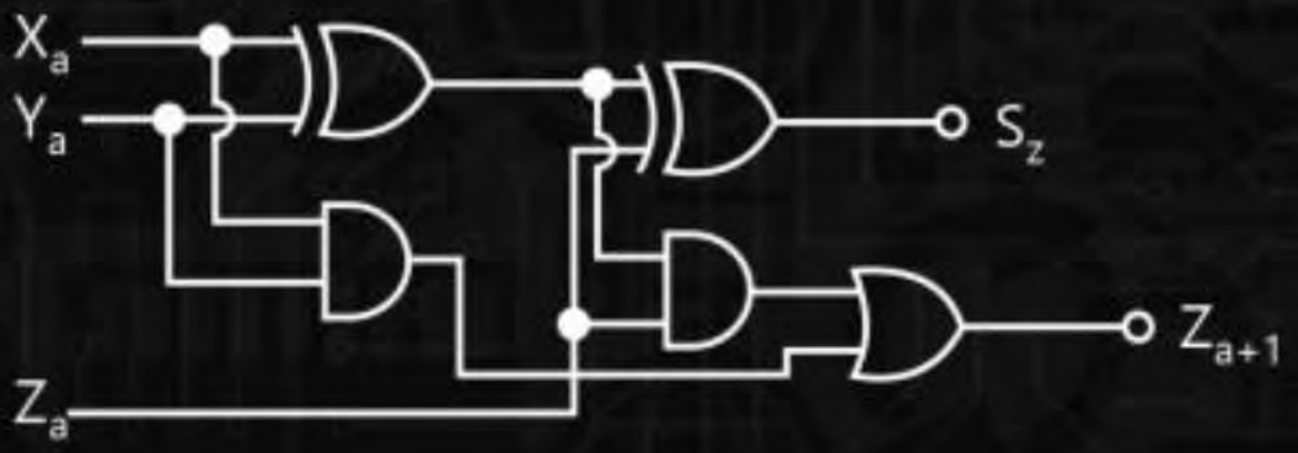
Parallel Adder



Parallel Adder

Q.3 A 16-bit ripple carry adder is realized using 16 identical full adders (FA) as shown in the figure. The carry-propagation delay of each FA is 12 ns and the sum-propagation delay of each FA is 15 ns. The worst case delay (in ns) of this 16-bit adder will be _____.





Parallel Adder

$T_{AND} = 1.2\ \mu s$
$T_{OR} = 1.2\ \mu s$
$T_{XOR} = 2.4\ \mu s$

Q.4

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple-carry binary adder is implemented by using full adders. The total propagation time of this 4-bit binary adder in microseconds is,

$$T = (n-1)\{T_{AND} + T_{OR}\} + 2T_{XOR}$$

$T = 3 \times \{1.2 + 1.2\} + 2 \times 2.4$

$T = 3 \times 2.4 + 4.8$

$T = 7.2 + 4.8$

$T = 12\ \mu s$

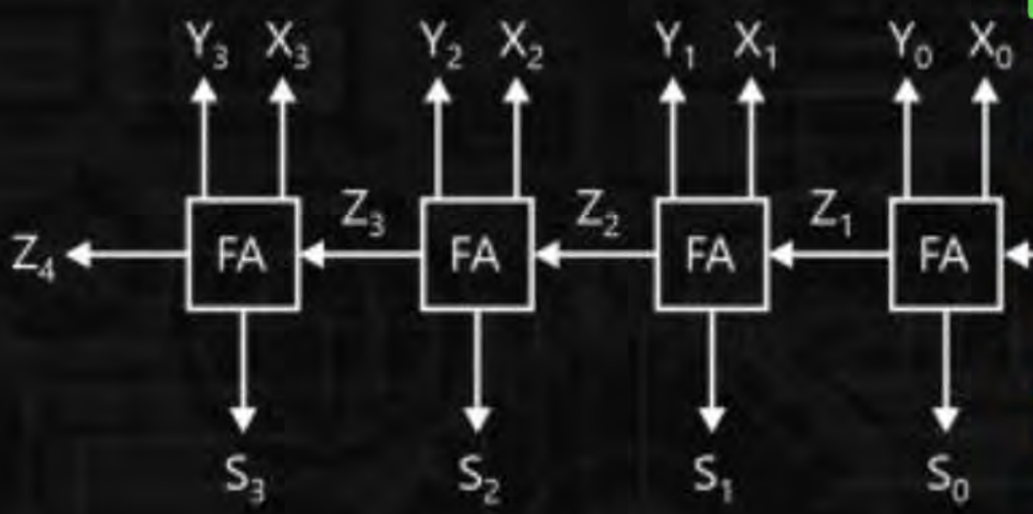


Figure-I

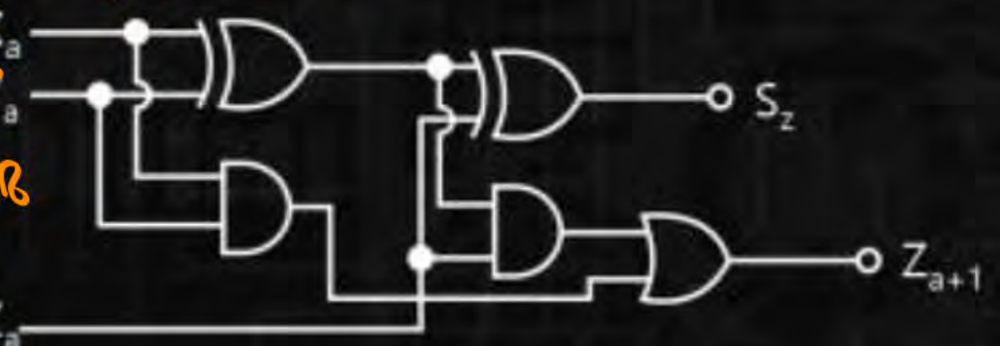
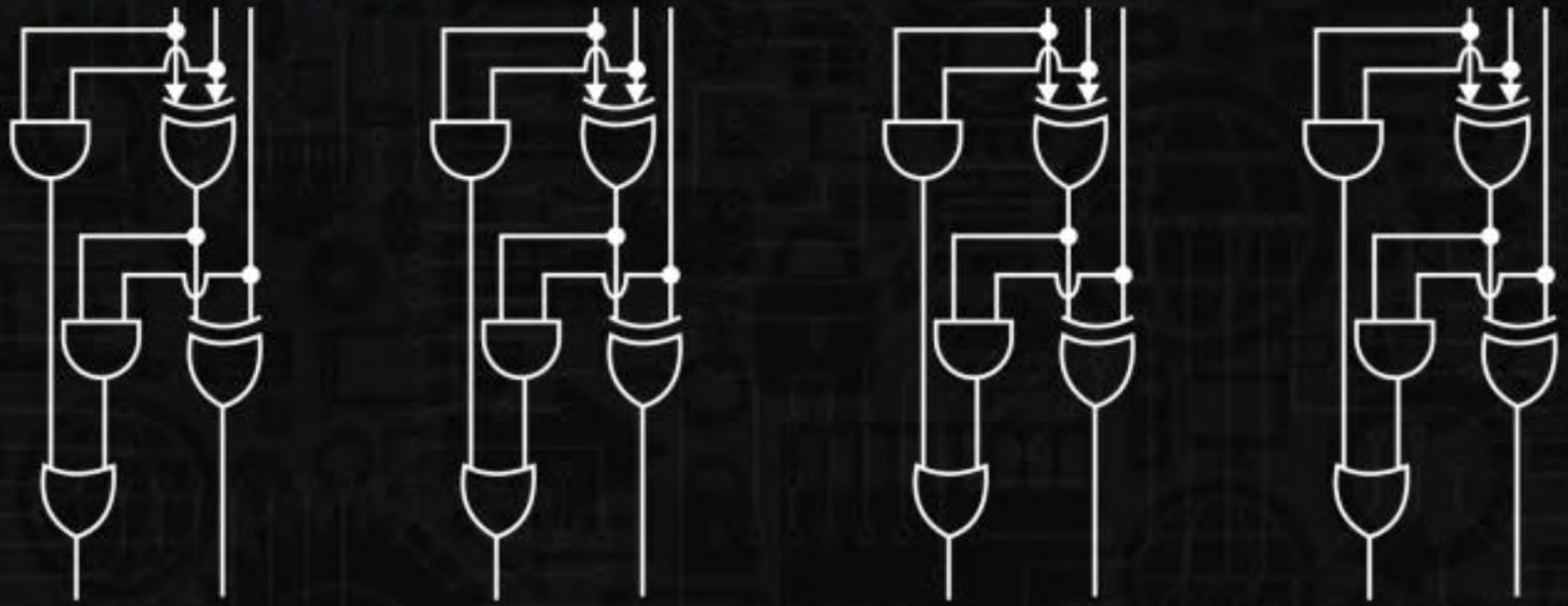


Figure-II

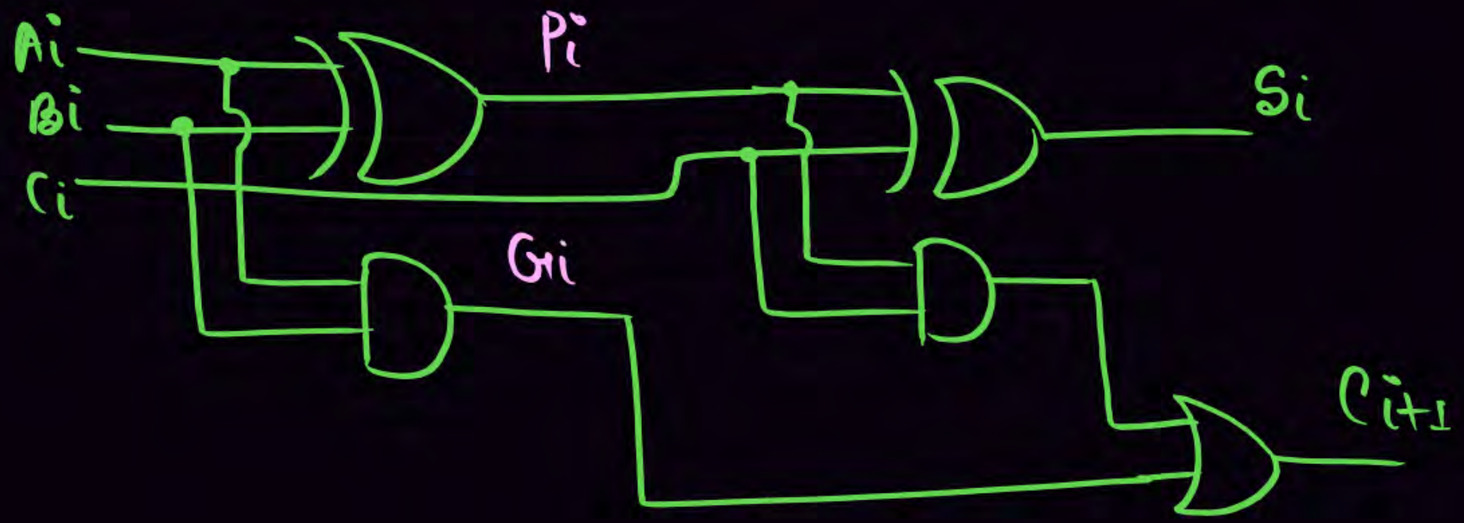
Parallel Adder

PARALLEL ADDER



Look Ahead Carry Odder (LACA)

→ fastest adder among all the adder.



P_i → carry propagating term

G_i → carry generating term.

$P_i = A_i \oplus B_i$

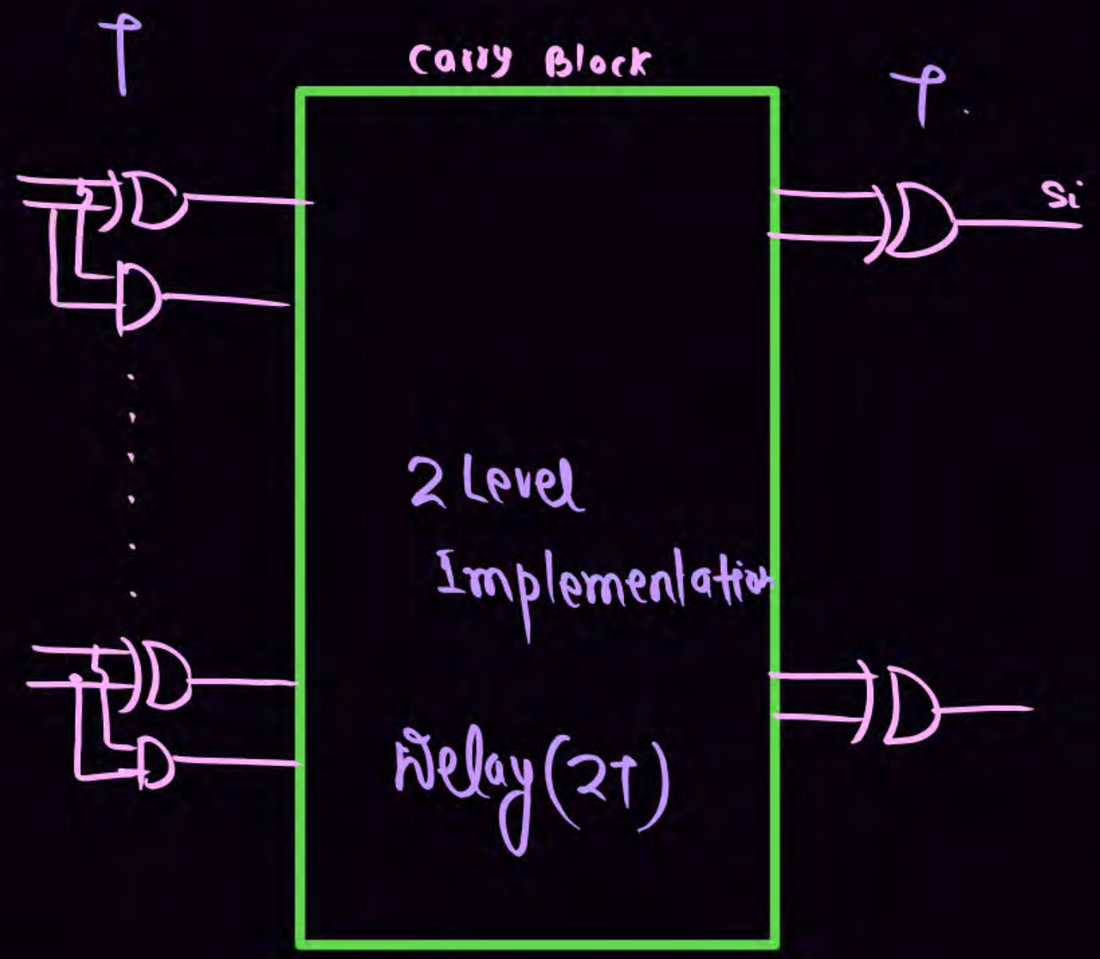
$G_i = A_i B_i$

Total Delay

$= 4T$

Carry Block Delay

$= 2T$



In Carry Block

Number of AND GATE $= \frac{n(n+1)}{2}$

Number of OR GATE $= n$.


THANK YOU GW
SOLDIERS !