CS & IT ENGINEERING

DIGITAL LOGIC

SEQUENTIAL CIRCUIT

Counter part 1

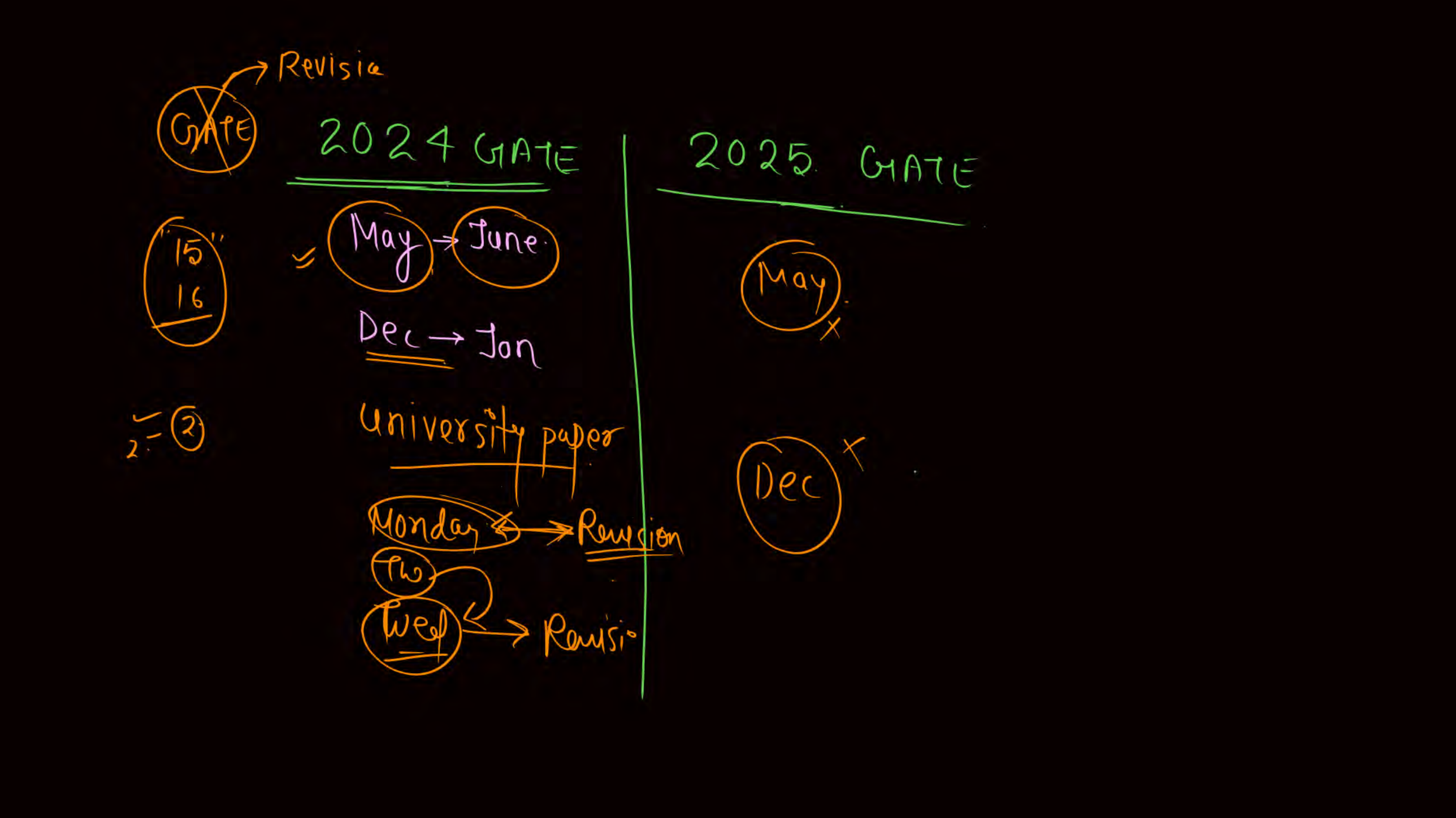
Lecture No. 5

By- CHANDAN SIR

01 Counters

02 Practice

03 Discussion

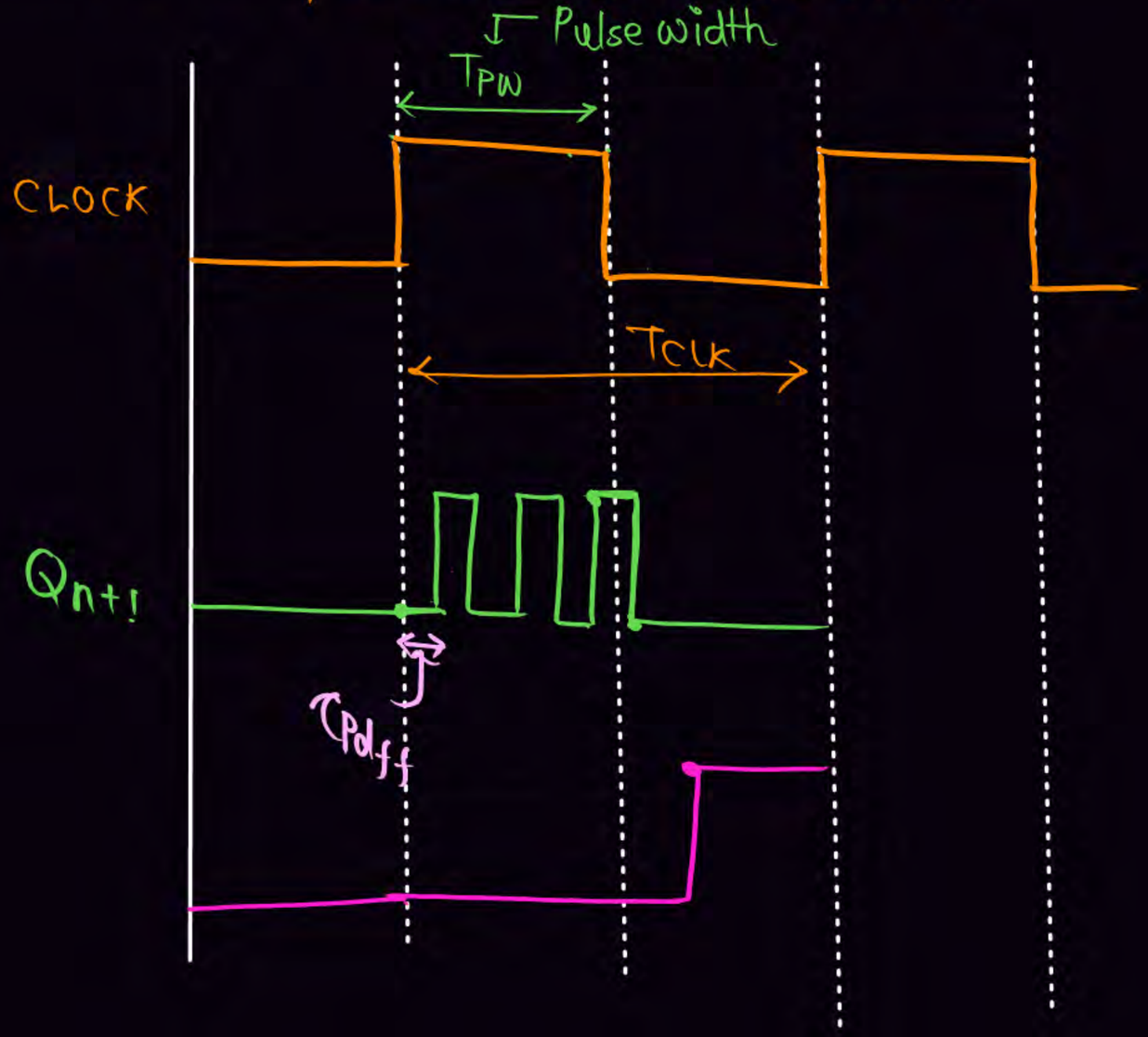

Revisio
GATE
2024 GATE
2025 GATE
"15"
16
May → June
Dec → Jon
May
Dec
university paper
Monday
Revision
Tu
Wed
Revisio

Latches → Flip-Flop → Designing of FF

Latches
↓
Truth table

Flip-Flop
- SR
- JK
- D FF
- T FF

NOTE :→ JK FF suffers from the problem of Race Around.



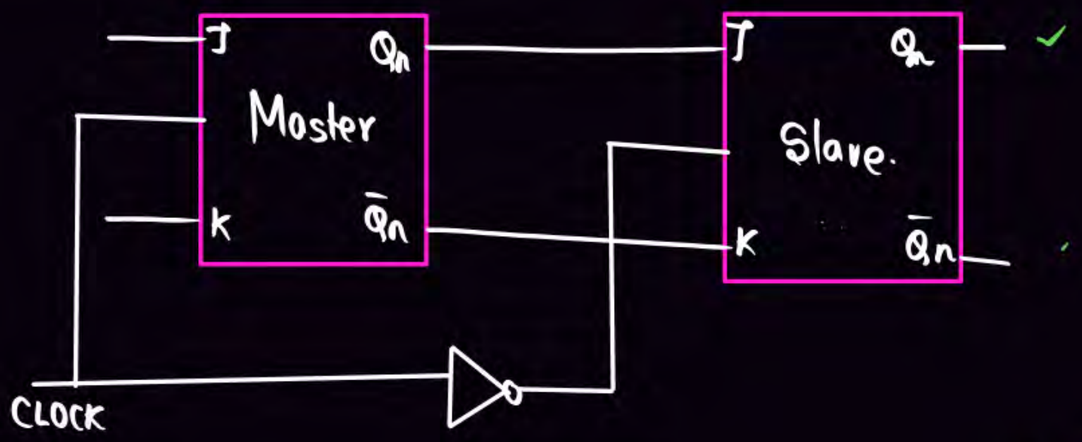
Whenever $J=K=1$ is applied and if is Level sensitive.
Then with in the duration of pulse width o/p of the circuit will be toggle so many times and at the end of the pulse width o/p will be settle either at "1" or "0" depends on pulse width and propagation delay of circuit are called Race around problem.

To avoide the Race around problem

① $T_{Pw} < T_{Pd_{FF}} < T_{Clk}$

② Master - slave FF

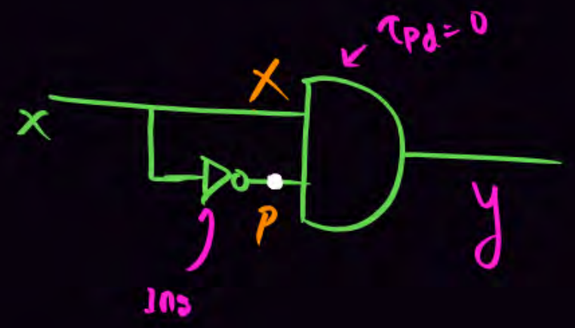
Master- slave FF



① Master- slave FF is use to store single bit because o/p is taken only from slave.

② Inverted clock is given to the slave as compared to Master.

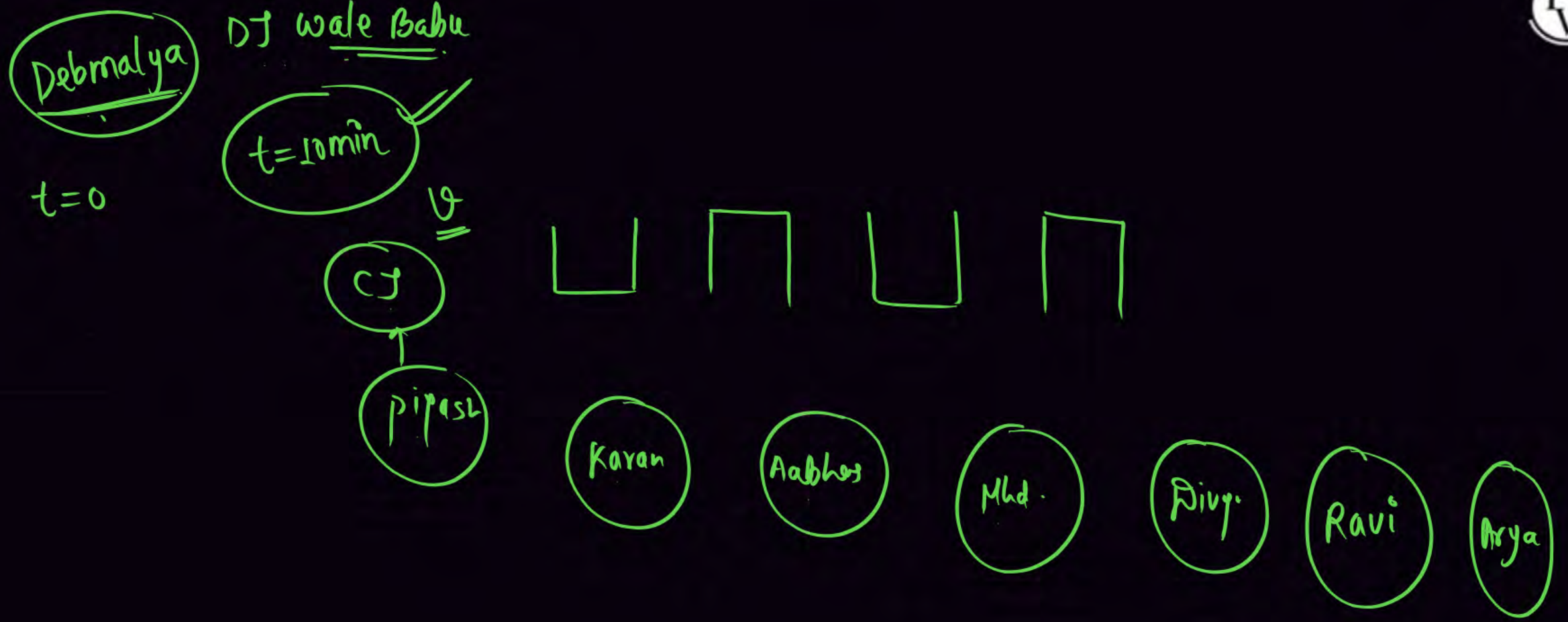
★ ③ By the operation it seems that master is Level triggered whereas slave is -ve edge triggered.



X

P

$y = x \cdot p$


Debmalya
DJ wale Babu
t=10min
t=0
CJ
Pipasl
Karan
Aabhas
Mhd.
Divy.
Ravi
Arya

Register

SHIFT REGISTER

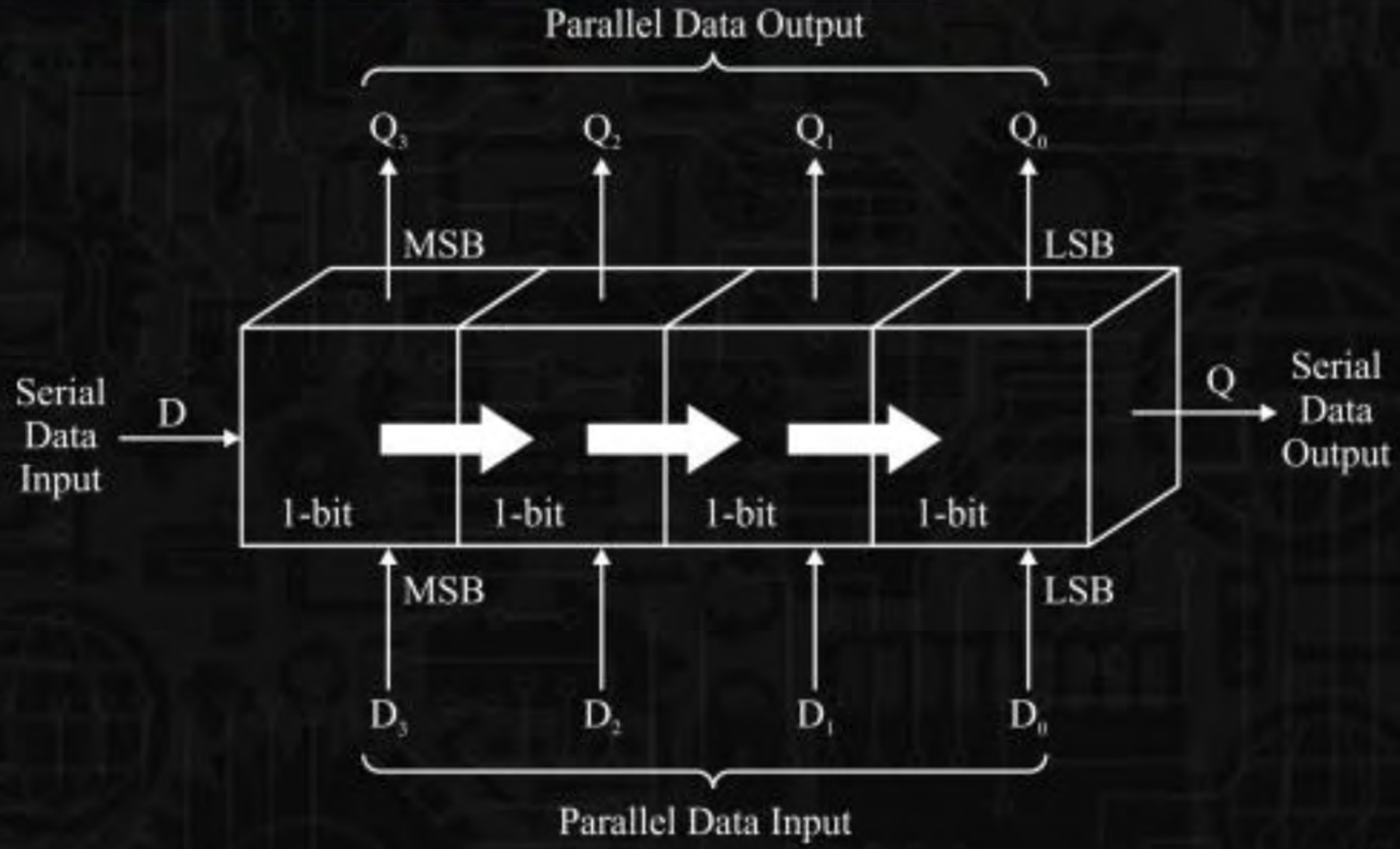
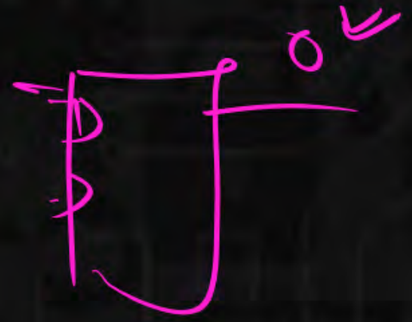


Figure 1: Shift Registers

SHIFT REGISTER

1. Registers are used to store group of bits
2. To store "n" bits minimum "n" Flip Flips are required
3. Generally D Flip Flops are used to Design Register



SHIFT REGISTER

1. Serial input serial output shift register [SISO]
2. Serial input parallel output shift register [SIPO]
3. Parallel input serial output shift register [PISO]
4. Parallel input parallel output shift register [PIPO]

① SERIAL INPUT SERIAL OUTPUT (SISO) SHIFT REGISTER

3bit SISO

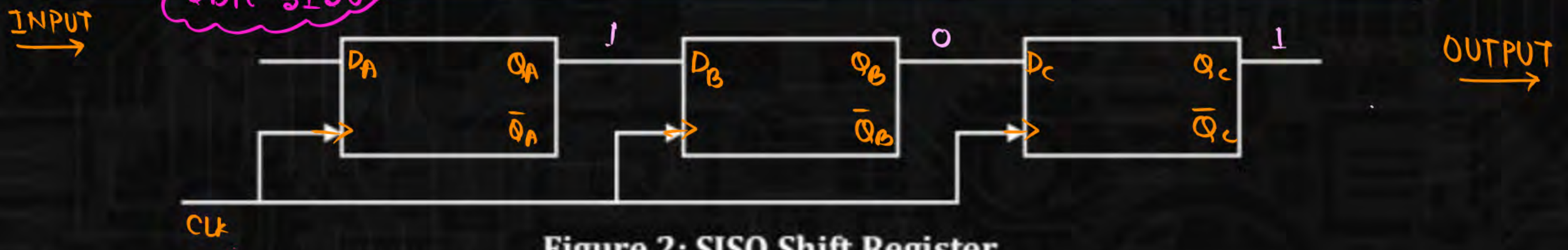


Figure 2: SISO Shift Register

Clock	Input	Q_A	Q_B	Q_C
0	1 0 1	0	0	0
1		1	0	0
2		0	1	0
3		1	0	1

- To store 'n" bits in "n" bit SISO minimum "n" clocks are required.

- To Retrive "n" bits from "n" bit SISO minimum (N-1) Clocks are required.

- Slowest shift Register among all the shift Register.

Q. If mode-5 counter is cascaded with mod-2 counter, then it will become?

A. Mod 10 counter

B. BCD Counter

C. Both A and B

D. None


THANK YOU GW
SOLDIERS !