EE, EC, CS & IT ENGINEERING



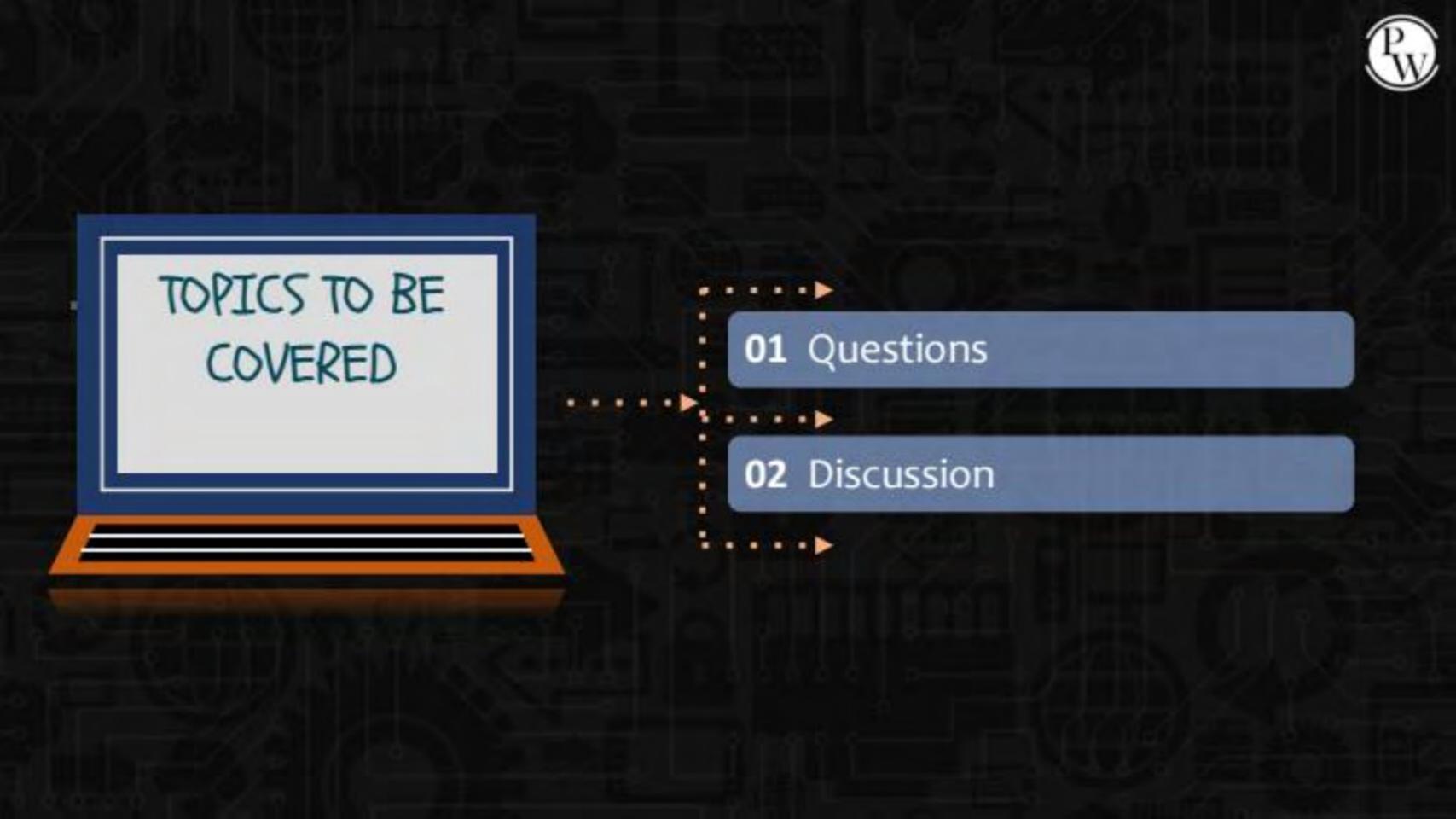
Digital Logic

ASYNCHRNOUS COUNTER-FEEDBACK

DPP Solution

04 Discussion Notes





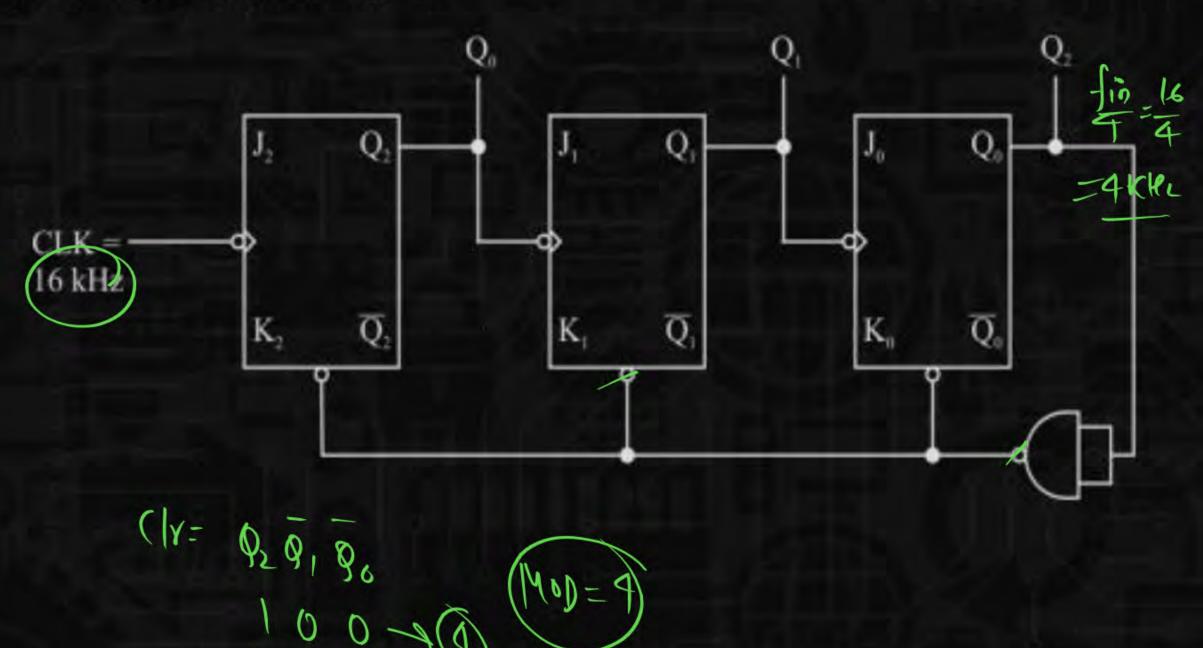
Q.1

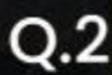
What is the output signal frequency of the following counter if the clock signal frequency is 16 kHz? All 'J' and 'K' inputs are connected to 1.





- B. 8 kHz
- c. 10 kHz
- D. 16 kHz

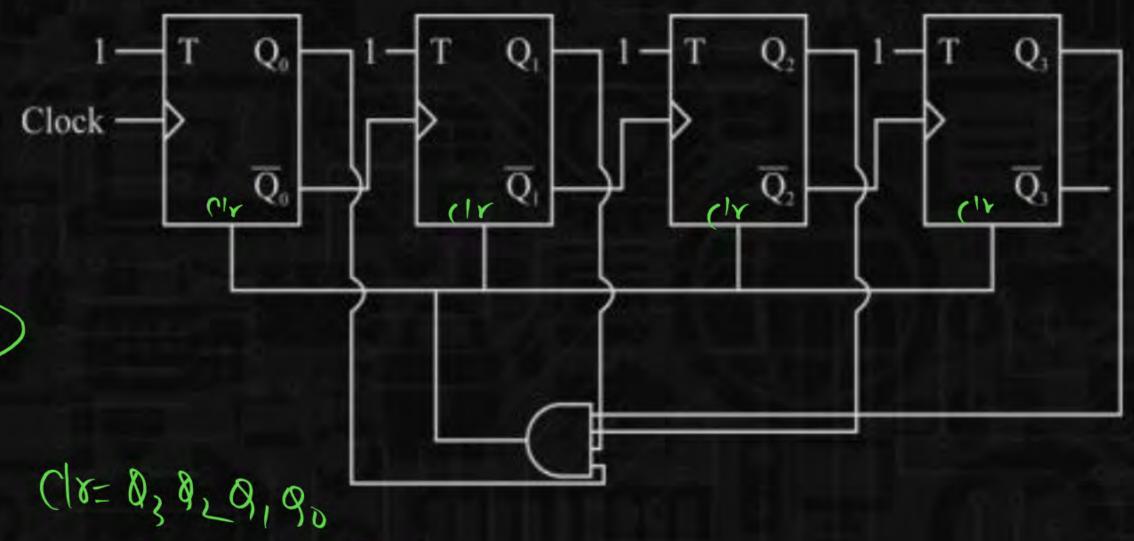


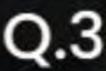




The circuit is counter of mod

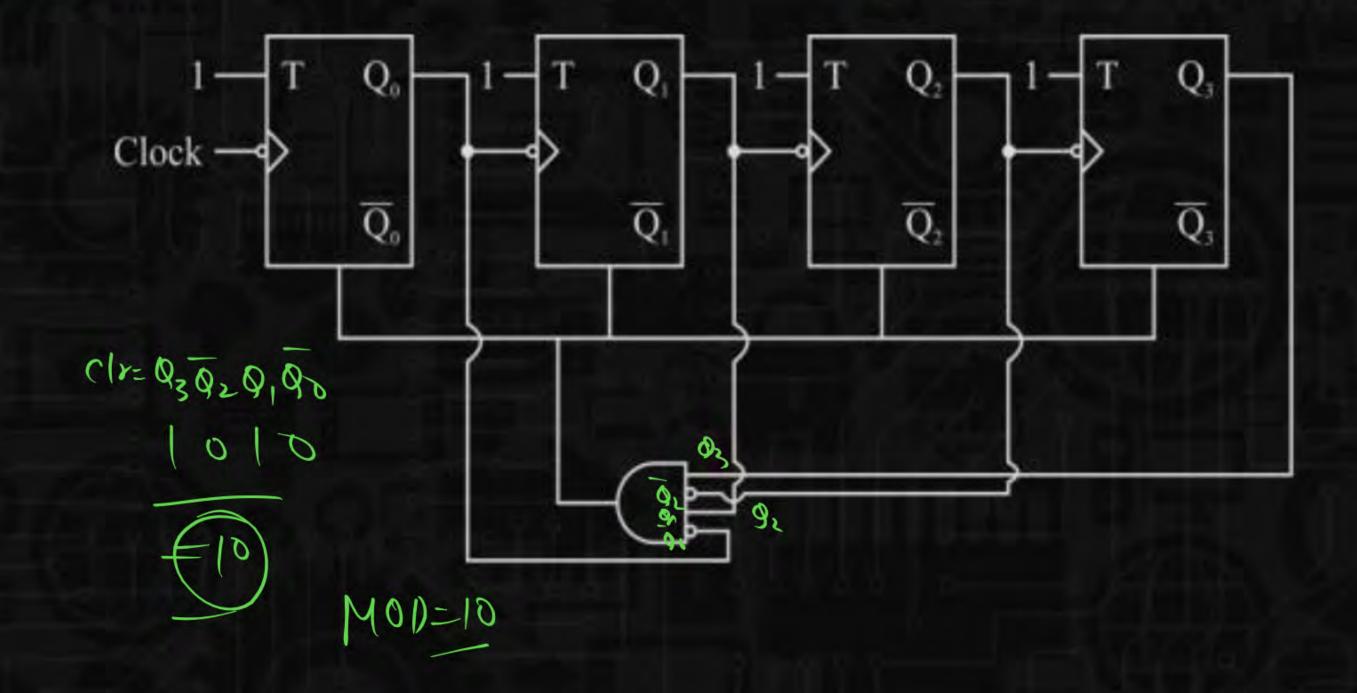
- A. Mod-0
- B. Mod-16
- Mod-15
- D. Mod-14





The circuit is a counter of mod

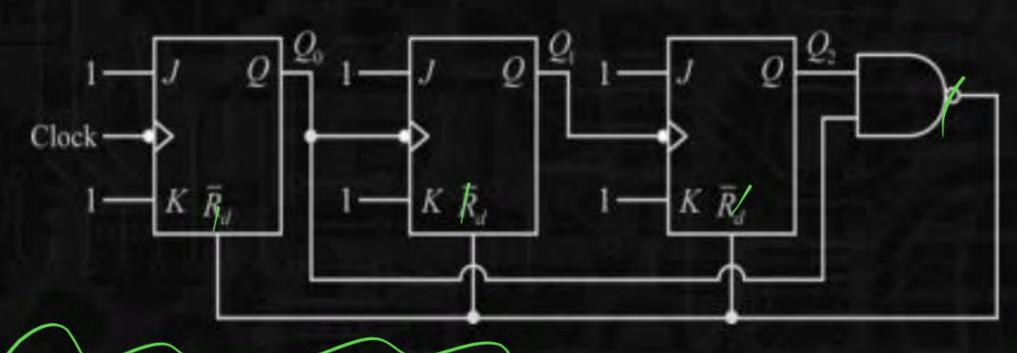






The circuit shown consists of J-K flip-flops, each with an active low asynchronous reset (\bar{R}_d input). The counter corresponding to this circuit is







a modulo-5 binary up counter.

В.

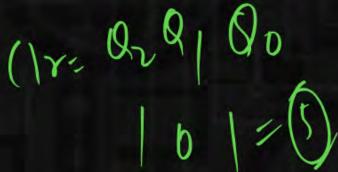
a modulo-6 binary down counter.

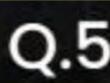
c.

a modulo-5 binary down counter.

D.

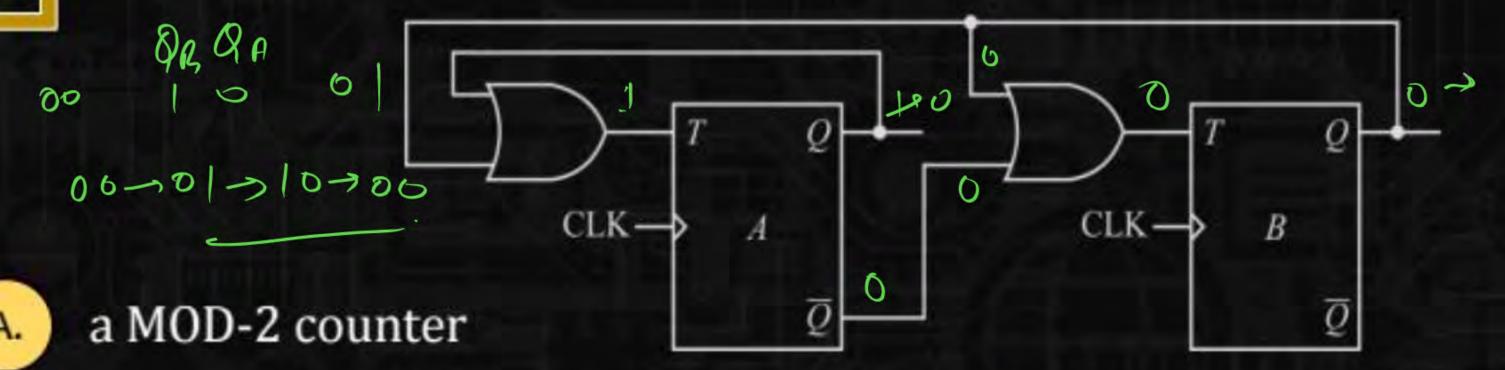
a modulo-6 binary up counter.





The circuit shown in figure is





a MOD-3 counter

generate sequence 00, 10, 01, 00..... 1 0 1

D. generate sequence 00, 10, 00, 10, 00 3 0 0



