

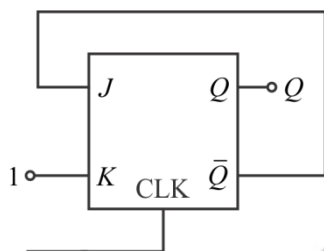
Subject : Digital Logic

DPP - 2

Chapter: Sequential Circuit

Topic : JK, D, T FF & FF Design

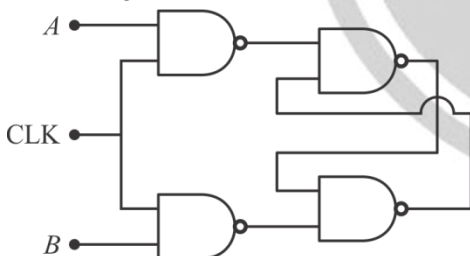
1. Consider the following J - K flip-flop



In the above J - K flip-flop, $J = \bar{Q}$ and $K = 1$. Assume that the flip-flop was initially cleared and then clocked for 6 pulses. What is the sequence at the Q output?

- (a) 010000 (b) 011001
(c) 010010 (d) 010101

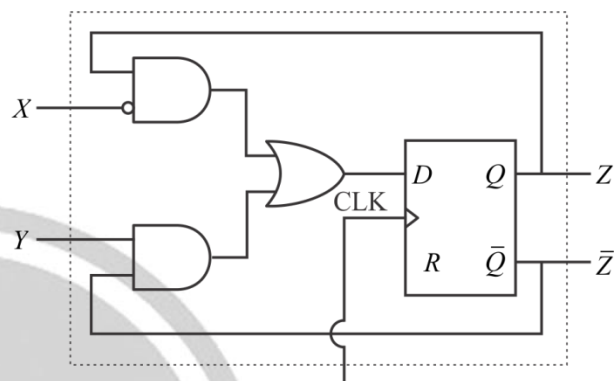
2. Consider the given circuit.



In this circuit, the race around

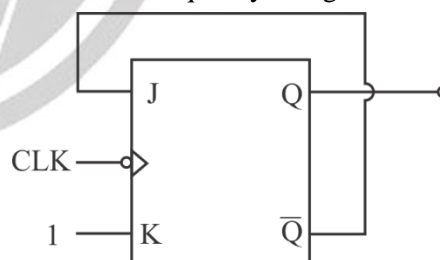
- (a) does not occur.
(b) occurs when $\text{CLK} = 0$.
(c) occurs when $\text{CLK} = 1$ and $A = B = 1$.
(d) occurs when $\text{CLK} = 1$ and $A = B = 0$.

3. A sequential circuit using D Flip-Flop and logic gates is shown in figure, where X and Y are the inputs and Z is the output. The circuit is



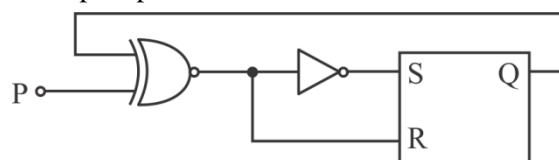
- (a) S - R Flip-Flop with inputs $X = R$ and $Y = S$.
(b) S - R Flip-Flop with inputs $X = S$ and $Y = R$.
(c) J - K Flip-Flop with inputs $X = J$ and $Y = K$.
(d) J - K Flip-Flop with inputs $X = K$ and $Y = J$.

4. The frequency of the clock signal applied to the negative going edge triggered JK flip flop shown below is 5 kHz. What is frequency of signal available at Q ?



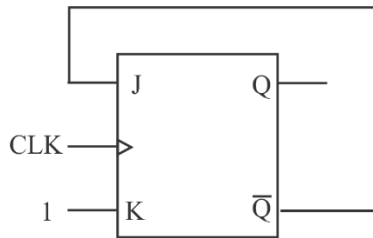
- (a) 2.5 kHz (b) 5 kHz
(c) 10 kHz (d) 1.25 kHz

5. The RS flip flop is modified so as to realize a flip flop with single input P . The characteristic equation of a new flip-flop will be



- (a) $Q(t+1) = P \oplus Q$
(b) $Q(t+1) = \overline{P \oplus Q}$
(c) $Q(t+1) = P + Q$
(d) $Q(t+1) = P$

6. The J-K FF shown below is initially cleared and then clocked for 5 pulses, the sequence at the Q output will be



- (a) 010000 (b) 011001

- (c) 010010 (d) 010101
7. For a J-K flip-flop, J input is tied to its own \bar{Q} output and its K input is connected to its own Q output. If the flip-flop is fed with a clock of frequency 1 MHz, its Q output frequency (in MHz) will be_____.



Answer Key

1. (d)
2. (a)
3. (d)
4. (a)
5. (a)
6. (d)
7. (0.5)



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