CS & IT ENGINEERING

DIGITAL LOGIC

SEQUENTIAL CIRCUIT

Counter part 2

Lecture No. 6

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01 Counters

02 Practice

03 Discussion

SHIFT REGISTER

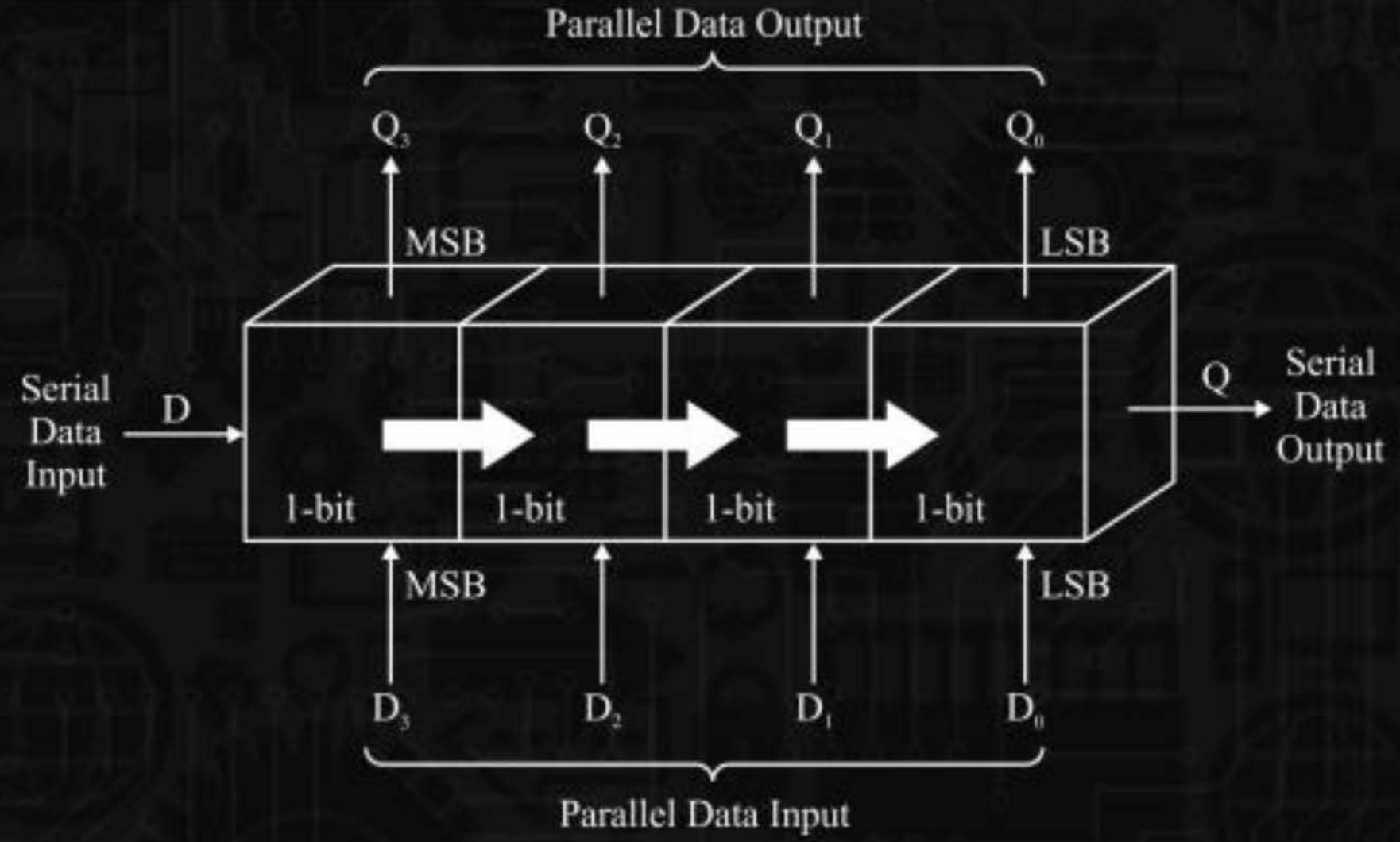


Figure 1: Shift Registers

SHIFT REGISTER

1. Registers are used to store group of bits
2. To store "n" bits minimum "n" Flip Flips are required
3. Generally D Flip Flops are used to Design Register

SHIFT REGISTER

1. Serial input serial output shift register [SISO]
2. Serial input parallel output shift register [SIPO]
3. Parallel input serial output shift register [PISO]
4. Parallel input parallel output shift register [PIPO]

SERIAL INPUT SERIAL OUTPUT (SISO) SHIFT REGISTER

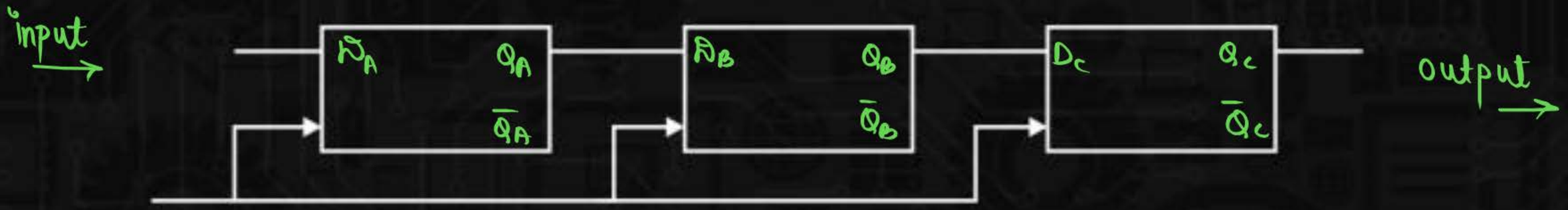


Figure 2: SISO Shift Register

Clock	Input	Q_A	Q_B	Q_C
0	1 0 1	0	0	0
1		1	0	0
2		0	1	0
3		1	0	1

Store ⟶ $n \cdot T_{clk}$

Retrive ⟶ $(n-1)\, T_{clk}$

② SERIAL INPUT PARALLEL OUTPUT (SIPO) SHIFT REGISTER

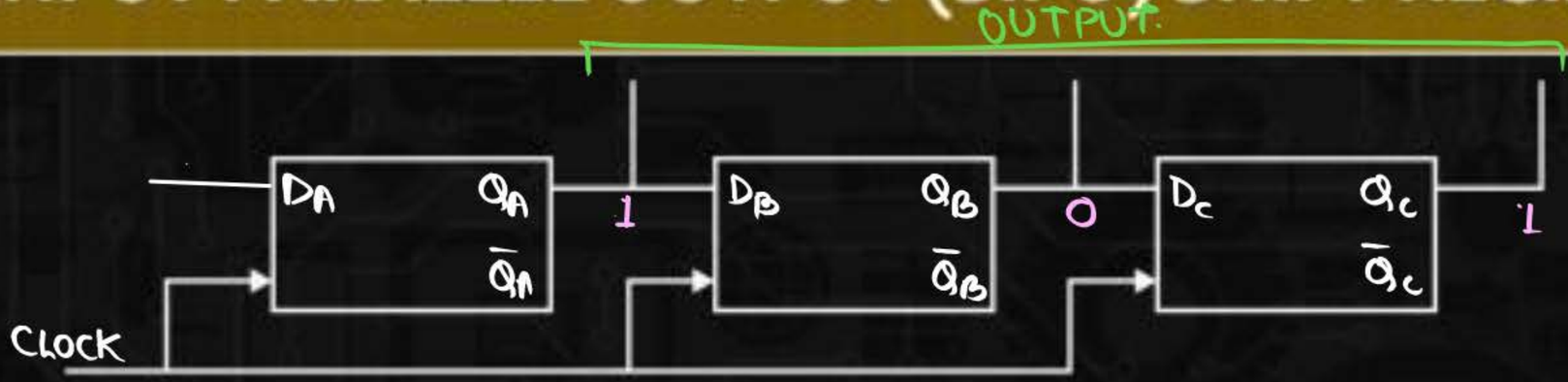


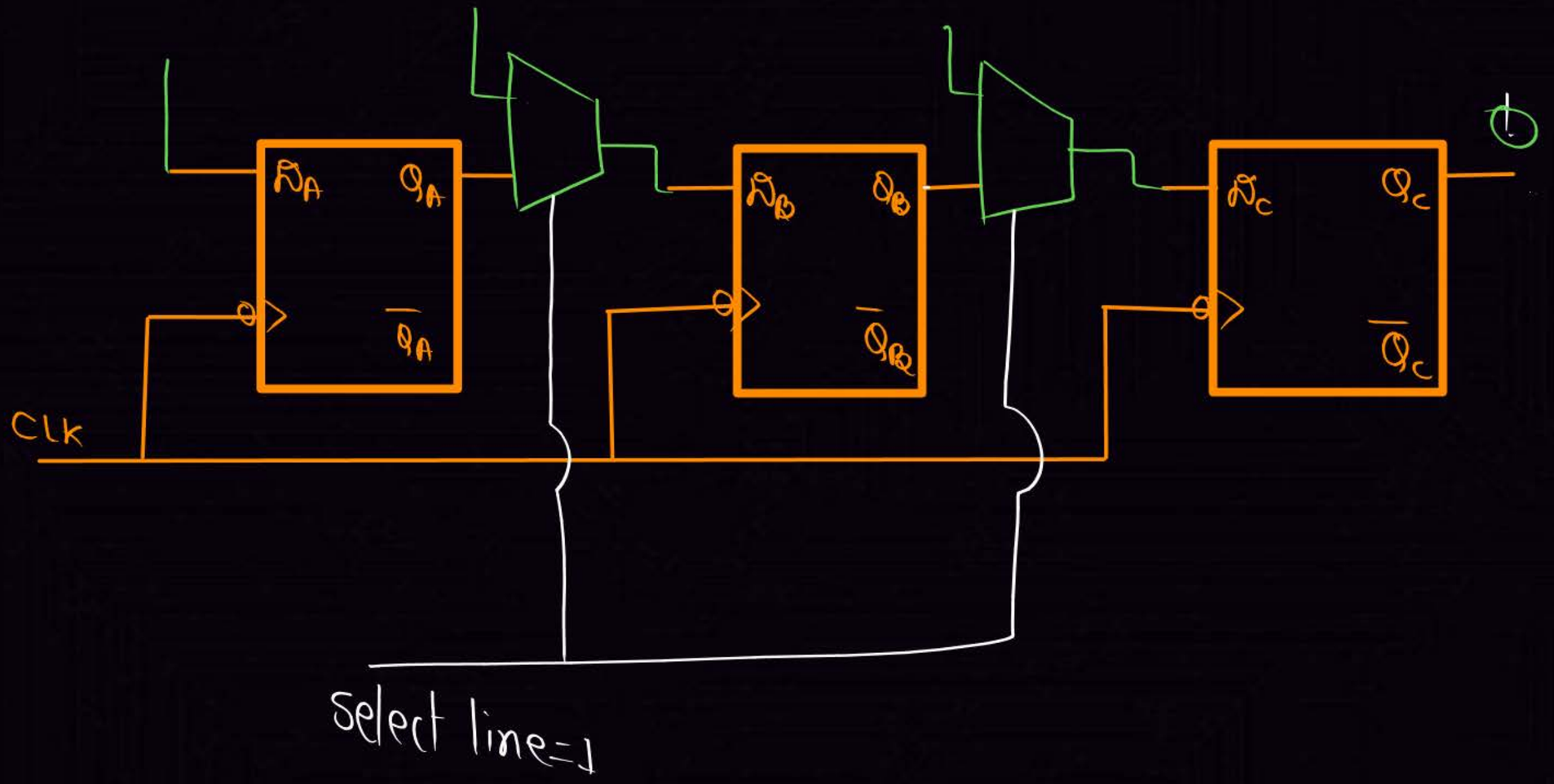
Figure 3: SIPO Shift Register

Clock	Input	Q_A	Q_B	Q_C
0	1 0 1	0	0	0
1		1	0	0
2		0	1	0
3		1	0	1

→ To store 'n' bit in 'n' bit SIPO minimum "n" clocks are required.

→ To Retrive "n" bits from 'n' bit SIPO there is no clock requirement.

③ Parallel input serial output shift Register :→ [PISO]



↳ To store "n" bit in "n" bit PISO minimum One clocks are required

↳ To Retrive "n" bits from "n" bit PISO minimum (n-1) clocks are required

PARALLEL INPUT PARALLEL OUTPUT (PIPO) SHIFT REGISTER

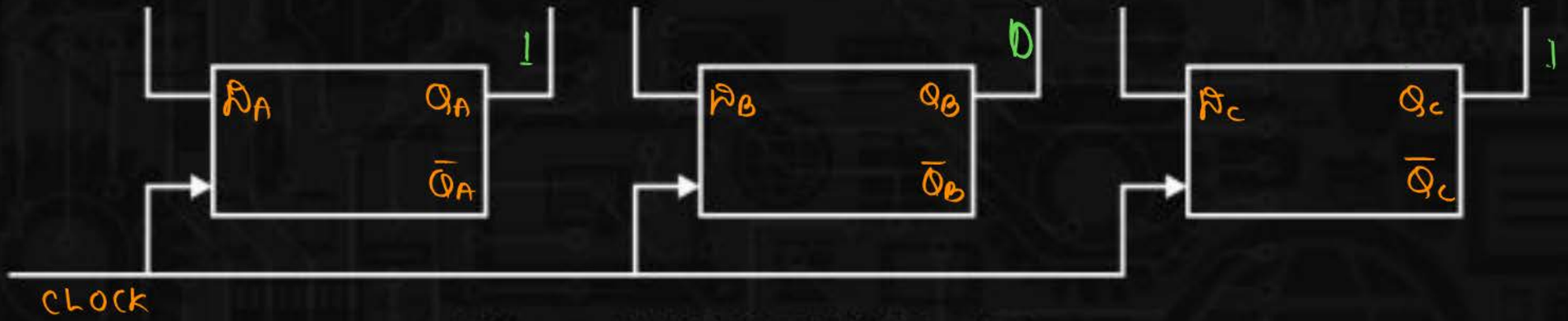


Figure 5: PIPO Shift Register

Clock	Input	Q_A	Q_B	Q_C
0	1 0 1	0	0	0
1		1	0	1
2				
3				

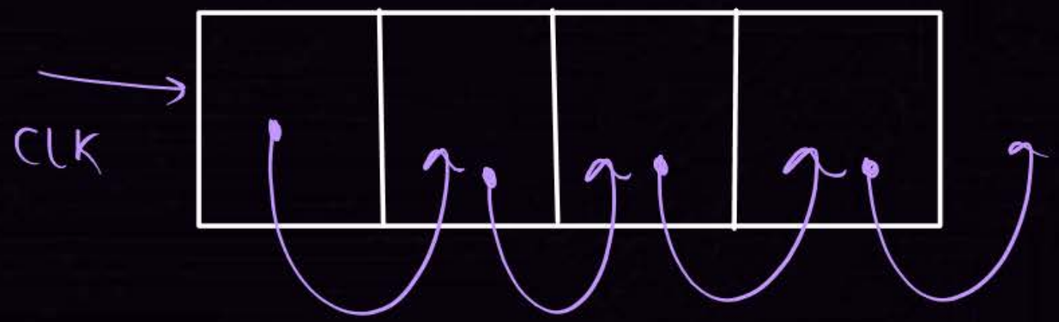
↳ To store "n" bits in n bit PIPO minimum one clock is required

↳ To Retrive "n" bits from n bit PIPO there is no clock requirement.

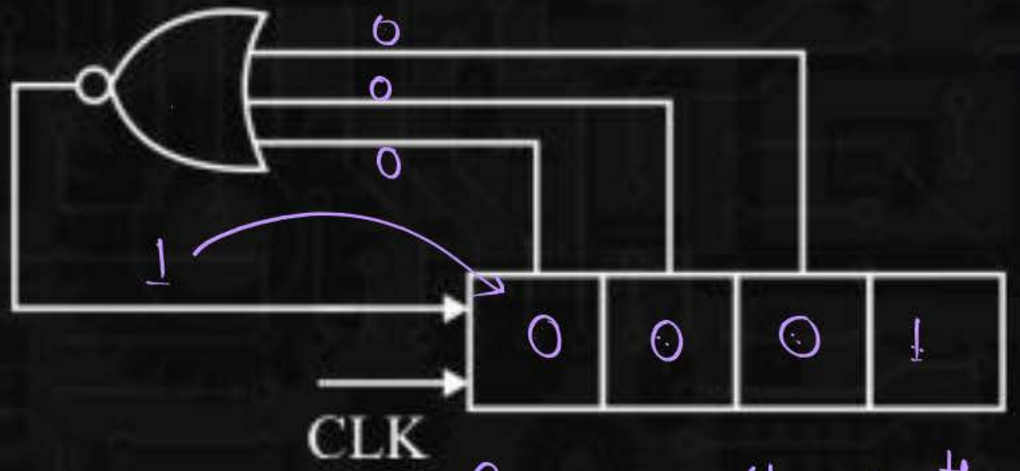
↳ PIPO is the fastest shift Register among all the shift Register.

	Store	Retrive	Total	
SISO	n	n-1	2n-1	→ slowest
SIPO	n	0	n	
PISO	1	n-1	n	
PIPO	1	0	1	→ fastest

Shift Register



Q. Write the state of the Register given below? (Assume initially all flips flops are reset)



9 5 1 → 1000 — R = 1
10 6 2 → 0100 — R = 2
11 7 3 → 0010 — R = 3
12 8 4 → 0001 — R = 0

after 100th
21 ==
106
4

R = 0

Clock	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0
6	0	1	0	0
7	0	0	1	0
8	0	0	0	1
9	1	0	0	0

					R
13	9	5	1	→ a	1
14	10	6	2	→ b	2
15	11	7	3	→ c	3
12	8	4		→ d	0

R = 0

Mentos zindgi

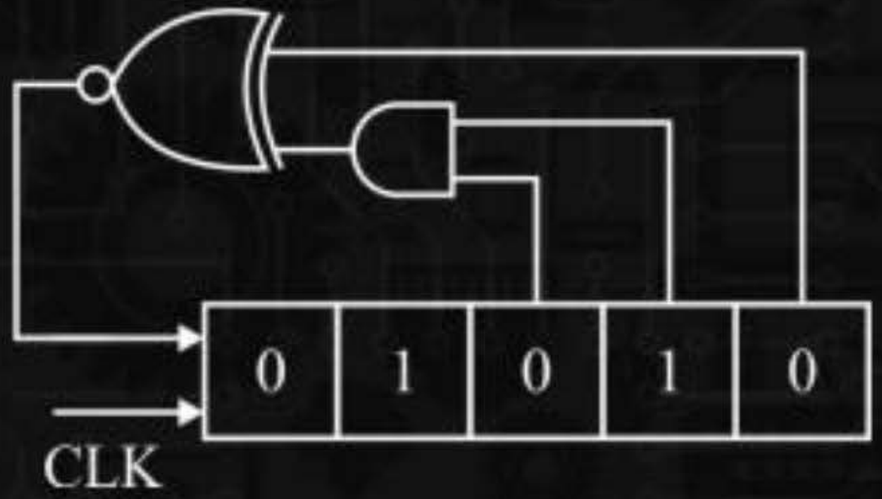
50 Rs

10th

4

(2)

Q. After 137th clock the output will be?



Clock	Q_4	Q_3	Q_2	Q_1	Q_0
0	0	1	0	1	0
1	1	0	1	0	1
2	0	1	0	1	0
3	1	0	1	0	1
4	0	1	0	1	0
5	1	0	1	0	1
6	0	1	0	1	0
7	1	0	1	0	1
8					
9					
10					
11					
12					
13					
14					

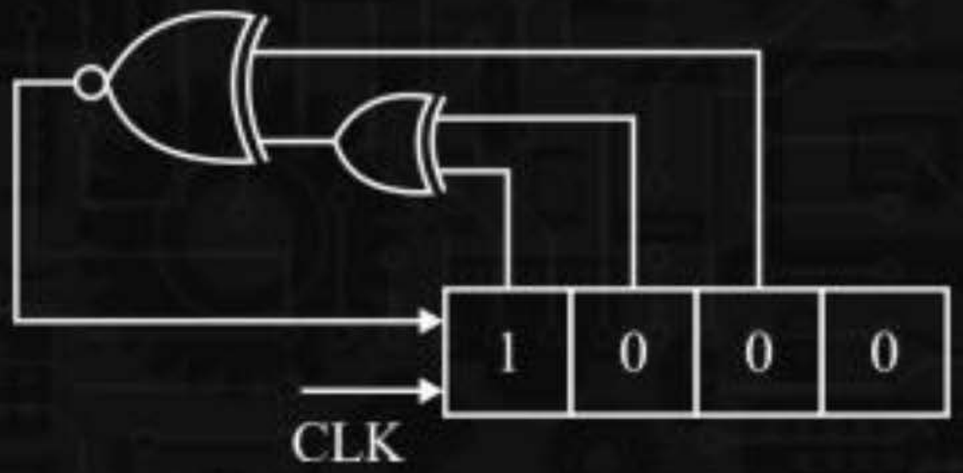
odd

odd

even

10101

Q. HW After 97th clock the output ill be?



Clock	Q_3	Q_2	Q_1	Q_0
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				


THANK YOU GW
SOLDIERS !