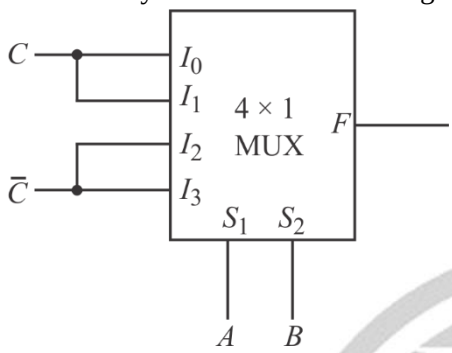
CS & IT

Digital Logic
MUX Part 2

DPP - 2

1. The logic realized by the circuit shown in figure is



(a) $F = A \odot C$ (b) $F = A \oplus C$

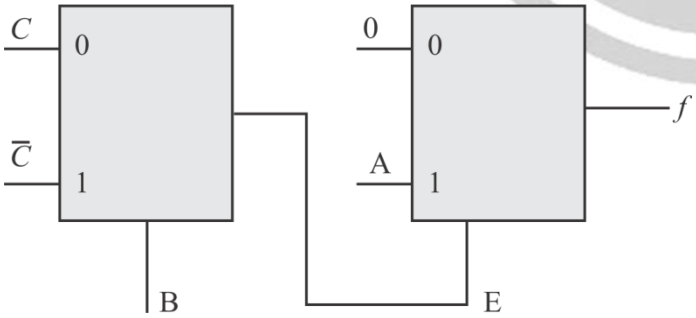
(c) $F = B \odot C$ (d) $F = B \oplus C$

2. The minimum number of 2-to-1 multiplexers required to realize a 4-to-1 multiplexer is

(a) 1 (b) 2

(c) 3 (d) 4

3. The Boolean function f implemented in the figure using two input multiplexers is



(a) $A\bar{B}C + AB\bar{C}$ (b) $ABC + A\bar{B}\bar{C}$

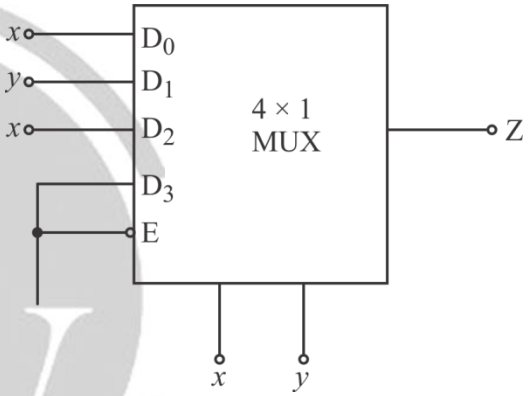
(c) $\bar{A}BC + \bar{A}\bar{B}\bar{C}$ (d) $\overline{ABC} + \bar{A}B\bar{C}$

4. A designer has multiplexer units of size 2 × 1 and multiplexer of size 16 × 1 is to be realized. The number of units of 2 × 1 MUXs required, will be

(a) 30 (b) 7

(c) 15 (d) 11

5. The logic function implemented by 4 × 1 MUX, is



(a) $Z = xy$ (b) $Z = x + y$

(c) $Z = \overline{x + y}$ (d) $x \oplus y$

6. The minimum number of multiplexers of size 2 × 1 required to implement a 2-input XNOR gate and 2-input AND gate, are

(a) 1 and 1 (b) 2 and 1

(c) 2 and 2 (d) 3 and 1

Answer Key

1. **(b)**
2. **(c)**
3. **(a)**
4. **(c)**
5. **(d)**
6. **(b)**

Hints and solutions

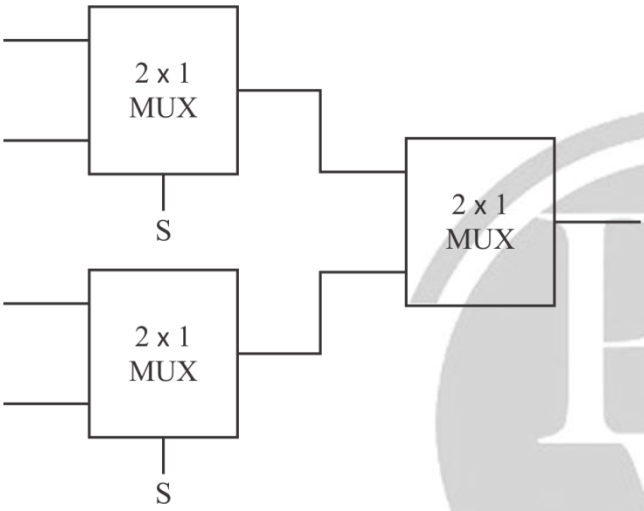
1. $F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + AB\bar{C}$

$F = \bar{A}C(B + \bar{B}) + A\bar{C}(B + \bar{B})$

$F = \bar{A}C + A\bar{C}$

$F = A \oplus C$

2.



3. $E = \bar{B}C + B\bar{C}$

$f = AE$

$f = A(\bar{B}C + B\bar{C})$

$f = A\bar{B}C + AB\bar{C}$

4. $\frac{16}{2} = 8$

$\frac{8}{2} = 4$

$\frac{4}{2} = 2$

$\frac{2}{2} = 1$

$\overline{15}$

Total 15 2×1 MUX required to implemented 16×1 MUX.

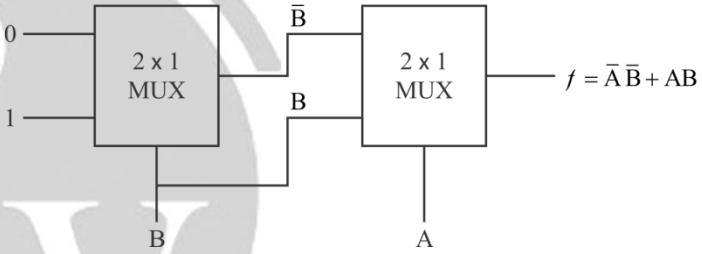
5. $z = \bar{x}\,y\,x + \bar{x}\,y\,y + x\,\bar{y}\,x + x\,y \cdot 0$

$z = \bar{x}\,y + x\,\bar{y}\,x$

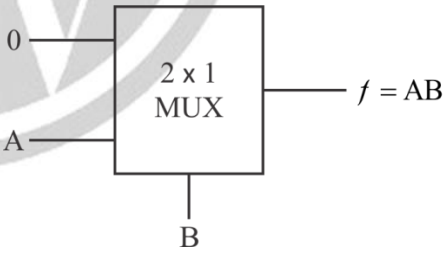
$z = \bar{x}\,y + x\,\bar{y}$

$z = x \oplus y$

6. X-NOR gate implementation



Two 2×1 MUX required to implementation X-NOR gate.



One 2×1 MUX required to implementation AND gate.