

EE, EC, CS & IT ENGINEERING

Digital Logic
Sequential circuit



LATCHES

DPP Solution 01

Discussion NOTES



By- CHANDAN SIR

TOPICS TO BE COVERED

01 Questions

02 Discussion

Q.1

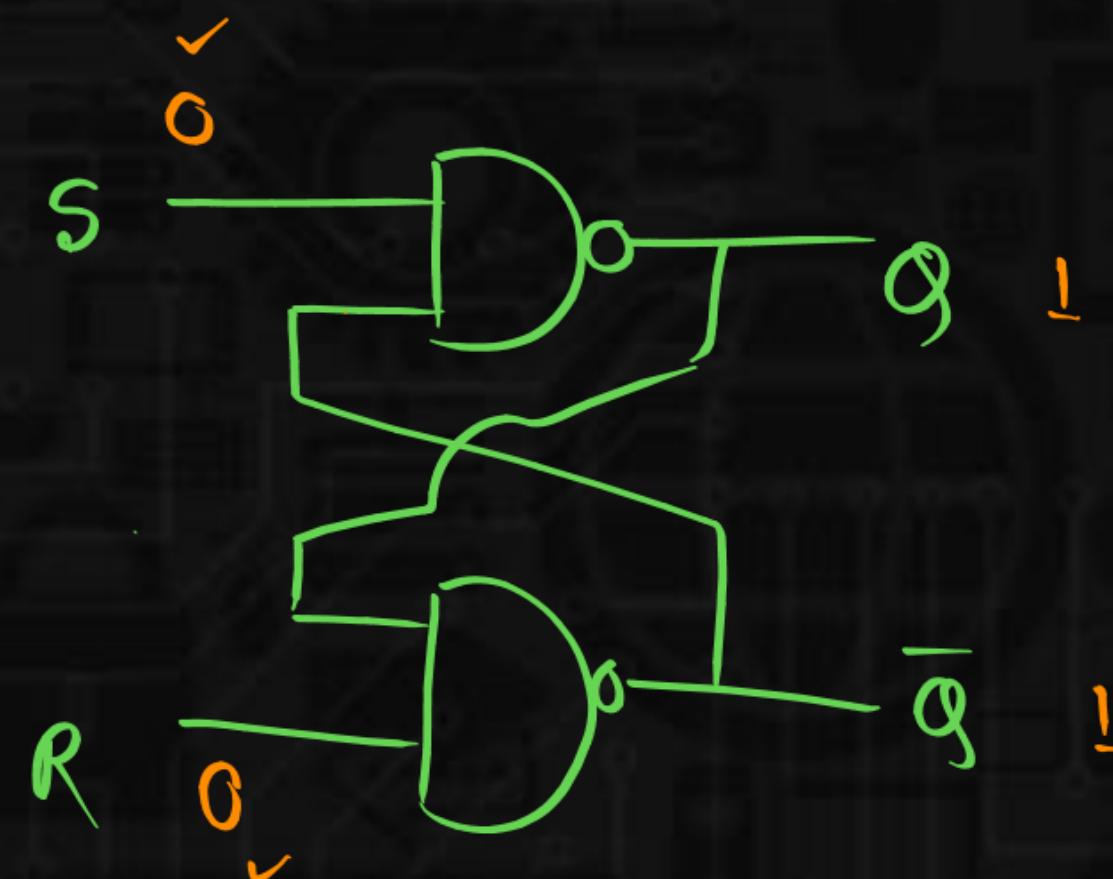
In an SR latch made by cross-coupling two NAND gates, if both S and R inputs are set to 0, then it will result in

A. $Q = 0, Q' = 1$

B. $Q = 1, Q' = 0$

C. $Q = 1, Q' = 1$ *InValid*

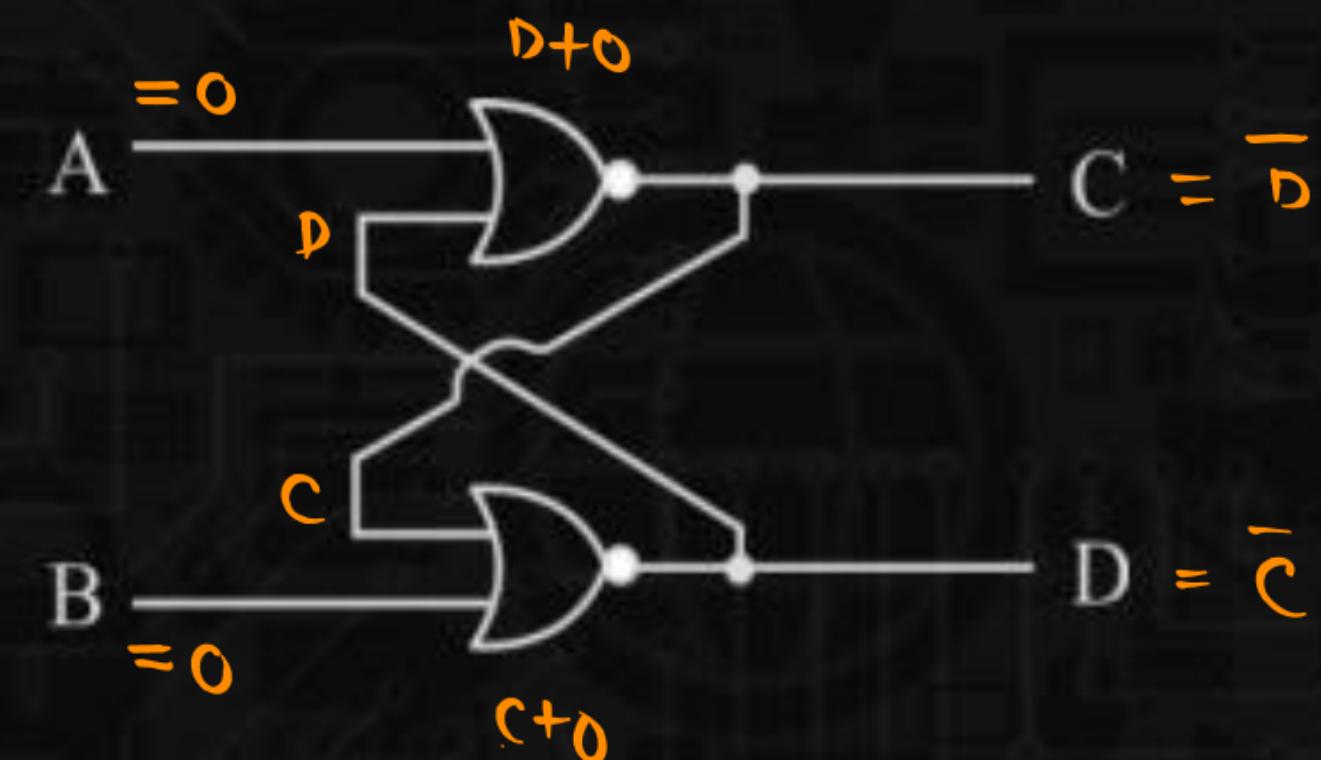
D. Indeterminate states



Q.2

In the circuit shown below, when inputs $A = B = 0$, the possible logic states of C and D are

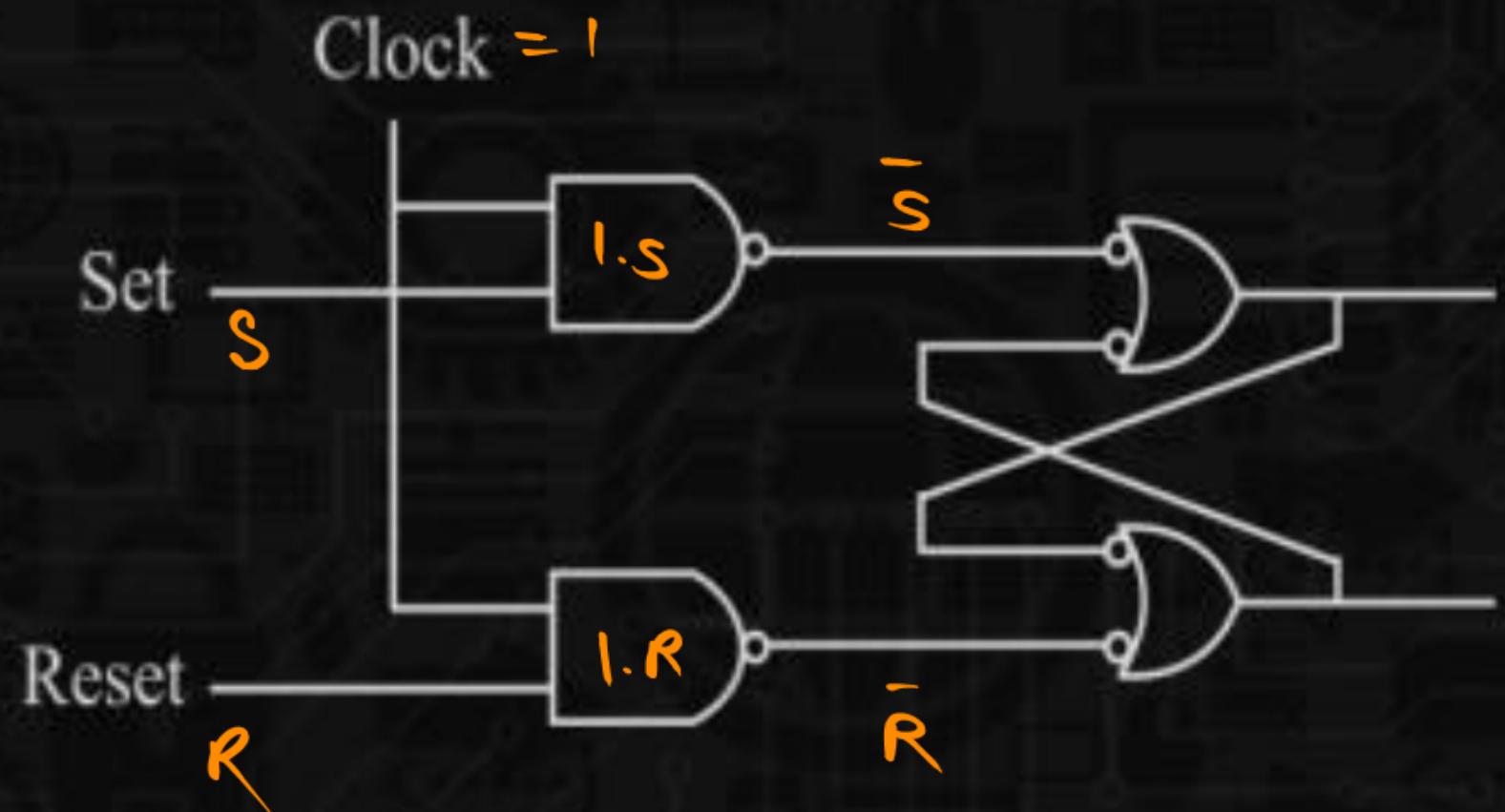
- A. $C = 0, D = 1$ or $C = 1, D = 0$
- B. $C = 1, D = 0$
- C. $C = 1, D = 1$ or $C = 0, D = 0$
- D. $C = 0, D = 1$



Q.3

The two NAND gates before the latch circuit shown below, are used to

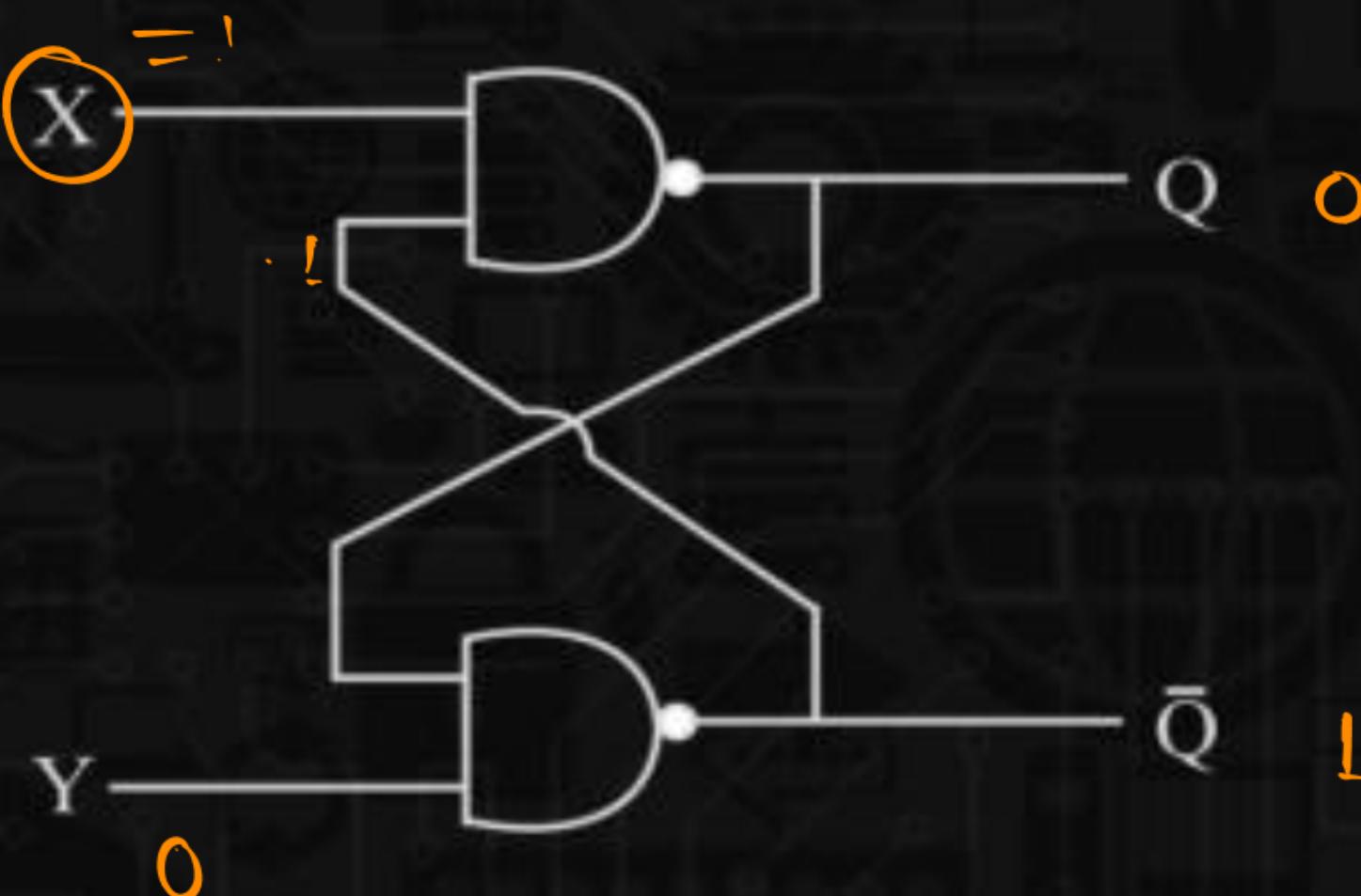
- A. act as buffers
- B. operate the latch faster
- C. avoid racing
- D. invert the latching action



Q.4

In the circuit shown below, outputs $Q\bar{Q} = 01$, the possible values of X and Y are

- A. $X = 1, Y = 0$
- B. $X = 1, Y = 1$
- C. $X = 0, Y = 1$
- D. $X = 0, Y = 0$



Q.5

Latch is a device with

- A. One stable state
- B. Two stable state
- C. Three stable state
- D. Infinite stable states

