CS & IT

NOT GATE , AND, OR GATE

Logic gate

Lecture No. 1

By- CHANDAN SIR

01 Syllabus

02 Weightage

03 Reference Books

04 NOT GATE

05 AND GATE

OR GATE

CS & IT ENGINEERING

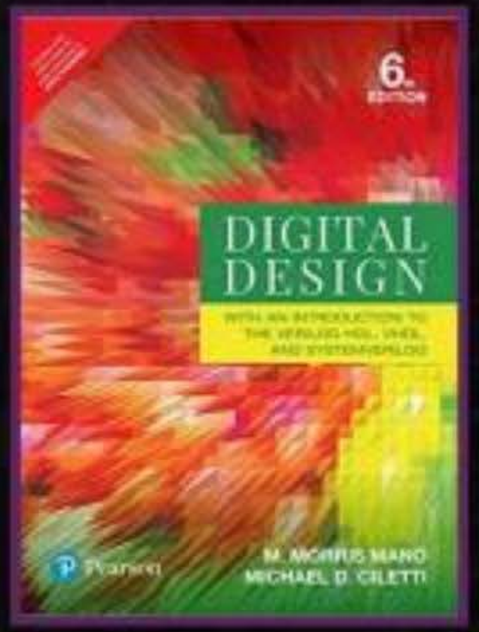
Digital Logic

Boolean algebra. Combinational and sequential circuits. Minimization. Number representations and computer arithmetic (fixed and floating point).

CS & IT ENGINEERING

DIGITAL LOGIC	
No. of Questions	2 to 4
Marks	4 to 6
Frequently Asked Topics	Boolean algebra. Combinational and sequential circuits. Minimization. Number representations

Reference Books



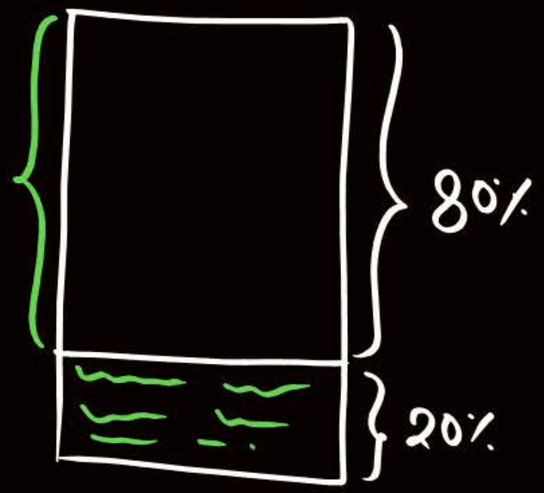
Book Name: Digital Design
Author: M. Morris Mano & Michael D. Ciletti
Publisher: Pearson Publishers

Book Name: Digital fundamental
Author: Thomas L. Floyd
Publisher: Pearson Publishers

Guidelines to Attend Live Class

- ✓ Attend the class with positive attitude.
- ✓ Punctuality is necessary.
- ✓ Follow the day-wise study plan.
- ✓ Attempt DPP daily as per the schedule.
- ✓ Hold chat while attending the class. We will allow you to ask and put your questions in the comment box.

CLASS NOTES



chapter-1

20 pages

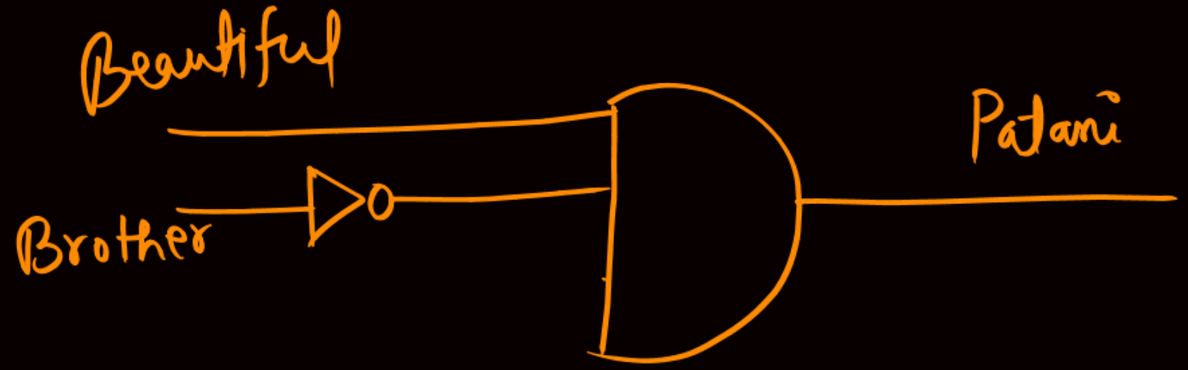
2 pages

chapter

300 pages

Short NOTES

GATE-O-PEDIA


Beautiful
Brother
Patani

CS

S.N.	Chapter	TOPIC
1	Logic Gate	NOT, AND, OR, NAND, NOR, X-OR, X-NOR
2	Minimization	Boolean algebra, K-MAP
3	Combinational Circuit	Designing, Comparator, MUX, DE-MUX, Encoder, Decoder, HA, FA, HS, FS, Serial adder, parallel adder, LACA
4	Sequential Circuit	Latches, Flip-Flops, Registers, counters
5	Number System	Base conversion, Magnitude Representation

Questions.

DPP → 150 question.

Theory → NOTES.

① Previous Year GATE → 20 years.

- CS → 300
- EC → 300
- EE → 300
- IN → 300

1200

Books < unsolved ✓ / solved ✓

Kanodia → 500

1700

Flip-Flop

JK Flip-Flop

Jack Keilby

IC → Integrated circuit

→ papa of IC

1 element → 1958

2 element → 1960

4 element → 1962

8 element → 1964

14 years

1965

Gorden E. Moore

1962 → "दुकान"

Intel

Nobel prize

Statement

Moore's Law

+ve Logic.

0 ⟶ Low Voltage

1 ⟶ High Voltage.

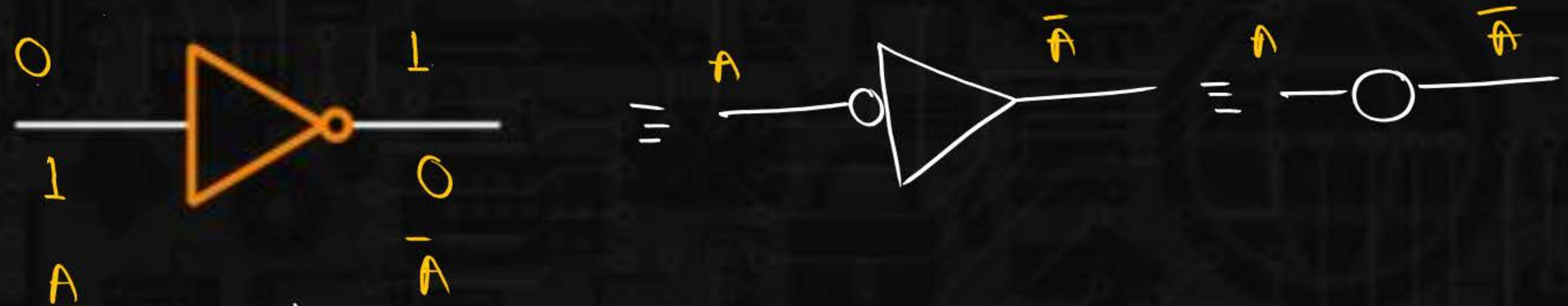
1 ⟶ 10V
0 ⟶ 2V
} +ve Logic.

INVERTER & AND GATE

LOGIC GATE

1. NOT GATE [INVERTER, NEGATION]

1)

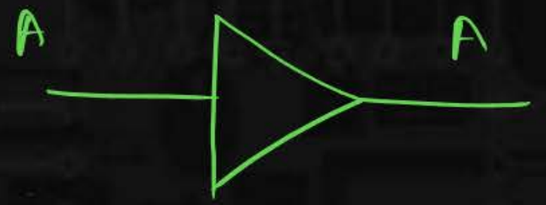


→ propagation delay (τ_{pd})

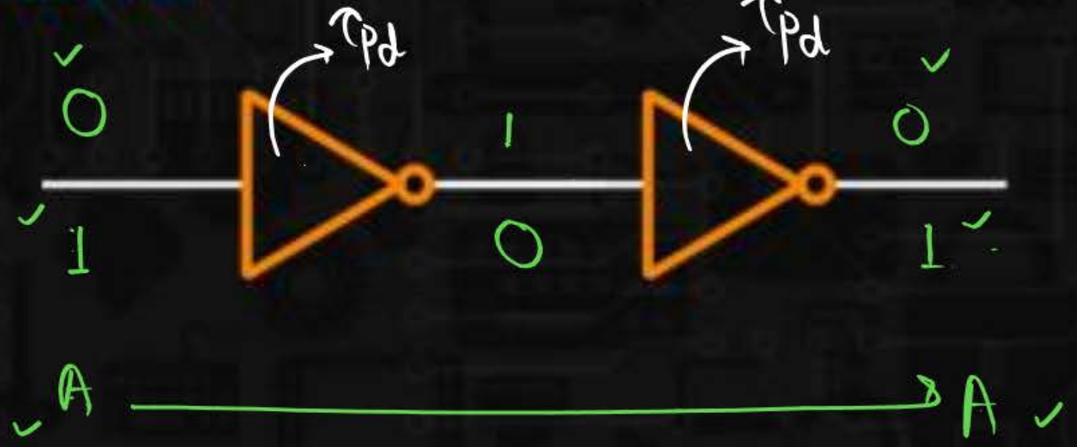
INVERTER & AND GATE

LOGIC GATE

1. NOT GATE



2)



Buffer

→ used to provide Delay.

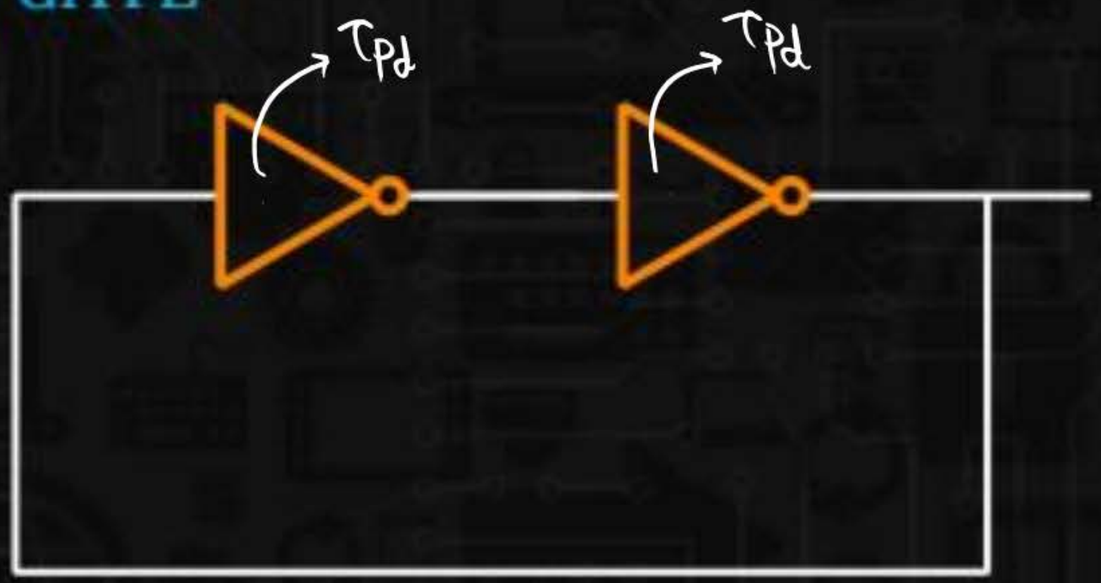
INVERTER & AND GATE

LOGIC GATE

1. NOT GATE

When Even no. of NOT GATE in Loop :→

3)



$2\tau_{pd}$ $2\tau_{pd}$ $2\tau_{pd}$

✓ 1 → 1 → 1 → . . .

$2\tau_{pd}$ $2\tau_{pd}$ $2\tau_{pd}$

✓ 0 → 0 → 0 → . . .

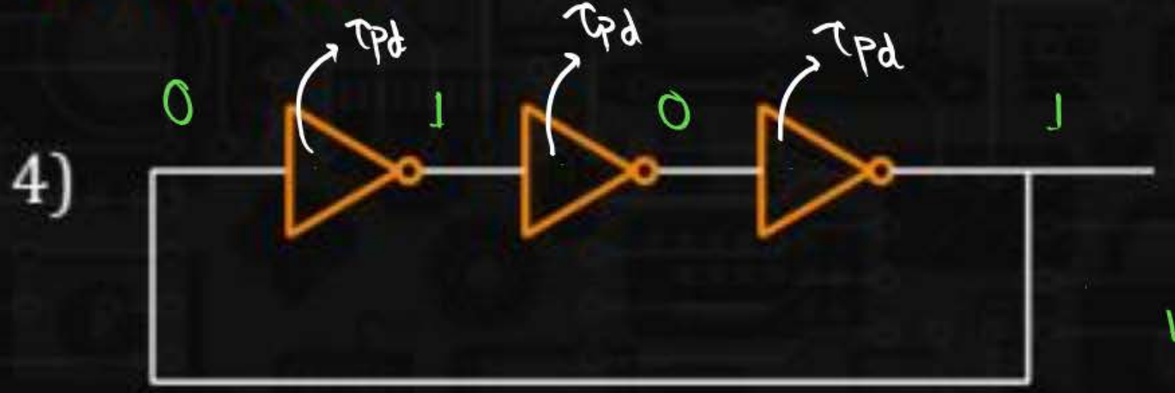
{ 1> Basic memory element
{ 2> Bistable Multivibrator

INVERTER & AND GATE

LOGIC GATE

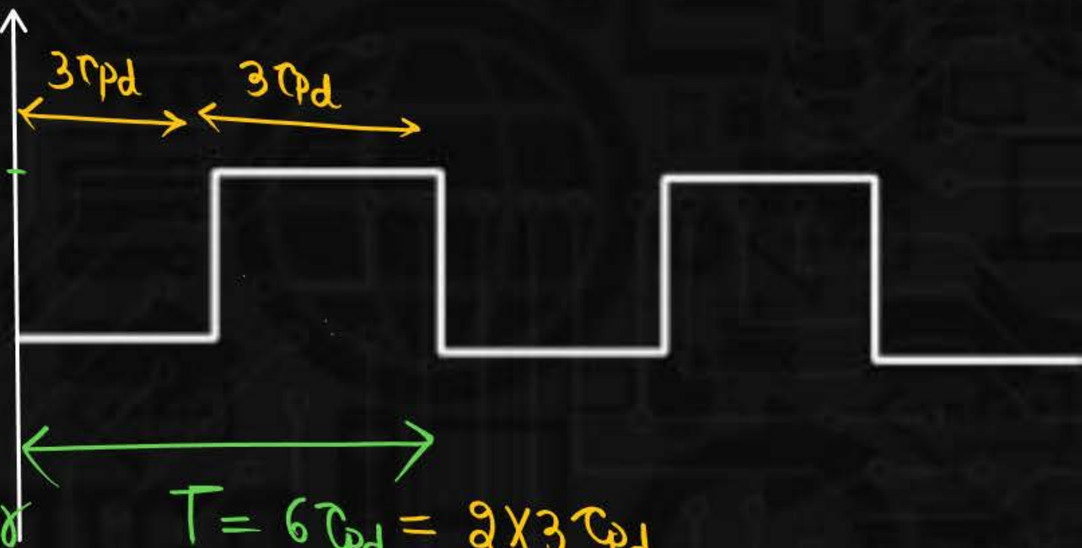
1. NOT GATE

When ODD number of NOT GATES in Loop :-



$3\tau_{pd}$ $3\tau_{pd}$ $3\tau_{pd}$ $3\tau_{pd}$

0 → 1 → 0 → 1 →



1. Astable multivibrator
2. Square wave generator
3. clock generator
4. Free Runing circuit
5. Ring oscillator

$$T = 2 \times N \times \tau_{pd}$$

$$T = 2 \times N \times \tau_{pd}$$

N → No. of NOT GATE in Loop

τ_{pd} → Propagation Delay of NOT GATE

$$f = \frac{1}{T} = \frac{1}{2N \times \tau_{pd}}$$

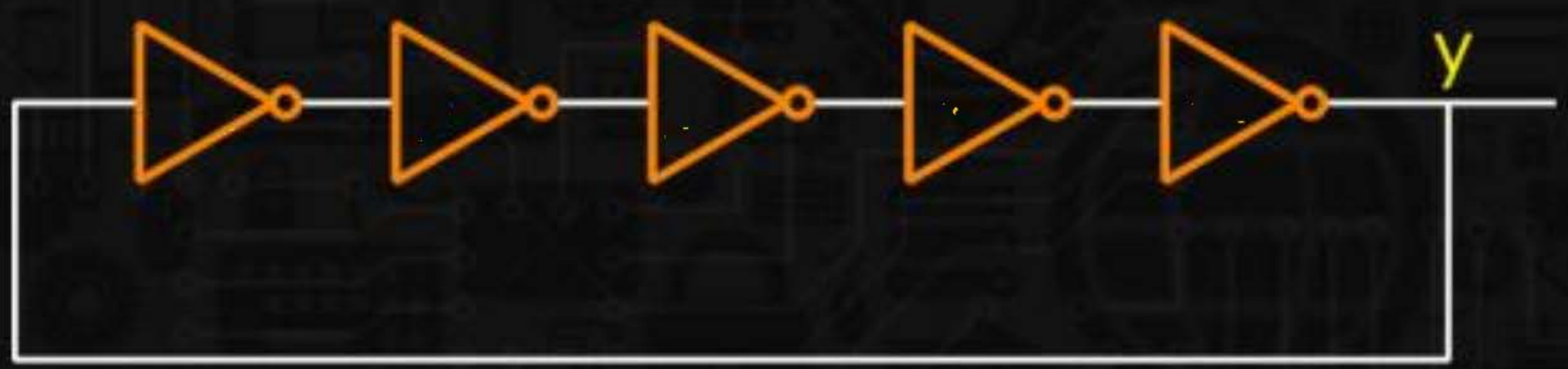
Q.1 For the circuit given below, all NOT Gates are identical to each other and having propagation delay 10 ps. Find the frequency of generated wave form?

↳ 10^{-12}

$$f = \frac{1}{2N \times \tau_{pd}}$$

$\tau_{pd} = 10 \times 10^{-12}$ sec

$N \rightarrow 5$



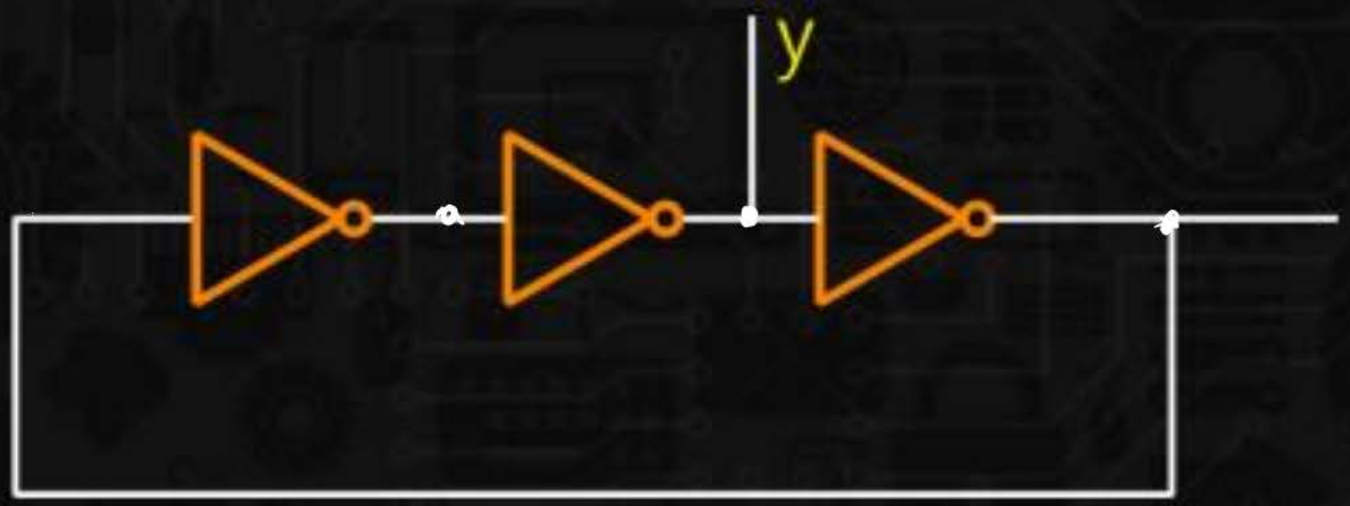
$$f = \frac{1}{2 \times 5 \times 10 \times 10^{-12}} \text{ Hz}$$

$$f = \frac{10^{12}}{10 \times 10} \text{ Hz} = \frac{1000 \times 10^{9}}{10 \times 10} \text{ Hz}$$

$= 10 \times 10^{9}$ Hz

$f = 10$ GHz Ans

Q.2 Circuit given below are called.

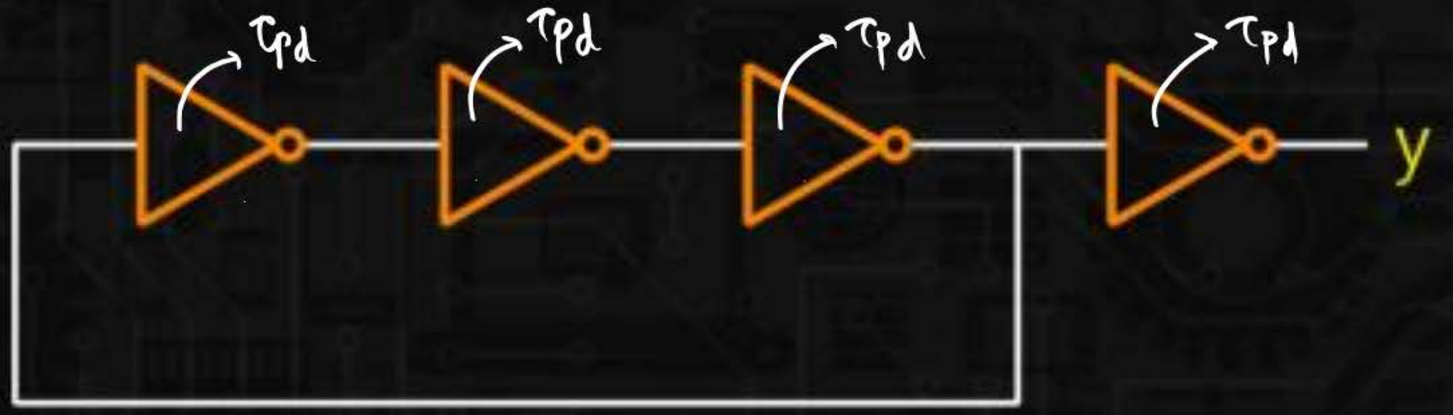


(A) Astable multivibrator

(B) Bistable multivibrator

Q.3 Sketch the waveform of y?

HW



Q.4 For the circuit given below x & y condition will be–

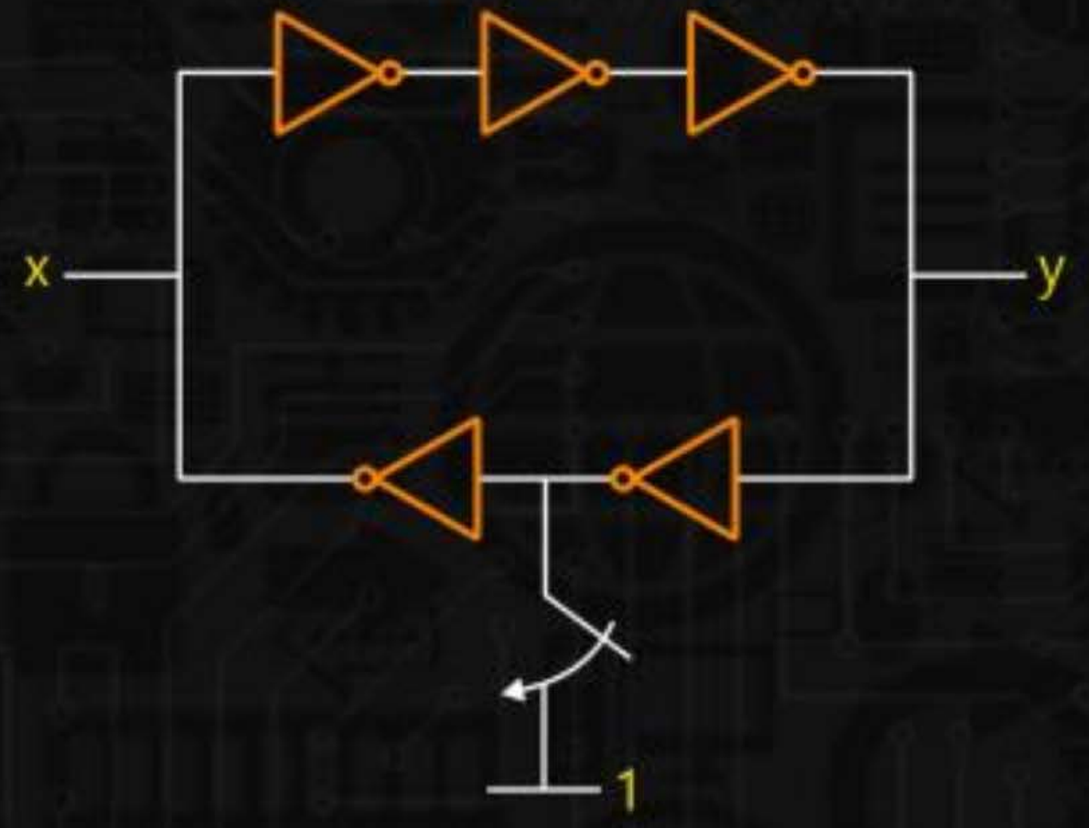
HW

A. x stable y toggle

B. x toggle y stable

C. x & y both toggle

D. x & y both stable




THANK YOU GW
SOLDIERS !