

EE, EC, CS & IT ENGINEERING

Digital Logic
Logic Gate



OR, NAND and NOR Gate

DPP Solution 02 Discussion



By- CHANDAN SIR

TOPICS TO BE COVERED

01 Questions

02 Discussion

Q.1

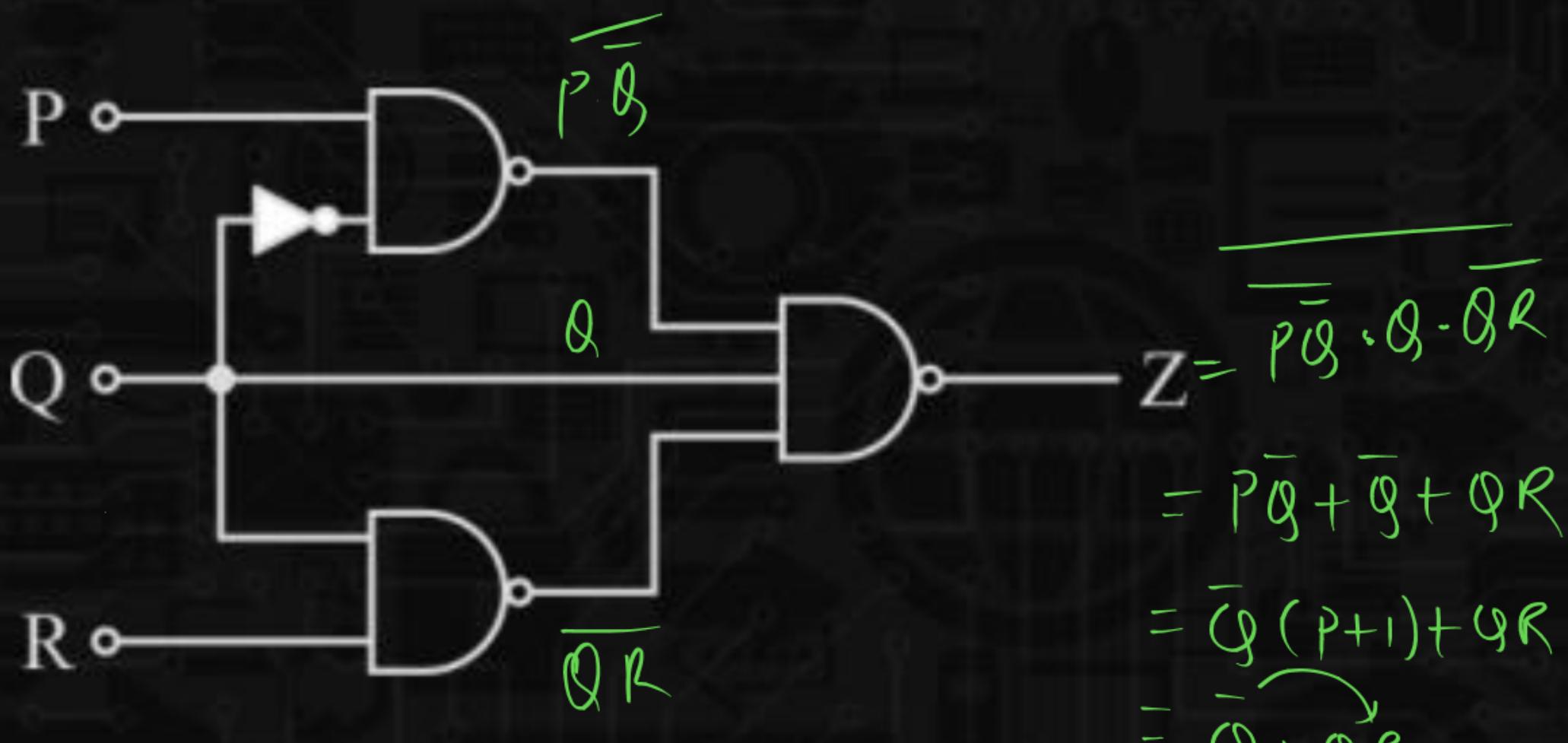
For a 3-input logic circuit shown below, the output Z can be expressed as

A. $Q + \bar{R}$

B. $P\bar{Q} + R$

C. $\bar{Q} + R$

D. $P + \bar{Q} + R$



$$\begin{aligned}Z &= \overline{\overline{P}\bar{Q} \cdot \bar{Q} \cdot \bar{Q}\bar{R}} \\&= \overline{\overline{P}\bar{Q}} + \overline{\bar{Q}} + \overline{Q}\bar{R} \\&= \overline{\bar{Q}(P+1)} + \overline{Q}\bar{R} \\&= \overline{\bar{Q}} + \overline{Q}\bar{R} \\&\equiv (\overline{\bar{Q}} + \overline{Q})(\overline{Q} + \bar{R}) \\&\equiv \underline{\underline{\bar{Q} + R}}\end{aligned}$$

Q.2

The complete set of only those Logic Gates designated as Universal Gates is

- A. NOT, OR and AND Gates
- B. XNOR, NOR and NAND Gates
- C. NOR and NAND Gates
- D. XOR, NOR and NAND Gates

Q.3

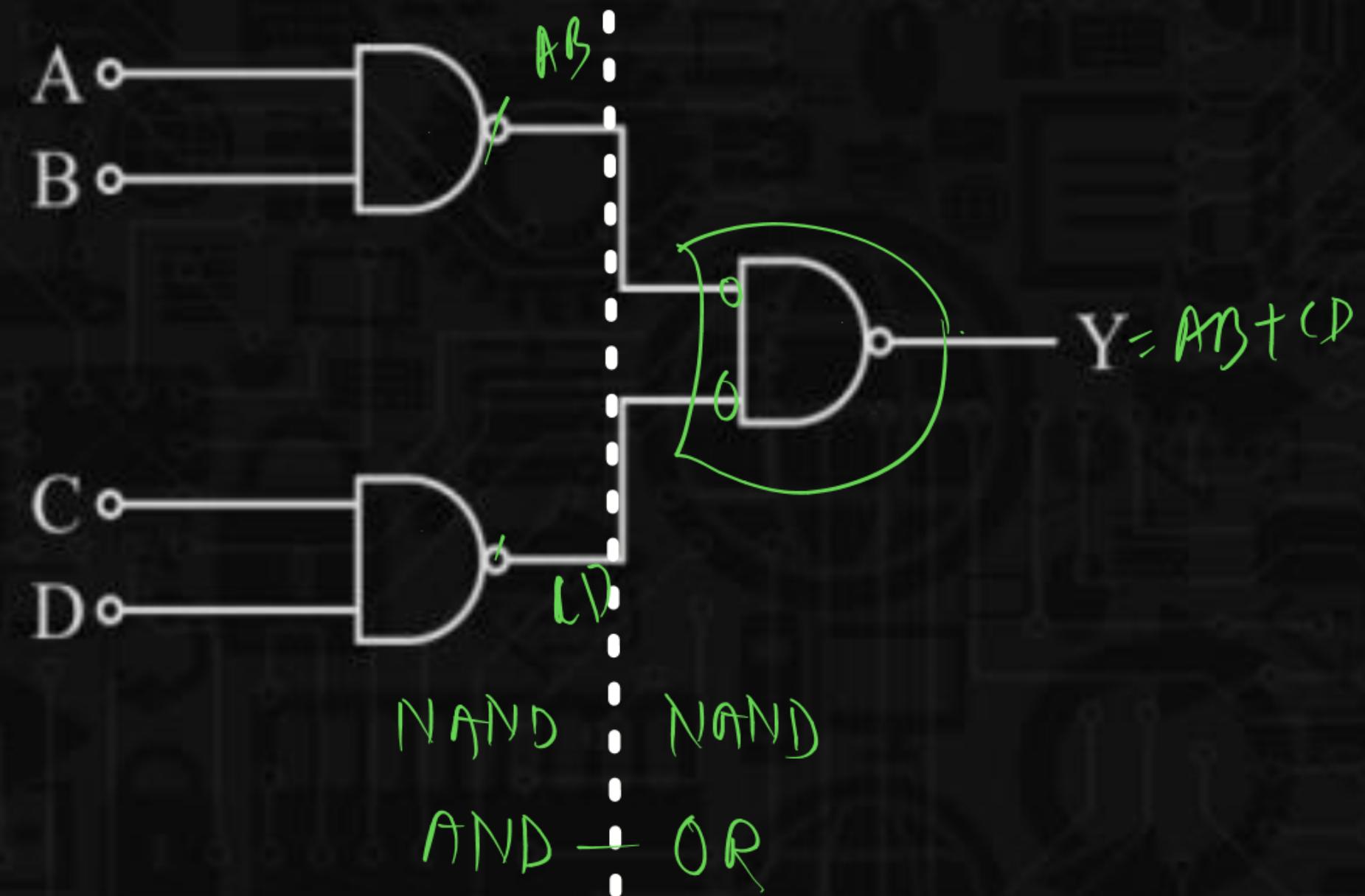
In the logic circuit shown in the figure, Y is given by

A. $Y = ABCD$

B. $Y = (A+B)(C+D)$

C. $Y = A + B + C + D$

D. $Y = AB + CD$



Q.4

$F = \textcircled{AB} + \textcircled{CD} + E$ will be implemented with how many minimum number NAND gates?

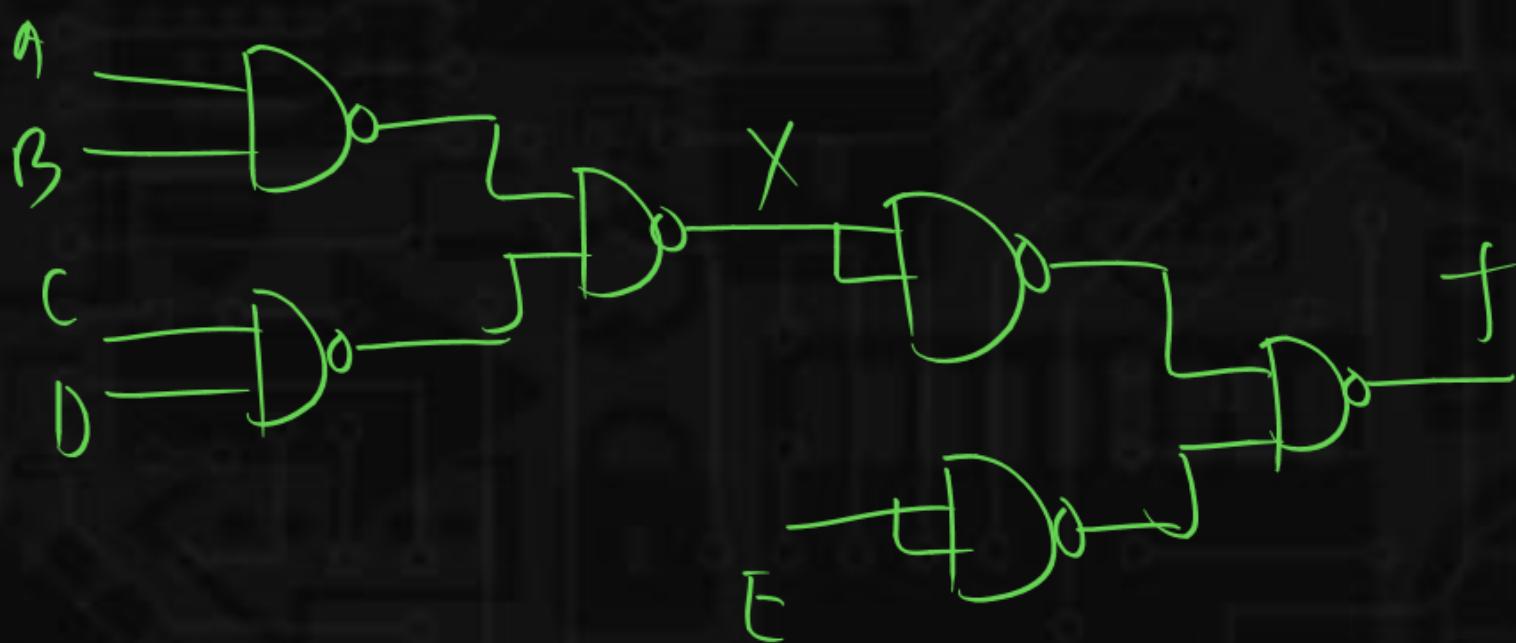
A. Three

$$AB + CD = X \quad \boxed{③}$$

B. Four

$$F = X + E \quad \boxed{③}$$

C. Five



D. Six

Q.5

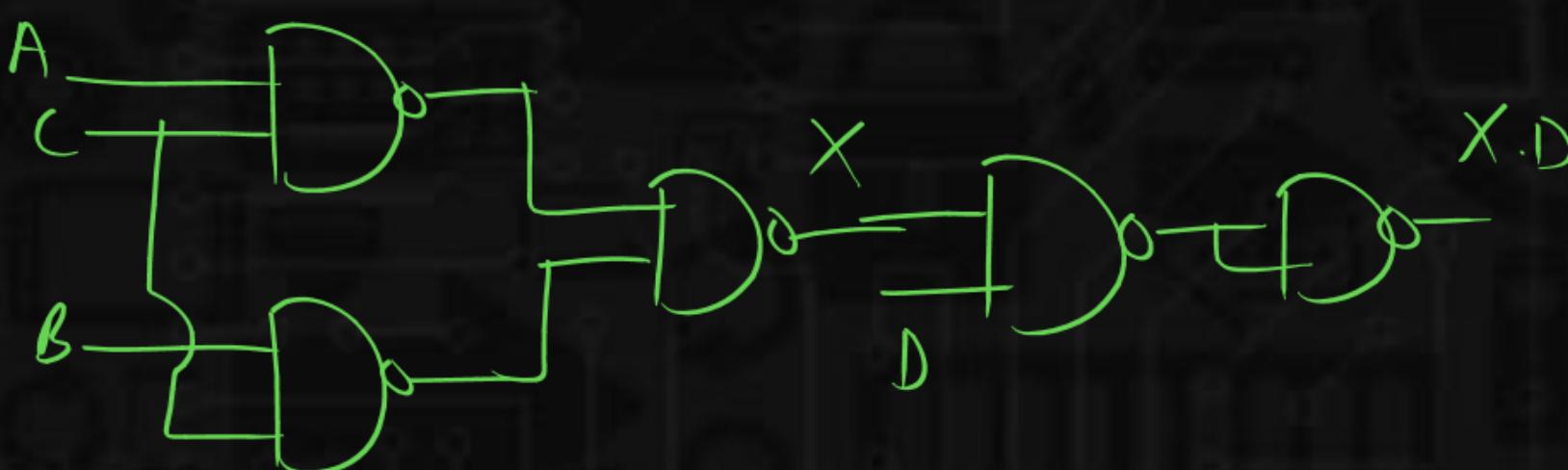
The minimum number of NAND gates required to reduce the expression $((A + B) C) D$ is

- A. 6
- B. 5
- C. 8
- D. 4

$$f = [AC + BC] \cdot D$$

$$X = AC + BC \rightarrow \textcircled{3}$$

$$f = X \cdot D \rightarrow \textcircled{2}$$

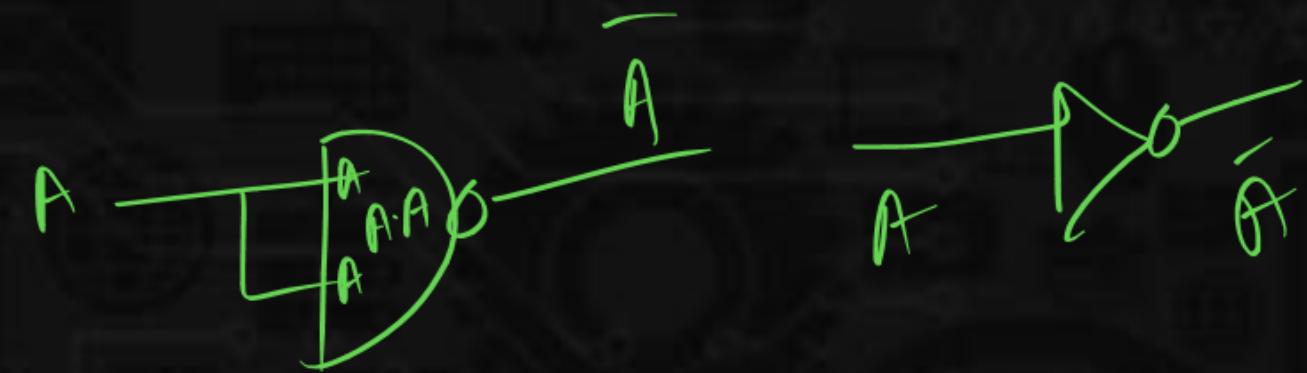


Q.6

In a two-input **NAND** gate, if both inputs are shorted, it will behave like a _____ gate.

P
W

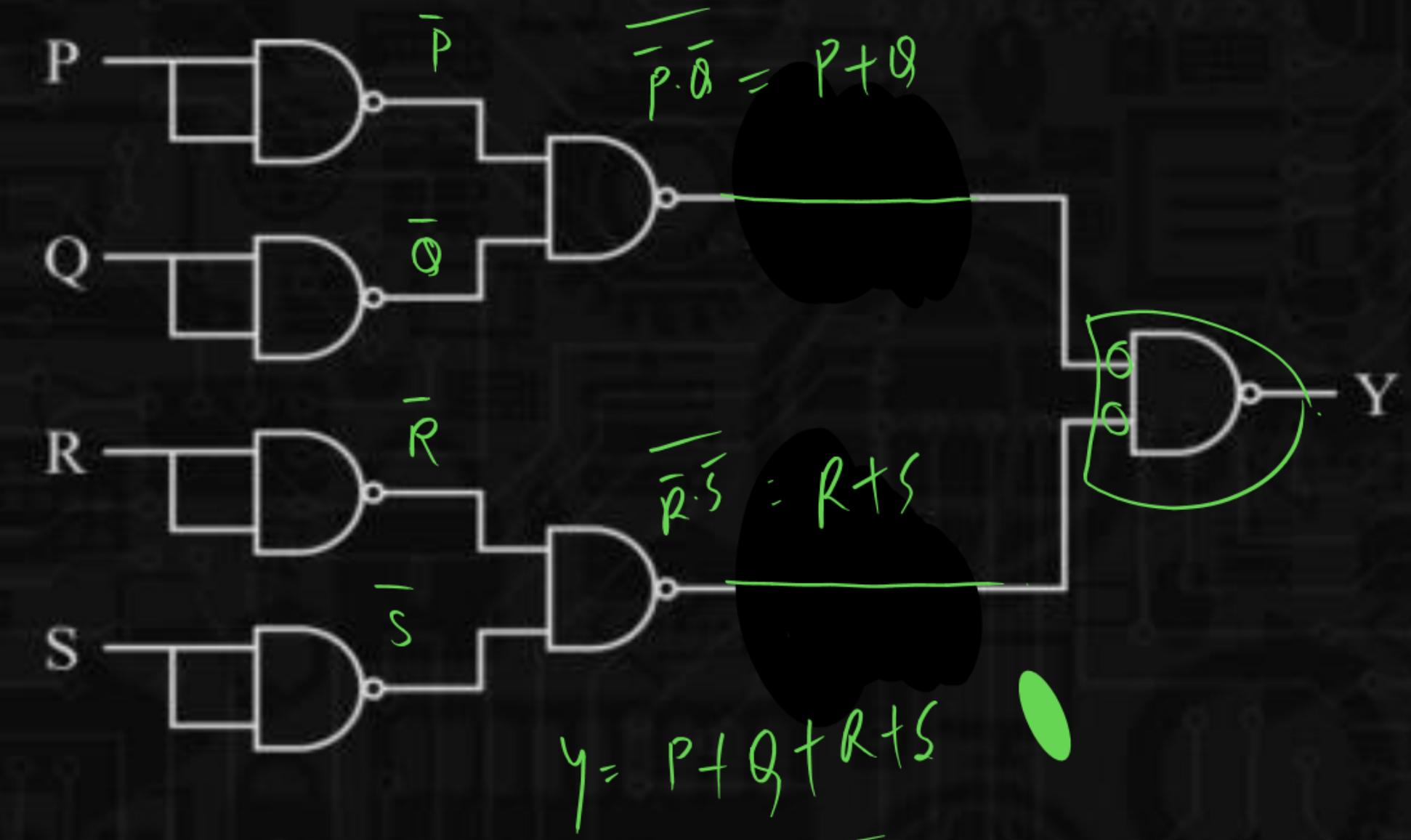
- A. Buffer
- B. AND
- C. NOT
- D. EX-OR



Q.7

For the circuit shown in figure the Boolean expression for the output Y in terms of inputs P, Q, R and S is

- A. $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$
- B. ~~$P + Q + R + S$~~
- C. $(\bar{P} + \bar{Q}) + (\bar{R} + \bar{S})$
- D. $(P + Q)(R + S)$



Q.8

A universal logic gate can implement any Boolean function by connecting sufficient number of them appropriately. Three gates are shown:

Which one of the following statements is TRUE ?

A.

Gate 1 is a universal gate.

B.

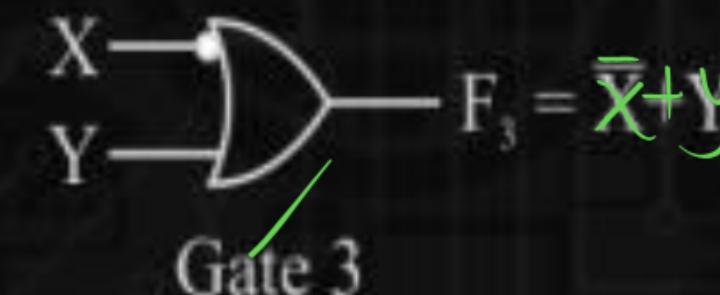
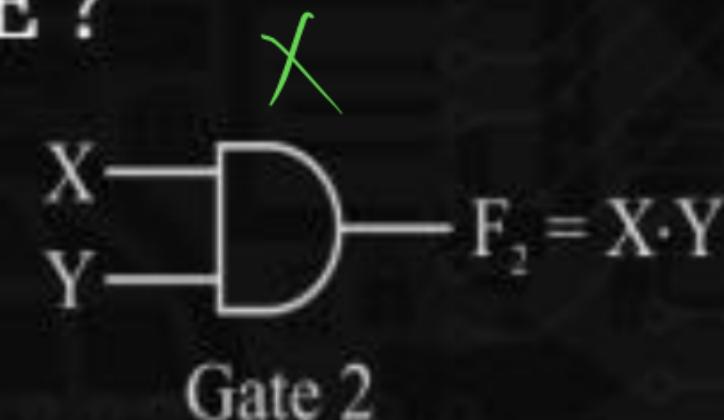
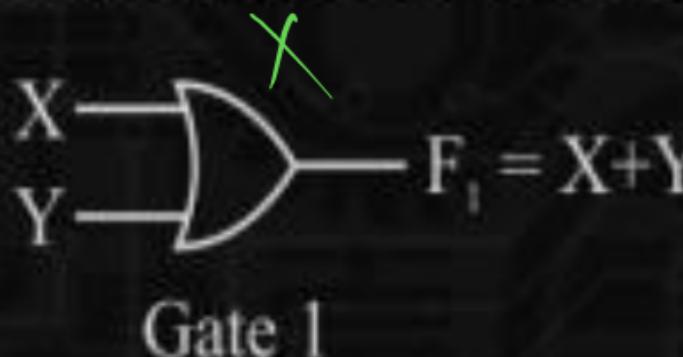
Gate 2 is a universal gate.

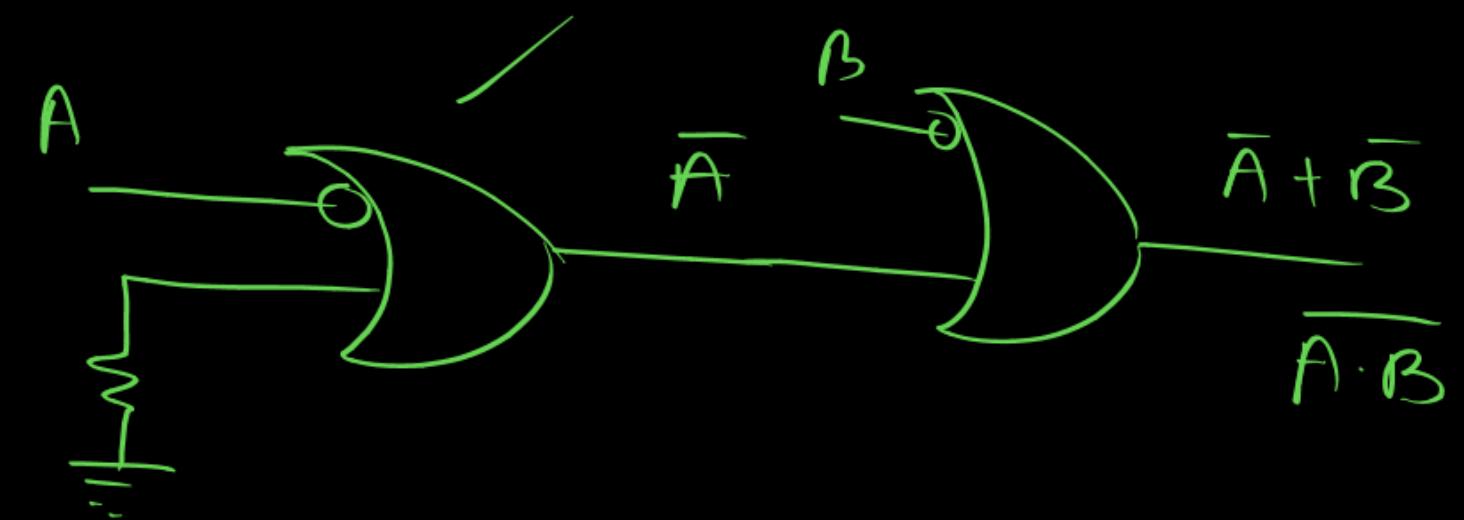
C.

Gate 3 is a universal gate

D.

None of the shown is a universal gate.





NAND

Q.9

Consider the following gate network:

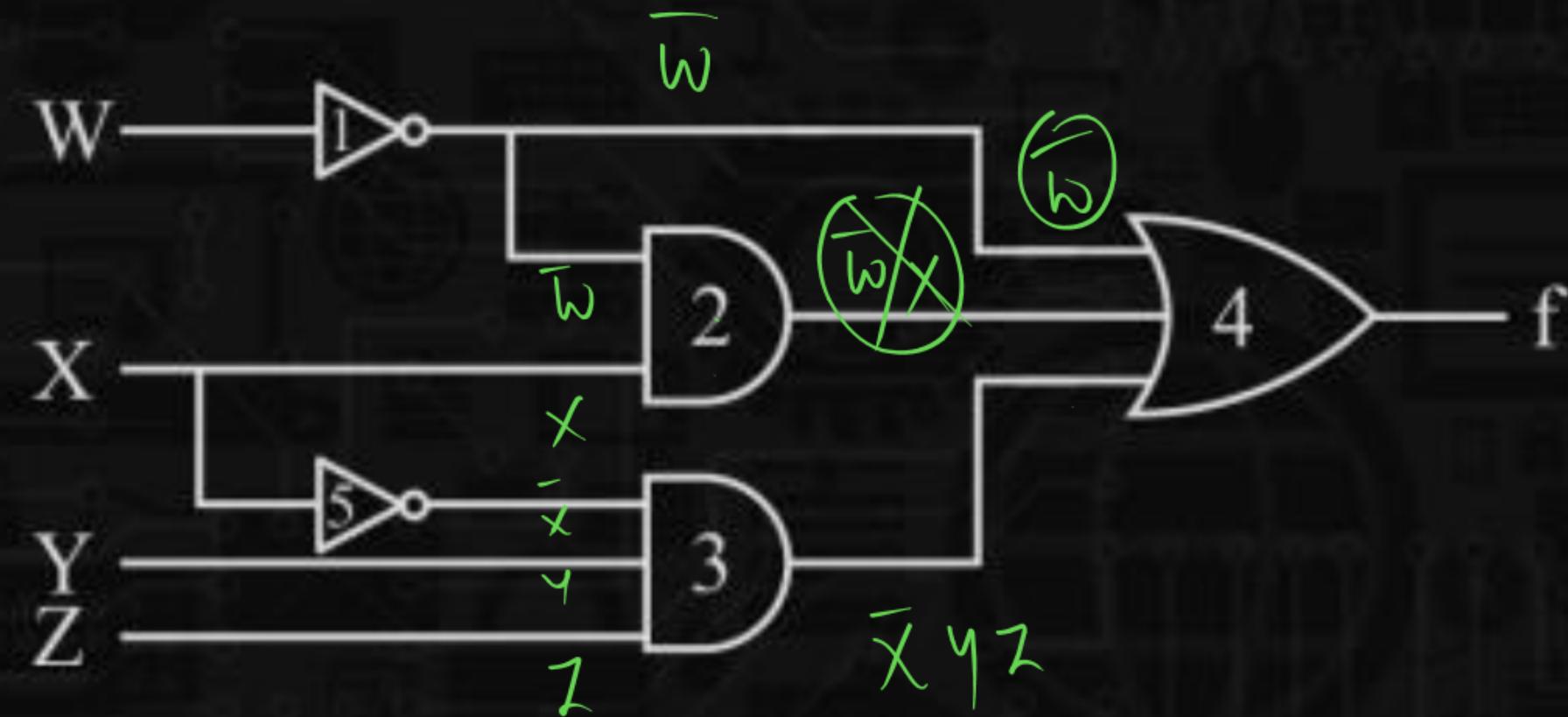
Which one of the following gates is redundant?

A. Gate No. 1

B. Gate No. 2

C. Gate No. 3

D. Gate No. 4



$$f = \bar{W} + \bar{W}\bar{X} + \bar{X}\bar{Y}\bar{Z}$$

$$= \bar{W}(1 + \bar{X}) + \bar{X}\bar{Y}\bar{Z}$$

$$= \bar{W} + \bar{X}\bar{Y}\bar{Z}$$

Q.10

The minimum of NAND gates required to implement $A + A \cdot B \cdot C$ is equal to

P
W

- A. 0
- B. 1
- C. 4
- D. 7

$$A + A \cdot B \cdot C$$
$$A(1 + B \cdot C)$$

