CS & IT ENGINEERING

Digital Logic

Question Practice Session 01

By- CHANDAN SIR

01 QUESTION PRACTICE

02 DISCUSSION

Questions based on Logic Gate

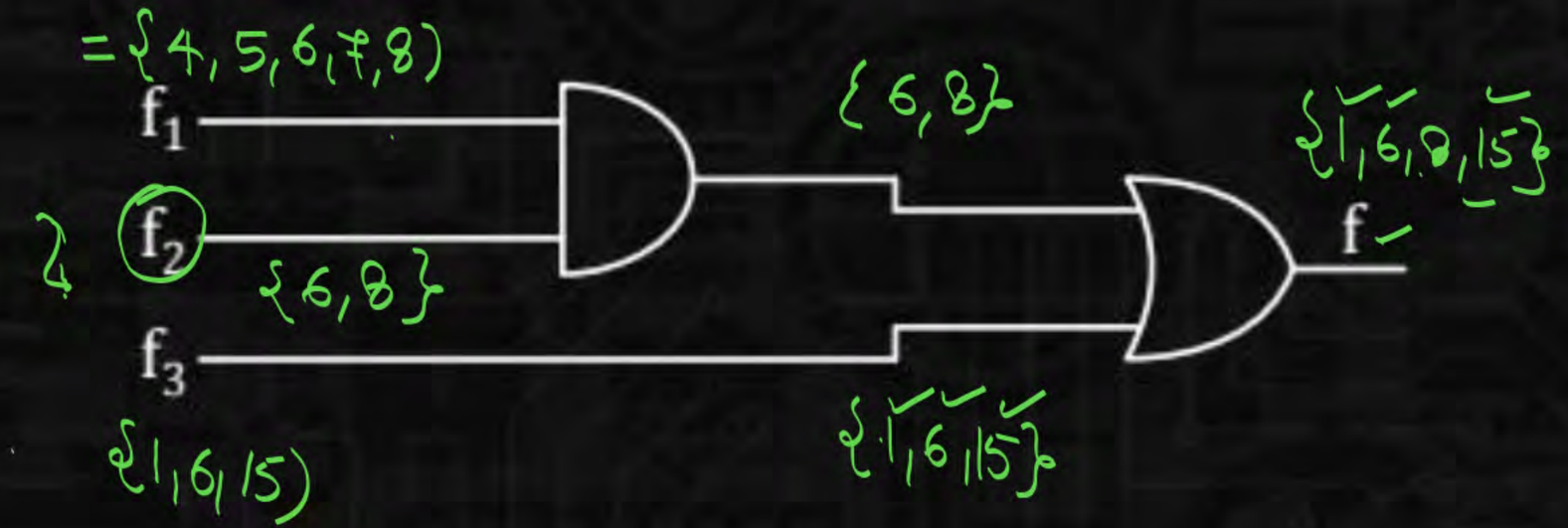
Q.1 $f_1 = \Sigma m(4, 5,6,7,8)$ $f_3 = \Sigma m(1,6,15)$ $f = \Sigma m(1,6,8,15)$
Then f_2 will be-

A. $\Sigma m\ (4, 6)$

B. $\Sigma m\ (4, 8)$

C. $\Sigma m\ (6, 8)$

D. $\Sigma m\ (4, 6, 8)$



Questions based on Logic Gate

Q.2 If $x \copyright y = \bar{x} + y$ and $z = x \copyright y$ then $z \copyright y$ will be

A. x

B. ✓ x + y

C. 0

D. None

$z \copyright y = \bar{z} + y$

$= \overline{x \copyright y} + y$

$= \overline{\bar{x} + y} + y$

$= \bar{\bar{x}} \cdot \bar{y} + y$

$= x \cdot \bar{y} + y$

$\Rightarrow (x+y)(\bar{y}+y)$

$= x + y$ Ans

Q. $x \circledcirc y = \bar{x} + y$ $\quad z = x \circledcirc y$

Then $z \circledcirc x$ will be—

$z \circledcirc x = \overline{z} + x$ $\Rightarrow x(\bar{y}+1)$

$= \overline{x \circledcirc y} + x$ $\Rightarrow x$

$= \overline{\bar{x} + y} + x$

$= \bar{\bar{x}} \cdot \bar{y} + x \Rightarrow x \cdot \bar{y} + x$

Questions based on Logic Gate

Q.3 Minimized expression will be $Y = A \oplus (A + B)$

A. $A \oplus B$

B. $A \odot B$

C. ✓ $\overline{A} \cdot B$

D. $A + B$

Questions based on Logic Gate

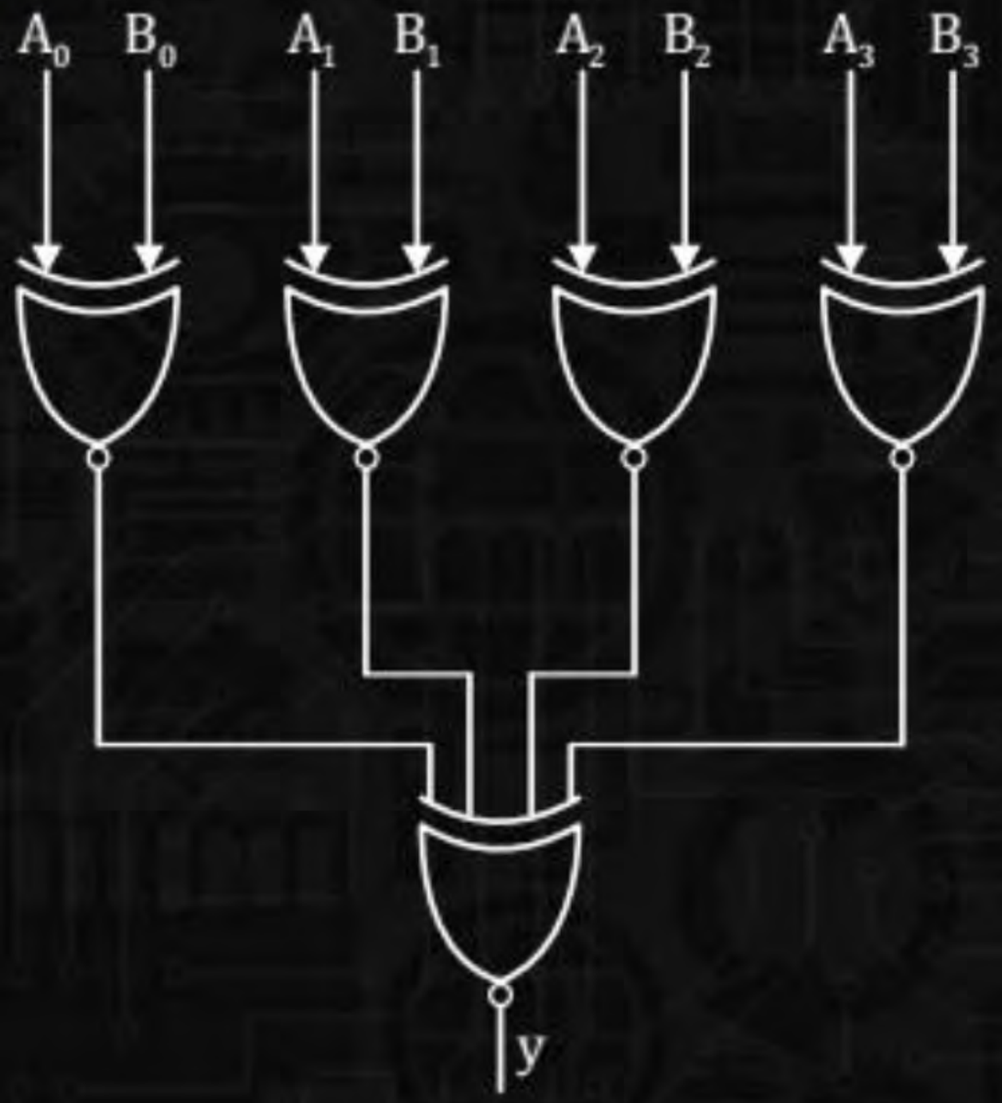
Q.4 If the output y = 1
Then correct input is/are-

A. 1111, 0000

B. 1010, 0111

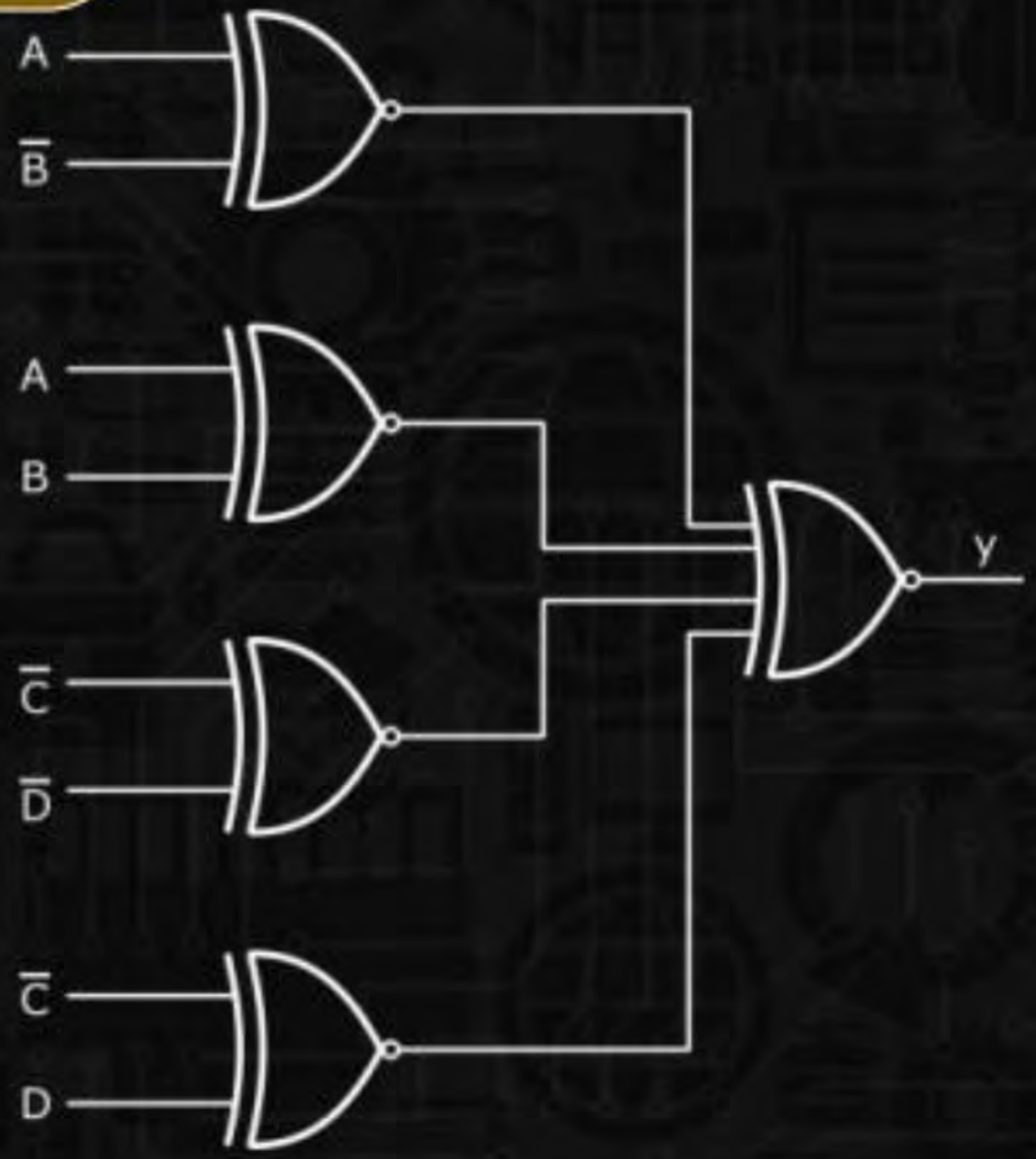
C. 0101, 0101

D. 1100, 1110



Questions based on Logic Gate

Q.5 Output y will be-



A. 0

B. 1

C. $A \oplus B$

D. $A \oplus B \oplus C \oplus D$

Questions based on Logic Gate

Q.6

The logic gates shown in the digital circuit below use strong pull-down nMOS transistors for LOW logic level at the outputs. When the pull-downs are off, high-value resistors set the output logic levels to HIGH (i.e. the pull-ups are weak). Note that some nodes are intentionally shorted to implement "wired logic". Such shorted nodes will be HIGH only if the outputs of all the gates whose outputs are shorted are HIGH.

The number of distinct values of X3X2X1X0 (out of the 16 possible values) that given Y = 1 is _____.

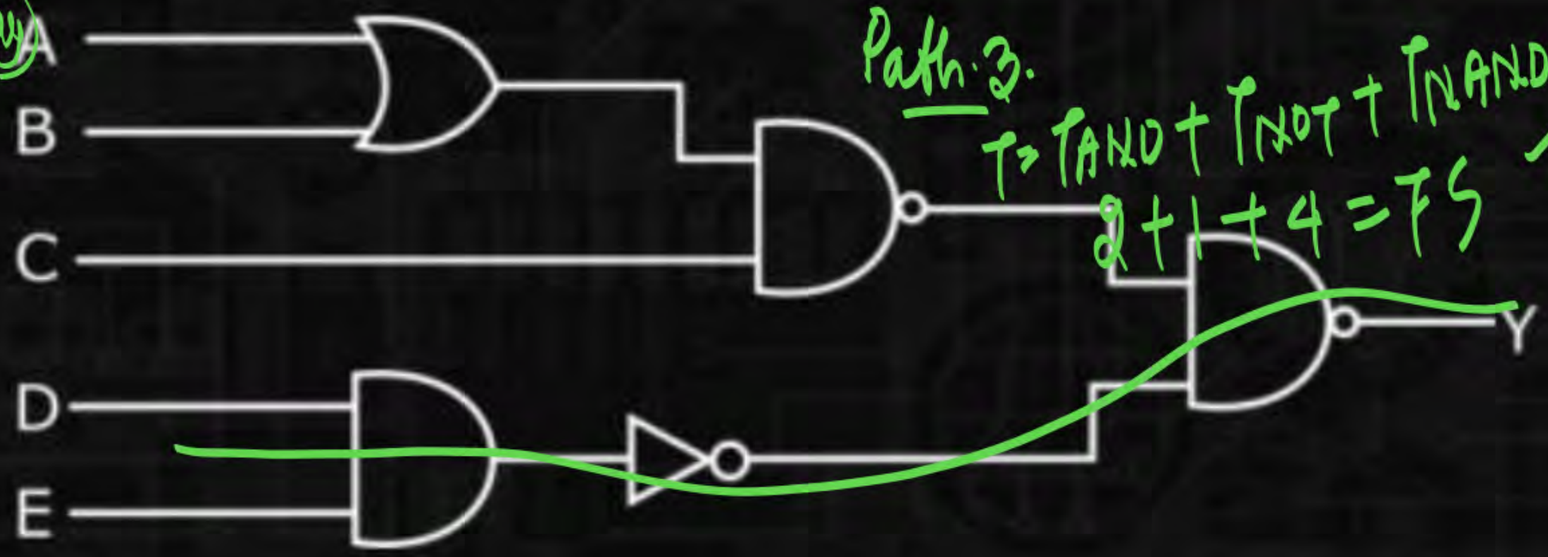
Questions based on Logic Gate

Q.7

If delays through, the gate are given as
OR gate = 5 sec
NAND gate = 4 sec
AND gate = 2 sec
Inverter gate = 1 sec
The worst case propagation delay is

(maximum delay)

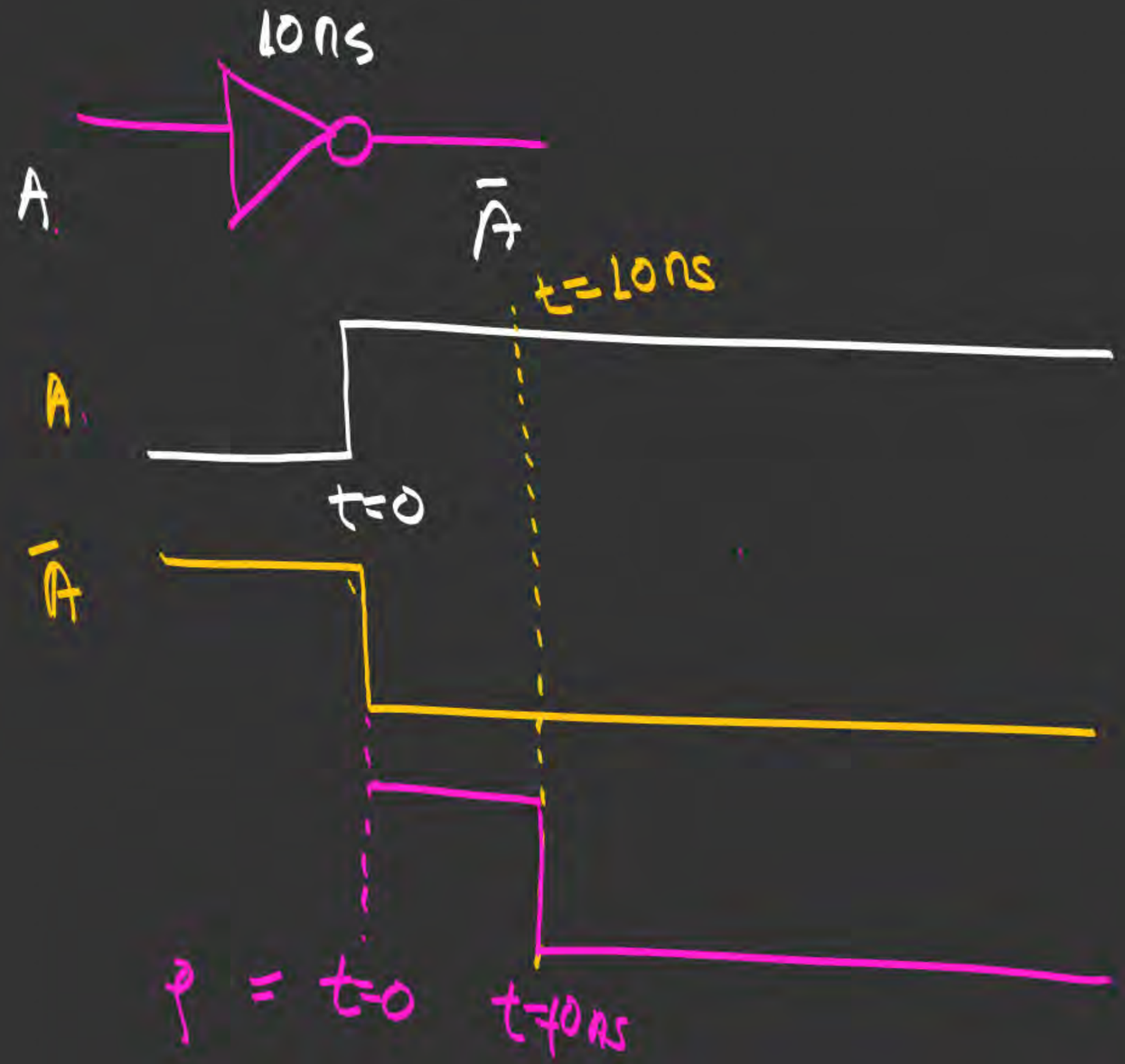
A. 12 sec
B. 16 sec
C. 13 sec
D. 5 sec



Path-1
$T = T_{OR} + T_{NAND} + T_{NAND}$
$= 5 + 4 + 4 = 13$ S

Path-2.
$T = T_{NAND} + T_{NAND}$
$= 4 + 4 = 8$ S

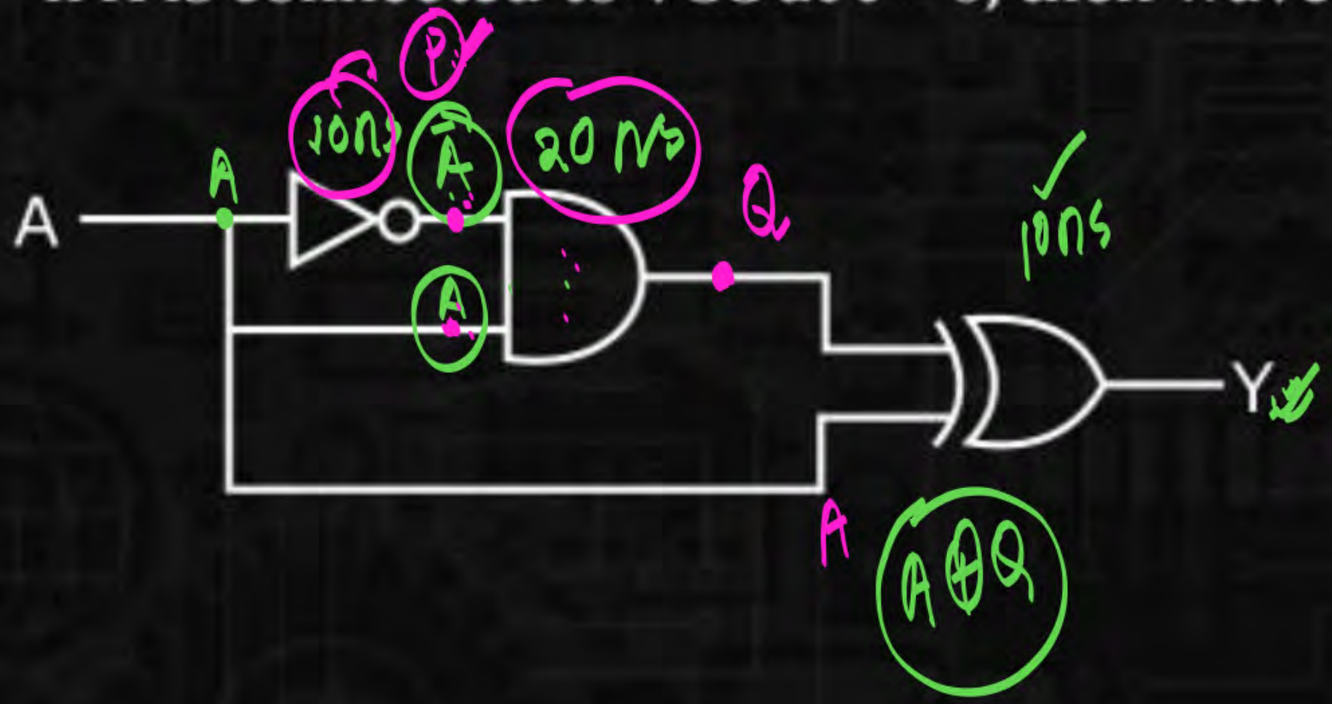
Path-3.
$T = T_{AND} + T_{NOT} + T_{NAND}$
$2 + 1 + 4 = 7$ S

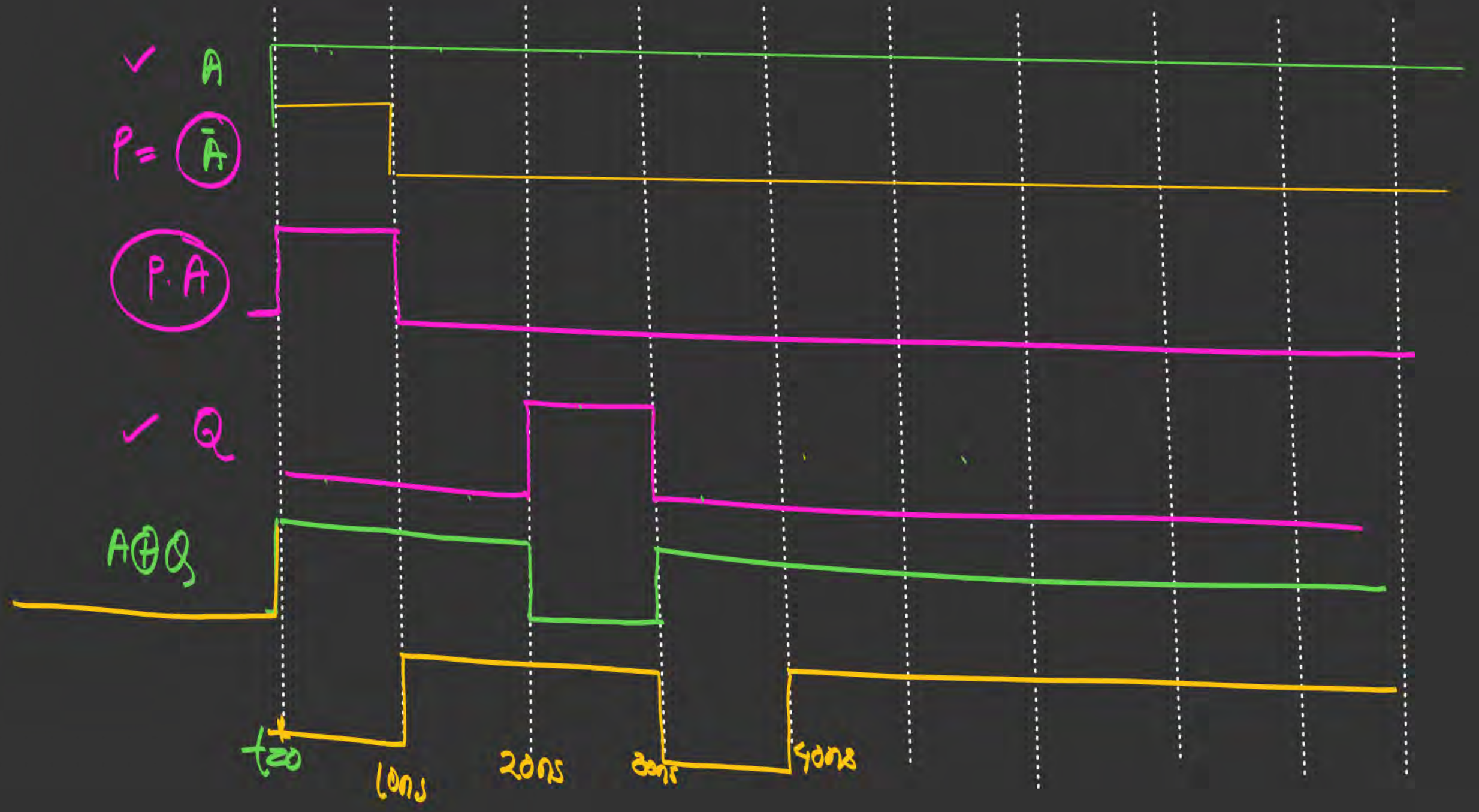

10ns
A
$\bar{A}$
t=10ns
A
t=0
$\bar{A}$
P = t=0
t=70ns

Questions based on Logic Gate

Q.8

Consider the circuit shown in figure below
If propagation delay of NOT gate is 10 nsec, AND gate is 20 nsec and X-OR gate is 10 nsec.
If A is connected to VCC at t = 0, then waveform for output Y is

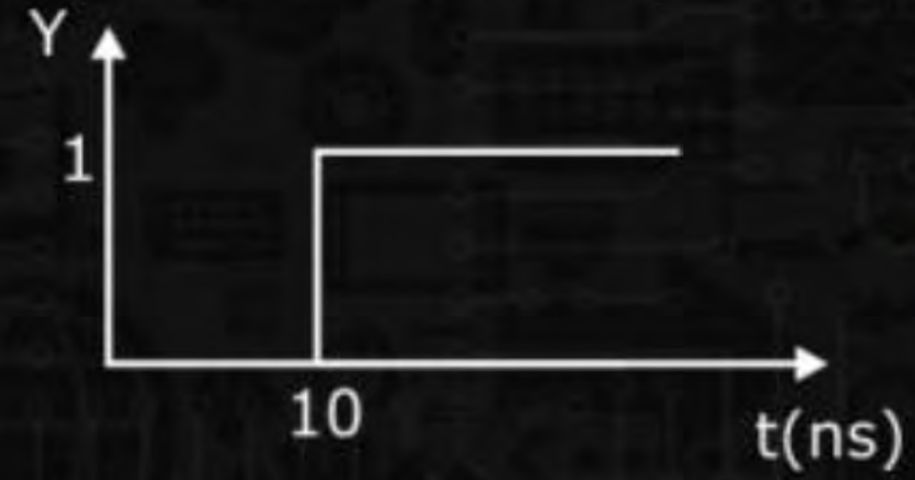



A
P = Ā
P·A
Q
A⊕Q
t=0
10ns
20ns
30ns
40ns

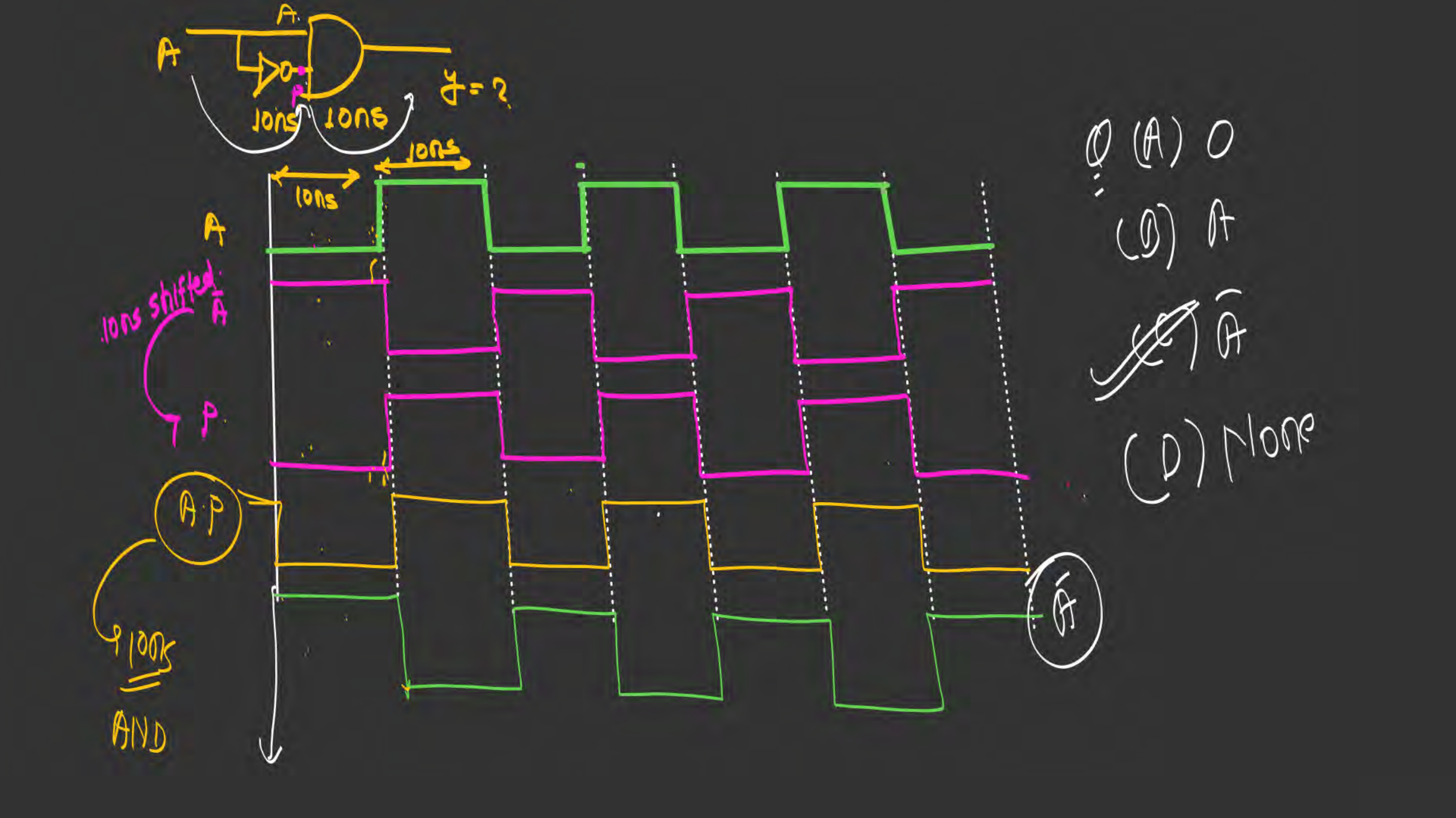
A.

B.

C.



D.



Q (A) 0

(B) A

(C) $\bar{A}$

(D) None


5ns
P
10ns
Q
A
Y
A
5ns
5ns
5ns
5ns
A
Ā
P
AP
Y

Questions based on Logic Gate

Q.9 Find the minimum number of two input NAND GATE required to implement the Boolean function-

$f = AB + CD + F$

$\Rightarrow x + F \rightarrow 3$

3

$3 + 3 = 6$

A. 9

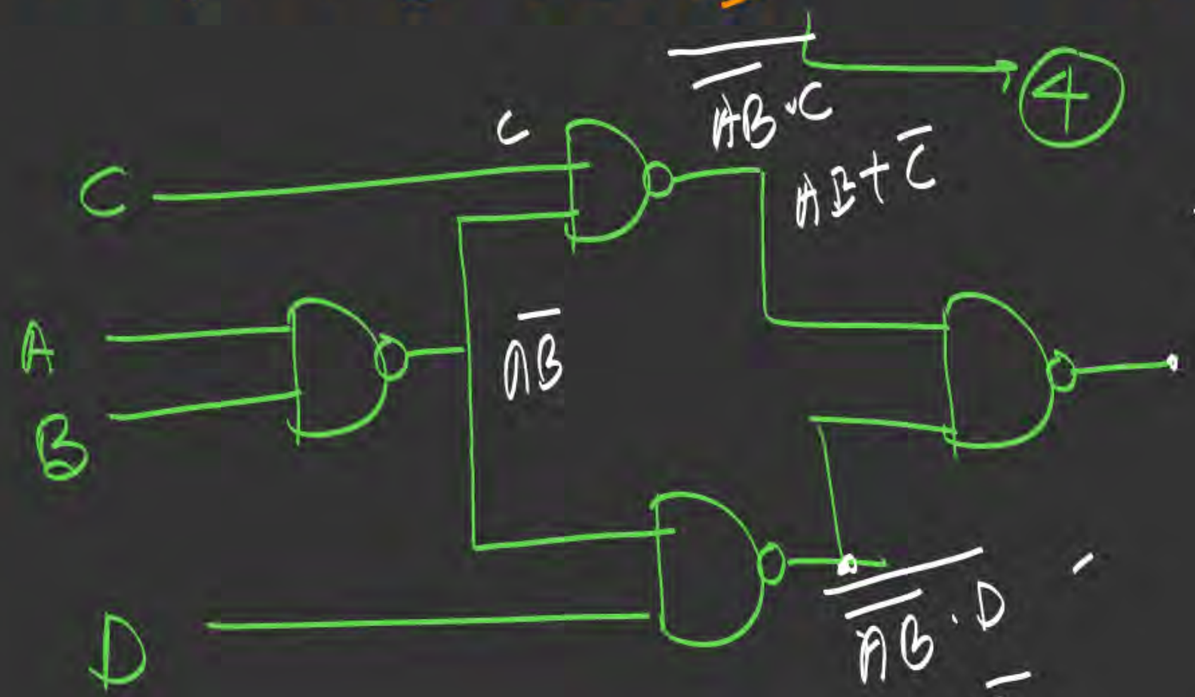
B. 8

C. 6

D. 12

$$(A+B)(\bar{A}+\bar{B}) = A\bar{B}+\bar{A}B = A \oplus B$$

Q $f = (\bar{A}+\bar{B})(C+D)$ Minimum no. of NAND GATES



$$\overline{(AB+\bar{C}) \cdot (AB+\bar{D})}$$

$$\overline{AB+\bar{C}} + \overline{AB+\bar{D}}$$

$$\overline{AB} \cdot C + \overline{AB} \cdot D$$

$$\overline{AB}(C+D)$$

$$(\bar{A}+\bar{B})(C+D)$$ Ans

Q $f = \bar{A} \cdot B \cdot \bar{C} \cdot \bar{D}$

NAND = ?

$(2n-2)' + r \Rightarrow (2 \times 4 - 2)' + 3 = 9$ Ans

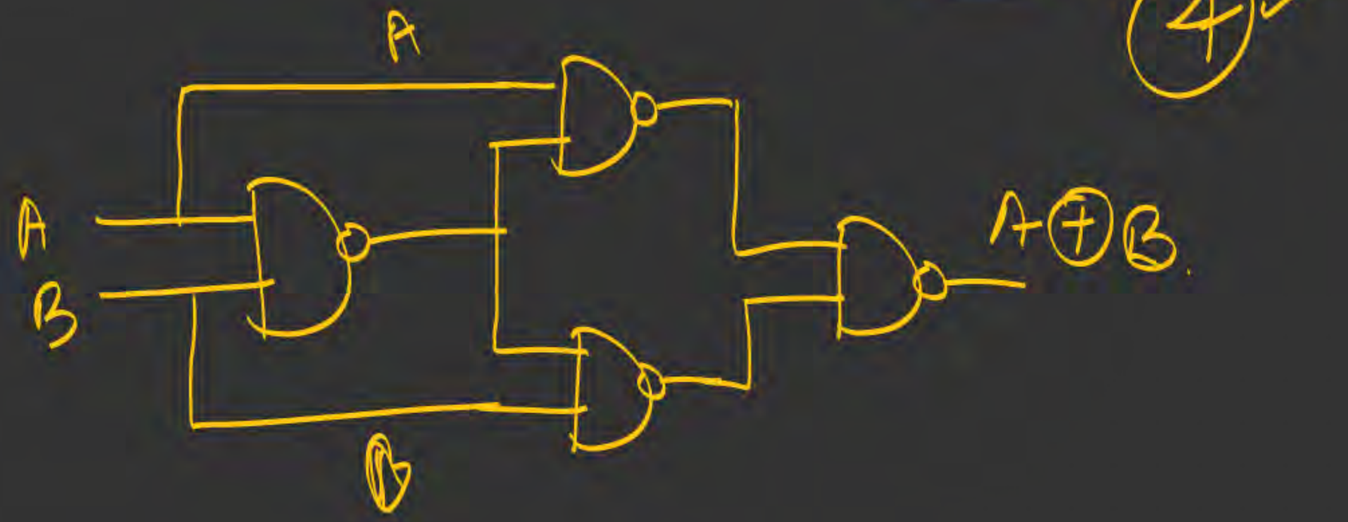
NOR = ?

$(3n-3)' r' \Rightarrow (3 \times 4 - 3)' - 3 = 6$ Ans

Q. $\bar{A}B + A\bar{B} = A \oplus B = (\bar{A} + \bar{B})(A + B)$

C + D

4




THANK YOU GW
SOLDIERS !