

# EE, EC, CS & IT ENGINEERING

Digital Logic  
Combinational Circuit



Decoder, HA, FA

DPP Solution 3 Discussion



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## TOPICS TO BE COVERED

01 Questions

02 Discussion

Q.1

A 3 line to 8 line decoder with active low outputs, is used to realize Boolean function involving three variables x, y and z (x is MSB and z is LSB) as shown below.

The minimized Boolean function  $f(x, y, z)$  in POS format, will be

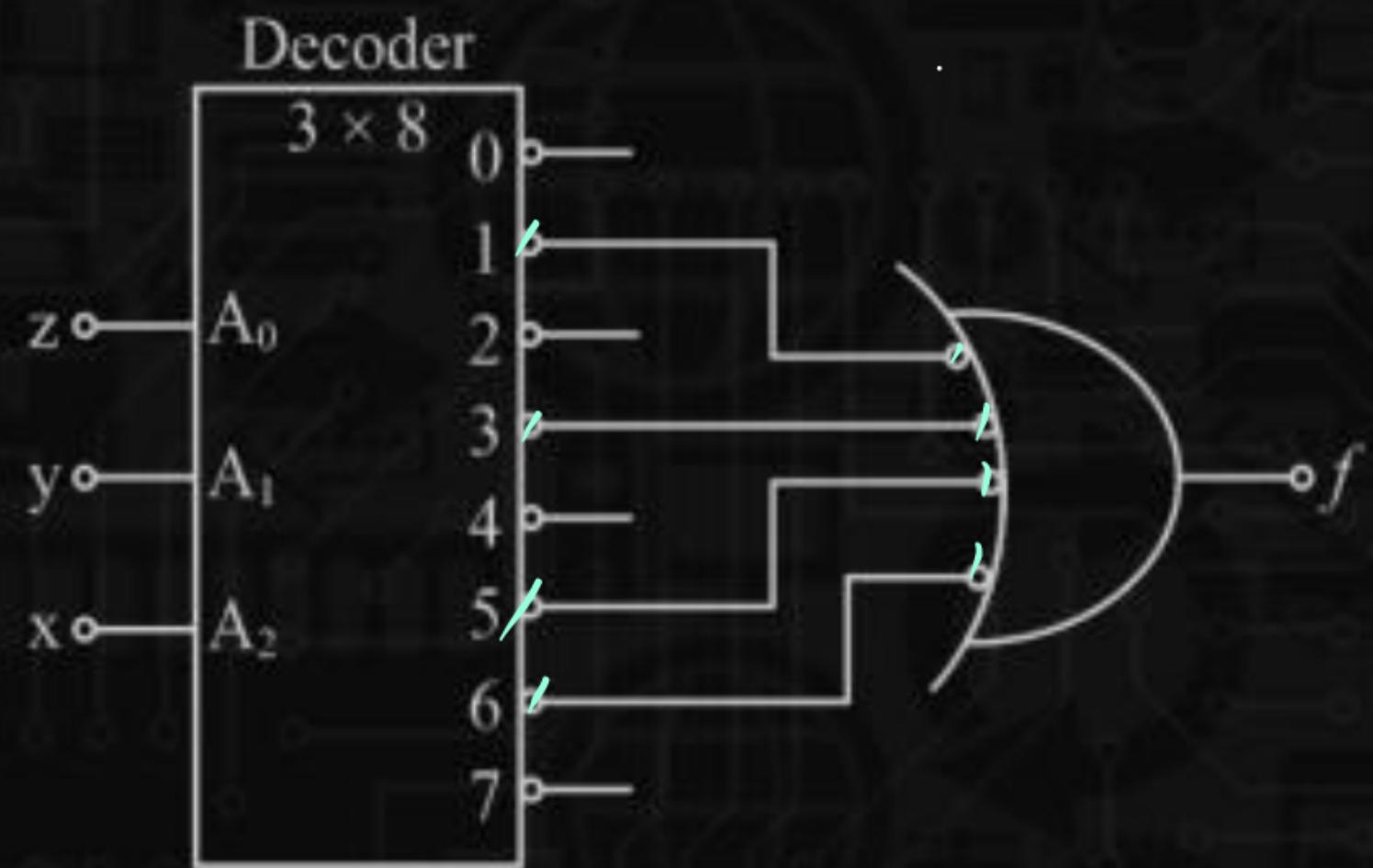
A.  $(\bar{x} + \bar{y} + \bar{z})(x + y + z)(x + \bar{y} + \bar{z})(\bar{x} + y + \bar{z})$

B.  $(\bar{x} + \bar{y} + z)(\bar{x} + y + z)(x + \bar{y} + z)(x + y + \bar{z})$

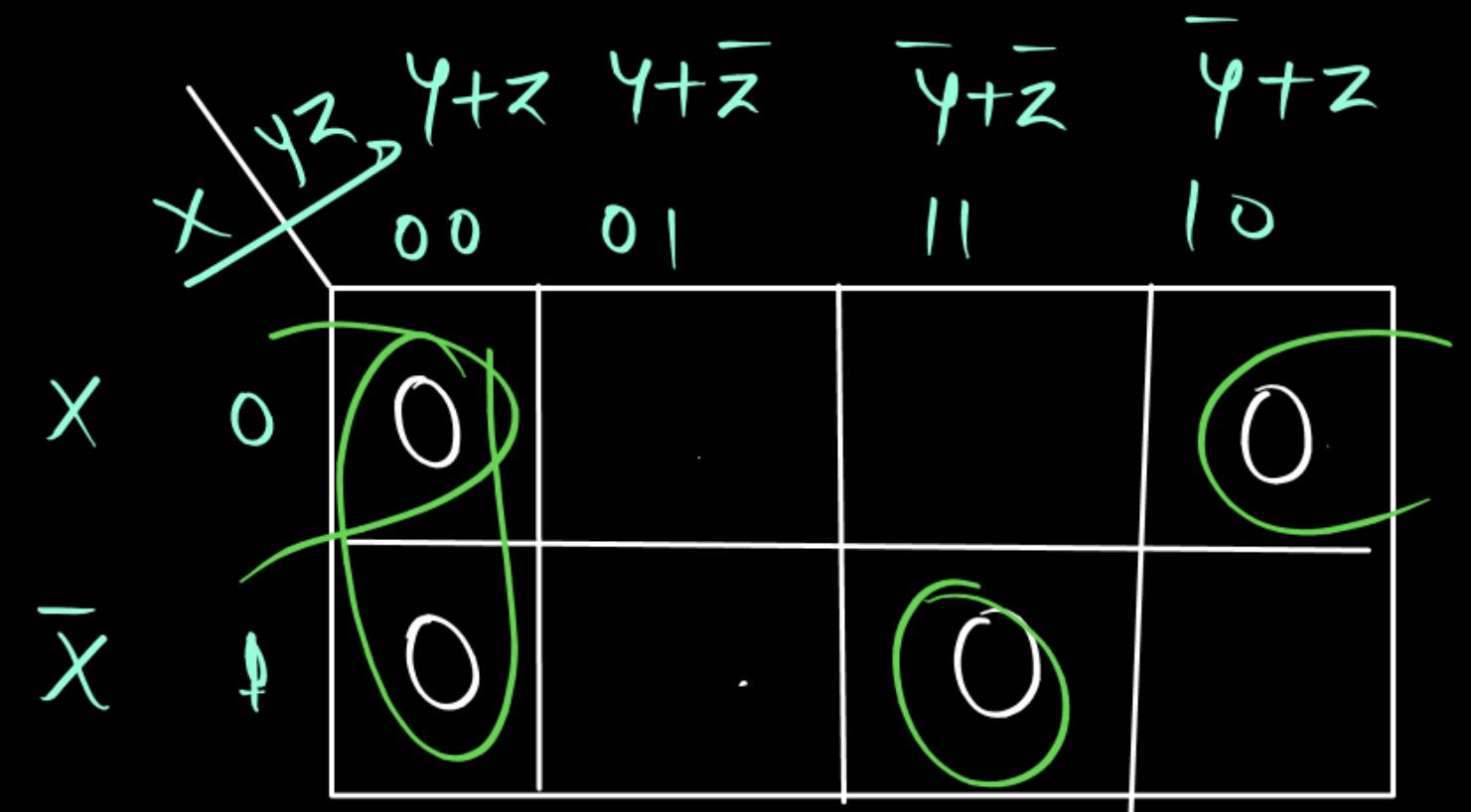
C.  $\checkmark (x + z)(y + z)(\bar{x} + \bar{y} + \bar{z})$

$$\begin{aligned} f(x, y, z) &= \sum m(1, 3, 5, 6) \\ &= \prod M(0, 2, 4, 7) \end{aligned}$$

D.  $(\bar{x} + \bar{z})(\bar{y} + \bar{z})(x + y + z)$



$$f(x,y,z) = \overline{IM}(0,2,4,7)$$



$$f = (y+z) \cdot (x+z) \cdot (\bar{x} + y + z)$$

Q.2

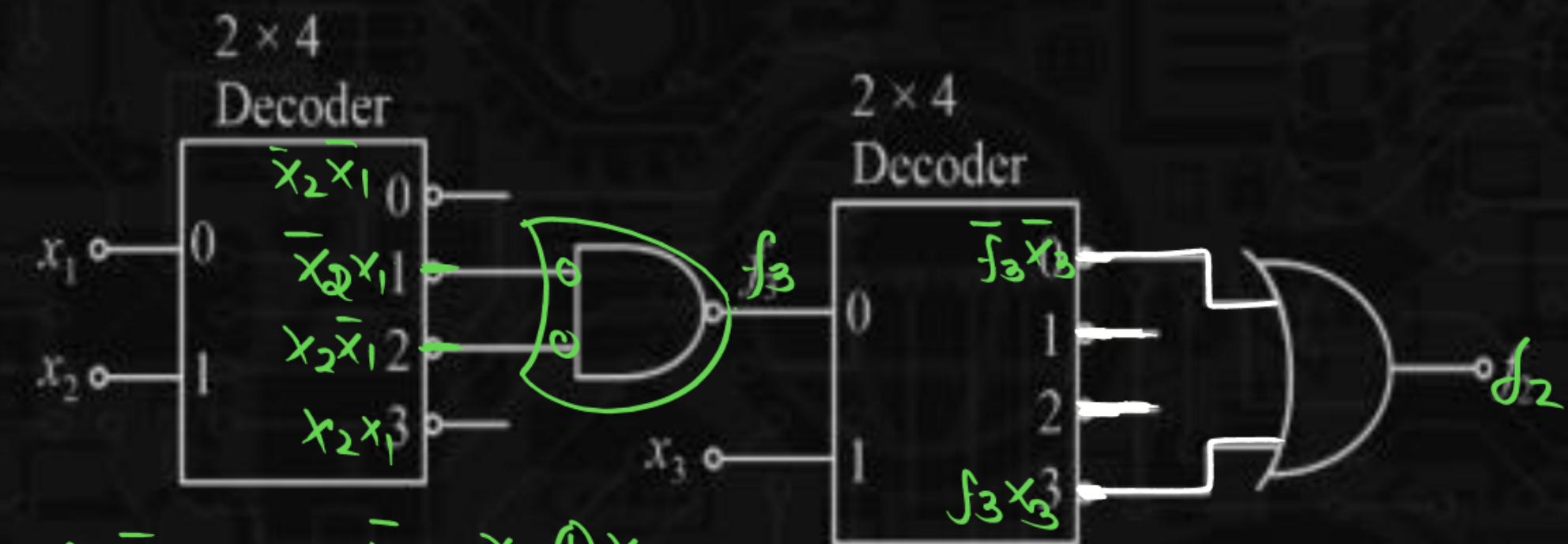
Two  $2 \times 4$  decoders one with active low outputs and another with active high outputs are interconnected as shown below. The output function  $f_2(x_3, x_2, x_1)$  will be

A.  $f_2 = (x_1 \oplus x_2) \odot x_3$

B.  $f_2 = (x_1 \oplus x_2) \ominus x_3$

C.  $f_2 = (x_1 \oplus x_2) \oplus x_3$

D.  $f_2 = (x_1 \oplus x_2) \odot x_3$



$$\bar{f}_3 = \bar{x}_2 \bar{x}_1 + x_2 \bar{x}_1 = x_2 \oplus x_1$$

$$\begin{aligned} \bar{f}_2 &= \bar{\bar{f}}_3 \bar{x}_3 + \bar{f}_3 x_3 = \bar{f}_3 \odot x_3 \\ &= (x_2 \oplus x_1) \odot x_3 \end{aligned}$$

**Q.3**

A designer has sufficient number of units of decoder with enable input of size  $4 \times 2^4$  and a decoder of size  $8 \times 2^8$  is to be realized. The number of units of  $4 \times 2^4$  decoders, required will be

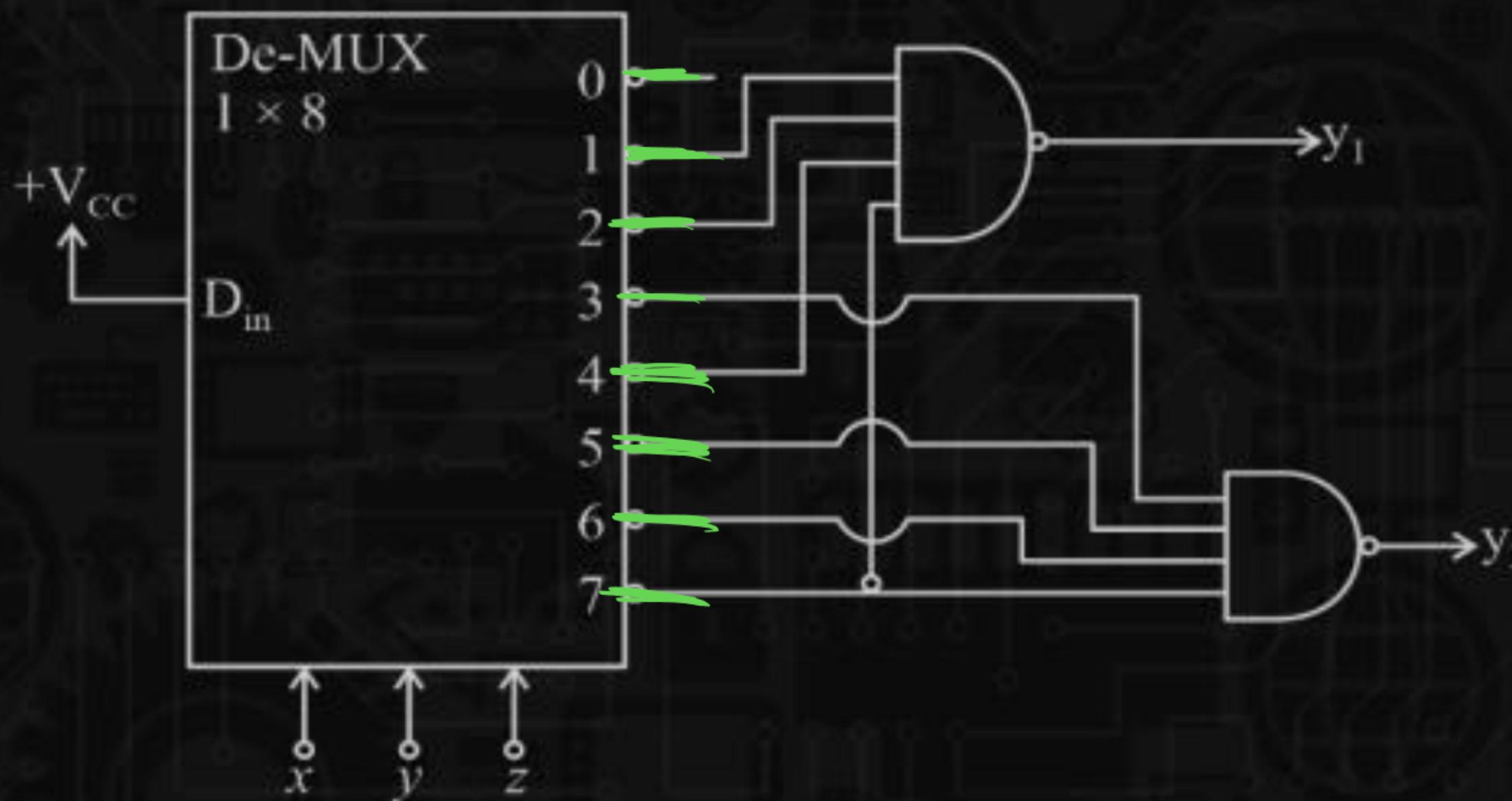
- A. 17
- B. 12
- C. 8
- D. 16

$$4 \times 16 \xrightarrow{\frac{256}{16} + \frac{16}{16}} 8 \times 256$$
$$16 + 1 = \textcircled{17}$$



**Common date for Q.No. 4 & 5**

A demultiplexer of size  $1 \times 8$  with active low outputs, is programmed as shown below. The circuit has three inputs  $x, y, z$  and generates two outputs  $y_1, y_2$ .



**Q.4**

What is this circuit?

A. Half subtractor

B. Full subtractor

C. Half adder

D.

Full adder

**Q.5**

If de-multiplexer has active high outputs instead of active low outputs, then in order that outputs do not change

- A. NAND gates should be replaced by NOR gates
- B. NAND gates should be replaced by OR gates
- C. NAND gates should be replaced by AND gates
- D. the inputs x, y, z should be inverted

**Q.6**

Consider the following statements.

- I. A  $2 \times 4$  decoder with enable input can also be used as a  $1 \times 4$  de-multiplexer.
- II. In order to use d-multiplexer as decoder, the select lines of de-multiplexer should be used as input lines of decoder and input line of de-multiplexer as enable input of decoder.
- III. The de-multiplexer does many to one data operation.

Of these, the INCORRECT statements is (are)

- A. only I
- C. only III

- B. only II
- D. I and II



**Q.7**

Notwithstanding overflow, the addition/subtraction of k bit signed binary numbers can be realized by using k full adders and

- A. k 2-input AND
- B. k 2-input OR
- C. k 2-input X-OR
- D. k 2-input NOR

$$\frac{k-2}{2} \times \text{OR}$$

**Q.8**

How many half adders, will be required to add two k bit numbers?

P  
W

- A.  $2k + 1$
- ~~B.~~  $2k - 1$
- C.  $2k$
- D.  $2(k + 1)$

$$\frac{(2k-1) \text{ HA} + (R-1) \text{ OR}}{}$$

$$x \oplus x = 1$$

$$x \oplus 1 = x$$

$$x \oplus \bar{x} = 0$$

$$x \oplus 0 = \bar{x}$$



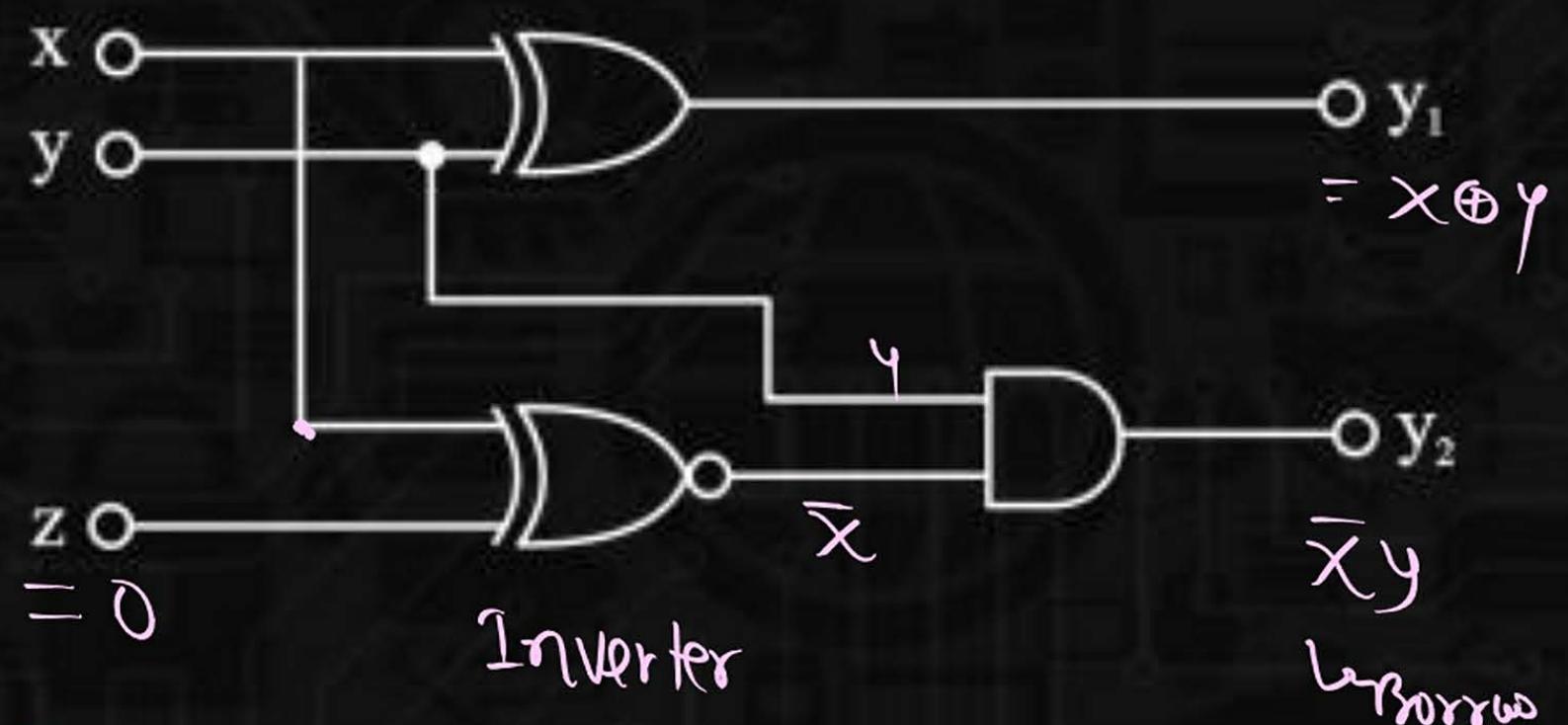
INVERTER



BUFFER

Q.9

The circuit shown below, is a controlled half adder/ half subtractor. The inputs to half adder/ half subtractor are  $x$  and  $y$  while  $z$  is a control. The outputs are  $y_1$  and  $y_2$ .



A. Half adder for  $z = 0$

B. Half subtractor for  $z = 1$

C. Half adder for  $z = 1$  and half subtractor for  $z = 0$

D. Half adder regardless of whether  $z = 0$  or  $z = 1$  due to design defect.

Q.10

Three half adders  $HA_1$ ,  $HA_2$  and  $HA_3$  are inter-coupled as shown below. The four output functions  $y_1$ ,  $y_2$ ,  $y_3$  and  $y_4$  are expressed in terms of inputs  $a$ ,  $b$  and  $c$ . Which one of the following output expressions, is correct?

A.

$$y_1 = (a \oplus b)c \times$$

B.

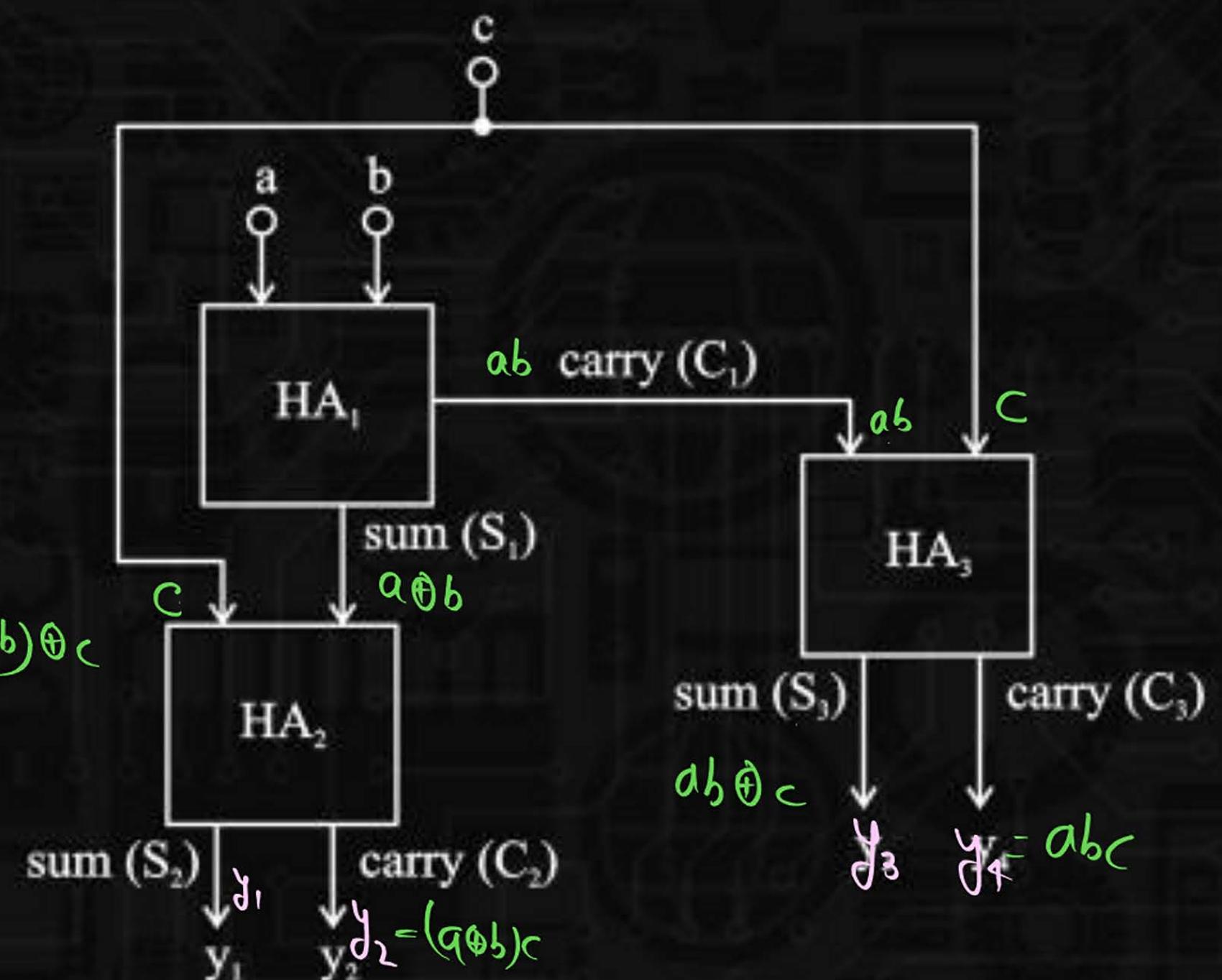
$$y_2 = (a \oplus b) \oplus c \checkmark$$

C.

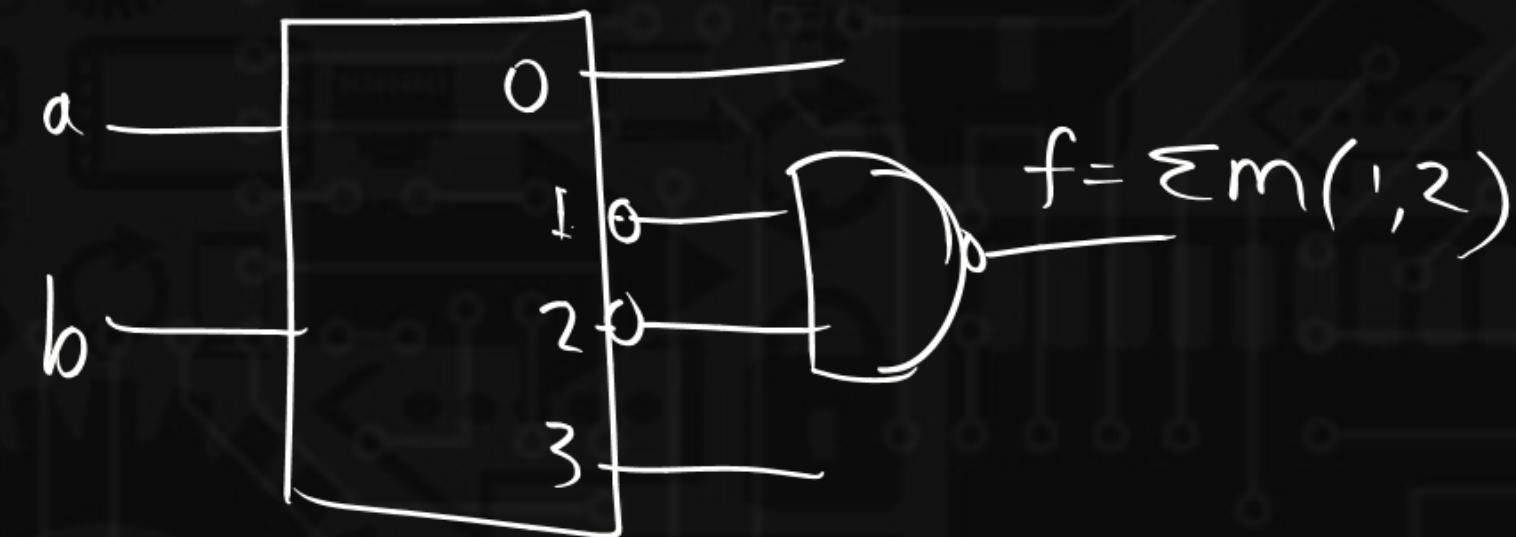
$$y_3 = ab \oplus c \checkmark$$

D.

$$y_4 = a(b \oplus c)$$



$$\begin{array}{c} A \xrightarrow{\text{OR}} \bar{A} \\ B \xrightarrow{\text{OR}} \bar{B} \end{array} \quad \begin{array}{c} \bar{A} \cdot \bar{B} \\ \text{---} \\ A + B \end{array} = \quad \begin{array}{c} A \\ B \end{array} \quad \text{NAND gate} \quad A + B$$

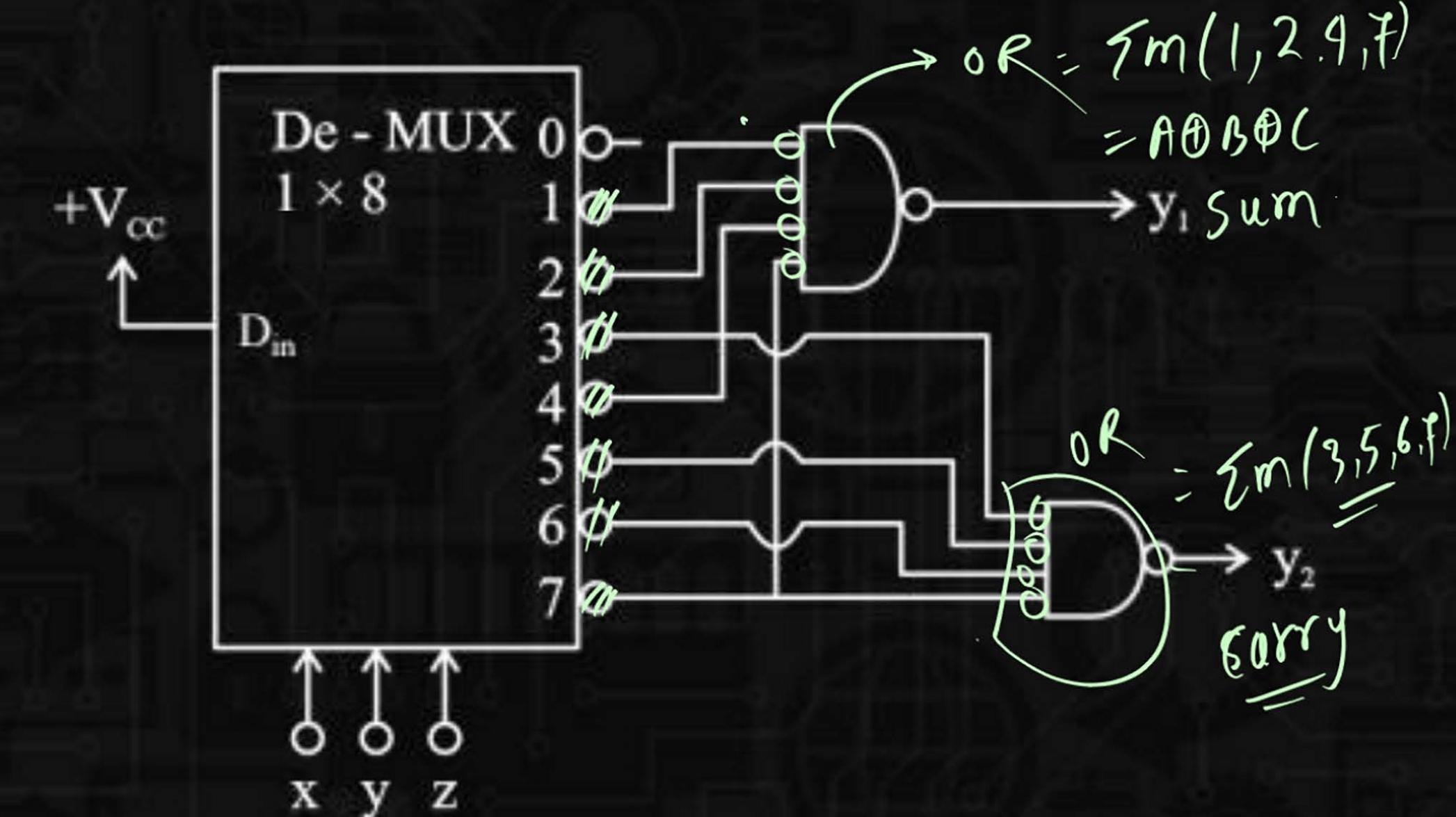


Q.11 A demultiplexer of size  $1 \times 8$  with active low outputs, is

programmed as shown below. The circuit has three inputs  $x_4$ ,  $y$ ,  $z$  and generates two outputs  $y_1$ ,  $y_2$ .

What is circuit?

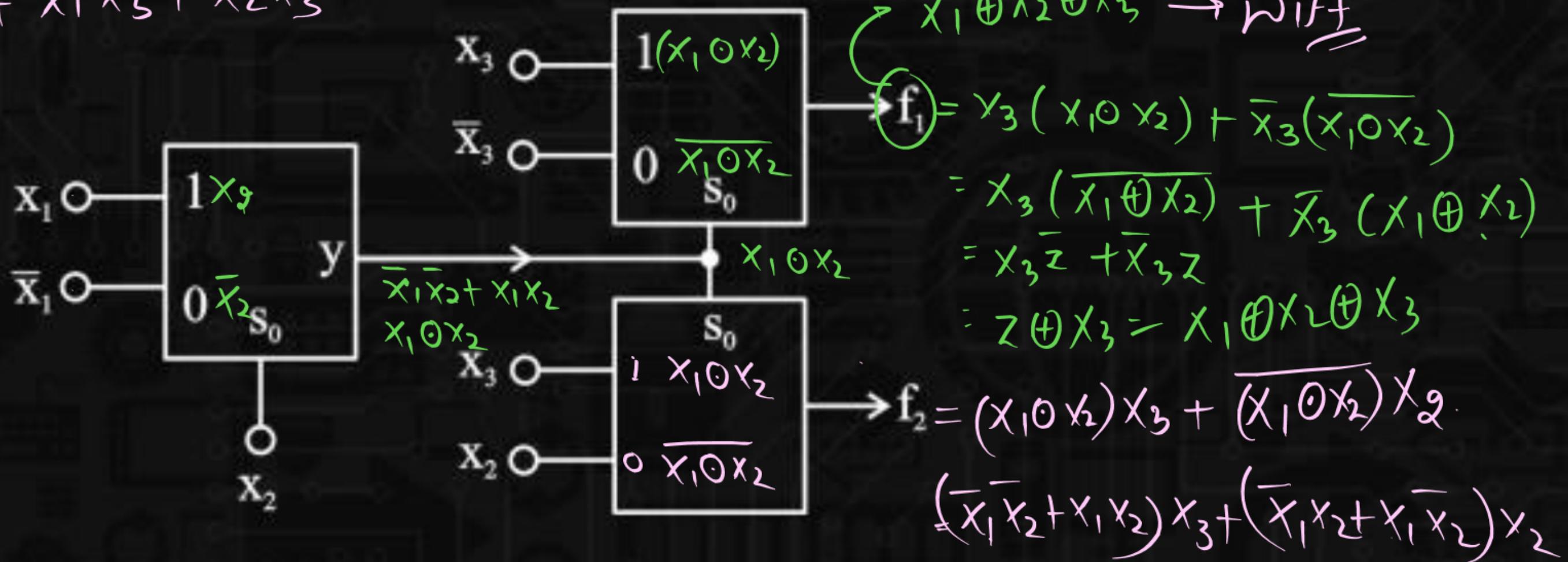
- A. Half subtracter
- B. Full subtractor
- C. Half adder
- D. Full adder



## Statement for question 4 & 5.

$$x_1 \oplus x_2 = z$$

$$\bar{x}_1 x_2 + \bar{x}_1 x_3 + x_2 x_3$$



Full Subtractor

Q.12 The function  $f_1$  and  $f_2$  are

A.

$$f_1 = (x_1 \oplus x_2)x_3 \text{ and } f_2 = x_1\bar{x}_2 + x_1\bar{x}_3 + x_2x_3$$

B.

~~$$f_1 = x_1 \oplus x_2 \oplus x_3 \text{ and } f_2 = \overline{x_1x_2} + \overline{x_1x_3} + x_2x_3$$~~

C.

$$f_1 = \overline{(x_1 \oplus x_2 \oplus x_3)} \text{ and } f_2 = x_1x_2 + x_1x_3 + x_2x_3$$

D.

$$f_1 = x_1(x_2 \oplus x_3) \text{ and } f_2 = x_1x_2 + x_1x_3 + \overline{x_2x_3}$$

Q 13

What is this circuit?

P  
W

- A. Full adder
- B. Full subtractor
- C. Magnitude comparator
- D. Priority encoder

Full adder

Full subtractor

Magnitude comparator

Priority encoder

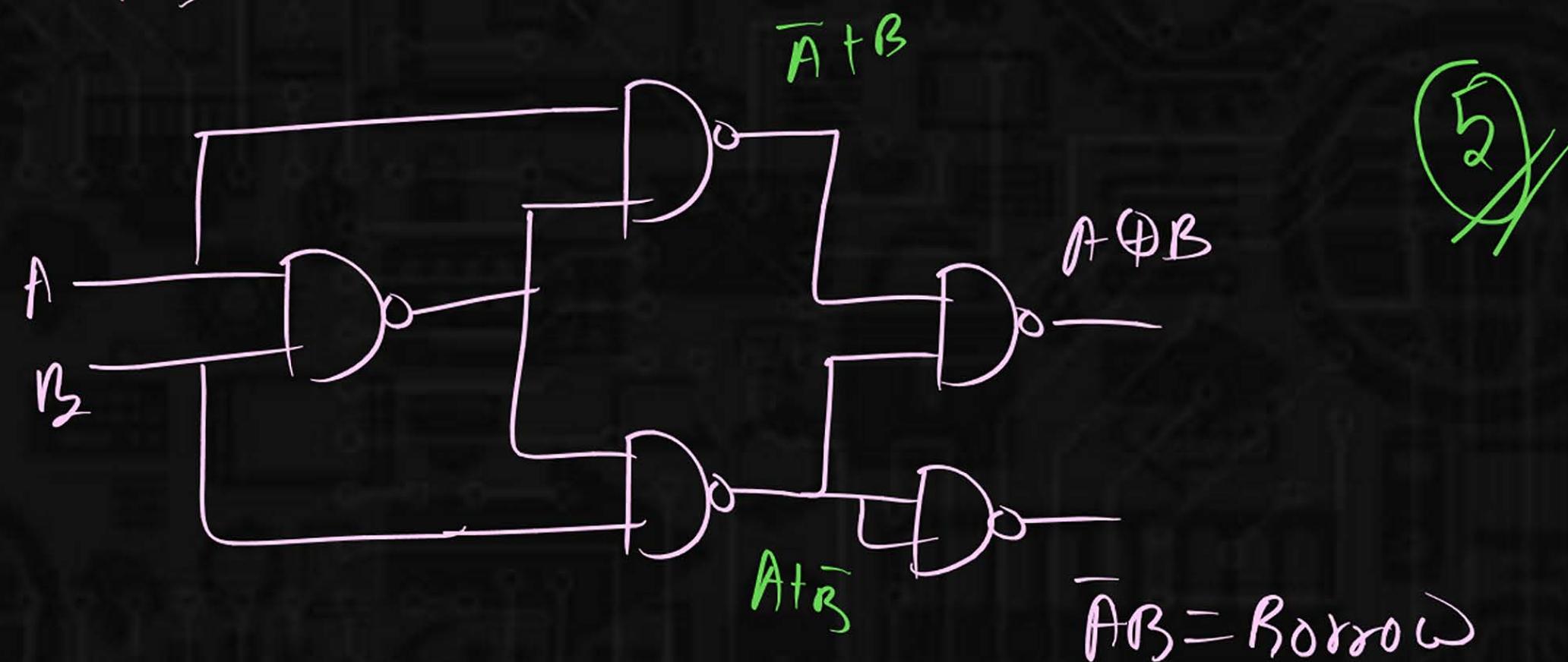
Q.14

Minimum number of NAND gate required to implements  
Half Subtractor?

HALF → ⑤

$$\Delta = A \oplus B$$

$$\text{Borrow} = \bar{A}B$$



Q.15

Minimum number of NAND gate required to implements Full Subtractor?

(9)

(9)

