EE, EC, CS & IT ENGINEERING

DIGITAL ELECTRONICS

Counter

Lecture No. 06 10

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01 Synchronous Counter Design

02 Practice

03 Discussion

Synchronous counter :→

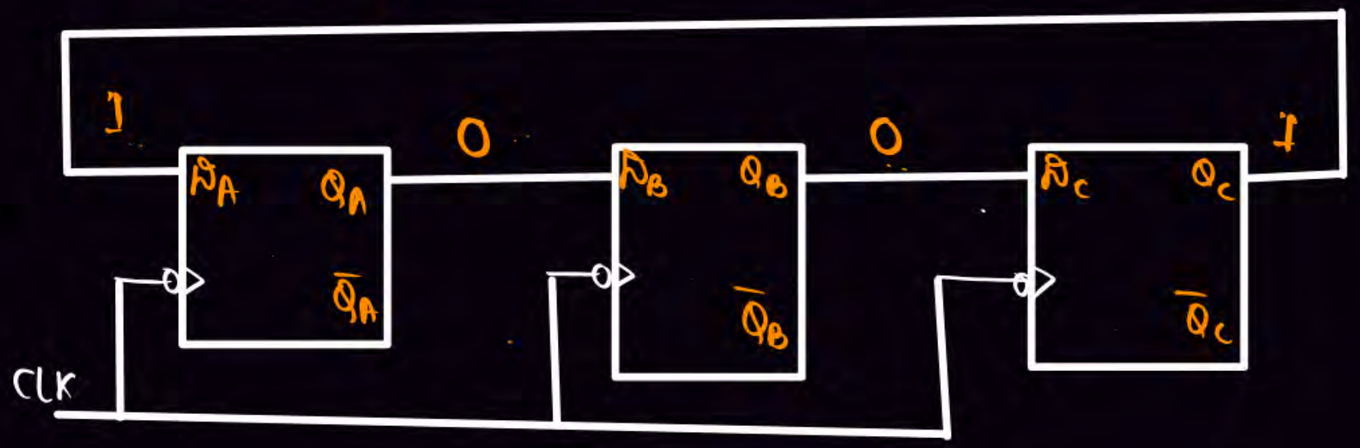
✓ 1) Ring counter

✓ 2) Johnson counter

① RING COUNTER :→

↳ It is a SISO shift Register in the form of Ring.

3 bit Ring counter



CLK	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	0	1	0
3	0	0	1
4	1	0	0
5	0	1	0
6	0	0	1

3 bit Ring counter

1 0 0
0 1 0
0 0 1

MOD-3

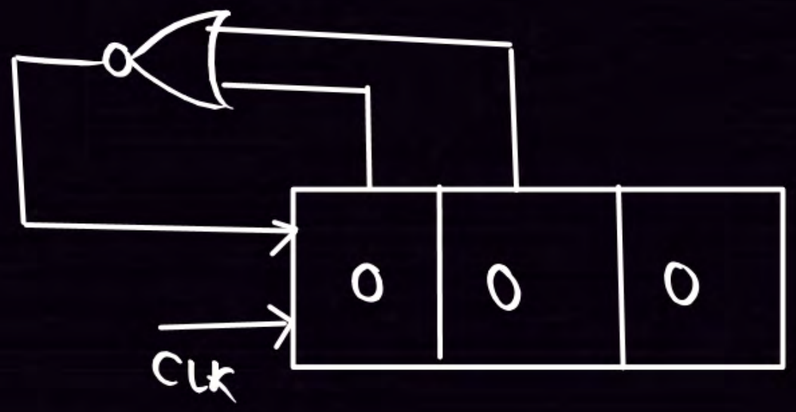
4 bit Ring counter

1 0 0 0
0 1 0 0
0 0 1 0
0 0 0 1

MOD-4

"N" bit Ring counter

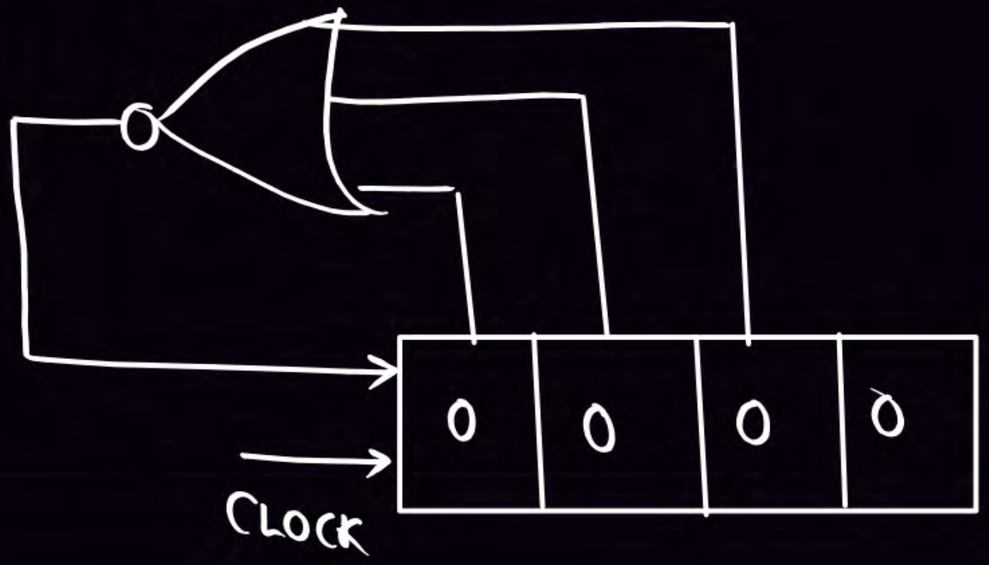
MOD = used states = N



1 0 0

0 1 0

0 0 1

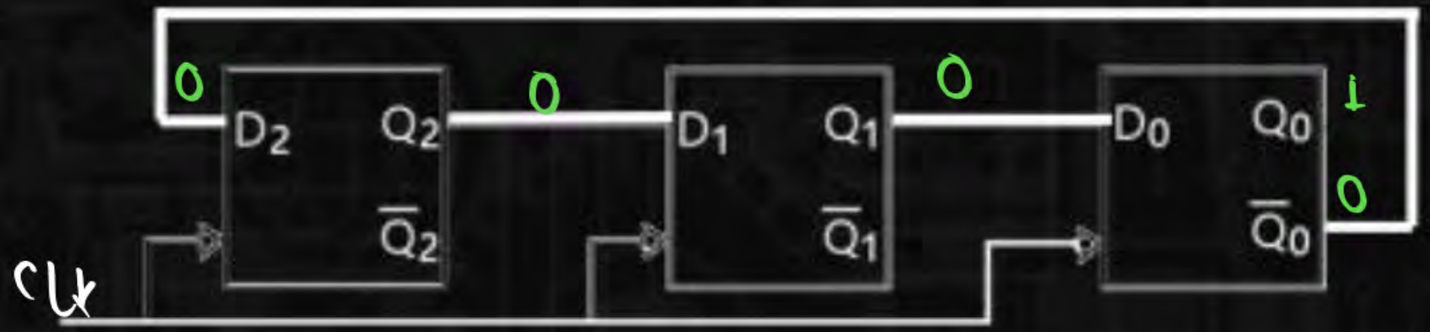


1 0 0 0
0 1 0 0
0 0 1 0
0 0 0 1

Self starting Ring counter

JOHNSON COUNTER

- Twisted Ring Counter
- Creeping Counter
- Mobies Counter
- Walking Counter



MOD - 6

Clock	Q_2	Q_1	Q_0
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1
6	0	0	0
7	1	0	0
8	1	1	0
9	1	1	1

3 bit Johnson counter

MOD-6

0	0	0
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1

4 bit Johnson counter

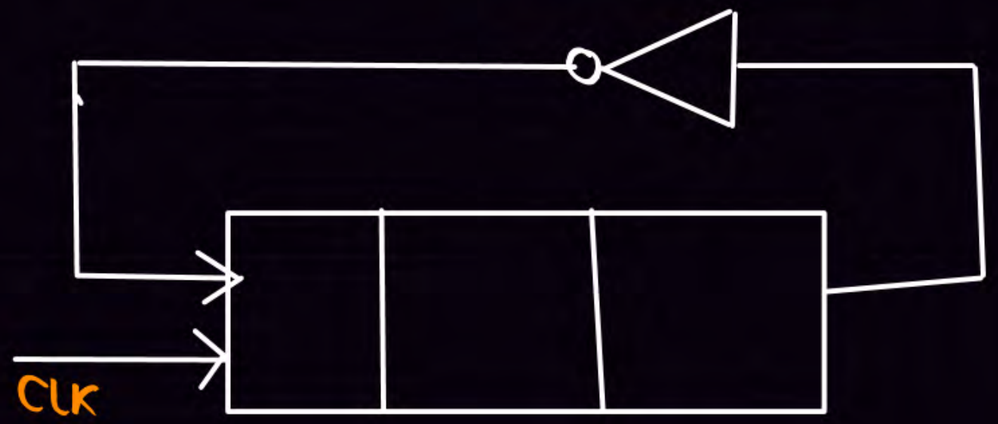
MOD-8

0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1

"N" bit Johnson counter

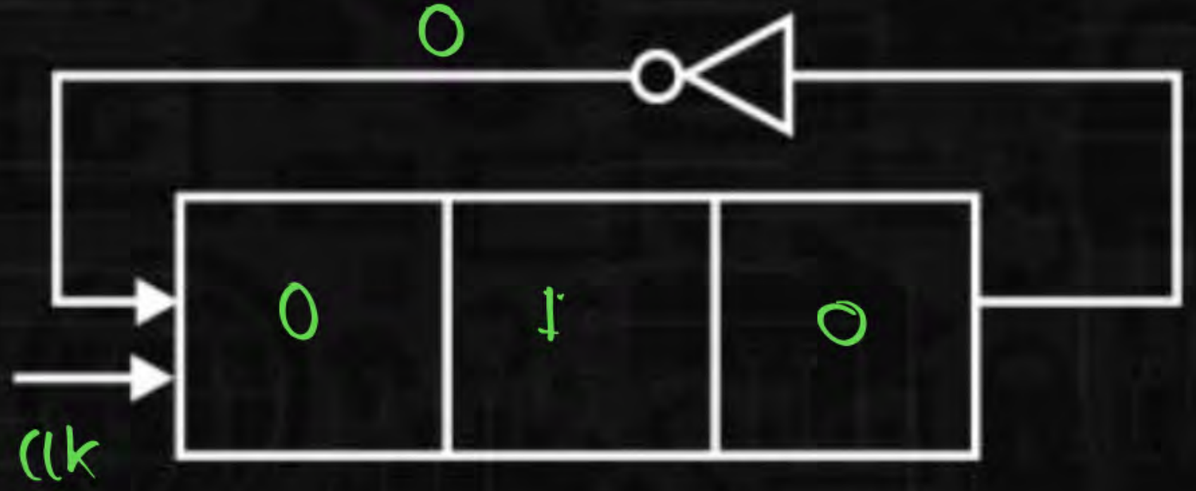
MOD = Used states = 2N

"Symbolic Representation."



LOCK OUT PROBLEM

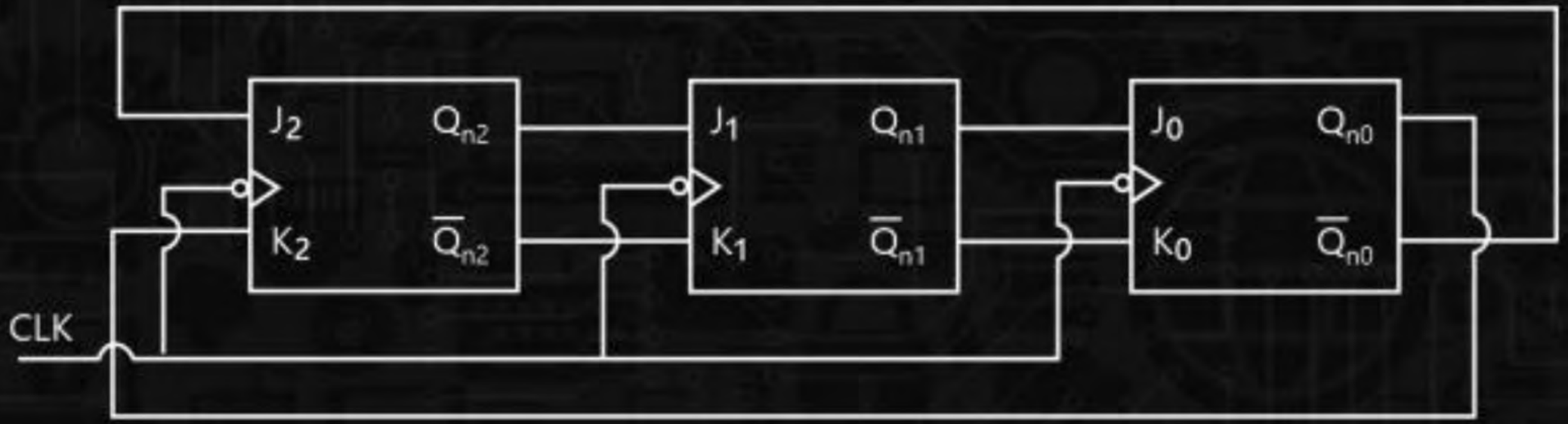
- Whenever Johnson Counter enters into its unused state then it will lock into its unused state is called lock out problem.



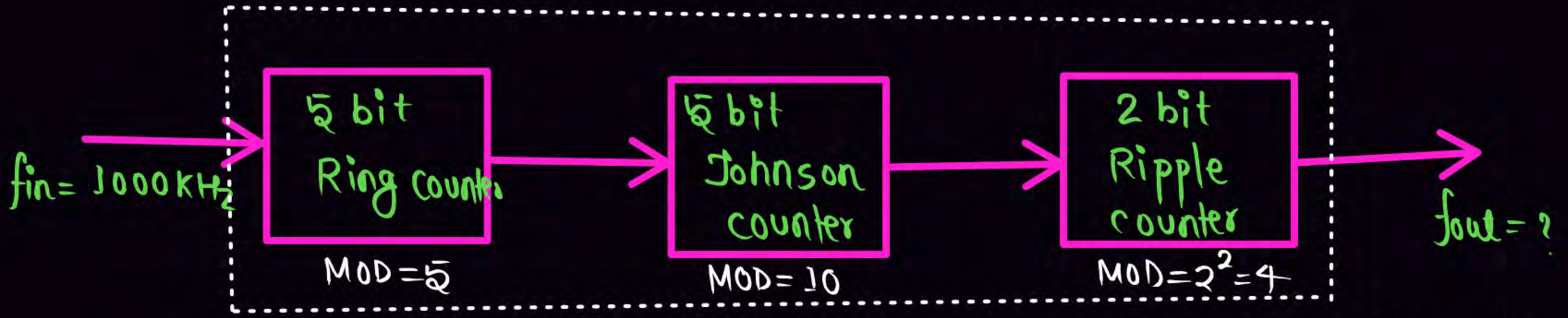
Clock	Q_2	Q_1	Q_0
0	0	1	0
1	1	0	1
2	0	1	0
3	1	0	1
4	0	1	0
5			
6			
7			
8			
9			

MOD-2

JOHNSON COUNTER BY USING JK FLIP FLOP



MOD [5x10x4] ⇒ MOD = 200



$$f_{out} = \frac{f_{in}}{MOD}$$

$$= \frac{1000\,kHz}{200}$$

$$= 5\,kHz$$

DESIGNING OF SYNCHRONOUS COUNTER

STEP 1. Write the Previous and Present State.

STEP 2. Write the Excitation Table of FF.

STEP 3. Write the Logical Expression.

STEP 4. Minimize the Logical expression.

STEP 5. Hardware Implementation.

Q. Design a Synchronous Counter by using D Flip Flop which count the sequence $0 \to 2 \to 1 \to 3 \to 0$

$\{00 \to 10 \to 01 \to 11 \to 00 \to \ldots\}$

Step 1 :→

Step 2.

Q_1	Q_0	Q_1^+	Q_0^+	D_1	D_0
0	0	1	0	1	0
0	1	1	1	1	1
1	0	0	1	0	1
1	1	0	0	0	0

Step 3.

$D_1 = \bar{Q}_1 \bar{Q}_0 + \bar{Q}_1 Q_0$

Step 4

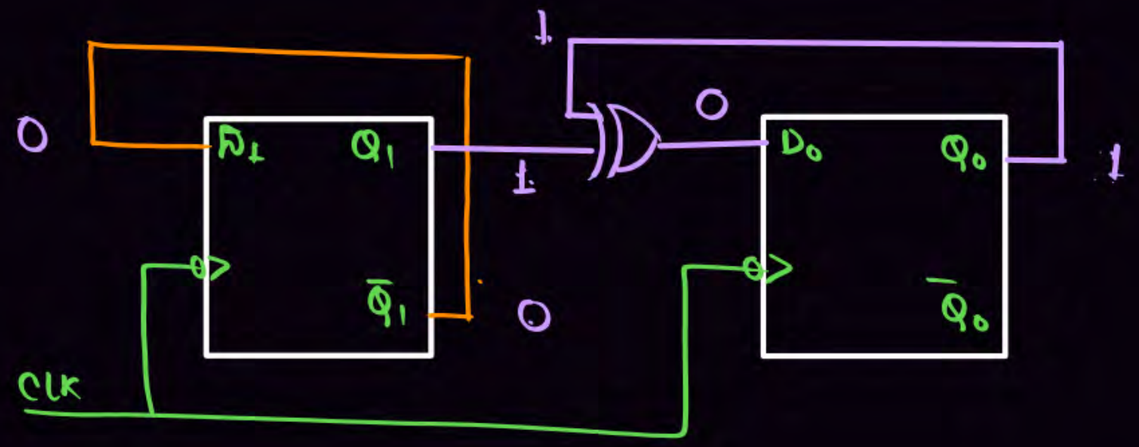
$D_1 = \bar{Q}_1 (\bar{Q}_0 + Q_0)$

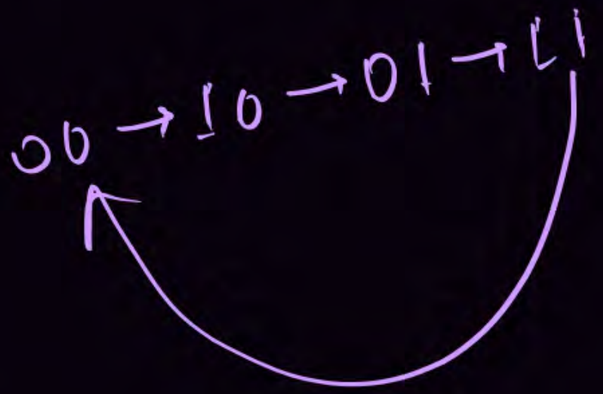
$D_1 = \bar{Q}_1$

$D_0 = \bar{Q}_1 Q_0 + Q_1 \bar{Q}_0$

$D_0 = Q_1 \oplus Q_0$

Step5.





Justification

CLK	Q_1	Q_0
0	0	0
1	1	0
2.	0	1
3.	1	1
4	0	0

MOD-4

Q. Design a Synchronous Counter by using T Flip Flop which count the sequence $0 \to 2 \to 3 \to 0$ $\{00 \to 10 \to 11 \to 00\}$

Step 1 & Step 2.

Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_0
0	0	1	0	1	0
0	1	x	x	x	x
1	0	1	1	0	1
1	1	0	0	1	1

Steps & Step 4.

T_1

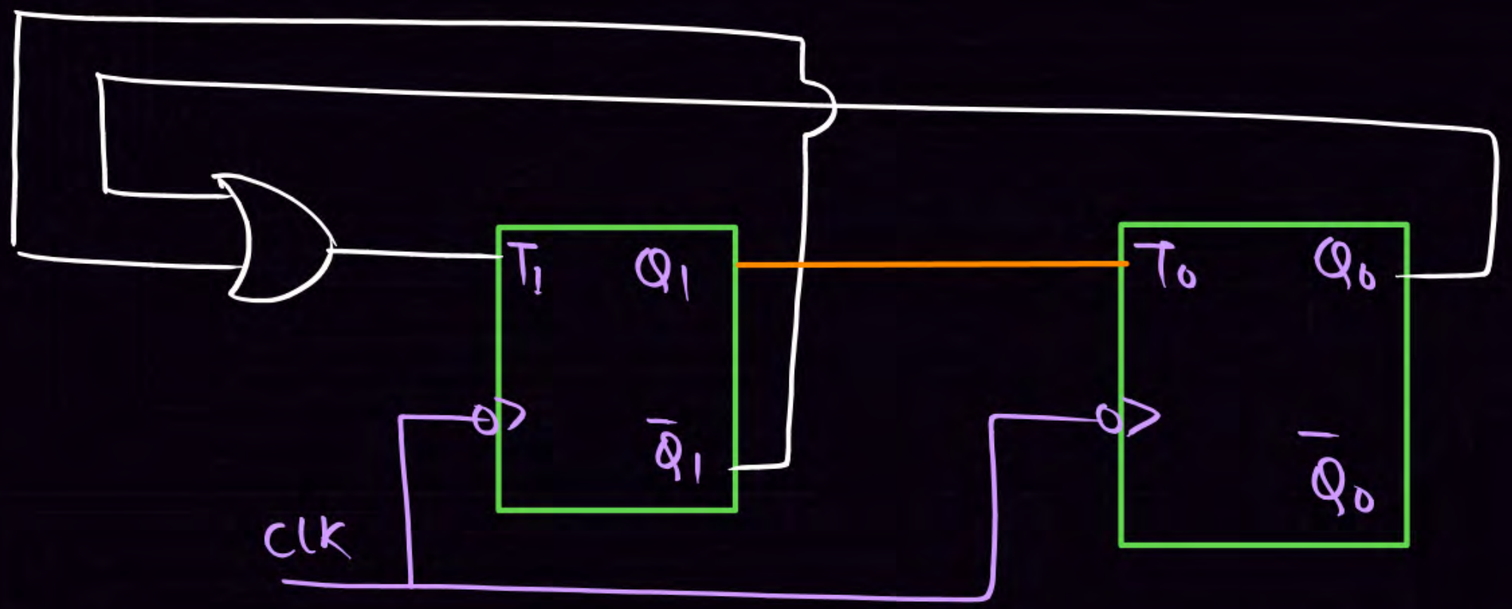
$T_1 = \bar{Q}_1 + Q_0$

Q_1 \ Q_0	0	1
0	1	X
1		1

T_0

$T_0 = Q_1$

Q_1 \ Q_0	0	1
0		X
1	1	1


T_1
Q_1
$\bar{Q}_1$
T_0
Q_0
$\bar{Q}_0$
CLK

Q.

Design a Synchronous Counter by using JK Flip Flop which count the sequence $0 \rightarrow 2 \rightarrow 3 \rightarrow 5 \rightarrow 1 \rightarrow 6 \rightarrow 0$

HW

Q.

HW

Design a Synchronous Counter by using T Flip Flop which count the sequence $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 0$


THANK YOU GW
SOLDIERS !