CS & IT ENGINEERING





Combinational Circuit

Lecture No. 6



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TOPICS TO BE COVERED **01** MULTIPLEXER

02 QUESTION PRACTICE

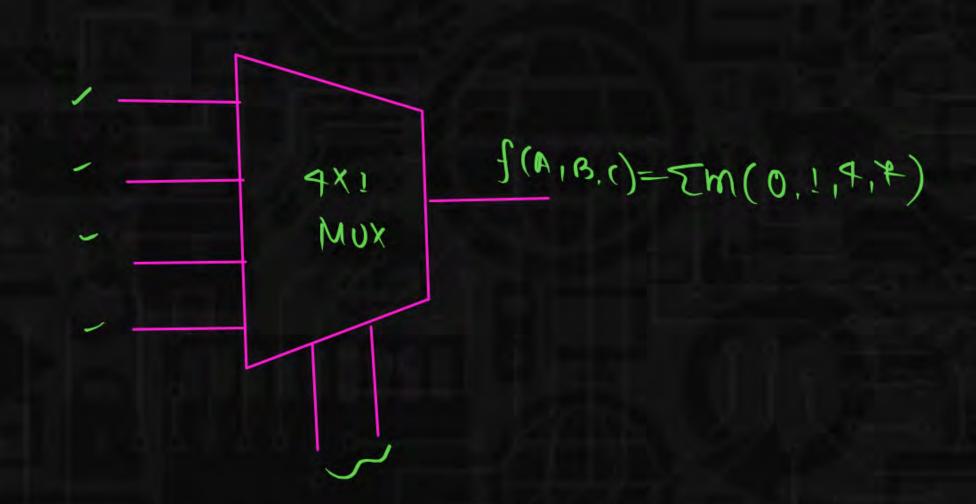
03 DISCUSSION

By using 4 x 1 MUX



$$f(A,B,C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC = \Xi m(0,1,4,7)$$

- 1. AB as a select line
- 2. BC as a select line
- 3. AC as a select line





1. AB is a select line



$$f(A,B,C) = (\overline{A}\overline{B})\overline{C} + (\overline{A}\overline{B})C + A\overline{B}\overline{C} + ABC$$

$$= \sum_{n=1}^{\infty} m(0,1)A_{n}^{n}$$

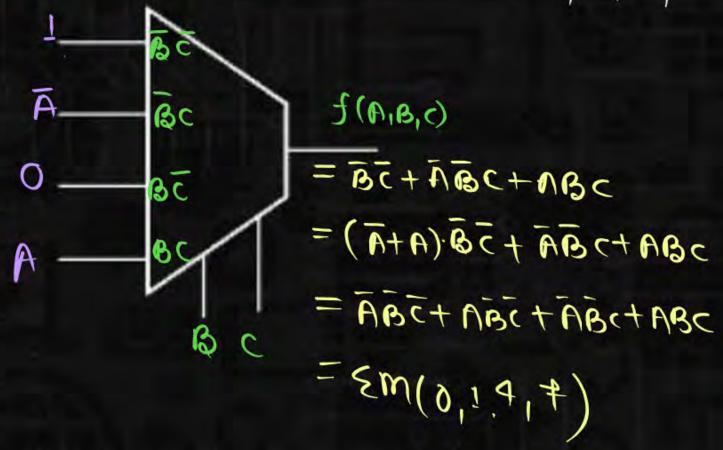
	ĀB	AB	AĒ	AB.
c	ĀĀŌ	AB C 2	ABC	ABT
C	ABC	ABC 8	ABC 5	ABC (7)
	1	0	10	С



BC is a select line

$$f(A,B,C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$$

$$\uparrow \uparrow \uparrow \uparrow = \leq m(0,1,4,7)$$

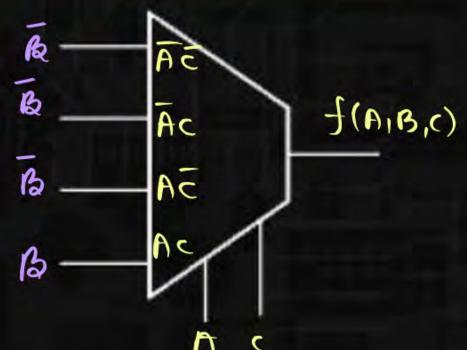


	R C	BC	B-C	BC	
Ā	ABC	ADC	ABC 2	ABC 3	
A	1 BE	₽ <u>8</u> c	₽8 <u>c</u>	ABC T	
	1	Ā	0	A	



3. AC as a select line

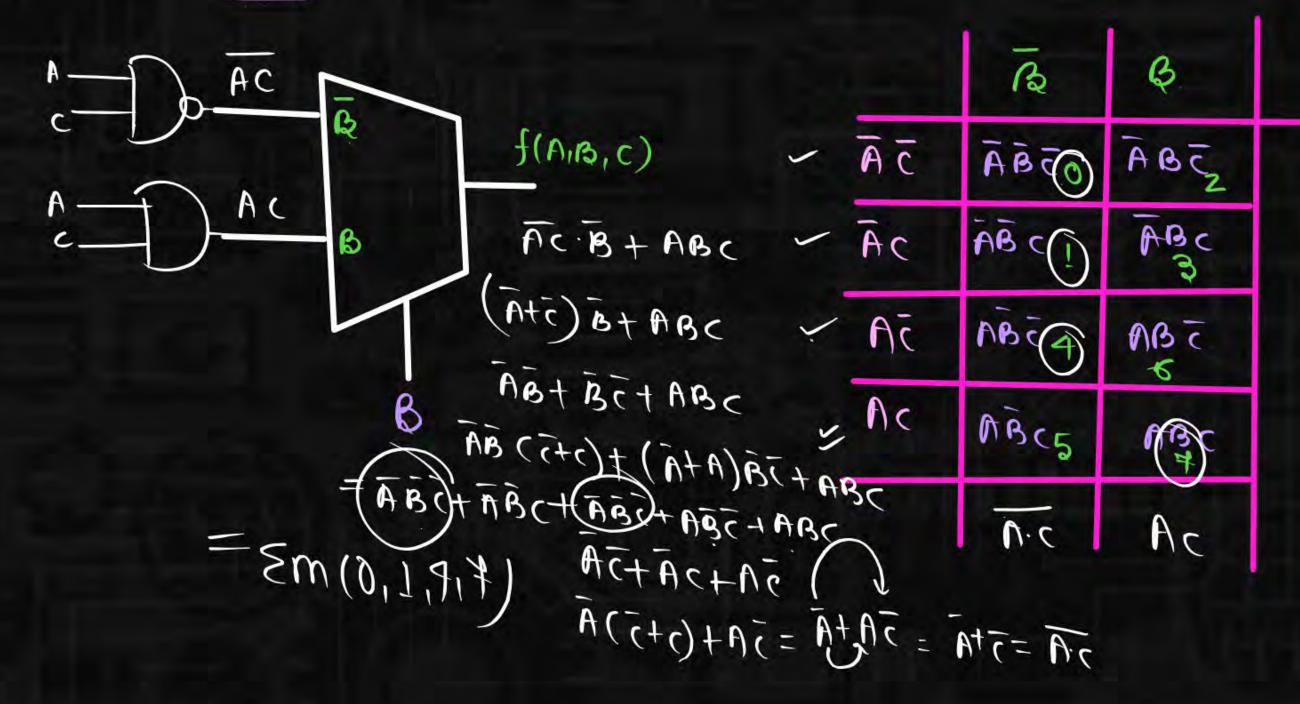
$$f(A,B,C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$$
$$= \bar{c}m(o,1,4,7)$$



	ĀĒ	ÃC.	5A	Ac
B	ABCO	Aē &	ABC	ABC S
Q	ABC 2	ABC	MBC 6	#BC
	-B	18	B	3

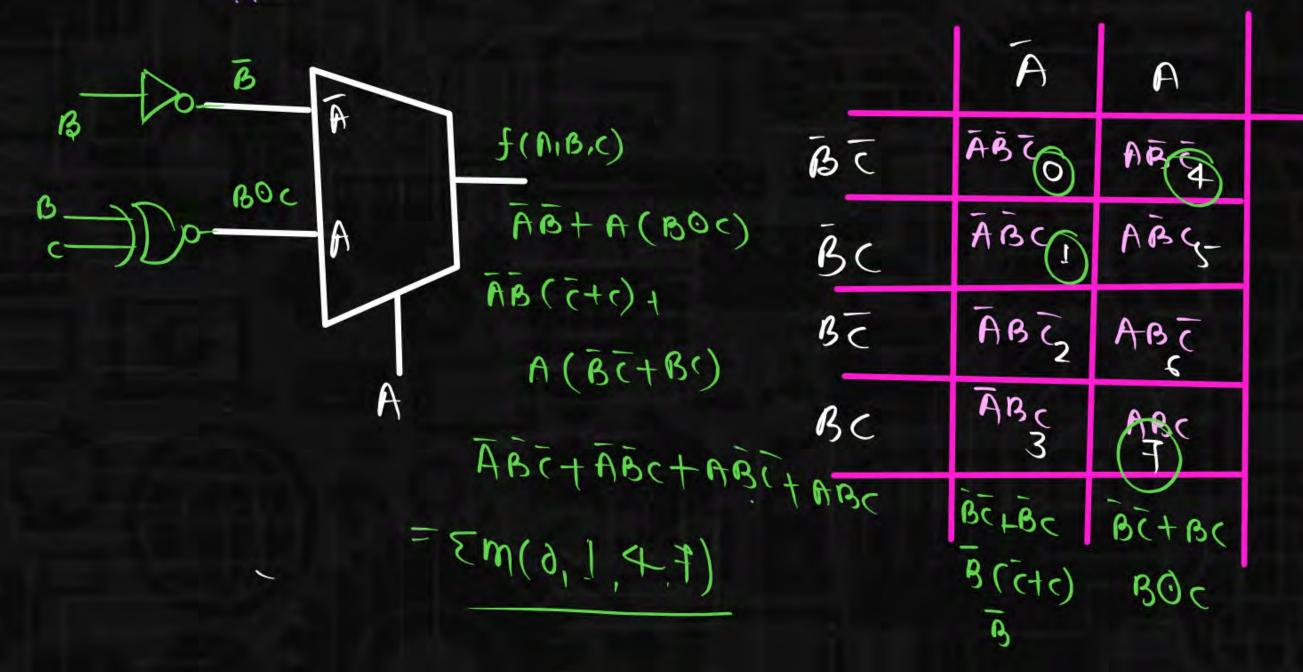
By using 2 x 1 MUX





By using 2 x 1 MUX





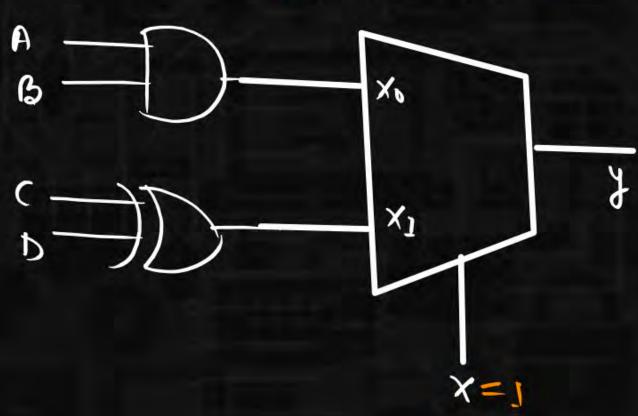


 $f(A,C,B,D) = \Sigma M(0, 1, 3, 5, 7, 9, 12, 15)$

- 1. ABD as select line SXIMUX
 2. ACD as a select line. SXIMUX
- b) Ara as a select line of AXI MUX

Type- 6 Delay







for 'y' find the maximum and minimum Belay?

Cose (1) X = 0 T = TAND + TMUY = 10 + 15 = (25 MS)Cose (2) X = 1

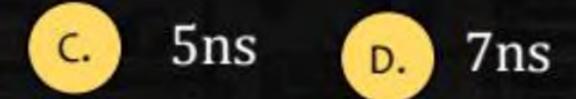




The propagation delays of the XOR gate, AND gate multiplexer (MUX) in the circuit shown in the figure are 4 ns, 2 ns and 1 ns, respectively.

If all the inputs P, Q, R, S and T are applied simultaneously and held constant, the maximum propagation delay of the circuit is

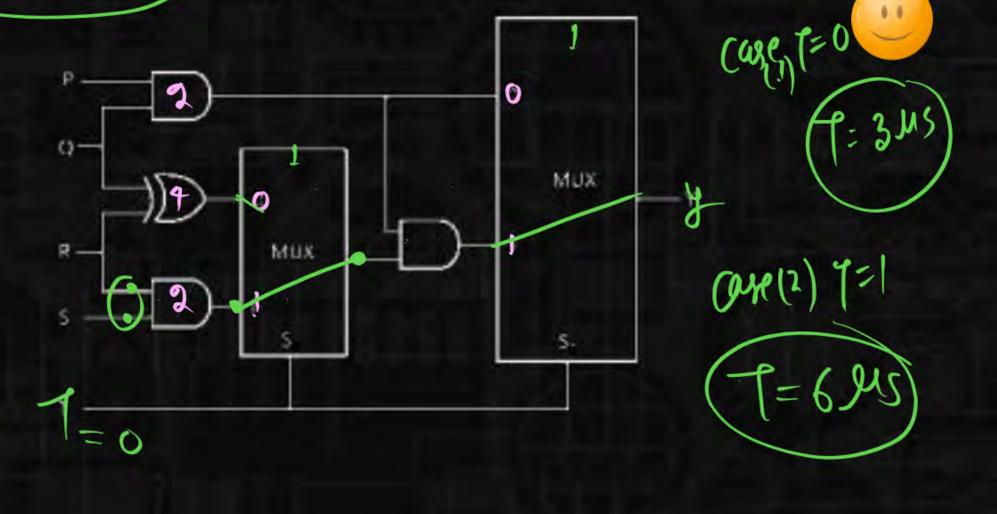




(E) Sir, Mujhe nahi ata,

Kyuki Mai Tare jameen T=0

par hum







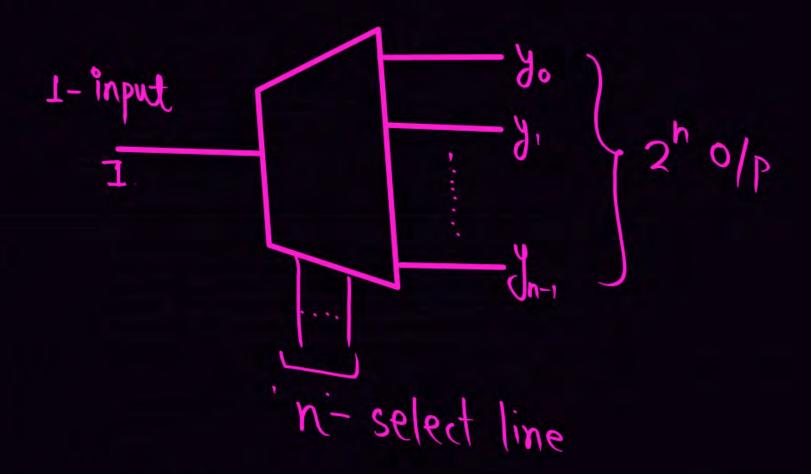
HALF Adder की वनाने के लिये कितने 2X1 MUX?

Sum =
$$A \oplus B = \overline{A}B + A\overline{B}$$

Corry = AB

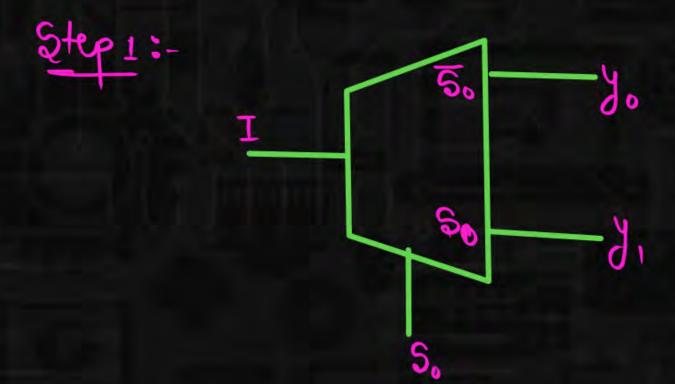


D-MUX.



Q.

Design a 1 × 2 DE-MUX?





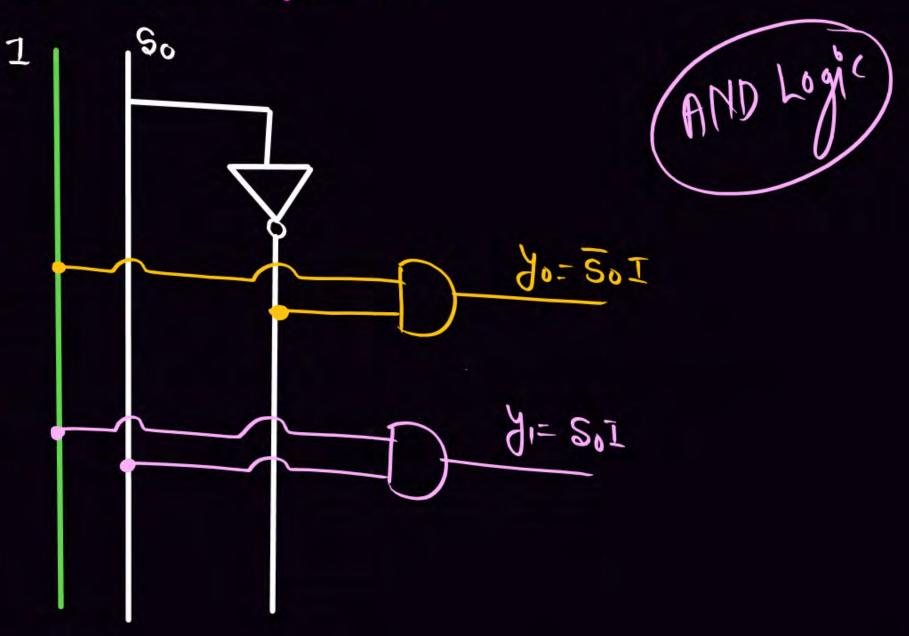
Step.a.

S.	7.	y ₁
0	I	0
1	0	1

Stepa: Minimization.



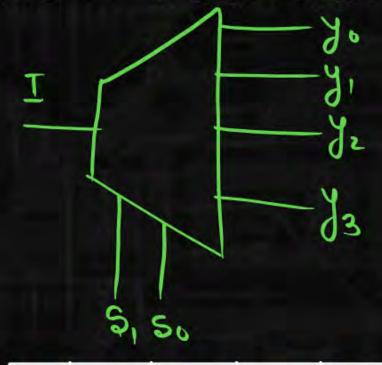
$$\partial_0 = \overline{S}_0 I$$
 $\partial_1 = S_0 I$



Q.

Design a 1 × 4 DE-MUX?





S,	So	9.		92	93
0	0	1	0	0	0
0	J.		I	0	0
1	0	0	0	Į	0
1	J	0	0	0	I





Step 5:

$$\begin{array}{c} \overline{S}_{1} & \overline{S}_{0} \\ \overline{S}_{1} & \overline{S}$$



(1X8 De-MUX

1 X 16 De-MUX





