

**SYSC 2310 A Introduction to Digital Systems**

**Lab Report**

**Lab 6: Sequential Logic Circuits**

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**Lab Section:** L2E

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## Pre-Lab

### Binary Counter Circuit Design

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## INTRODUCTION TO DIGITAL SYSTEMS

SYSC2310 (Fall 2021)

Dr. Mostafa Taha

D-Flip Flop

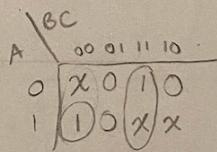
### Lab 6: Pre-Lab Answer Sheet [20% of the Discussion Grade]

#### Exercise 1.A: Design a Binary Counter

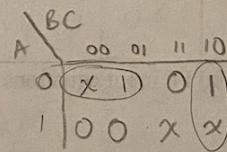
because 1,2,3,4,5

1- State Diagram:			3 State			2- State Table:			
PS	NS		A	B	C	FF in Eq	D <sub>A</sub>	D <sub>B</sub>	D <sub>C</sub>
000	xx x		x	x	x				
001	010		0	1	0				
010	011		0	1	1				
011	100		1	0	0				
100	101		1	0	1				
101	001		0	0	1				
110	xx x		x	x	x				
111	xx x		x	x	x				

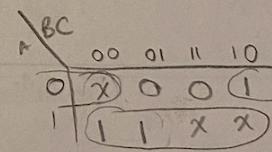
#### 3- K-Maps and FF input equations



$$DA = ABC + BC'$$



$$DB = A'B + BC'$$



$$DC = C' + A$$



## Binary Sequence Detector Design

**Exercise 2.A: Design a Binary Sequence Detector** D-FlipFlop

1- Problem Description:  
Detect  $1101 \rightarrow 1$

State 0	State 1	State 11	State 110	State 1101
O: NS = 0 1: NS = 1	O: NS = 0 1: NS = 11	O: NS = 110 1: NS = 11	O: NS = 0 1: NS = 1101	O: NS = 0 1: NS = 11

000    001    010    011    100

2- State Diagram

3- State Table

PS	IN	NS	OUT	FF
A'BC	X	A'BC	Y	D <sub>A</sub> D <sub>B</sub> D <sub>C</sub>
000	0	000	0	0 0 0
000	1	001	0	0 0 1
001	0	000	0	0 0 0
001	1	010	0	0 1 0
010	0	011	0	0 1 1
010	1	010	0	0 1 0
011	0	000	0	0 0 0
011	1	100	0	1 0 0
100	0	000	1	0 0 0
100	1	010	1	0 1 0

4- K-Maps and FF input equations

AB\CX	AB\CX	AB\CX
00 00 01 11 10	00 00 01 11 10	00 00 01 11 10
00 0 0 0 0	00 0 0 1 0	00 0 1 0 0
01 0 0 1 0	01 1 1 0 0	01 1 0 0 0
11 X X (X) X	11 X X X X	11 X X X X
10 0 0 X X	10 0 1 X X	10 0 0 X X

DA = BCX      DB = BC' + AX + BC'X      DC = A'B'C'X + BC'X

5- Circuit Schematic

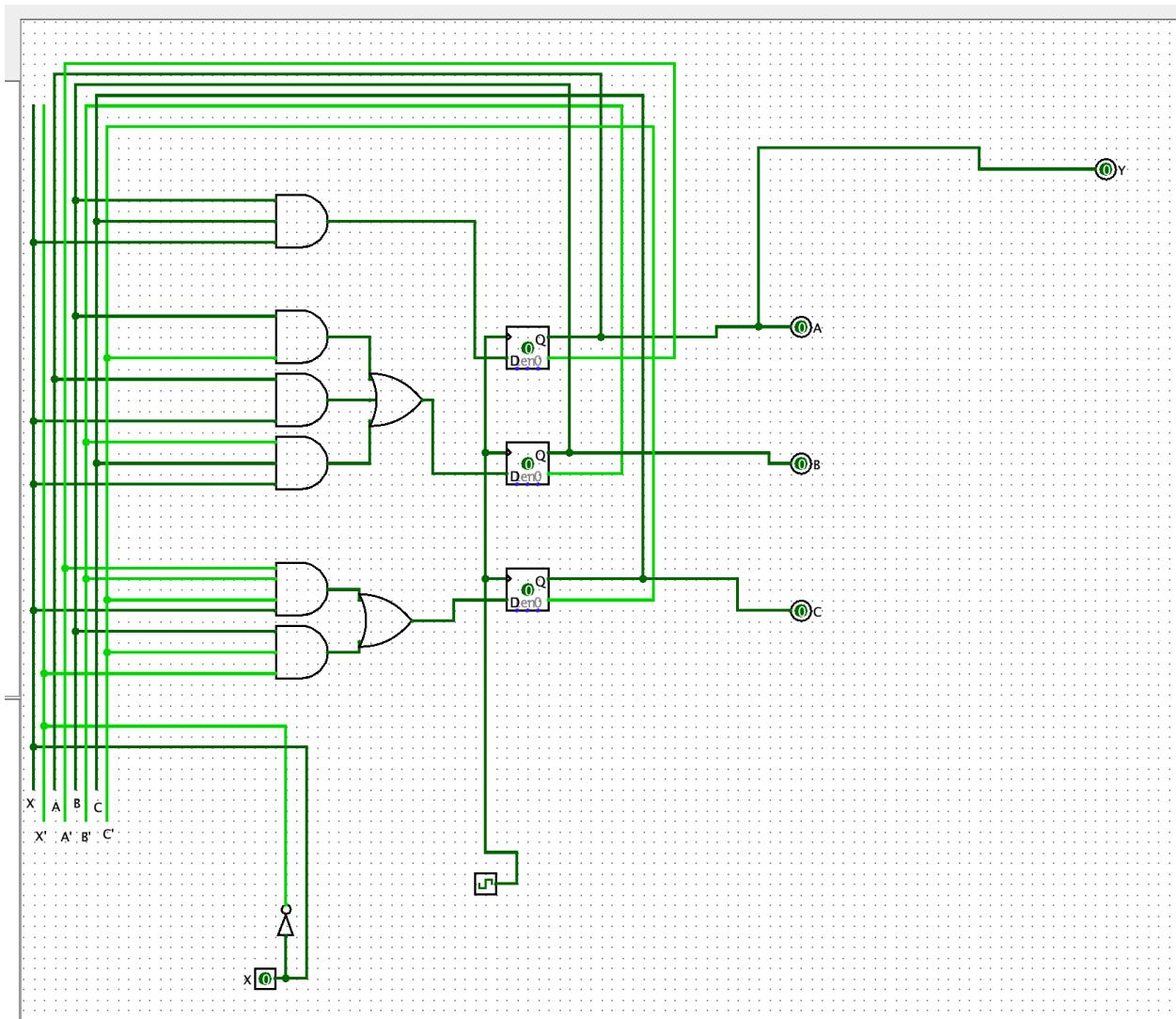
A / BC

AB	00 01 11 10
0	0 0 0 0
1	1 X X X

y = A

Total Number of Gates (excluding the D-FFs): ..... (you can use additional sheets if needed)

# Binary Sequence Detector Design circuit



Binary Sequence Detector Design logging

## Binary Sequence using Jk Flip flops design

### Exercise 3.A: Design a Binary Sequence Detector using JK flip-flops

Detect  $1101 \rightarrow 1$

#### 1- Problem Description:

State 0

State 1

State 11

State 110

State 1101

$$O: NS = 0 \\ I: NS = 1$$

$$O: NS = 0 \\ I: NS = 11$$

$$O: NS = 110 \\ I: NS = 11$$

$$O: NS = 0 \\ I: NS = 11$$

Invalid

$$Y_0 = 0 \\ Y_1 = 0$$

$$Y_0 = 0 \\ Y_1 = 0$$

$$Y_0 = 0 \\ Y_1 = 0$$

$$Y_0 = 0 \\ Y_1 = 1$$

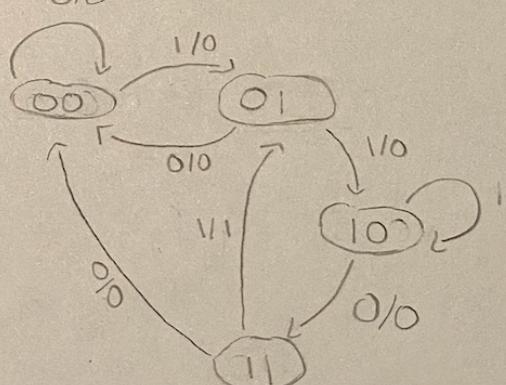
00

01

10

11

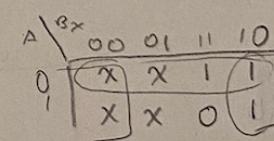
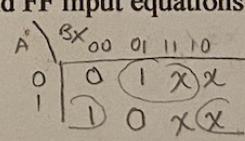
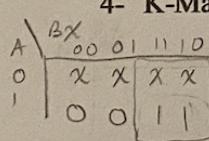
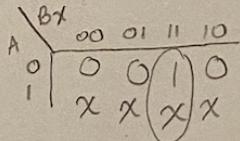
#### 2- State Diagram



#### 3- State Table

PS	IN	NS	OUT	FF
AB	X	AB	Y	J <sub>A</sub> K <sub>A</sub> J <sub>B</sub> K <sub>B</sub>
00	0	00	0	0X 0X
00	1	01	0	0X 1X
01	0	00	0	0X X1
01	1	10	0	1X X1
10	0	11	0	X0 1X
10	1	10	0	X0 0X
11	0	00	0	X1 X1
11	1	01	1	X1 X0

#### 4- K-Maps and FF input equations



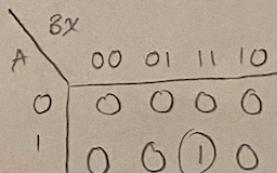
$$J_A = BX$$

$$K_A = B$$

$$J_B = A'X + AX'$$

$$K_B = A' + X'$$

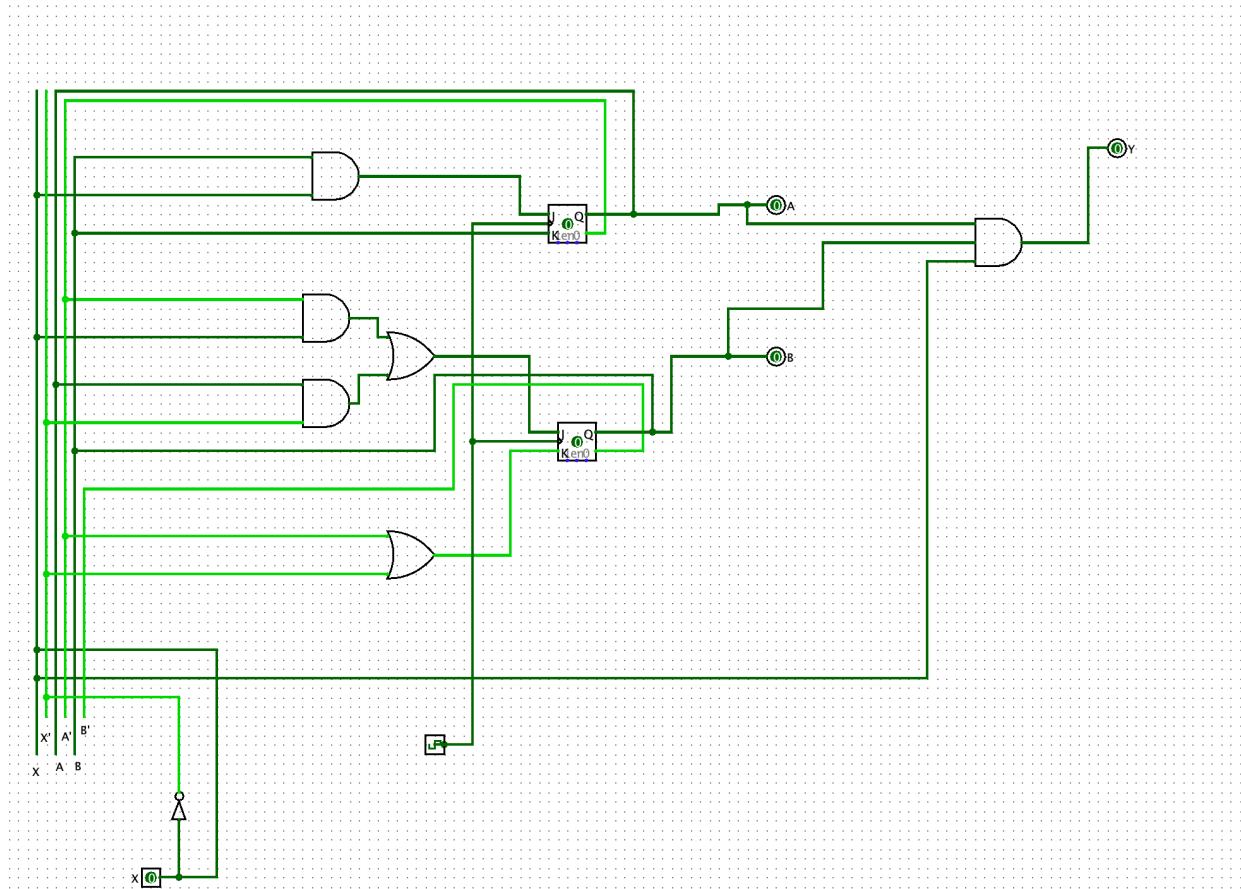
#### 5- Circuit Schematic



$$Y = ABX$$

Total Number of Gates (excluding the D-FFs used inside the JK-FF): .....

Binary Sequence using Jk Flip flops design circuit



Binary Sequence using Jk Flip flops design logging

File	Edit	Format	View	Help
X	CLK	Y		
0	1	0		
0	0	0		
1	0	0		
1	1	0		
1	0	0		
1	1	0		
1	0	0		
0	0	0		
0	1	0		
0	0	0		
1	0	1		
1	1	0		
1	0	0		
1	1	0		
1	0	0		
0	0	0		
0	1	0		
0	0	0		
1	0	1		
1	1	0		
1	0	0		
1	1	0		