LAB #2 - SYSC 2310 L2E
Riya Arora (101190033)
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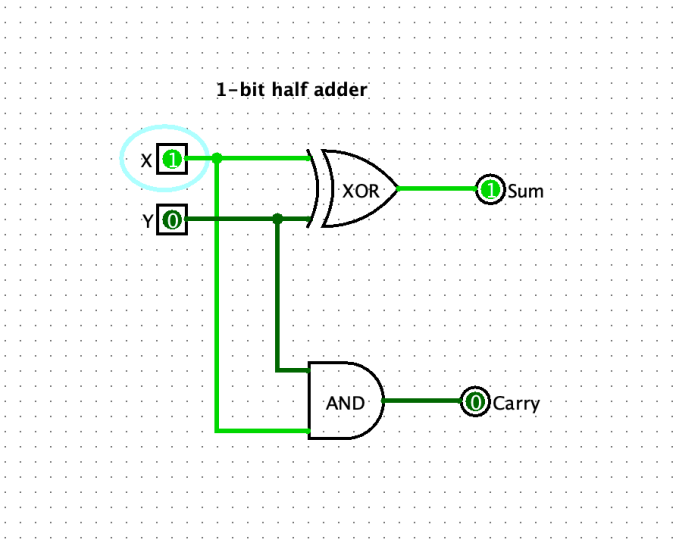
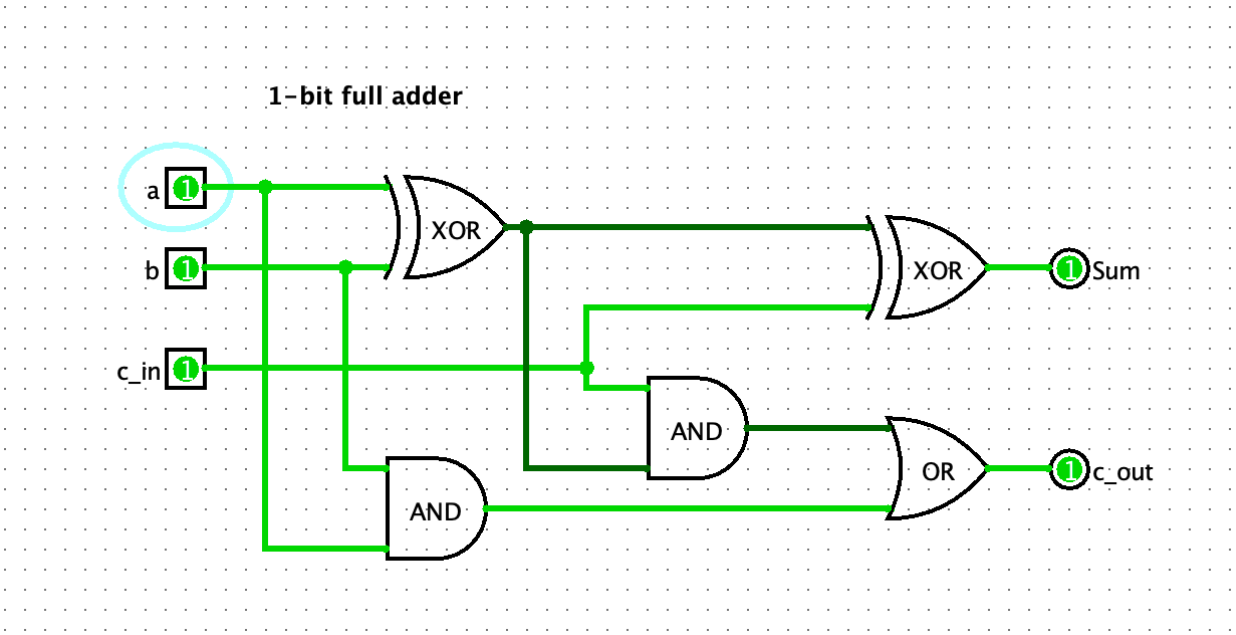
Screenshot 1: Build a 1-bit half adder



Screenshot 2: Simulation Logging File for 1-bit half adder

Carry	Sum	X	Y
0	0	0	0
0	1	0	1
1	0	1	1
0	1	0	1
0	0	0	0
0	1	0	1
1	0	1	1
0	1	0	1
1	0	1	1
0	1	1	0
0	0	0	0
0	1	1	0
0	0	0	0
0	1	1	0
0	0	0	0
0	1	0	1
0	0	0	0
0	1	0	1
0	0	0	0
0	1	1	0
0	0	0	0
0	1	1	0
0	0	0	0
0	1	1	0
1	0	1	1

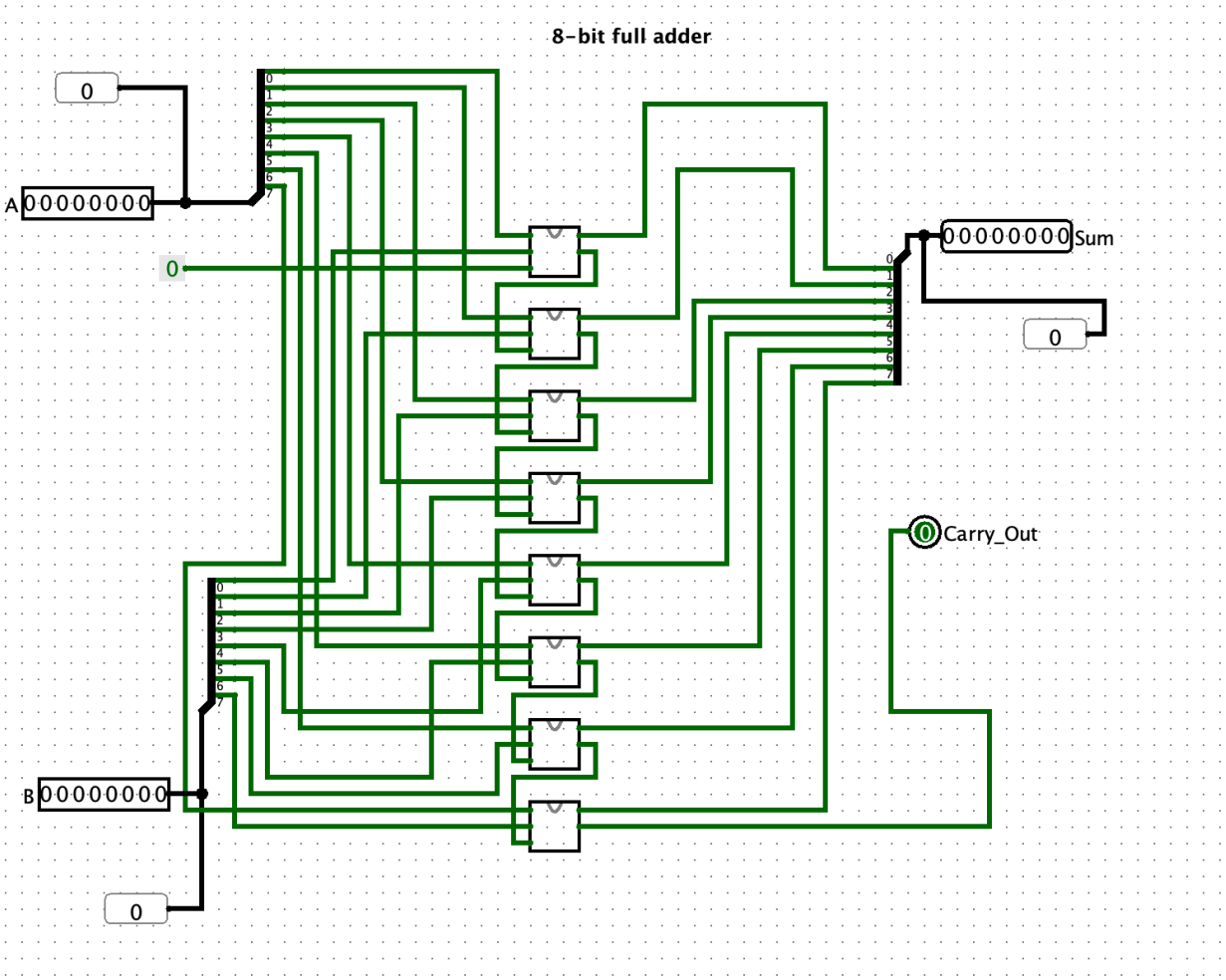
Screenshot 3: Build a 1-bit full adder



Screenshot 4: Simulation Logging File for 1-bit full adder

a	b	c_in	c_out	Sum
0	0	0	0	0
0	0	1	0	1
0	0	0	0	0
0	1	0	0	1
1	1	0	1	0
1	1	1	1	1
1	1	0	1	0
0	1	0	0	1
1	1	0	1	0
1	1	1	1	1
0	1	1	1	0
0	0	1	0	1
0	0	0	0	0
0	0	1	0	1
1	0	1	1	0
1	1	1	1	1
0	1	1	1	0
0	1	0	0	1
0	0	0	0	0
1	0	0	0	1
1	0	1	1	0

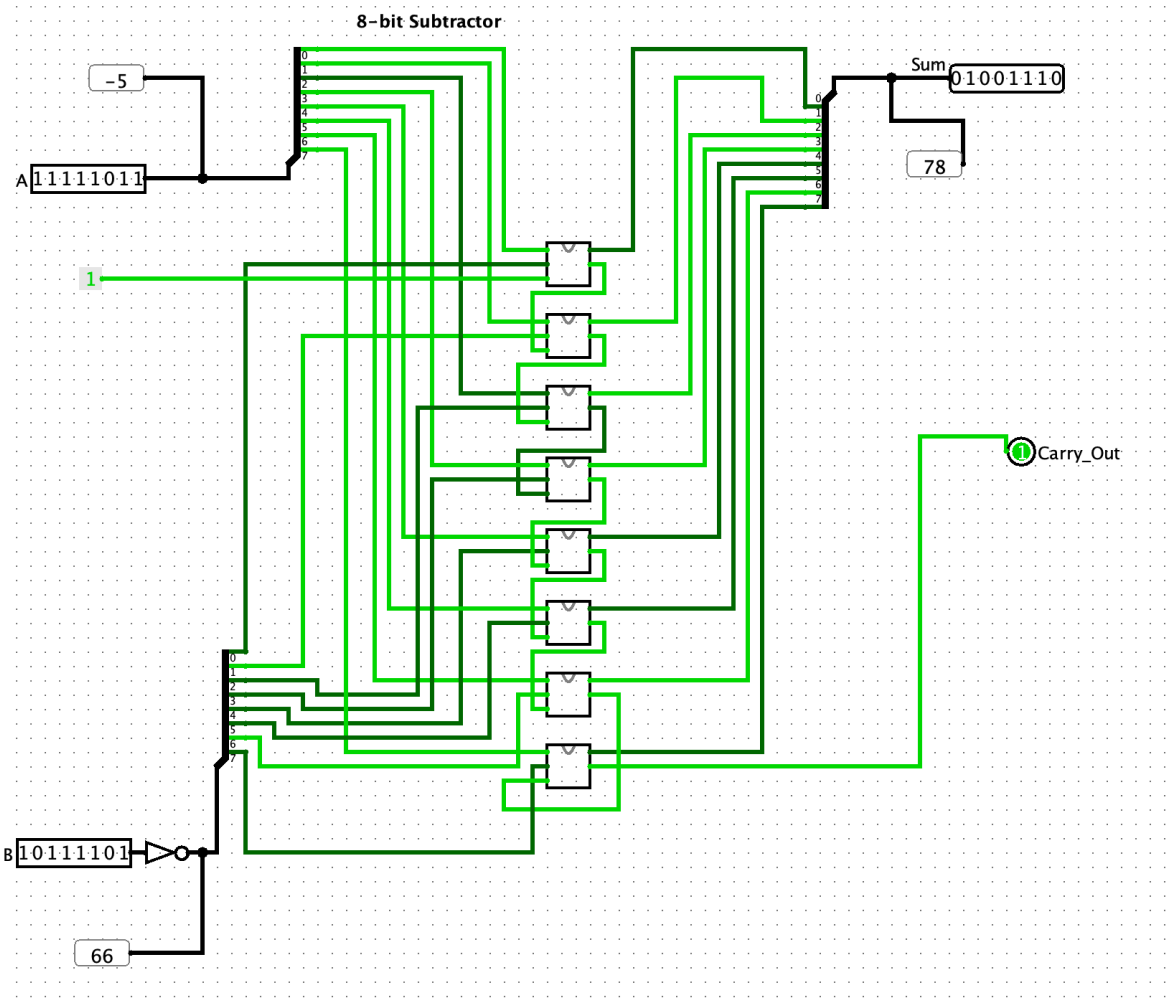
Screenshot 5: Build a 8-bit full adder



Screenshot 6: Simulation Logging File for 1-bit full adder

A	B	Carry_Out	Sum
0	128	0	128
0	144	0	144
0	208	0	208
0	240	0	240
0	248	0	248
0	252	0	252
0	253	0	253
0	249	0	249
128	249	1	121
192	249	1	185
208	249	1	201
216	249	1	209
217	249	1	210
221	249	1	214
223	249	1	216
159	249	1	152
223	249	1	216
255	249	1	248
239	249	1	232
231	249	1	224
229	249	1	222
228	249	1	221
224	249	1	217
232	249	1	225
248	249	1	241
184	249	1	177
56	249	1	49
24	249	1	17

Screenshot 7: Build an 8-bit Subtractor



Screenshot 8: Simulation Logging File for 8-but Subtractor

A	B	Carry_Out	Sum
0	14	0	242
128	14	1	114
192	14	1	178
224	14	1	210
240	14	1	226
248	14	1	250
252	14	1	246
254	14	1	Error
255	14	1	Error
255	15	1	Error
255	11	1	244
255	3	1	252
255	19	1	236
255	51	1	204
255	115	1	140
255	243	1	12
255	179	1	76
255	163	1	92
255	171	1	84
255	175	1	Error
255	174	1	Error
239	174	1	Error
235	174	1	Error
233	174	1	75