LAB #3 - SYSC 2310 L2E

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**Screenshot 1: Connect F1 and F2**

Diagram, schematic

Description automatically generated

**Screenshot 2: Connect F1 and F2 LOGGING**

A picture containing table

Description automatically generated

**Screenshot 3: MATH for part 1**

Text, letter

Description automatically generated

**Screenshot 4: Multiplier**

Diagram, schematic

Description automatically generated

**Screenshot 5: Multiplier LOGGING**

Shape

Description automatically generated

**Screenshot 6: 3-Bit by 2-Bit Binary Multiplier**

Diagram, schematic

Description automatically generated

**Screenshot 6: Simulation Logging File for 1-bit full adder**

**Screenshot 7: 3-Bit by 2-Bit Binary Multiplier LOGGING**

Table

Description automatically generated with medium confidence

**Screenshot 8: Simulation Logging File for 8-but Subtractor**

**Screenshot 8 – MATH FOR part 3**

**A piece of paper with writing on it

Description automatically generated**