

SYSC 2310 A Introduction to Digital Systems

Lab Report

Lab #4: Gate-Level Minimization

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Lab Section: L2E

Lab Section

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Pre-Lab

$$\begin{array}{l} \text{AND}_2 = 1 \\ \text{AND}_3 = 2 \end{array} \quad \begin{array}{l} \text{OR}_2 = 1 \\ \text{OR}_2 = 1 \end{array}$$

LAB 4 - Pre-Lab

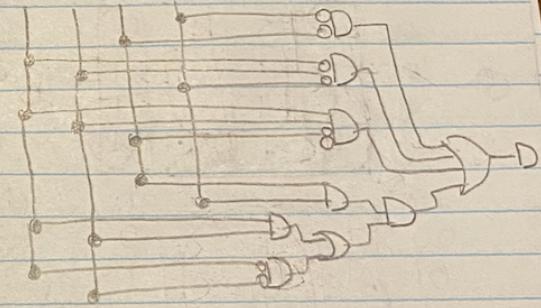
1A

A_3	A_2	A_1	A_0	P	D
0	0	0	0	0	1
0	0	0	1	0	0
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	1	0	1

$A_3 A_2$	00	01	11	10	D
00	1	0	0	0	1
01	1	0	0	0	1
11	1	0	0	0	0
10	1	1	1	0	0

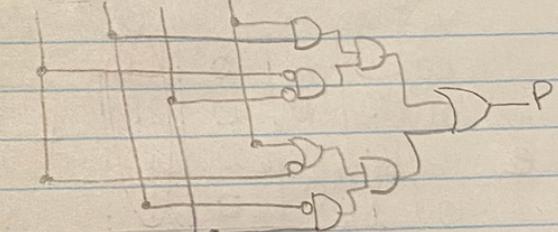
$$\begin{aligned} D &= A_1' A_0' + A_3' A_2 A_0' + A_3 A_2' A_1' \\ &\quad + A_3' + A_2' A_1 A_0 + A_3 A_2 A_1 A_0 \end{aligned}$$

$A_3 A_2 A_1 A_0$



$A_3 A_2$	00	01	11	10	P
00	0	0	0	1	0
01	0	1	1	0	1
11	0	1	0	0	0
10	0	0	1	0	1

$A_3 A_2 A_1 A_0$



$$\begin{aligned} P &= A_2 A_1' A_0 + A_2' A_1 A_0 + A_3' + \\ &\quad A_2' A_1 + A_3' A_2 A_0 \end{aligned}$$

$$P = A_2 A_0 (A_3' + A_1') + A_2' A_1 (A_3' + A_0)$$

(AND₂: 4)
OR₂: 3

Hilroy

D3	D2	D1	D0	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	0	1	0	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

a

A ₃ A ₂		A ₁ A ₀		
00	01	11	10	
00	1	0	1	1
01	0	1	1	1
11	x1	x1	x1	x1
10	1	1	x1	x1

b

A ₃ A ₂		A ₁ A ₀		
00	01	11	10	
00	1	1	0	0
01	1	0	1	0
11	x1	x0	x1	x0
10	1	1	x0	x1

c

A ₃ A ₂		A ₁ A ₀		
00	01	11	10	
00	1	1	1	1
01	1	1	1	1
11	x1	x1	x1	x1
10	1	1	x1	x0

d

A ₃ A ₂		A ₁ A ₀		
00	01	11	10	
00	1	0	1	1
01	0	1	0	1
11	x1	x1	x1	x1
10	1	1	x1	x1

e

A ₃ A ₂		A ₁ A ₀		
00	01	11	10	
00	1	0	0	1
01	0	0	0	1
11	x0	x0	x0	x1
10	1	0	x0	x1

f

A ₃ A ₂		A ₁ A ₀		
00	01	11	10	
00	1	0	0	0
01	1	1	0	1
11	x1	x1	x1	x1
10	1	1	x1	x1

g

A ₃ A ₂		A ₁ A ₀		
00	01	11	10	
00	0	0	1	1
01	1	1	0	1
11	x1	x1	x1	x1
10	1	x1	x1	x1

D3	D2	D1	D0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	x	x	x	x	x	x	x
1	0	1	1	x	x	x	x	x	x	x
1	1	0	0	x	x	x	x	x	x	x
1	1	0	1	x	x	x	x	x	x	x
1	1	1	0	x	x	x	x	x	x	x
1	1	1	1	x	x	x	x	x	x	x

12A

$$S_a = D'_2 D'_0 + D_1 + D_2 D_0 + D_3 D'_0$$

$$S_b = D'_2 + D'_1 D'_0 + D_1 D_0$$

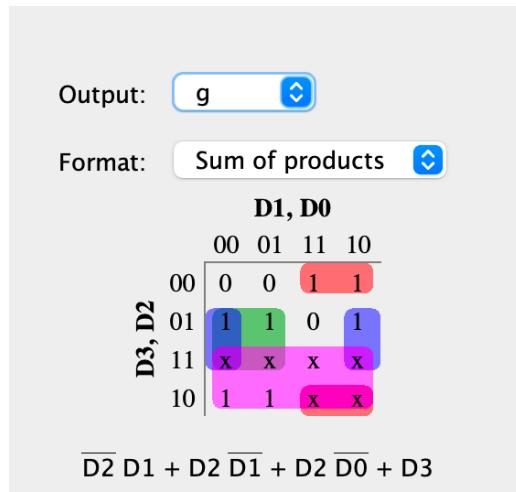
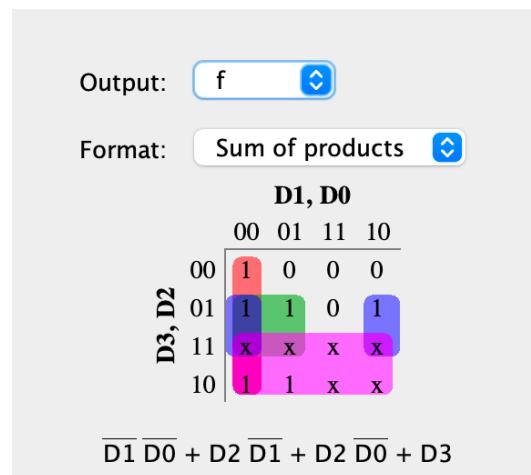
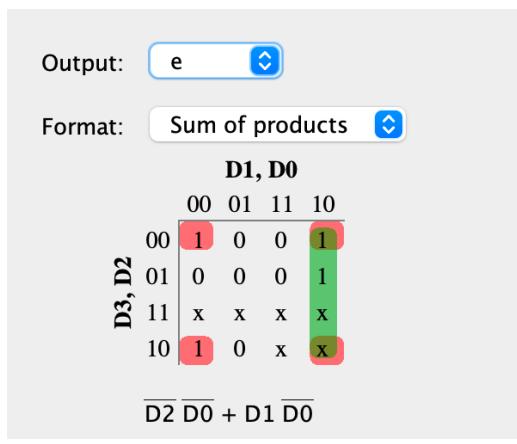
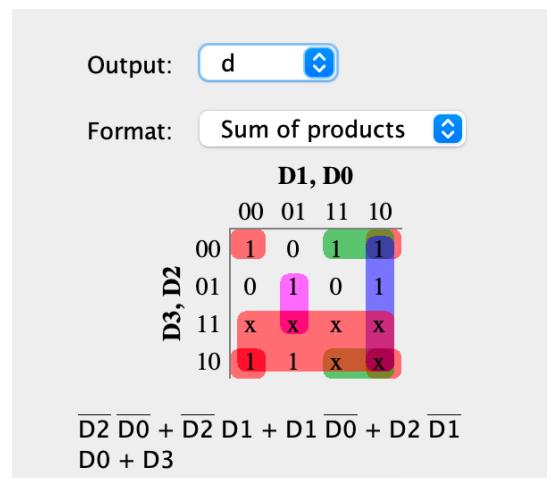
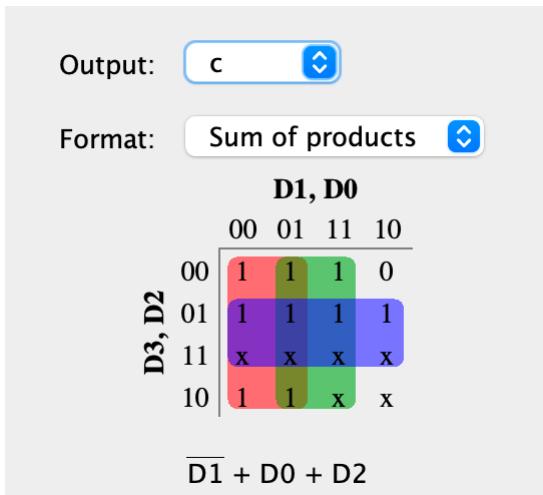
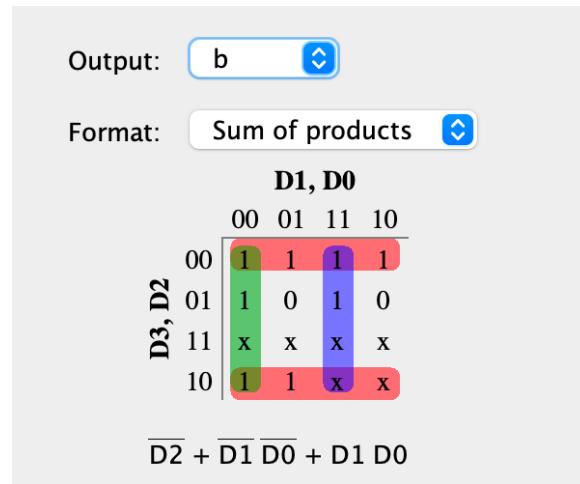
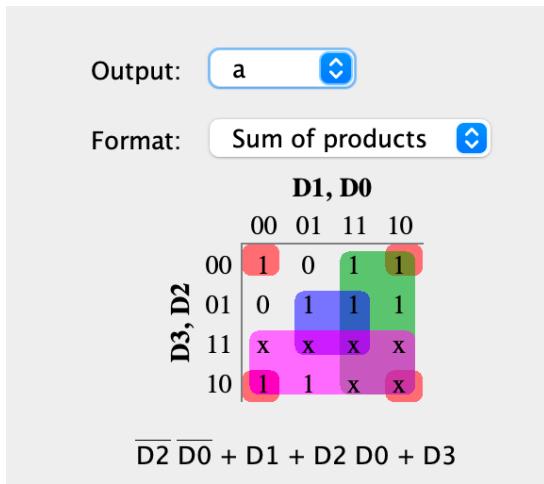
$$S_c = D'_1 + D_0 + D_2$$

$$S_d = D'_2 D'_0 + D'_2 D_1 + D_1 D'_0 + D_2 D'_1 D_0 + D_3$$

$$S_e = D'_2 D'_0 + D_1 D'_0$$

$$S_f = D'_1 D'_0 + D_2 D'_1 + D_2 D'_0 + D_3$$

$$S_g = D'_2 D_1 + D_2 D'_1 + D_2 D'_0 + D_3$$



Exercise 1

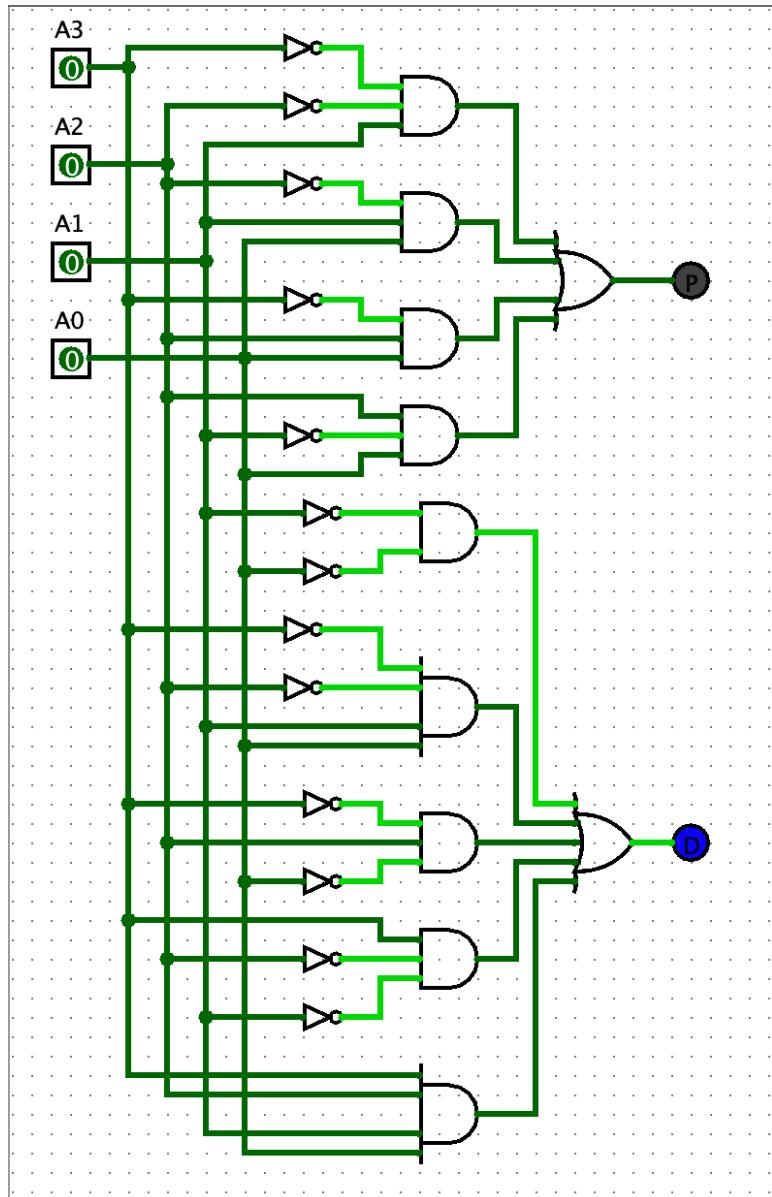
a. Equations Used for the Design

$$P = A_2 A_1' A_0 + A_2' A_1 A_0 + A_3' A_2' A_1 + A_3' A_2 A_0$$

$$D = A_1' A_0' + A_3' A_2 A_0' + A_3 A_2' A_1' + A_3' A_2' A_1 A_0 + A_3 A_2 A_1 A_0$$

b. Circuit Design

arbitrary function



c. Logging file Results

A0	A1	A2	A3	D	P
1	1	0	0	1	1
0	1	0	0	0	1
0	0	0	0	1	0
0	0	0	1	1	0
0	0	1	1	1	0
1	0	1	1	0	1
0	0	1	1	1	0
0	1	1	1	0	0
0	1	0	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0
1	1	1	0	0	1
0	1	1	0	1	0
0	1	0	0	0	1
0	0	0	0	1	0
0	1	0	0	0	1
0	1	1	0	1	0
1	1	1	0	0	1
1	1	1	1	1	0
1	1	1	0	0	1
1	1	1	1	1	0
1	1	1	0	0	1
1	1	1	1	1	0
1	1	1	0	0	1
1	1	1	1	1	0
1	1	1	0	0	1
1	1	1	1	1	0
1	1	1	0	0	1
1	1	0	0	1	1
1	0	0	0	0	0
0	0	0	0	1	0
1	0	0	0	0	0
0	0	0	0	1	0
0	0	1	0	1	0
0	0	0	0	1	0
0	0	0	1	1	0
0	0	0	0	1	0
0	0	1	1	1	0
0	0	0	1	1	0
0	1	0	1	0	0
0	0	0	1	1	0
1	0	0	1	1	0
0	0	0	1	1	0
1	0	0	1	1	0

d. Comments

Circuit Design and Logging File above.

Exercise 2

a. Equations Used for the Design

$$S_a = A_3 + A_1 + A_2 A_0 + A_2' A_0'$$

$$S_b = A_2' + A_1' A_0' + A_1 A_0$$

$$S_c = A_1' + A_0 + A_2$$

$$S_d = A_2 A_1' A_0 + A_2' A_0' + A_3 + A_1 A_0' + A_2' A_1$$

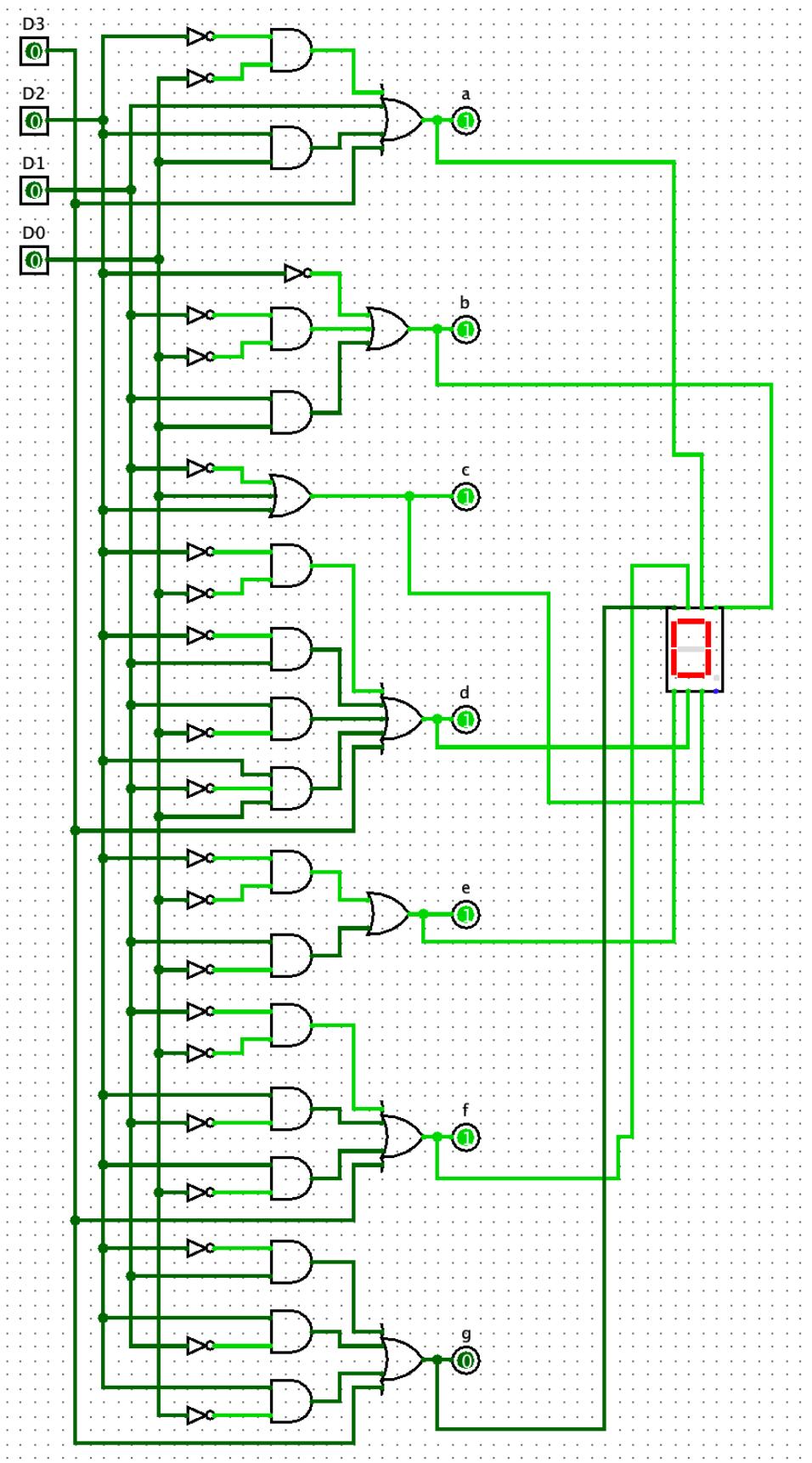
$$S_e = A_2' A_0' + A_1 A_0'$$

$$S_f = A_3 + A_1' A_0' + A_2 A_0' + A_2 A_1'$$

$$S_g = A_3 + A_2 A_1' + A_2 A_0' + A_2' A_1$$

7 Segement decoder

b. Circuit Design



c. Logging file Results



D3	D2	D1	D0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	1	1	1	1	1	1
1	1	0	0	1	0	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	1
1	1	1	1	1	1	1	0	0	1	1
0	1	1	1	1	1	1	0	0	0	0
0	0	1	1	1	1	1	1	0	0	1
0	0	0	1	0	1	1	0	0	0	0
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
1	0	0	1	0	1	1	1	0	1	1
1	1	0	1	1	0	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1	1
1	1	1	0	1	0	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1	1
1	1	0	1	1	0	1	1	0	1	1
1	1	1	0	1	1	0	1	0	1	1
1	1	1	1	1	0	1	1	0	1	1
1	0	0	1	0	1	1	1	0	1	1
1	1	0	1	1	0	1	1	0	1	1
1	0	0	1	0	1	1	1	0	1	1
0	0	0	1	0	1	1	0	0	0	0
1	0	0	1	0	1	1	1	0	1	1
0	0	0	1	0	1	1	0	0	0	0
0	1	0	1	1	0	1	1	0	0	0
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	0	0	0	0	0
0	1	0	1	1	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	0
0	1	0	0	1	1	0	1	0	1	1
1	1	0	0	1	1	0	1	0	1	1
0	1	0	0	1	0	1	1	0	1	1

Lab4_Ex2_Log.txt

d. Comments

Circuit Design and Logging File above.