

SYSC 2310 A Introduction to Digital Systems

Lab Report

Lab 5: Combinational Logic Circuits

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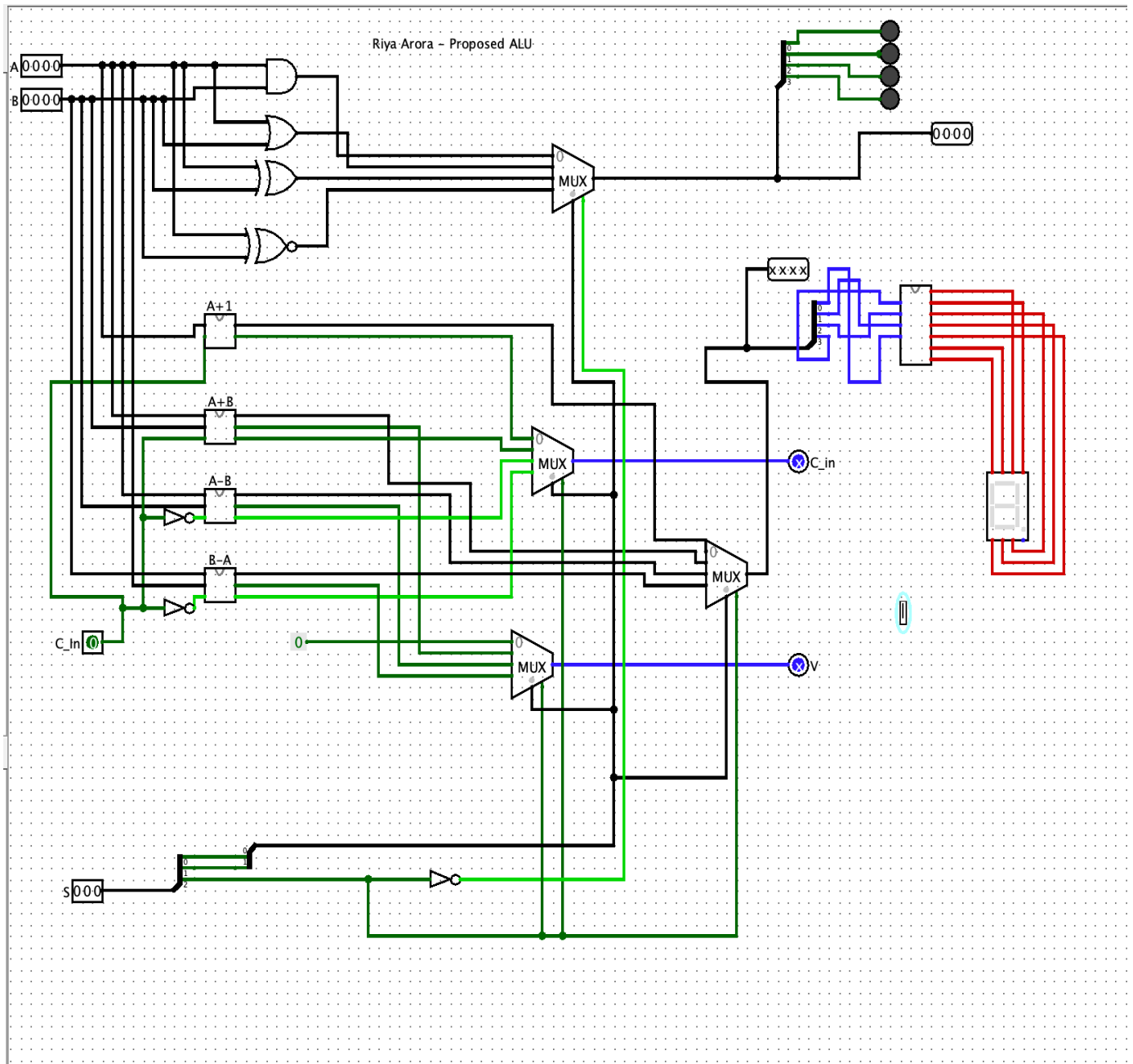
Lab Section: L2E

Lab Date: November 22nd, 2021

Date Completed: November 29th, 2021

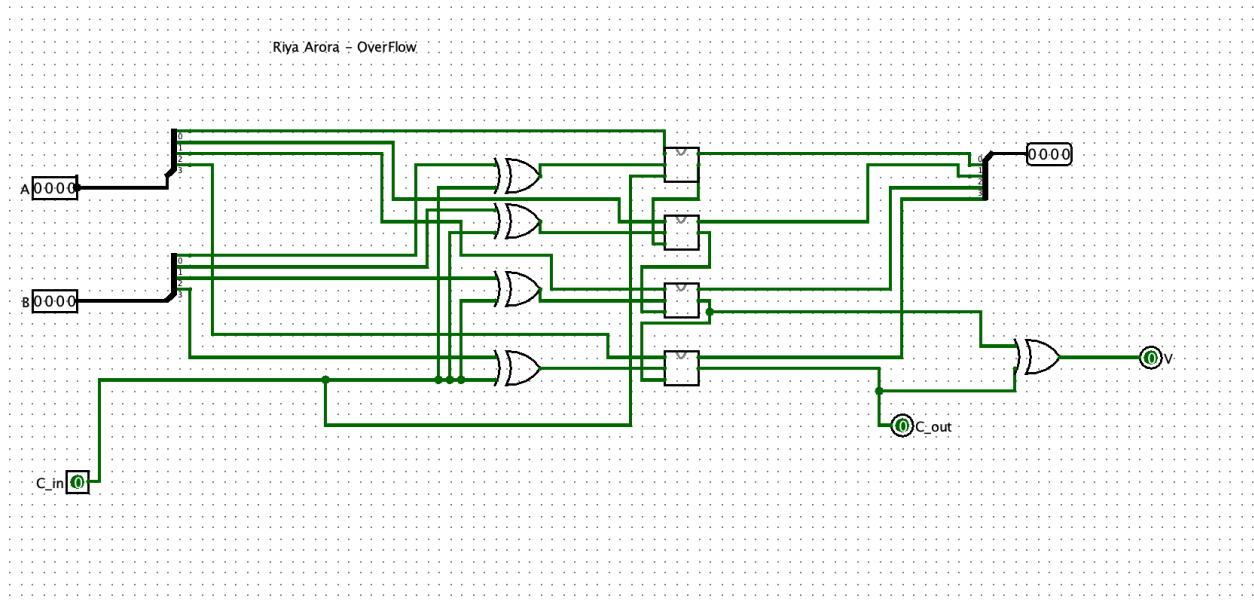
Exercise 1.A: (PRE-LAB)

1. Draw a Complete Block Diagram of proposed ALU

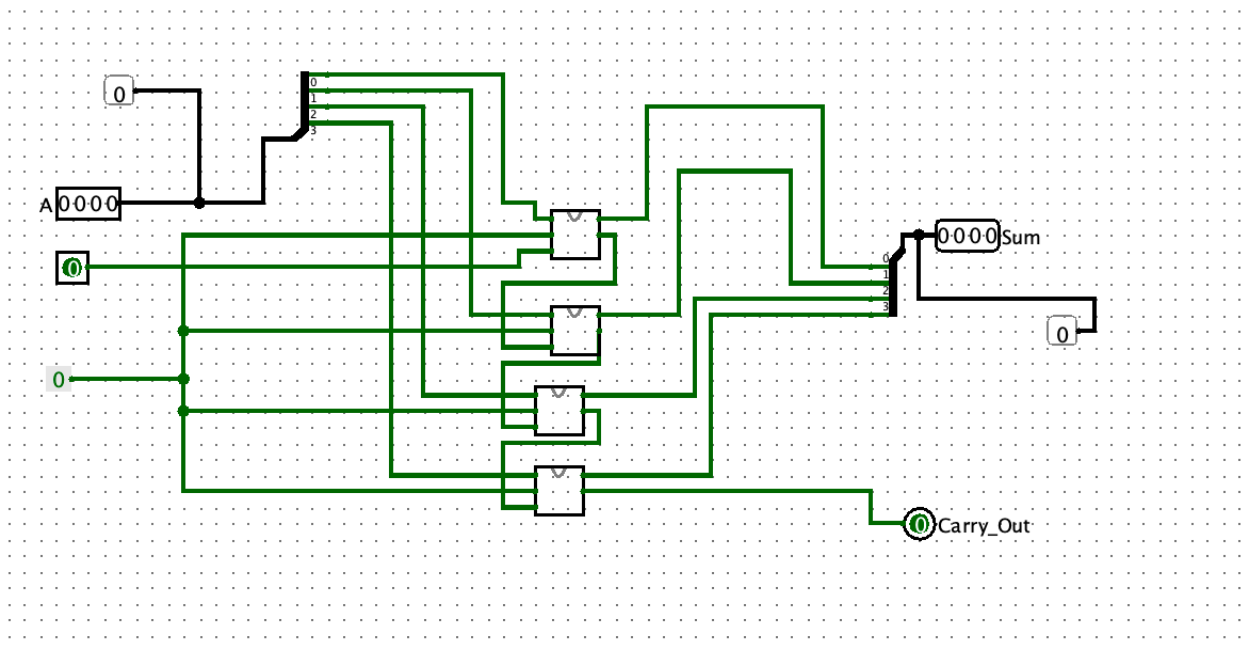


2. Any Block that has not been designed previously

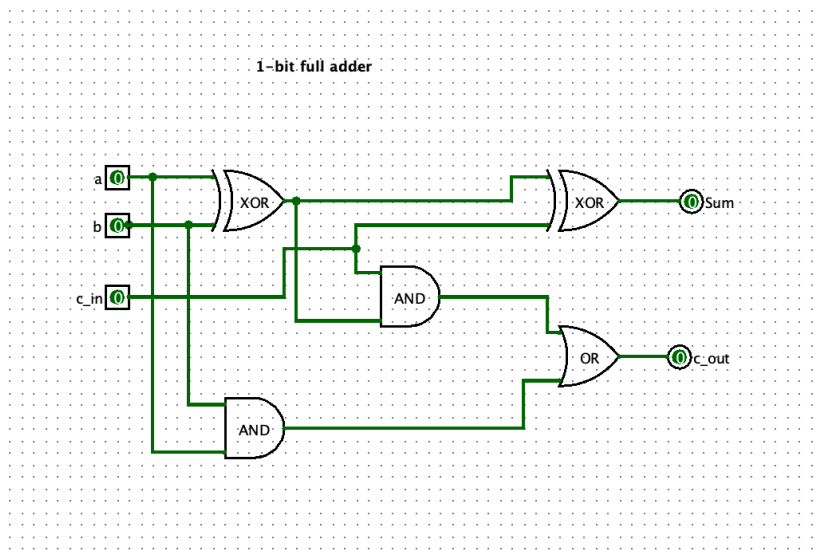
a) 4-bit adder-subtractor with overflow detection



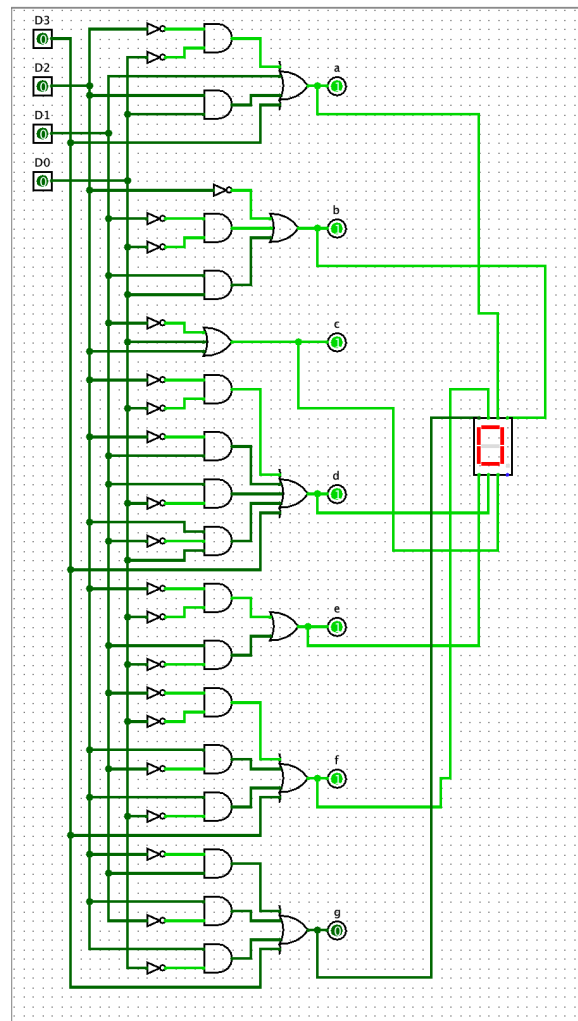
b) 4-bit $A+1$ adder



c) 1-bit full adder



d) 7 Segment Decoder



3. Computer the total number of gates

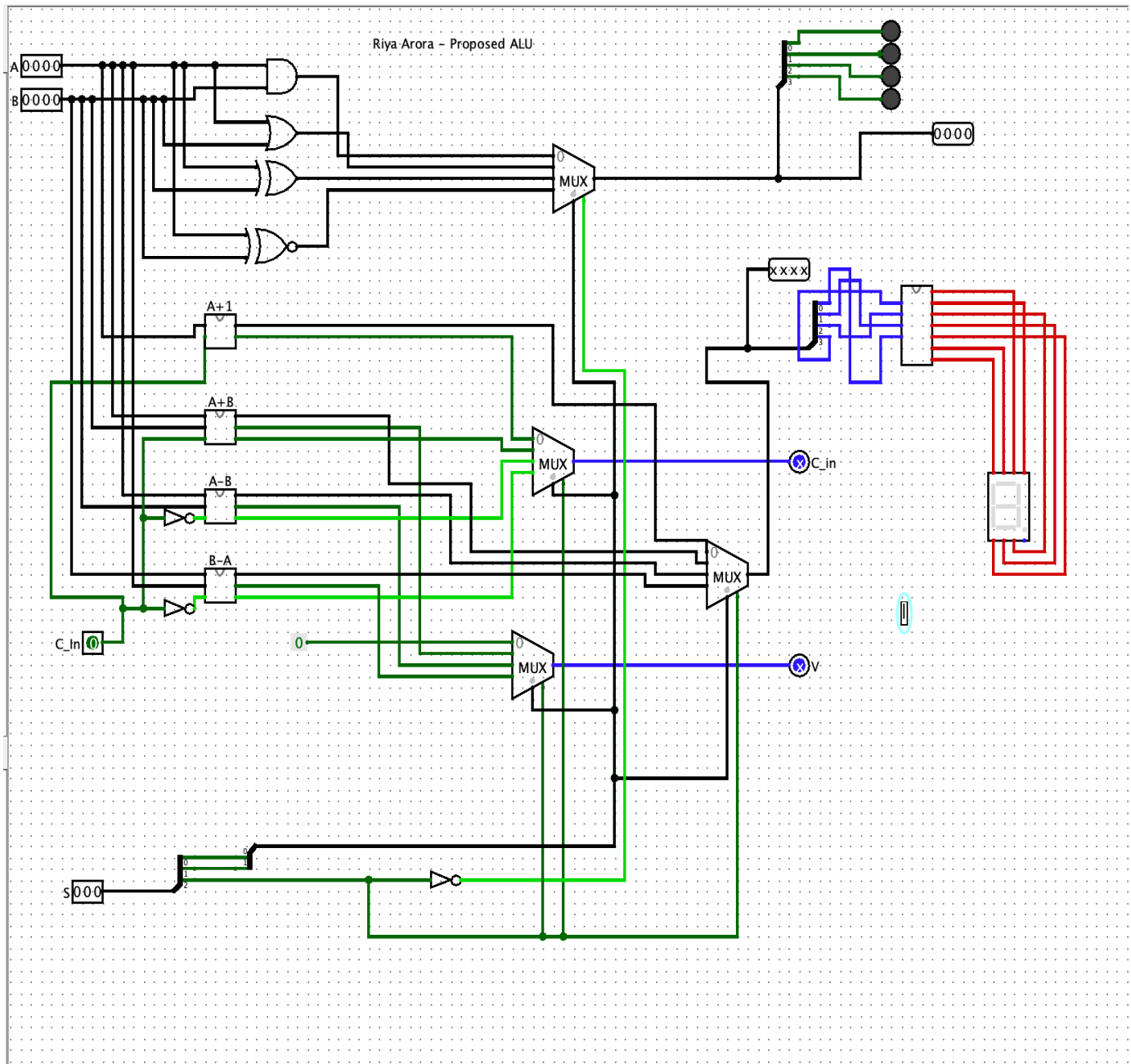
Assuming the gates have the same implementation area, the total number of gates in the proposed ALU design is 150 gates.

4. Compute the Critical Path Delay (CPD)

Assuming all of the gates have the same delay, the CPD of the proposed ALU design is 9 gates.

Exercise 1.B

1. Implement Circuit in Logisim



2. Logging File for ALU

Lab5_Ex1_log.txt

A	B	C_In	S	Final	C_out	V	LED(850_20)	LED(850_40)	LED(850_60)	LED(850_80)	7 segment(900_250).a	7 segment(900_250).b	7 segment(900_250).c	7 segment(900_250).d	7 segment(900_250).e	7 segment(900_250).f	7 segment(900_250).g
0010	0000	0	000	xxxx	x	x	0	0	0	0	E	E	E	E	E	E	E
0010	0000	0	000	xxxx	x	x	0	0	0	0	E	E	E	E	E	E	E
1110	0000	0	000	xxxx	x	x	0	0	0	0	E	E	E	E	E	E	E
1111	0000	0	000	xxxx	x	x	0	0	0	0	E	E	E	E	E	E	E
1111	0000	1	000	xxxx	x	x	0	0	0	0	E	E	E	E	E	E	E
1111	0000	1	001	xxxx	x	x	0	0	0	0	E	E	E	E	E	E	E
1111	0010	1	001	xxxx	x	x	0	0	0	0	E	E	E	E	E	E	E
1111	1010	1	001	xxxx	x	x	0	1	0	1	E	E	E	E	E	E	E
1111	0000	1	001	xxxx	x	x	0	0	0	0	E	E	E	E	E	E	E
1111	1001	1	001	xxxx	x	x	1	0	0	1	E	E	E	E	E	E	E
0101	1001	1	001	xxxx	x	x	1	1	0	0	E	E	E	E	E	E	E
0101	0001	1	001	xxxx	x	x	0	1	0	0	E	E	E	E	E	E	E
0101	1001	1	001	xxxx	x	x	1	1	0	0	E	E	E	E	E	E	E
0101	0001	1	001	xxxx	x	x	0	1	0	0	E	E	E	E	E	E	E
0101	1101	1	001	xxxx	x	x	1	1	1	0	E	E	E	E	E	E	E
0111	1011	0	001	xxxx	x	x	0	0	0	0	E	E	E	E	E	E	E
0110	1101	0	001	xxxx	x	x	0	0	1	0	E	E	E	E	E	E	E
1110	1001	0	001	xxxx	x	x	0	0	0	0	E	E	E	E	E	E	E
1010	1001	0	001	xxxx	x	x	0	0	0	1	E	E	E	E	E	E	E
1010	1000	0	001	xxxx	x	x	1	0	1	1	E	E	E	E	E	E	E
1010	1000	0	001	xxxx	x	x	0	0	1	0	E	E	E	E	E	E	E
1010	1000	0	101	0010	1	1	0	0	0	0	1	1	0	1	1	0	1
1010	1000	0	101	0110	1	1	0	0	0	0	1	1	0	1	1	0	1
1010	1110	0	101	1000	1	0	0	0	0	0	1	1	1	1	1	1	1
1000	1110	0	101	0110	1	1	0	0	0	0	1	1	0	1	1	1	1
1001	1110	0	101	0111	1	1	0	0	0	0	1	1	1	0	0	0	0
1011	1100	0	101	0001	1	0	0	0	0	0	1	1	0	0	0	0	0
0001	1110	0	101	0001	1	0	0	0	0	0	1	1	0	0	0	0	0
0001	1110	0	101	0011	1	0	0	0	0	0	1	1	1	0	0	0	0
0111	1110	0	101	0011	1	0	0	0	0	0	1	1	1	1	0	0	0
0111	1010	0	101	0001	1	0	0	0	0	0	1	1	0	0	0	0	0
0111	1010	0	101	0001	1	0	0	0	0	0	1	1	0	0	0	0	0
0111	0000	0	101	0111	0	0	0	0	0	0	1	1	1	0	0	0	0
0111	0010	0	101	0001	0	1	0	0	0	0	1	1	0	0	0	0	0
0111	0000	0	101	0111	0	0	0	0	0	0	1	1	1	0	0	0	0
0111	0000	0	101	0111	0	0	0	0	0	0	1	1	1	0	0	0	0
0111	0100	0	101	0011	0	1	0	0	0	0	1	1	1	0	0	0	0
0101	0100	0	101	1001	0	1	0	0	0	0	1	1	1	0	0	0	0
0111	0100	0	101	0011	0	0	0	0	0	0	1	1	1	0	0	0	0
1111	0100	0	101	0011	1	0	0	0	0	0	1	1	1	0	0	0	0
1011	0100	0	101	1111	0	0	0	0	0	0	1	1	1	0	0	0	0
1001	0100	0	101	1101	0	0	0	0	0	0	1	0	1	1	0	0	0
1000	0100	0	101	1100	0	0	0	0	0	0	1	0	1	0	0	0	0
0000	0100	0	101	0100	0	0	0	0	0	0	1	1	0	0	0	0	0
0000	0110	0	101	0110	0	0	0	0	0	0	1	1	0	0	0	0	0
0000	0010	0	101	0010	0	0	0	0	0	0	1	1	0	0	0	0	0
0000	0010	0	101	0010	0	0	0	0	0	0	1	1	0	0	0	0	0
0010	0011	0	101	0011	0	0	0	0	0	0	1	1	0	0	0	0	0
0110	0011	0	101	0011	0	0	0	0	0	0	1	1	0	0	0	0	0
0110	0011	1	101	0011	0	0	0	0	0	0	1	1	1	0	0	0	0
0110	0011	1	101	0011	0	0	0	0	0	0	1	1	1	0	0	0	0
0010	0011	1	101	1111	0	0	0	0	0	0	1	1	1	0	0	0	0
0011	0011	1	101	0011	0	0	0	0	0	0	1	1	1	0	0	0	0
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1111	0011	1	101	1100	1	0	0	0	0	0	0	1	1	0	0	0	0
1111	0011	1	001	xxxx	x	x	1	1	1	1	E	E	E	E	E	E	E
1111	0011	1	001	xxxx	x	x	1	1	1	1	E	E	E	E	E	E	E
1111	0110	1	001	xxxx	x	x	1	1	1	1	E	E	E	E	E	E	E
1001	0110	1	001	xxxx	x	x	1	1	1	1	E	E	E	E	E	E	E
1011	0110	1	001	xxxx	x	x	1	1	1	1	E	E	E	E	E	E	E
0111	0110	1	001	xxxx	x	x	1	1	1	1	E	E	E	E	E	E	E
0111	0000	0	001	xxxx	x	x	1	1	0	0	E	E	E	E	E	E	E
1011	0000	0	111	0101	0	0	0	0	0	0	1	0	1	0	0	0	0
1011	0000	0	111	0111	0	0	0	0	0	0	1	0	1	0	0	0	0
1011	0110	0	111	0011	0	1	0	0	0	0	1	1	1	0	0	0	0
1011	0110	0	111	0011	0	1	0	0	0	0	1	1	1	0	0	0	0
1001	0100	0	111	0011	0	0	0	0	0	0	1	1	1	0	0	0	0
1011	0100	0	111	0011	0	0	0	0	0	0	1	1	1	0	0	0	0
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1011	0100	0	111	0011	0	0	0	0	0	0	1	1	1	0	0	0	0
1011	0100	0	111	0011	0	0	0	0	0	0	1	1	1	0	0	0	0
1011	0100	0	111	0011	0	0	0	0									

Exercise 2: Study an Industrial ALU

1. $A = [1001]$

$F = A + 1$

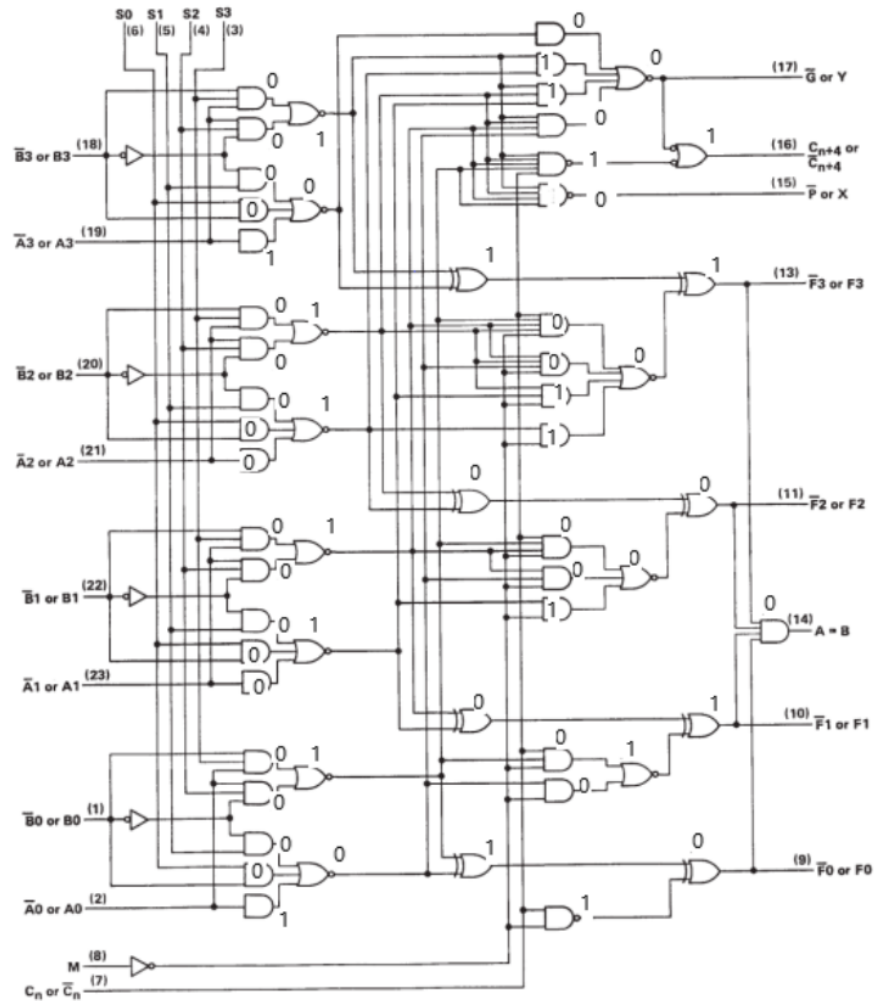
$F = [1010]$

$A = [1100]$

$F = A + 1$

$F = [1101]$

Solution of 2.1 $A = [1001]$



2. $A = [1001]$

$F = A + B$

$B = [1100]$

$F = [10101]$

3. $A = [1001]$

$F = A' + B$

$B = [1100]$

$F = [10010]$

Part 2

① $A = [1001]$

$$F = 1001$$

$$+ 0001$$

$$\hline 1010$$

$A = [1100]$

$$F = 1100$$

$$+ 0001$$

$$\hline 1101$$

② $A = [1001]$

$B = [1100]$

$$\bar{A} = [0110]$$

$$F = A + B$$

$$\begin{array}{r} 1001 \\ + 1100 \\ \hline 10101 \end{array}$$

③ $F = 0110$

$$+ 1100$$

$$\hline 10010$$

④ total number is 63 gates

⑤ max delay is 7 gates

Exercise 3: Describe the Circuit (BONUS)

Circuit Name: 4-bit ALU

8 Different Functions

1. Logic Functions (Only occur when S2 is equal to zero)

Output: LED's

Input: 4 bits

Uses a MUX

a) A AND B

Occurs when S1 = 0

Occurs when S0 = 0

b) A OR B

Occurs when S1 = 0

Occurs when S0 = 1

c) A XOR B

Occurs when S1 = 1

Occurs when S0 = 0

d) A XNOR B

Occurs when S1 = 1

Occurs when S0 = 1

2. Arithmetic Functions (Only occur when S2 is equal to one)

Output: 7 Segment Decoder

Input: 4 bits

Uses a MUX, C-Out and Overflow Indicator Included

a) A+1

Occurs when S1 = 0

Occurs when S0 = 0

Occurs when C_{in} = 0

b) A+B

Occurs when S1 = 0

Occurs when S0 = 1

Occurs when C_{in} = 0

c) A-B

Occurs when S1 = 1

Occurs when S0 = 0

Occurs when C_{in} = 1

d) B-A

Occurs when S1 = 1

Occurs when S0 = 1

Occurs when C_{in} = 1