LAB #2 - SYSC 2310 L2E

Riya Arora (101190033)

September 21st, 2021

**Screenshot 1: Build a 1-bit half adder**

Diagram

Description automatically generated

**Screenshot 2: Simulation Logging File for 1-bit half adder**

Shape, rectangle

Description automatically generated

**Screenshot 3: Build a 1-bit full adder**

Diagram

Description automatically generated

**Screenshot 4: Simulation Logging File for 1-bit full adder**

Table

Description automatically generated with medium confidence

**Screenshot 5: Build a 8-bit full adder**

Diagram, schematic

Description automatically generated

**Screenshot 6: Simulation Logging File for 1-bit full adder**

Table

Description automatically generated

**Screenshot 7: Build an 8-bit Subtractor**

Diagram, schematic

Description automatically generated

**Screenshot 8: Simulation Logging File for 8-but Subtractor**

Table

Description automatically generated