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Lab 1

Getting Started with FPGA and VHDL using the Zynq-7000 SoC boards family

SYSC 3320 L1E

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**Questions**

*1- What are the advantages of an ZyBo board for digital circuit design?*

* Flexible and scalable
* Very productive
* High system level performance because of optimized architecture
* Low power and cost
* Ready to use embedded software and digital circuit board

*2- How the Zybo board is different from a regular FPGA board?*

The Zybo board is different from just a regular FPGA board because it integrates the software programmability of a ARM processor with the hardware of a FPGA board.

*3- What are the limitations of Zybo board or FPGA board in general?*

Some limitations or disadvantages of a FPGA include:

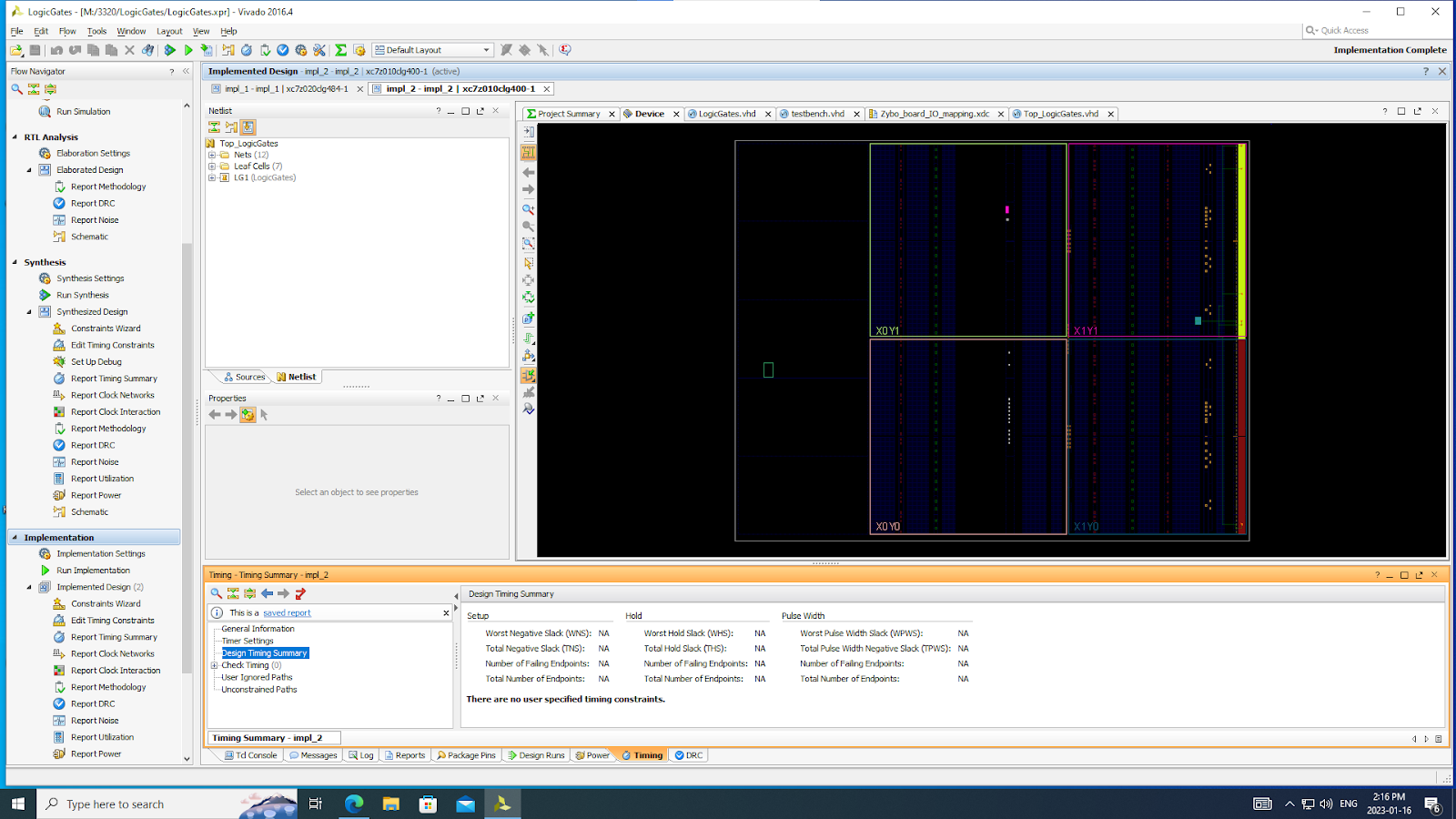
* Very slow
* Complex
* Need to know the programming language of the board such as VHDL or Verilog
* High power consumption
* Better for low quality production

**Explanation Summary of Lab**

In this lab we started off by learning how to design a FPGA using the Vivado 2016 software on the lab computers. We used VHDL language to write the software and a Zybo board to test on the hardware. We designed a digital system based on the truth table given to us in the lab, which included 4 different logic gates (AND, OR, XOR, NOR) with two inputs (A and B). Once we designed this system, we were able generate a schematic to see the logical design and run synthesis to see the FPGA design. We then created a testbench file to test our module and then viewed our results in the timing diagram. The last step was to test our software on the hardware (Zybo board) by writing a top level VHDL code and then generating a bitstream to program the FPGA board.

\*\*Screenshots on following pages

**Screenshots**



*Implemented Design Final Board*

Diagram

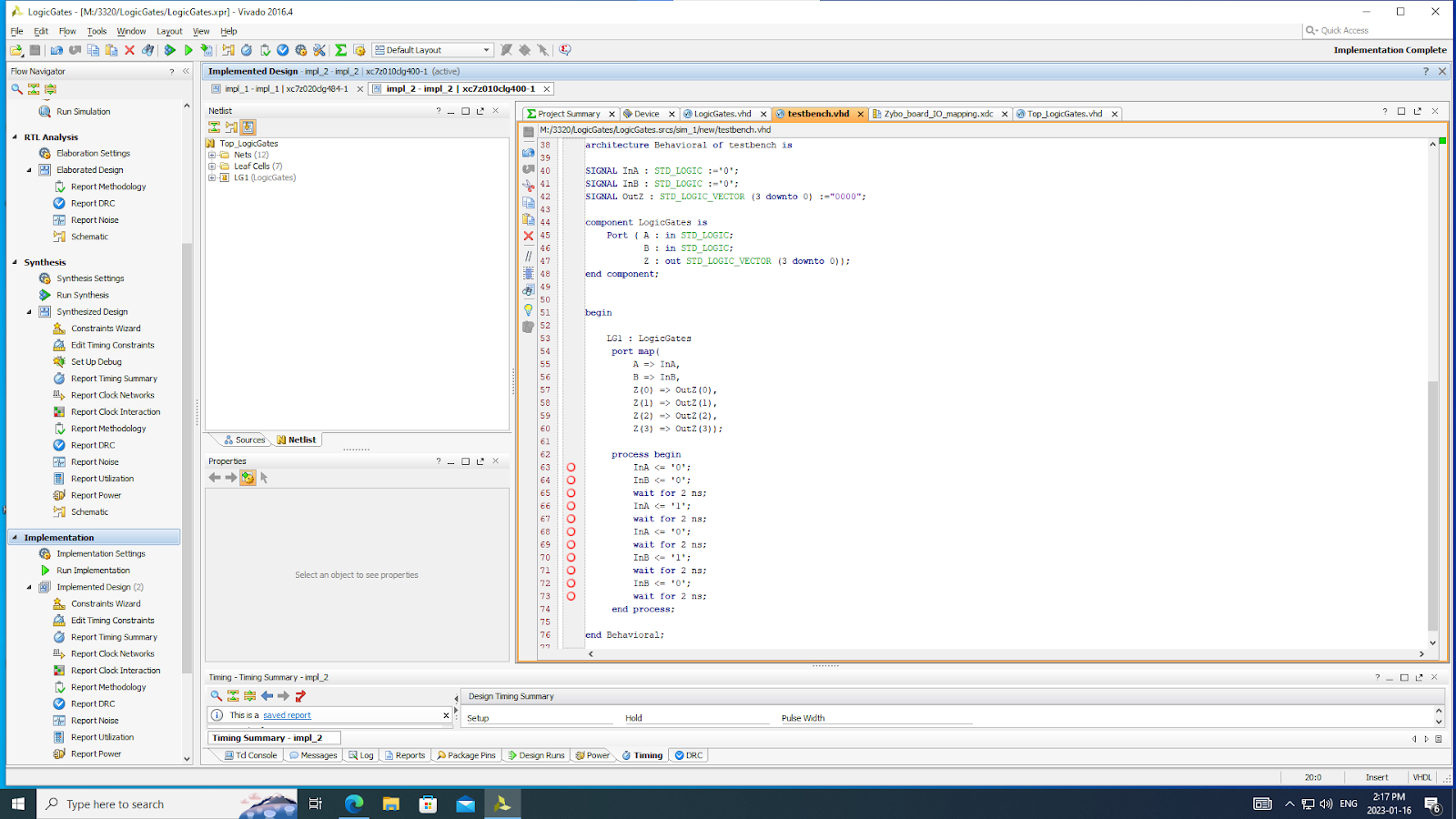
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*Schematic of Final Design*

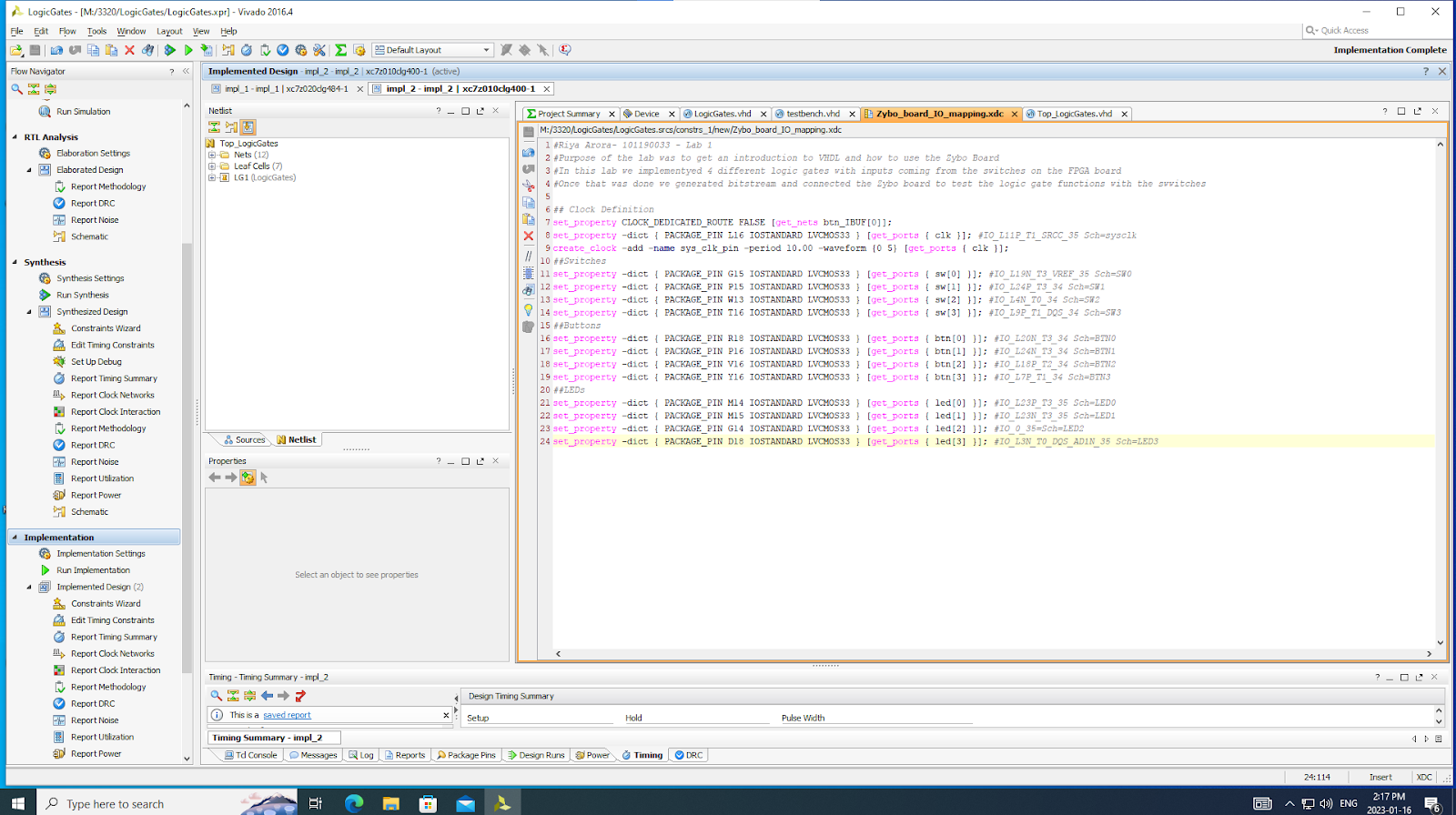
Graphical user interface, text, application

Description automatically generated

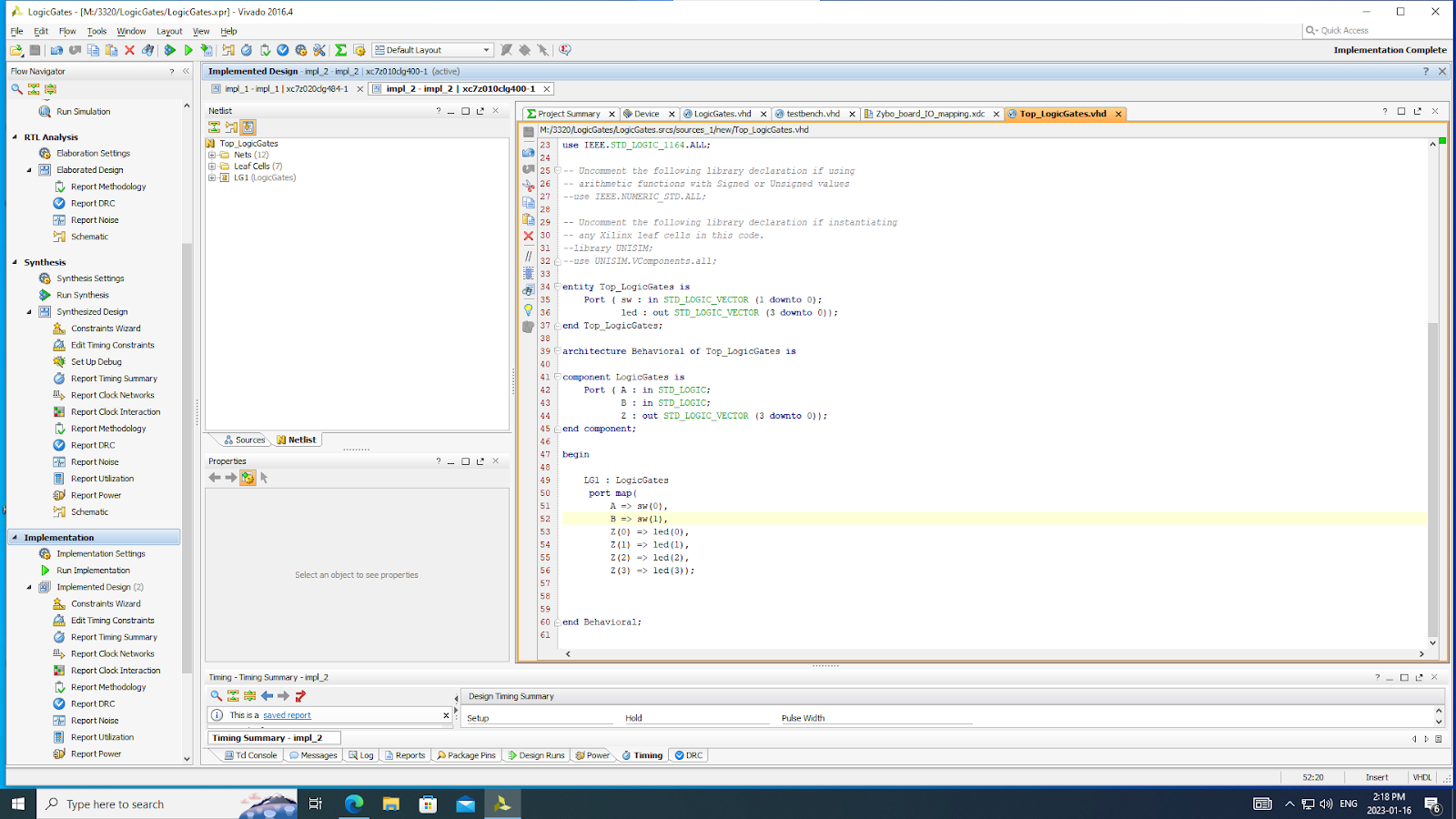
*LogicGates.vhd file*



*testbench.vhd file*



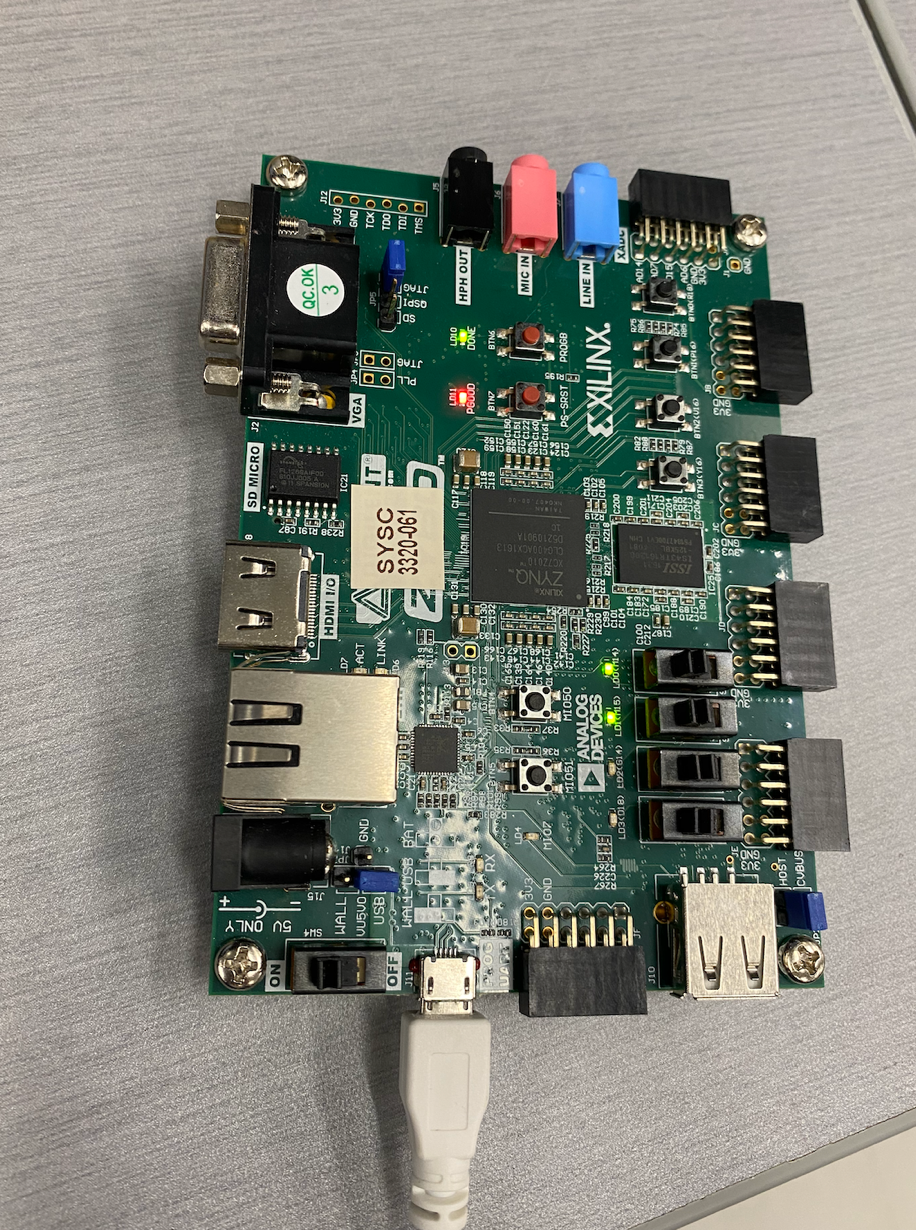
*Zybo\_board\_IO\_mapping.xdc file*



*Top\_LogicGates.vhd file*

Graphical user interface, text, application

Description automatically generated



*Simulation Result - Completed*

*Picture of board with the program loaded*