Bonus Instructions

ISA Description

Opcode	Instruction	Semantics	Syntax
10011	No Operation	Does nothing; adds delay	nop
10100	Increment	Performs reg1 += 1 If the computation overflows, then the overflow flag is set and 0 is written in reg1	incf reg1
10101	Decrement	Performs reg1 -= 1 In case reg1 = 0, 0 is written in reg1 and overflow flag is set	decf reg1
10110	Bit Set	Sets the (Imm)th bit in reg1 to 1. Bits are numbered from 0 to 15 starting from the leftmost bit.	bsf reg1 $Imm
10111	Bit Clear	Sets the (Imm)th bit in reg1 to 0. Bits are numbered from 0 to 15 starting from the leftmost bit.	bcf reg1 $Imm

Binary Encoding

- nop

opcode (5 bits)					unused bits (11 bits)										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

- incf and decf

opcode (5 bits)					unused bits (8 bits)								reg1 (3 bits)		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

- bcf and bsf

opcode (5 bits)					unused bits (4 bits)				reg1 (3 bits)			immediate value (4 bits)			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0