11 Tap FIR Filter - HLS

No Optimization

```
#include <stdio.h>
#include "ap_int.h"

#define N 11

typedef int coef_t;
typedef int data_t;
typedef int acc_t;

void fir(data_t *output, data_t input);
void fir_sw(data_t *output, data_t input);

int main()
{
    //Input initialization
    data_t input = 5;
    data_t output_sw, output_hw;

    //Call to hardware function
    fir(&output_hw, input);

    //Call to software function
    fir_sw(&output_sw, input);

    if (output_hw == output_sw)
    {
        printf("Result: %d\n", output_hw);
    }

    //Result: 265
```

```
    else
    {
        printf("Data mismatch!");
        printf("HW: %d", output_hw);
        printf("SW: %d", output_sw);
        return 1;
    }

    return 0;
}

void fir_sw(data_t *output, data_t input)
{
    coef_t c[N] = {53, 0, -91, 0, 313, 500, 313, 0, -91, 0, 53};
    static data_t shift_reg[N];
    acc_t acc = 0;

    Shift_Accum_Loop:
    for (int i = N - 1; i >= 0; i--)
    {
        if (i == 0)
        {
            acc += input * c[0];
            shift_reg[0] = input;
        }

        else
        {
            shift_reg[i] = shift_reg[i - 1];
            acc += shift_reg[i] * c[i];
        }
    }

    *output = acc;
```

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.510	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
23	45	23	45	none

Detail

Instance

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Shift_Accum_Loop	22	44	2 ~ 4	-	-	11	no

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	4	0	105	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	0	-	74	8	0
Multiplexer	-	-	-	120	-
Register	-	-	213	-	-
Total	0	4	287	233	0
Available	280	220	106400	53200	0
Utilization (%)	0	1	~0	~0	0

Cosimulation Report for 'fir'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	43	43	43	NA	NA	NA

Export the report(.html) using the Export Wizard

Optimization 1 - Symmetric Coefficients

```
void fir(data_t *output, data_t input)
{
    coef_t c[N/2 + 1] = {53, 0, -91, 0, 313, 500}; // Symmetric coefficients

    static data_t shift_reg[N/2 + 1];
    acc_t acc = 0;

    Shift_Accum_Loop:
    for (int i = N/2; i >= 0; i--)
    {
        if (i == 0)
        {
            acc += input * c[0];
            shift_reg[0] = input;
        }

        else
        {
            shift_reg[i] = shift_reg[i - 1];
            acc += shift_reg[i] * c[i];
        }
    }

    *output = acc;
}
```

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.510	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
13	25	13	25	none

Detail

Instance

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Shift_Accum_Loop	12	24	2 ~ 4	-	-	6	no

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	4	0	101	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	0	-	74	4	0
Multiplexer	-	-	-	120	-
Register	-	-	212	-	-
Total	0	4	286	225	0
Available	280	220	106400	53200	0
Utilization (%)	0	1	~0	~0	0

Cosimulation Report for 'fir'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	23	23	23	NA	NA	NA

Varying the Clock Period
1 ns

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	1.00	2.792	0.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
43	169	43	169	none

Detail

Instance

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Shift_Accum_Loop	24	150	4 ~ 25	-	-	6	no

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	22	-
FIFO	-	-	-	-	-
Instance	-	4	953	173	-
Memory	0	-	74	4	0
Multiplexer	-	-	-	275	-
Register	-	-	287	-	-
Total	0	4	1314	474	0
Available	280	220	106400	53200	0
Utilization (%)	0	1	1	~0	0

Cosimulation Report for 'fir'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	148	148	148	NA	NA	NA

5 ns

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	5.00	4.644	0.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
17	53	17	53	none

Detail

Instance

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Shift_Accum_Loop	12	48	2 ~ 8	-	-	6	no

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	61	-
FIFO	-	-	-	-	-
Instance	-	4	430	2	-
Memory	0	-	74	4	0
Multiplexer	-	-	-	146	-
Register	-	-	220	-	-
Total	0	4	724	213	0
Available	280	220	106400	53200	0
Utilization (%)	0	1	~0	~0	0

Cosimulation Report for 'fir'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	47	47	47	NA	NA	NA

10 ns

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.510	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
13	25	13	25	none

Detail

Instance

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Shift_Accum_Loop	12	24	2 ~ 4	-	-	6	no

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	4	0	101	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	0	-	74	4	0
Multiplexer	-	-	-	120	-
Register	-	-	212	-	-
Total	0	4	286	225	0
Available	280	220	106400	53200	0
Utilization (%)	0	1	~0	~0	0

Cosimulation Report for 'fir'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	23	23	23	NA	NA	NA

Best Performance: 10 ns
Best Area: 10 ns

Optimization 2 - Code Hoisting

```
void fir(data_t *output, data_t input)
{
    coef_t c[N/2 + 1] = {53, 0, -91, 0, 313, 500};

    static data_t shift_reg[N/2 + 1];
    acc_t acc = 0;

    for (int i = N/2; i > 0; i--)
    {
        shift_reg[i] = shift_reg[i - 1];
        acc += shift_reg[i] * c[i];
    }

    acc += input * c[0];
    shift_reg[0] = input;

    *output = acc;
}
```

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.510	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
22	22	22	22	none

Detail

Instance

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Loop 1	20	20	4	-	-	5	no

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	4	0	139	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	0	-	74	4	0
Multiplexer	-	-	-	92	-
Register	-	-	153	-	-
Total	0	4	227	235	0
Available	280	220	106400	53200	0
Utilization (%)	0	1	~0	~0	0

Cosimulation Report for 'fir'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	22	22	22	NA	NA	NA

Optimization 3 - Loop Fission

```
void fir(data_t *output, data_t input)
{
    coef_t c[N/2 + 1] = {53, 0, -91, 0, 313, 500};

    static data_t shift_reg[N/2 + 1];
    acc_t acc = 0;

    //TDL - Tapped Delay Line
    for (int i = N/2; i > 0; i--)
    {
        shift_reg[i] = shift_reg[i - 1];
    }

    shift_reg[0] = input;
    acc = 0;

    //MAC
    for (int i = N/2; i > 0; i--)
    {
        acc += shift_reg[i] * c[i];
    }

    acc += input * c[0];
    shift_reg[0] = input;

    *output = acc;
}
```

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.510	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
33	33	33	33	none

Detail

Instance

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Loop 1	10	10	2	-	-	5	no
- Loop 2	20	20	4	-	-	5	no

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	4	0	160	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	0	-	74	4	0
Multiplexer	-	-	-	113	-
Register	-	-	158	-	-
Total	0	4	232	277	0
Available	280	220	106400	53200	0
Utilization (%)	0	1	~0	~0	0

Cosimulation Report for 'fir'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	33	33	33	NA	NA	NA

Optimization 4 - Loop Unrolling
Unrolling the TDL Loop
Factor 4

```
void fir(data_t *output, data_t input)
{
    coef_t c[N/2 + 1] = {53, 0, -91, 0, 313, 500};

    static data_t shift_reg[N/2 + 1];
    acc_t acc = 0;

    //TDL - Tapped Delay Line
    for (int i = N/2; i > 0; i--)
    #pragma HLS unroll factor = 4
    {
        shift_reg[i] = shift_reg[i - 1];
    }

    shift_reg[0] = input;
    acc = 0;

    //MAC
    for (int i = N/2; i > 0; i--)
    {
        acc += shift_reg[i] * c[i];
    }

    acc += input * c[0];
    shift_reg[0] = input;

    *output = acc;
}
```

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.510	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
22	22	22	22	none

Detail

Instance

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Loop 1	20	20	4	-	-	5	no

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	4	0	139	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	0	-	74	4	0
Multiplexer	-	-	-	71	-
Register	-	-	150	-	-
Total	0	4	224	214	0
Available	280	220	106400	53200	0
Utilization (%)	0	1	~0	~0	0

Cosimulation Report for 'fir'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	22	22	22	NA	NA	NA

Complete Unrolling

```
void fir(data_t *output, data_t input)
{
    coef_t c[N/2 + 1] = {53, 0, -91, 0, 313, 500};

    static data_t shift_reg[N/2 + 1];
    acc_t acc = 0;

    //TDL - Tapped Delay Line
    for (int i = N/2; i > 0; i--)
    #pragma HLS unroll
    {
        shift_reg[i] = shift_reg[i - 1];
    }

    shift_reg[0] = input;
    acc = 0;

    //MAC
    for (int i = N/2; i > 0; i--)
    {
        acc += shift_reg[i] * c[i];
    }

    acc += input * c[0];
    shift_reg[0] = input;

    *output = acc;
}
```

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.510	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
22	22	22	22	none

Detail

Instance

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Loop 1	20	20	4	-	-	5	no

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	4	0	139	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	0	-	74	4	0
Multiplexer	-	-	-	71	-
Register	-	-	150	-	-
Total	0	4	224	214	0
Available	280	220	106400	53200	0
Utilization (%)	0	1	~0	~0	0

Cosimulation Report for 'fir'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	22	22	22	NA	NA	NA

Unrolling the MAC Loop
Factor 4

```
void fir(data_t *output, data_t input)
{
    coef_t c[N/2 + 1] = {53, 0, -91, 0, 313, 500};

    static data_t shift_reg[N/2 + 1];
    acc_t acc = 0;

    //TDL - Tapped Delay Line
    for (int i = N/2; i > 0; i--)
    {
        shift_reg[i] = shift_reg[i - 1];
    }

    shift_reg[0] = input;
    acc = 0;

    //MAC
    for (int i = N/2; i > 0; i--)
    #pragma HLS unroll factor = 4
    {
        acc += shift_reg[i] * c[i];
    }

    acc += input * c[0];
    shift_reg[0] = input;

    *output = acc;
}
```

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.510	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
11	11	11	11	none

Detail

Instance

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Loop 1	10	10	2	-	-	5	no

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	2	0	41	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	0	-	64	3	0
Multiplexer	-	-	-	66	-
Register	-	-	9	-	-
Total	0	2	73	110	0
Available	280	220	106400	53200	0
Utilization (%)	0	~0	~0	~0	0

Cosimulation Report for 'fir'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	11	11	11	NA	NA	NA

Complete Unrolling

```
void fir(data_t *output, data_t input)
{
    coef_t c[N/2 + 1] = {53, 0, -91, 0, 313, 500};

    static data_t shift_reg[N/2 + 1];
    acc_t acc = 0;

    //TDL - Tapped Delay Line
    for (int i = N/2; i > 0; i--)
    {
        shift_reg[i] = shift_reg[i - 1];
    }

    shift_reg[0] = input;
    acc = 0;

    //MAC
    for (int i = N/2; i > 0; i--)
    #pragma HLS unroll
    {
        acc += shift_reg[i] * c[i];
    }

    acc += input * c[0];
    shift_reg[0] = input;

    *output = acc;
}
```

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.510	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
11	11	11	11	none

Detail

Instance

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Loop 1	10	10	2	-	-	5	no

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	2	0	41	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	0	-	64	3	0
Multiplexer	-	-	-	66	-
Register	-	-	9	-	-
Total	0	2	73	110	0
Available	280	220	106400	53200	0
Utilization (%)	0	~0	~0	~0	0

Cosimulation Report for 'fir'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	11	11	11	NA	NA	NA

Both Loops with Factor 4

```
void fir(data_t *output, data_t input)
{
    coef_t c[N/2 + 1] = {53, 0, -91, 0, 313, 500};

    static data_t shift_reg[N/2 + 1];
    acc_t acc = 0;

    //TDL - Tapped Delay Line
    for (int i = N/2; i > 0; i--)
    #pragma HLS unroll factor = 4
    {
        shift_reg[i] = shift_reg[i - 1];
    }

    shift_reg[0] = input;
    acc = 0;

    //MAC
    for (int i = N/2; i > 0; i--)
    #pragma HLS unroll factor = 4
    {
        acc += shift_reg[i] * c[i];
    }

    acc += input * c[0];
    shift_reg[0] = input;

    *output = acc;
}
```

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.510	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
0	0	0	0	none

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	2	0	20	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	-	-
Register	-	-	-	-	-
Total	0	2	0	20	0
Available	280	220	106400	53200	0
Utilization (%)	0	~0	0	~0	0

Cosimulation Report for 'fir'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	0	0	0	0	0	0

Optimization 5 - Loop Pipelining

Loop II value should not be greater than the iteration latency of the for loop.
Iteration Latency of TDL Loop - 2 cycles
Iteration Latency of MAC Loop - 4 cycles

TDL Loop

```
void fir(data_t *output, data_t input)
{
    coef_t c[N/2 + 1] = {53, 0, -91, 0, 313, 500};

    static data_t shift_reg[N/2 + 1];
    acc_t acc = 0;

    //TDL - Tapped Delay Line
    for (int i = N/2; i > 0; i--)
    #pragma HLS pipeline II=1
    {
        shift_reg[i] = shift_reg[i - 1];
    }

    shift_reg[0] = input;
    acc = 0;

    //MAC
    for (int i = N/2; i > 0; i--)
    {
        acc += shift_reg[i] * c[i];
    }

    acc += input * c[0];
    shift_reg[0] = input;

    *output = acc;
}
```

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.510	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
22	22	22	22	none

Detail

Instance

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Loop 1	20	20	4	-	-	5	no

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	4	0	139	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	0	-	74	4	0
Multiplexer	-	-	-	71	-
Register	-	-	150	-	-
Total	0	4	224	214	0
Available	280	220	106400	53200	0
Utilization (%)	0	1	~0	~0	0

Cosimulation Report for 'fir'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	22	22	22	NA	NA	NA

MAC Loop

```
void fir(data_t *output, data_t input)
{
    coef_t c[N/2 + 1] = {53, 0, -91, 0, 313, 500};

    static data_t shift_reg[N/2 + 1];
    acc_t acc = 0;

    //TDL - Tapped Delay Line
    for (int i = N/2; i > 0; i--)
    {
        shift_reg[i] = shift_reg[i - 1];
    }

    shift_reg[0] = input;
    acc = 0;

    //MAC
    for (int i = N/2; i > 0; i--)
    #pragma HLS pipeline II=1
    {
        acc += shift_reg[i] * c[i];
    }

    acc += input * c[0];
    shift_reg[0] = input;

    *output = acc;
}
```

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.510	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
11	11	11	11	none

Detail

Instance

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Loop 1	10	10	2	-	-	5	no

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	2	0	41	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	0	-	64	3	0
Multiplexer	-	-	-	66	-
Register	-	-	9	-	-
Total	0	2	73	110	0
Available	280	220	106400	53200	0
Utilization (%)	0	~0	~0	~0	0

Cosimulation Report for 'fir'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	11	11	11	NA	NA	NA