RTL to GDS : 8-Bit Counter

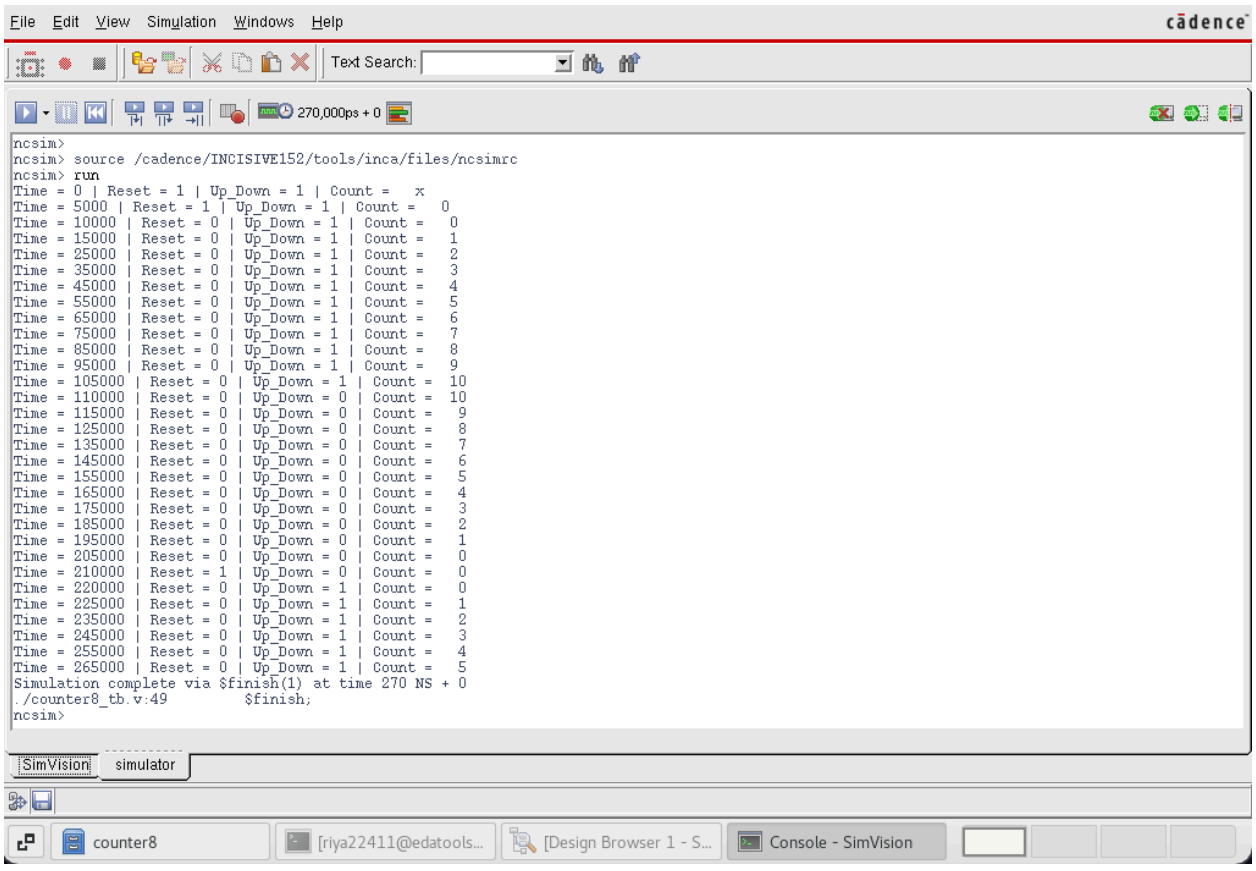
Design

The module is an 8-bit counter with a synchronous reset and an ‘up_down’ input to determine if it will be an up counter or a down counter. The technology libraries used are FreePDK45_lib_v1.0_typical_scan.lib and FreePDK45_lib_v1.0.lef.

Simulation

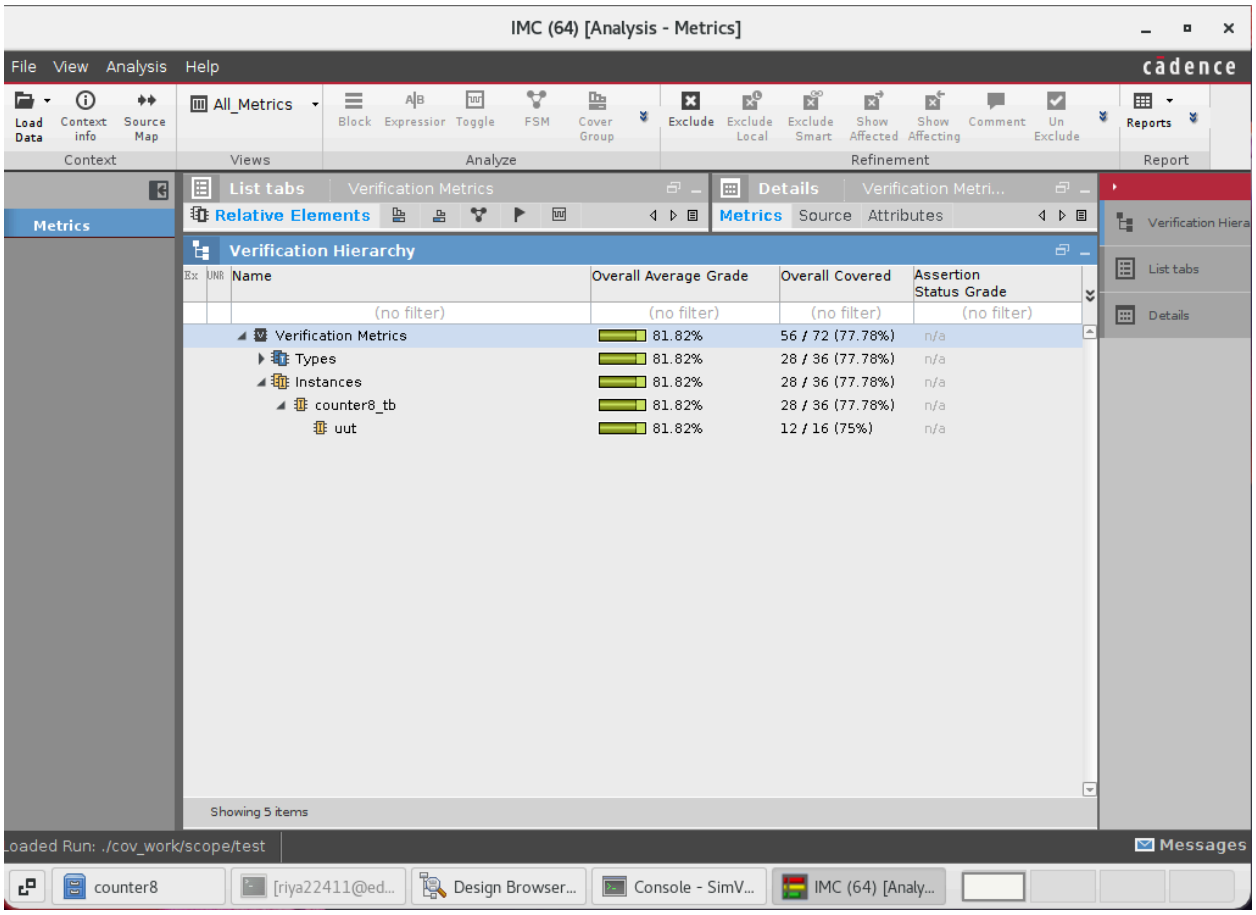
Testbench Output

The simulation of the verilog code works as expected.



Coverage Report

The coverage is not 100% because the test bench only tests counting up to 10 (4 bits), so the upper 4 bits are left untested.



Synthesis

The timing intent results are as expected.

```
Lint summary
 Unconnected/logic driven clocks                                  0
 Sequential data pins driven by a clock signal                    0
 Sequential clock pins without clock waveform                     0
 Sequential clock pins with multiple clock waveforms              0
 Generated clocks without clock waveform                          0
 Generated clocks with incompatible options                       0
 Generated clocks with multi-master clock                         0
 Paths constrained with different clocks                          0
 Loop-breaking cells for combinational feedback                   0
 Nets with multiple drivers                                       0
 Timing exceptions with no effect                                 0
 Suspicious multi_cycle exceptions                                0
 Pins/ports with conflicting case constants                       0
 Inputs without clocked external delays                           0
 Outputs without clocked external delays                          0
 Inputs without external driver/transition                        0
 Outputs without external load                                    0
 Exceptions with invalid timing start-/endpoints                  0

                                                  Total:          0
```

The post-synthesis power report is as follows:

```
Instance: /counter8
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------
       memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     register     2.45672e-08  1.61905e-06  2.11981e-07  1.85560e-06  57.56%
        latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        logic     2.55873e-08  6.29439e-07  3.86522e-07  1.04155e-06  32.31%
         bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        clock     0.00000e+00  0.00000e+00  3.26400e-07  3.26400e-07  10.13%
          pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
           pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
    Subtotal     5.01545e-08  2.24849e-06  9.24903e-07  3.22355e-06 100.00%
  Percentage           1.56%       69.75%       28.69%      100.00% 100.00%
  ------------------------------------------------------------------------
```

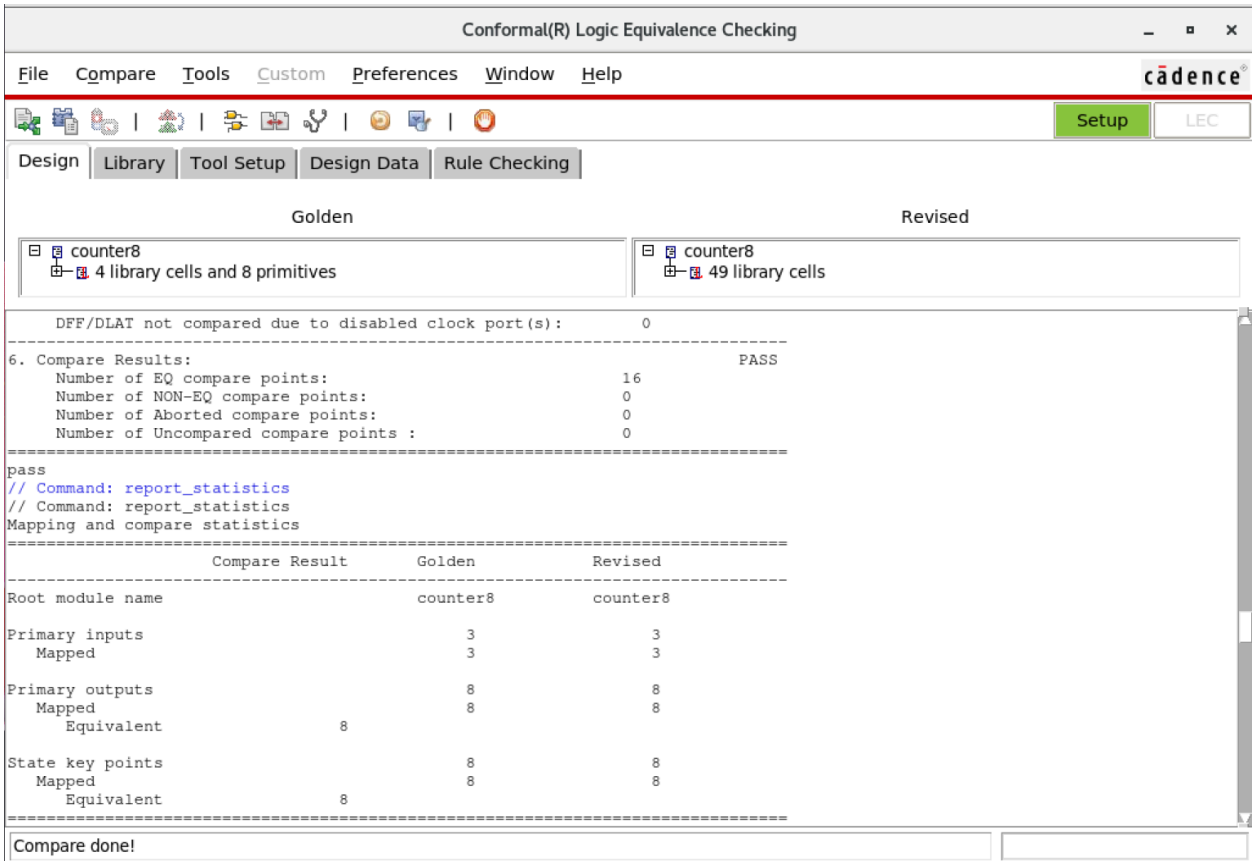
The post-synthesis area report is as follows:

Gate	Instances	Area	Library
AOI21_X1	2	2.128	FreePDK45_lib_v1.0
DFF_X1	7	35.378	FreePDK45_lib_v1.0
INV_X2	3	1.596	FreePDK45_lib_v1.0
INV_X4	4	2.128	FreePDK45_lib_v1.0
NAND2_X1	5	3.990	FreePDK45_lib_v1.0
NOR2_X1	5	3.990	FreePDK45_lib_v1.0
NOR2_X2	1	0.798	FreePDK45_lib_v1.0
OAI21_X1	3	3.192	FreePDK45_lib_v1.0
OAI22_X1	6	7.980	FreePDK45_lib_v1.0
OR2_X1	1	1.064	FreePDK45_lib_v1.0
OR2_X2	4	4.256	FreePDK45_lib_v1.0
SDFF_X2	1	6.916	FreePDK45_lib_v1.0
XOR2_X2	7	13.034	FreePDK45_lib_v1.0
total	49	86.450	

Type	Instances	Area	Area %
sequential	8	42.294	48.9
inverter	7	3.724	4.3
logic	34	40.432	46.8
physical_cells	0	0.000	0.0
total	49	86.450	100.0

Logical Equivalence Check

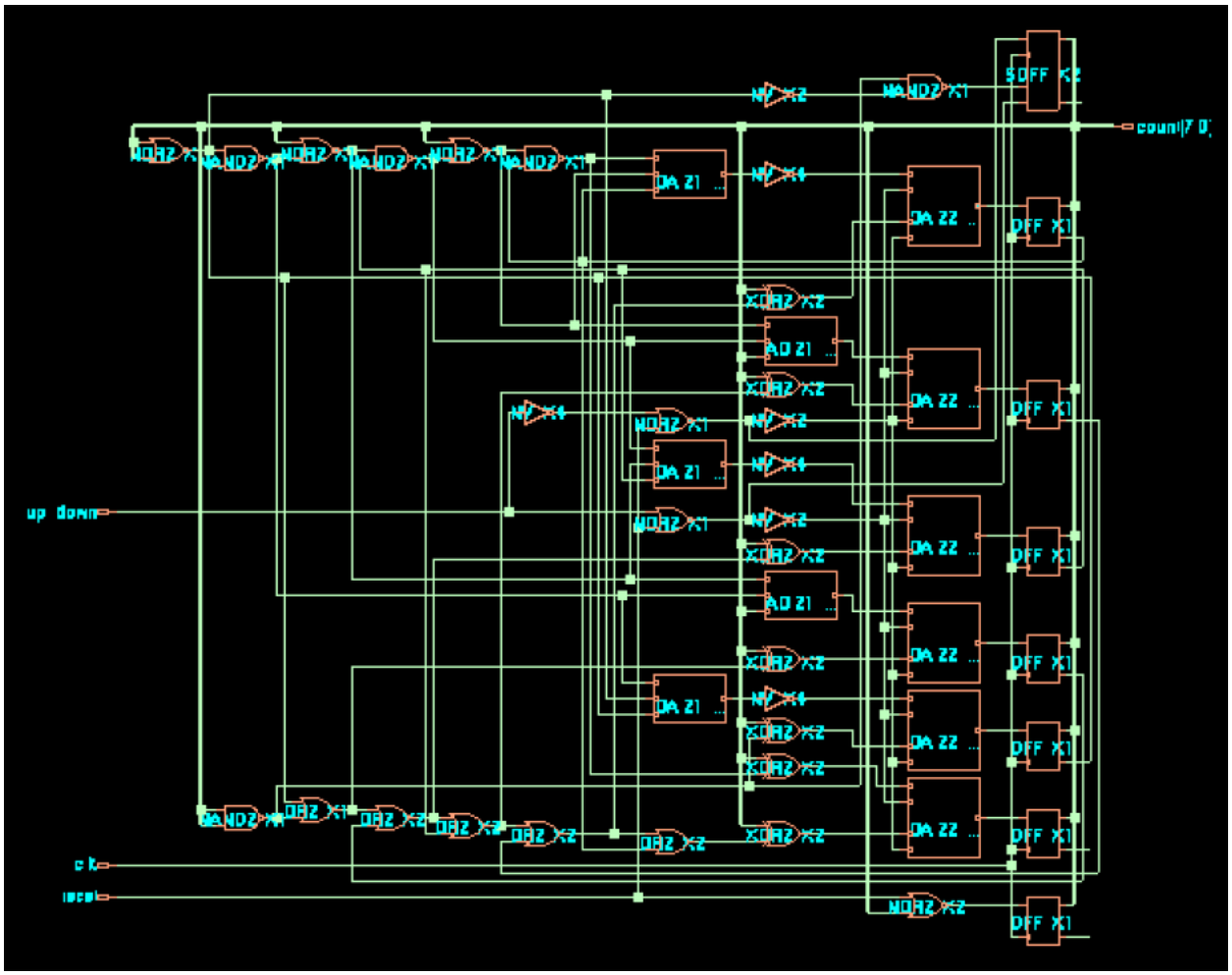
The verilog code and the netlist are equivalent.



Static Timing Analysis (before DFT)

Schematic

The pre-DFT schematic is as follows:



Graph Based Analysis

The setup and hold slacks are positive.

```
Path 1: MET Setup Check with Pin count_reg[7]/CK
Endpoint:   count_reg[7]/D (^) checked with  leading edge of 'clk'
Beginpoint: count_reg[0]/Q (^) triggered by  leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time          0.500
- Setup                         0.432
+ Phase Shift                  10.000
- Uncertainty                   0.020
= Required Time                10.048
- Arrival Time                  5.156
= Slack Time                    4.892
     Clock Rise Edge                     0.000
     + Clock Network Latency (Ideal)     0.500
     = Beginpoint Arrival Time           0.500
      ------------------------------------------------------------
      Instance      Arc           Cell      Delay  Arrival  Required
                                                   Time     Time
      ------------------------------------------------------------
      count_reg[0]  CK ^          -         -      0.500    5.392
      count_reg[0]  CK ^ -> Q ^   DFF_X1    1.614  2.114    7.006
      g811          A1 ^ -> ZN v  NAND2_X1  0.169  2.283    7.175
      g804          A2 v -> ZN v  OR2_X1    0.396  2.679    7.571
      g797          A1 v -> ZN v  OR2_X2    0.384  3.063    7.955
      g793          A1 v -> ZN v  OR2_X2    0.385  3.448    8.340
      g787          A1 v -> ZN v  OR2_X2    0.385  3.832    8.724
      g779          A1 v -> ZN v  OR2_X2    0.363  4.196    9.088
      g772          B v -> Z v    XOR2_X2   0.367  4.562    9.454
      g767          B1 v -> ZN ^  OAI22_X1  0.594  5.156    10.048
      count_reg[7]  D ^           DFF_X1    0.000  5.156    10.048
      ------------------------------------------------------------
```

```
Path 1: MET Hold Check with Pin count_reg[0]/CK
Endpoint:   count_reg[0]/D (v) checked with  leading edge of 'clk'
Beginpoint: reset          (^) triggered by  leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time          0.500
+ Hold                          0.073
+ Phase Shift                   0.000
+ Uncertainty                   0.020
= Required Time                 0.593
  Arrival Time                  0.937
  Slack Time                    0.344
     Clock Rise Edge                     0.000
     + Input Delay                       0.300
     + Drive Adjustment                  0.057
     + Source Insertion Delay            0.500
     = Beginpoint Arrival Time           0.857
      ------------------------------------------------------------
      Instance      Arc           Cell     Delay  Arrival  Required
                                                  Time     Time
      ------------------------------------------------------------
      -             reset ^       -        -      0.857    0.513
      g810          A1 ^ -> ZN v  NOR2_X2  0.080  0.937    0.593
      count_reg[0]  D v           DFF_X1   0.000  0.937    0.593
      ------------------------------------------------------------
```

There are no untested paths and no timing violations.

```
    ------------------------------------------------------------------------------------------
                                TIMING CHECK COVERAGE SUMMARY
    ------------------------------------------------------------------------------------------
     Check Type                      No. of    Met              Violated         Untested
                                     Checks
    ------------------------------------------------------------------------------------------
    ExternalDelay (Early)            8         8 (100%)         0 (0%)           0 (0%)
    ExternalDelay (Late)             8         8 (100%)         0 (0%)           0 (0%)
    Hold                             10        10 (100%)        0 (0%)           0 (0%)
    PulseWidth                       16        16 (100%)        0 (0%)           0 (0%)
    Setup                            10        10 (100%)        0 (0%)           0 (0%)
    ------------------------------------------------------------------------------------------

------------------------------------------------------------------------------------------
                                          TIMING CHECK COVERAGE
DETAILS

------------------------------------------------------------------------------------------
     Pin                         Reference Pin               Check Type                 Slack
Reason

------------------------------------------------------------------------------------------
```

Path Based Analysis

The GBA and PBA results are in agreement.

```
Path 1: MET Setup Check with Pin count_reg[7]/CK
Endpoint:   count_reg[7]/D (^) checked with  leading edge of 'clk'
Beginpoint: count_reg[0]/Q (^) triggered by  leading edge of 'clk'
Path Groups: {clk}
Retime Analysis { Data Path-Slew }
Other End Arrival Time          0.500
- Setup                         0.424
+ Phase Shift                  10.000
- Uncertainty                   0.020
= Required Time                10.056
- Arrival Time                  5.156
= Slack Time                    4.900
= Slack Time(original)          4.892
     Clock Rise Edge                 0.000
     + Clock Network Latency (Ideal) 0.500
     = Beginpoint Arrival Time       0.500
      ------------------------------------------------------------
      Instance      Arc           Cell      Retime  Arrival  Required
                                            Delay   Time     Time
      ------------------------------------------------------------
      count_reg[0]  CK ^          -         -       0.500    5.400
      count_reg[0]  CK ^ -> Q ^   DFF_X1    1.614   2.114    7.014
      g811          -             NAND2_X1  0.000   2.114    7.014
      g811          A1 ^ -> ZN v  NAND2_X1  0.169   2.283    7.184
      g804          -             OR2_X1    0.000   2.283    7.184
      g804          A2 v -> ZN v  OR2_X1    0.396   2.679    7.580
      g797          -             OR2_X2    0.000   2.679    7.580
      g797          A1 v -> ZN v  OR2_X2    0.384   3.063    7.964
      g793          -             OR2_X2    0.000   3.063    7.964
      g793          A1 v -> ZN v  OR2_X2    0.385   3.448    8.348
      g787          -             OR2_X2    0.000   3.448    8.348
      g787          A1 v -> ZN v  OR2_X2    0.385   3.832    8.733
      g779                        OR2_X2    0.000   3.832    8.733
```

```
Path 1: MET Hold Check with Pin count_reg[0]/CK
Endpoint:   count_reg[0]/D (v) checked with  leading edge of 'clk'
Beginpoint: reset          (^) triggered by  leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time          0.500
+ Hold                          0.073
+ Phase Shift                   0.000
+ Uncertainty                   0.020
= Required Time                 0.593
  Arrival Time                  0.937
  Slack Time                    0.344
     Clock Rise Edge                      0.000
     + Input Delay                        0.300
     + Drive Adjustment                   0.057
     + Source Insertion Delay             0.500
     = Beginpoint Arrival Time            0.857
      ------------------------------------------------------------
      Instance      Arc           Cell      Delay  Arrival  Required
                                                   Time     Time
      ------------------------------------------------------------
      -             reset ^       -         -      0.857    0.513
      g810          A1 ^ -> ZN v  NOR2_X2   0.080  0.937    0.593
      count_reg[0]  D v           DFF_X1    0.000  0.937    0.593
      ------------------------------------------------------------
```

TIMING CHECK COVERAGE SUMMARY

Check Type	No. of Checks	Met	Violated	Untested
ExternalDelay (Early)	8	8 (100%)	0 (0%)	0 (0%)
ExternalDelay (Late)	8	8 (100%)	0 (0%)	0 (0%)
Hold	10	10 (100%)	0 (0%)	0 (0%)
PulseWidth	16	16 (100%)	0 (0%)	0 (0%)
Setup	10	10 (100%)	0 (0%)	0 (0%)

TIMING CHECK COVERAGE DETAILS

Pin	Reference Pin	Check Type	Slack	Reason

Design For Test

All 8 flip-flops in the design pass the DFT rule check and are mapped to scan cells.

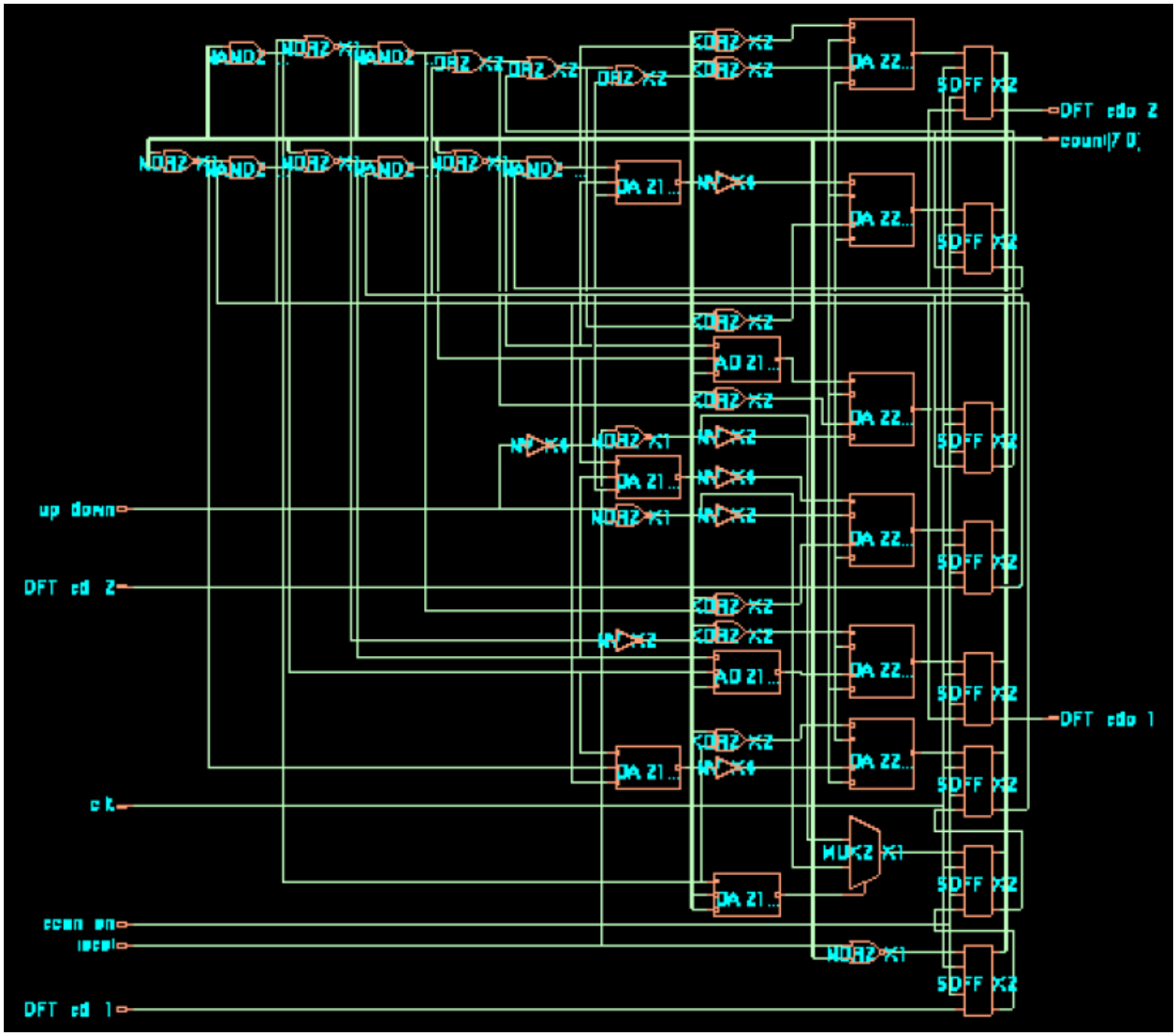
```
Detected 0 DFT rule violation(s)
        Summary of check_dft_rules
        **************************
        Number of usable scan cells: 4
Clock Rule Violations:
----------------------
          Internally driven clock net: 0
              Tied constant clock net: 0
                   Undriven clock net: 0
        Conflicting async & clock net: 0
                      Misc. clock net: 0

Async. set/reset Rule Violations:
---------------------------------
        Internally driven async net: 0
              Tied active async net: 0
                 Undriven async net: 0
                    Misc. async net: 0

   Total number of DFT violations: 0

Total number of Test Clock Domains: 1
  DFT Test Clock Domain: clk
        Test Clock 'clk' (Positive edge) has   8 registers
Number of user specified non-Scan registers:   0
    Number of registers that fail DFT rules:   0
    Number of registers that pass DFT rules:   8
Percentage of total registers that are scannable: 100%
```

```
Scan mapping status report
==========================
    Scan mapping: converting flip-flops that pass TDRC.
    Scan mapping done: 8 flip-flops mapped to scan.
    Category                                  Number    Percentage
    ------------------------------------------------------------
    Scan flip-flops mapped for DFT             8        100.00%
    Flip-flops not mapped for DFT
         flip-flops not scan replaceable       0          0.00%
         flip-flops not targeted for DFT       0          0.00%
    ------------------------------------------------------------
                                  Totals       8        100.00%
```

Static Timing Analysis (after DFT)

Schematic

In the post-DFT schematic, scan cells can be seen.



Graph Based Analysis

The setup and hold slacks are positive.

```
Path 1: MET Setup Check with Pin count_reg[7]/CK
Endpoint:   count_reg[7]/D (^) checked with  leading edge of 'clk'
Beginpoint: count_reg[0]/Q (^) triggered by  leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time          0.500
- Setup                         0.695
+ Phase Shift                  10.000
- Uncertainty                   0.020
= Required Time                 9.785
- Arrival Time                  4.751
= Slack Time                    5.033
     Clock Rise Edge                 0.000
     + Clock Network Latency (Ideal) 0.500
     = Beginpoint Arrival Time       0.500
      -------------------------------------------------------------
      Instance      Arc           Cell      Delay  Arrival  Required
                                                   Time     Time
      -------------------------------------------------------------
      count_reg[0]  CK ^          -         -      0.500    5.533
      count_reg[0]  CK ^ -> Q ^   SDFF_X2   1.179  1.679    6.712
      g338          A1 ^ -> ZN v  NAND2_X1  0.191  1.870    6.904
      g631          A2 v -> ZN ^  NOR2_X1   0.329  2.199    7.232
      g627          A1 ^ -> ZN v  NAND2_X1  0.197  2.395    7.429
      g619          A1 v -> ZN v  OR2_X2    0.402  2.798    7.831
      g613          A1 v -> ZN v  OR2_X2    0.385  3.182    8.215
      g606          A1 v -> ZN v  OR2_X2    0.363  3.545    8.579
      g599          B v -> Z v    XOR2_X2   0.367  3.912    8.945
      g594          B1 v -> ZN ^  OAI22_X1  0.839  4.751    9.785
      count_reg[7]  D ^           SDFF_X2   0.000  4.751    9.785
      -------------------------------------------------------------
```

```
Path 1: MET Hold Check with Pin count_reg[0]/CK
Endpoint:   count_reg[0]/SI (^) checked with  leading edge of 'clk'
Beginpoint: DFT_sdi_1       (^) triggered by  leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time          0.500
+ Hold                          0.015
+ Phase Shift                   0.000
+ Uncertainty                   0.020
= Required Time                 0.535
  Arrival Time                  0.839
  Slack Time                    0.304
     Clock Rise Edge                     0.000
     + Input Delay                       0.300
     + Drive Adjustment                  0.039
     + Source Insertion Delay            0.500
     = Beginpoint Arrival Time           0.839
      -------------------------------------------------------------
      Instance      Arc          Cell     Delay  Arrival  Required
                                                 Time     Time
      -------------------------------------------------------------
      -             DFT_sdi_1 ^  -        -      0.839    0.535
      count_reg[0]  SI ^         SDFF_X2  0.000  0.839    0.535
      -------------------------------------------------------------
```

There are no untested paths and no timing violations.

```
--------------------------------------------------------------------------------------------------
                                TIMING CHECK COVERAGE SUMMARY
--------------------------------------------------------------------------------------------------
 Check Type                       No. of    Met              Violated         Untested
                                  Checks
--------------------------------------------------------------------------------------------------
ExternalDelay (Early)          10         10 (100%)        0 (0%)           0 (0%)
ExternalDelay (Late)           10         10 (100%)        0 (0%)           0 (0%)
Hold                           24         24 (100%)        0 (0%)           0 (0%)
PulseWidth                     16         16 (100%)        0 (0%)           0 (0%)
Setup                          24         24 (100%)        0 (0%)           0 (0%)
--------------------------------------------------------------------------------------------------

--------------------------------------------------------------------------------------------------
                                              TIMING CHECK COVERAGE
DETAILS

--------------------------------------------------------------------------------------------------
     Pin                          Reference Pin               Check Type                  Slack
Reason

--------------------------------------------------------------------------------------------------
```

Path Based Analysis

The GBA and PBA results are in agreement.

```
Path 1: MET Setup Check with Pin count_reg[7]/CK
Endpoint:   count_reg[7]/D (^) checked with  leading edge of 'clk'
Beginpoint: count_reg[0]/Q (^) triggered by  leading edge of 'clk'
Path Groups: {clk}
Retime Analysis { Data Path-Slew }
Other End Arrival Time          0.500
- Setup                         0.690
+ Phase Shift                  10.000
- Uncertainty                   0.020
= Required Time                 9.790
- Arrival Time                  4.751
= Slack Time                    5.039
= Slack Time(original)          5.033
     Clock Rise Edge                0.000
     + Clock Network Latency (Ideal) 0.500
     = Beginpoint Arrival Time      0.500
      ------------------------------------------------------------
      Instance      Arc           Cell      Retime  Arrival  Required
                                            Delay   Time     Time
      ------------------------------------------------------------
      count_reg[0]  CK ^          -         -       0.500    5.539
      count_reg[0]  CK ^ -> Q ^   SDFF_X2   1.179   1.679    6.718
      g338          -             NAND2_X1  0.000   1.679    6.718
      g338          A1 ^ -> ZN v  NAND2_X1  0.191   1.870    6.909
      g631          -             NOR2_X1   0.000   1.870    6.909
      g631          A2 v -> ZN ^  NOR2_X1   0.329   2.199    7.238
      g627          -             NAND2_X1  0.000   2.199    7.238
      g627          A1 ^ -> ZN v  NAND2_X1  0.196   2.395    7.434
      g619          -             OR2_X2    0.000   2.395    7.434
      g619          A1 v -> ZN v  OR2_X2    0.402   2.797    7.836
      g613          -             OR2_X2    0.000   2.797    7.836
      g613          A1 v -> ZN v  OR2_X2    0.384   3.182    8.221
```

```
Path 1: MET Hold Check with Pin count_reg[0]/CK
Endpoint:   count_reg[0]/SI (^) checked with  leading edge of 'clk'
Beginpoint: DFT_sdi_1       (^) triggered by  leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time          0.500
+ Hold                          0.015
+ Phase Shift                   0.000
+ Uncertainty                   0.020
= Required Time                 0.535
  Arrival Time                  0.839
  Slack Time                    0.304
     Clock Rise Edge                      0.000
     + Input Delay                        0.300
     + Drive Adjustment                   0.039
     + Source Insertion Delay             0.500
     = Beginpoint Arrival Time            0.839
      ------------------------------------------------------------
      Instance      Arc          Cell     Delay  Arrival  Required
                                                 Time     Time
      ------------------------------------------------------------
      -             DFT_sdi_1 ^  -        -      0.839    0.535
      count_reg[0]  SI ^         SDFF_X2  0.000  0.839    0.535
      ------------------------------------------------------------
```

TIMING CHECK COVERAGE SUMMARY

Check Type	No. of Checks	Met	Violated	Untested
ExternalDelay (Early)	10	10 (100%)	0 (0%)	0 (0%)
ExternalDelay (Late)	10	10 (100%)	0 (0%)	0 (0%)
Hold	24	24 (100%)	0 (0%)	0 (0%)
PulseWidth	16	16 (100%)	0 (0%)	0 (0%)
Setup	24	24 (100%)	0 (0%)	0 (0%)

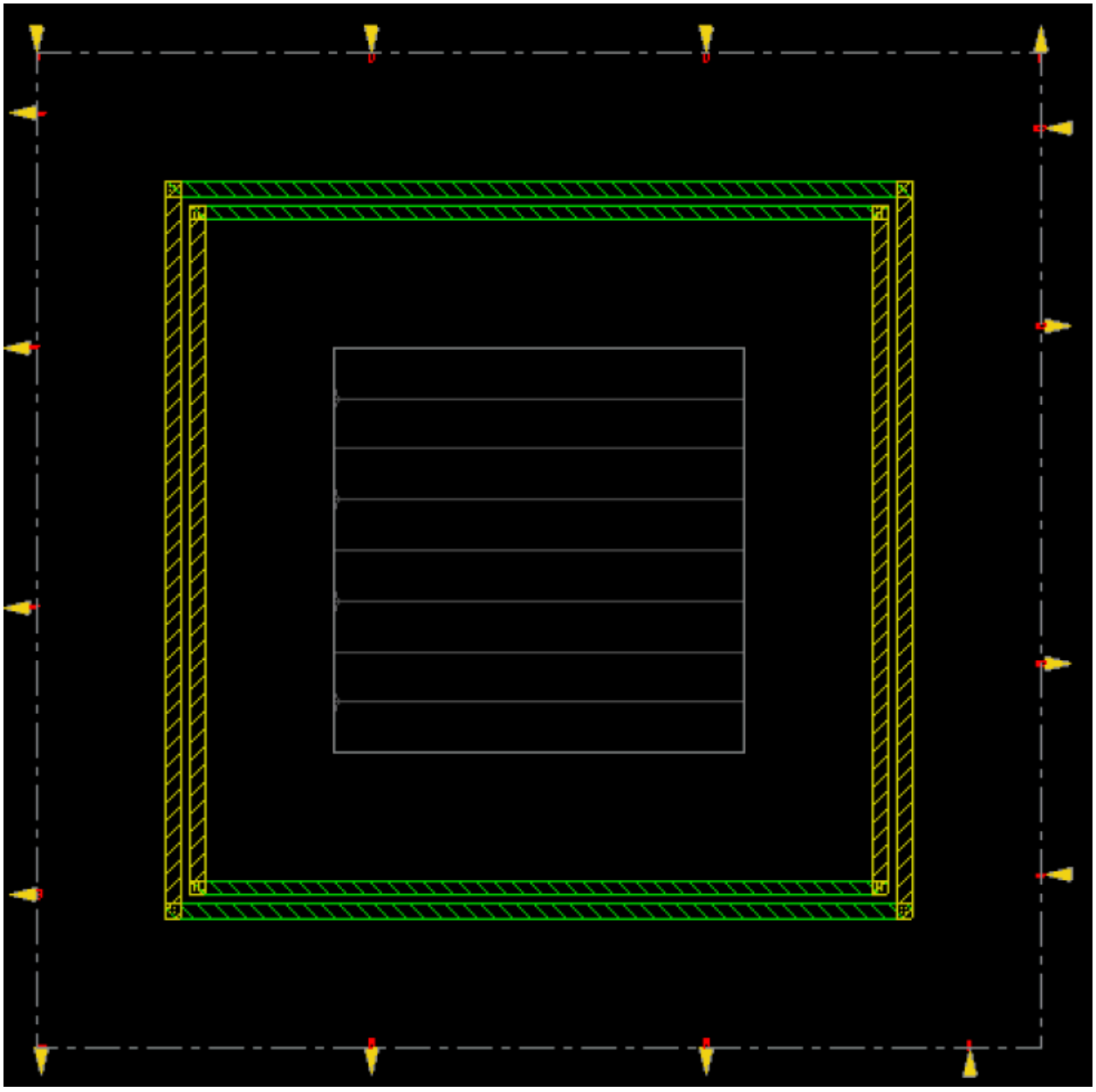
TIMING CHECK COVERAGE DETAILS

Pin	Reference Pin	Check Type	Slack	Reason

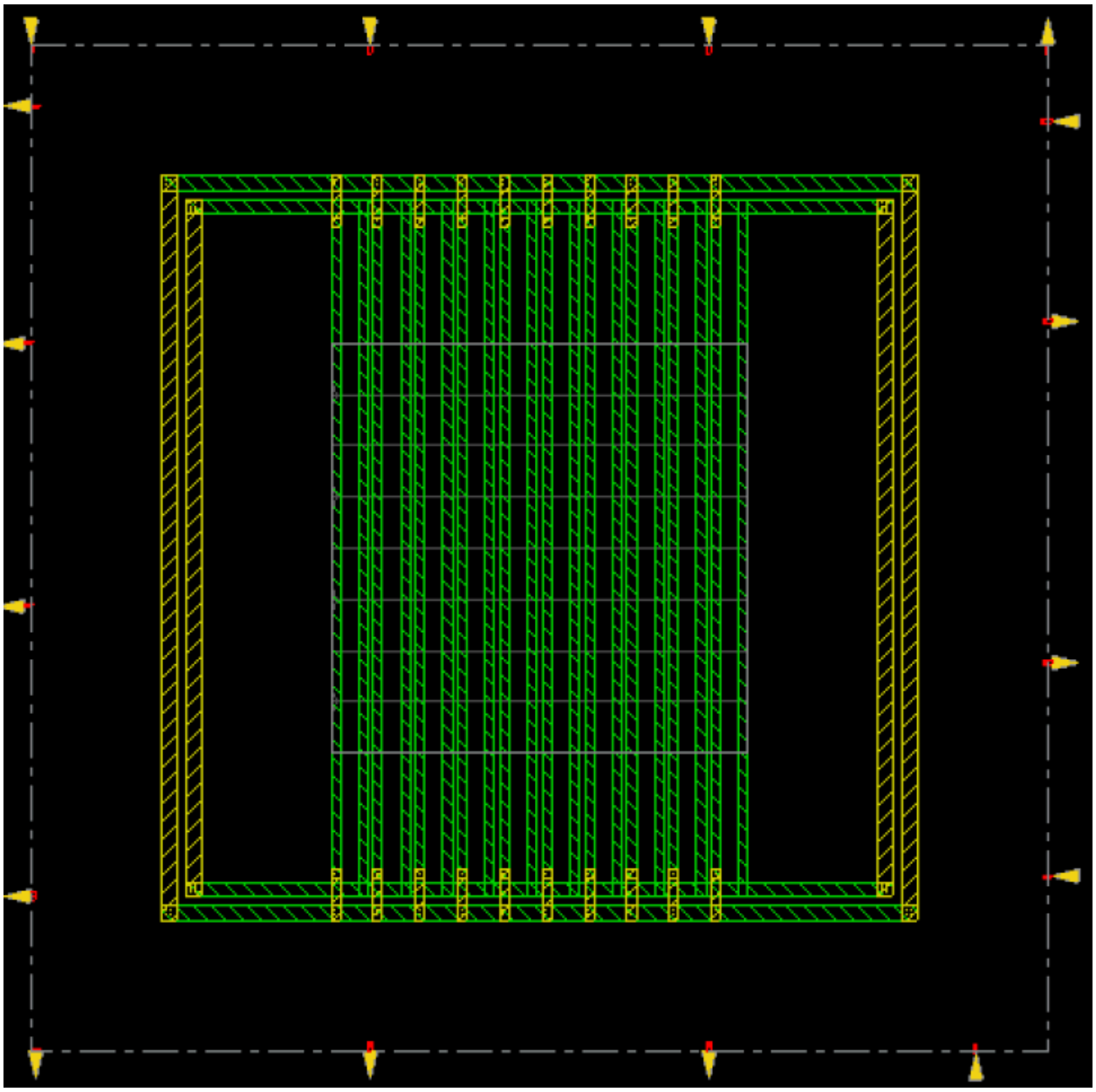
Placement and Routing

Utilization factor 0.8 is used.

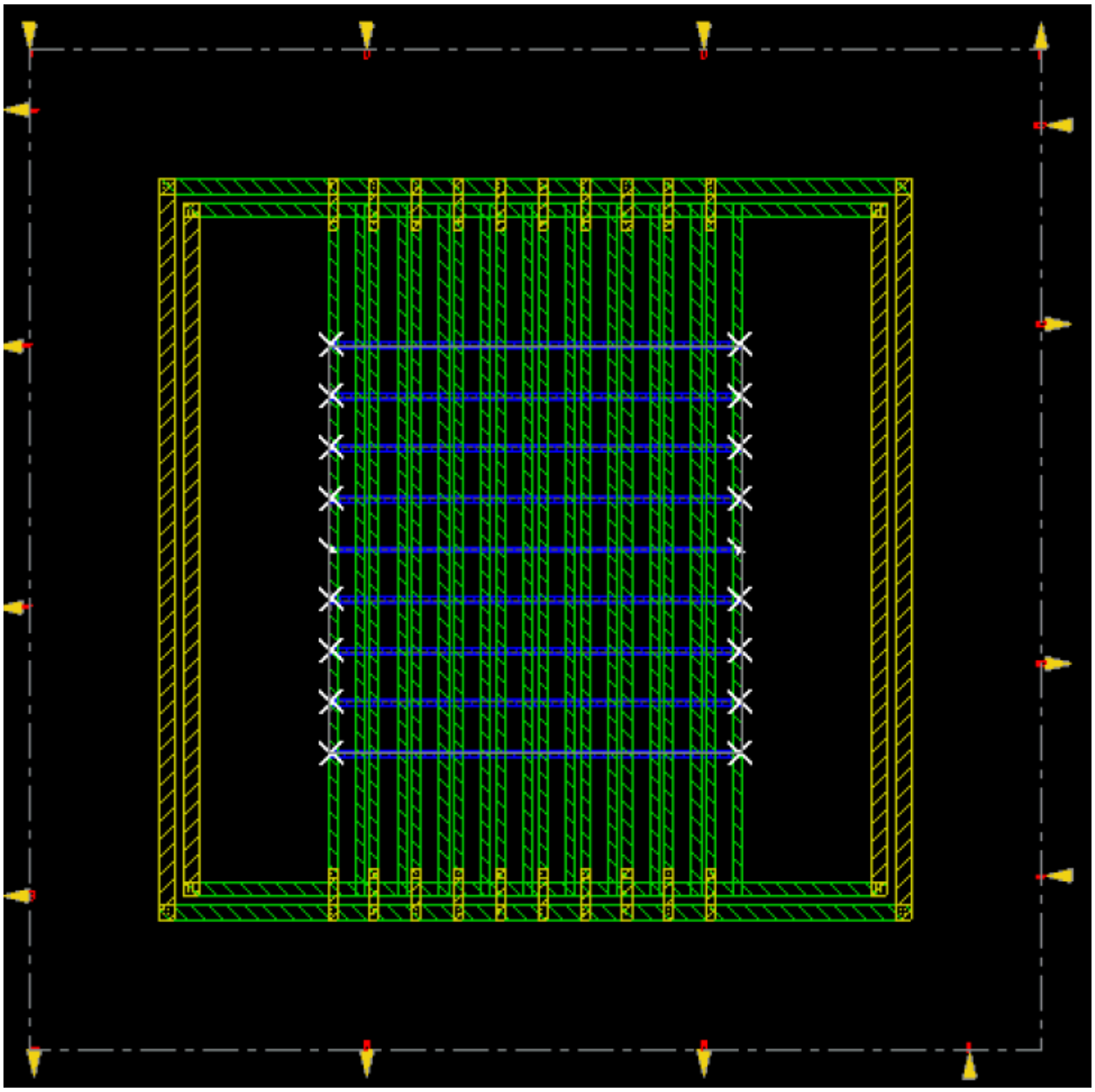
Adding Rings



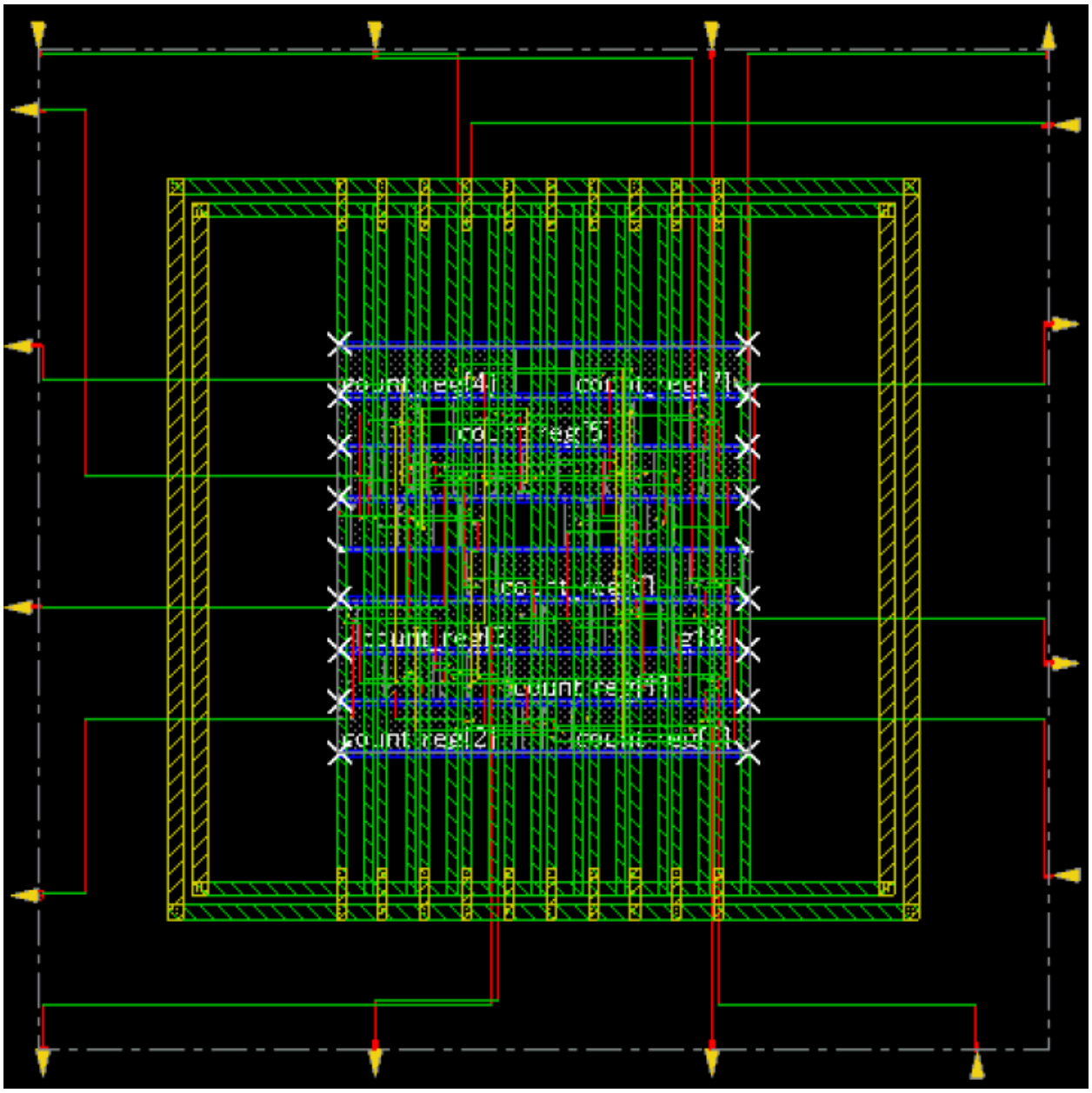
Adding Stripes



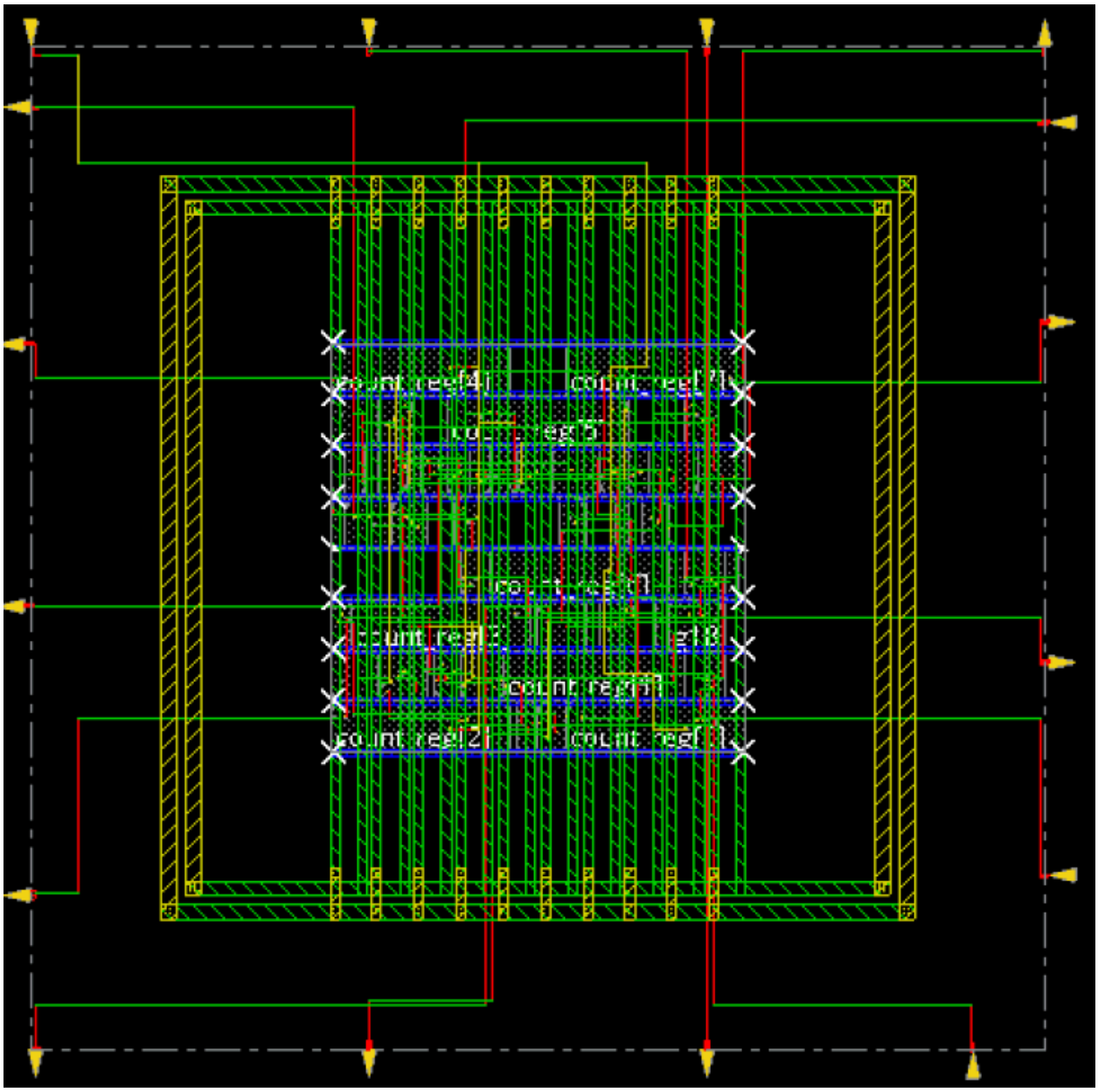
Global Routing



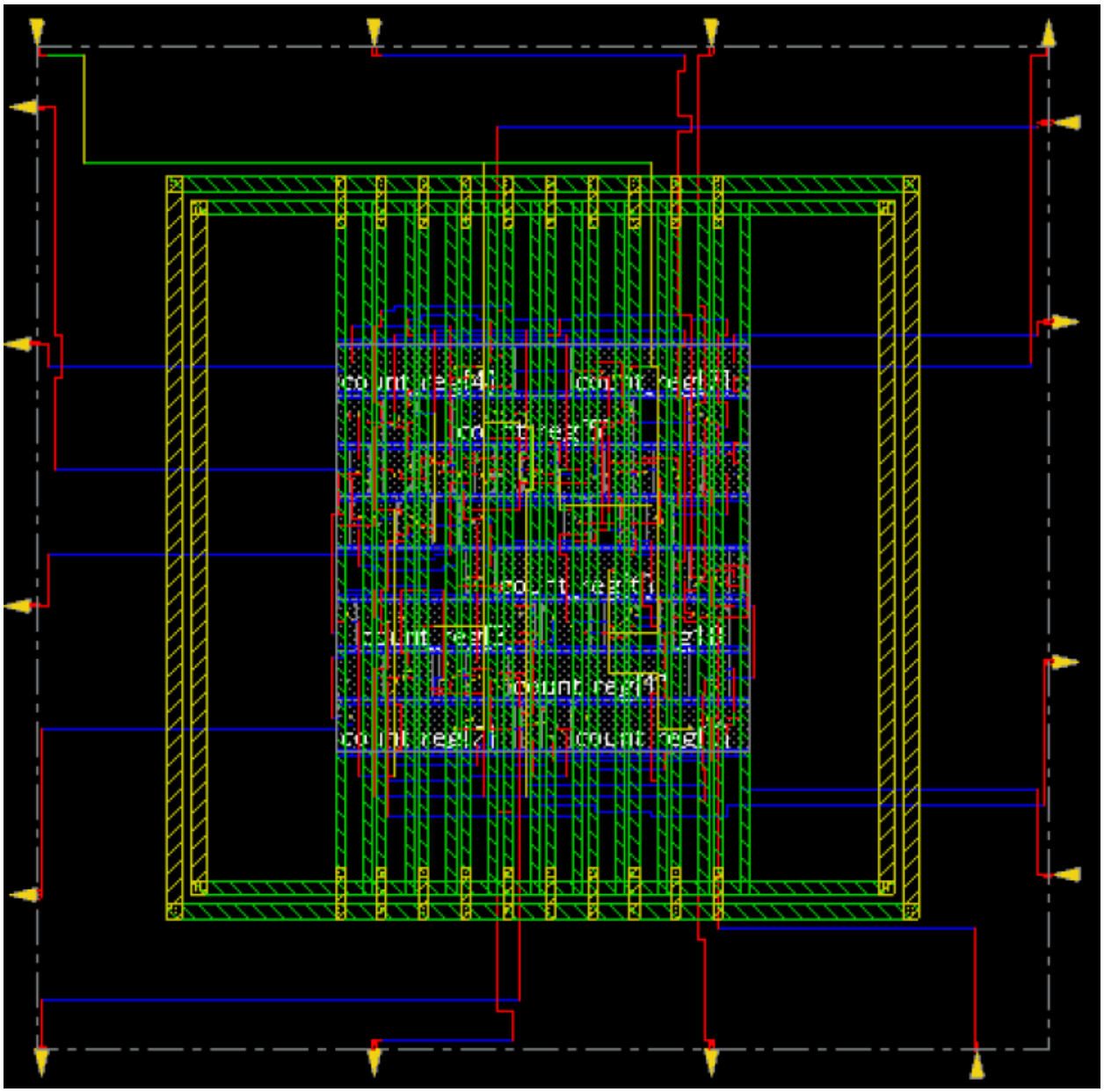
Placement



Clock Tree Synthesis



Detailed Routing



Issues and Learnings

- In verilog code, arrays are not synthesizable and should be replaced with address and data ports.
- Asynchronous inputs should not be constrained with respect to the clock.
- Using root and instance attributes to avoid optimizing parts of the design.
- Correcting unconnected pins in a design.
- To perform PBA instead of GBA, add flag -retime path_slew_propagation to report_timing command.
- A new constraint file needs to be created for DFT to include the new test mode and shift enable ports.
- DFT (in my version of the tool) requires the command **replace_scan** before **connect_scan_chains.** Otherwise, flip-flops are marked as non-scannable. Also, DFT only works for FreePDK45_lib_v1.0_typical_scan.lib and not for slow.lib (in my case).
- The LEF file (FreePDK45_lib_v1.0.lef) compatible with FreePDK45_lib_v1.0_typical_scan.lib supports only M1-M4 layers (as opposed to gsclib045_tech.lef, which supports more than 9 layers). Because of this, there are 12 DRC violations in the final design.