RTL to DFT: RISC V Processor

Design

The module is a simple RISC V processor with a synchronous reset. The register file, data memory and instruction memory are simulated in the testbench. The Program Counter is sent on the output port and used to index the instruction memory, and current instruction is taken as an input. Address, control and data signals for data memory and register file are also input/output signals of the module. The technology libraries used are FreePDK45_lib_v1.0_typical_scan.lib and FreePDK45_lib_v1.0.lef. Clock frequency is 15 ns.

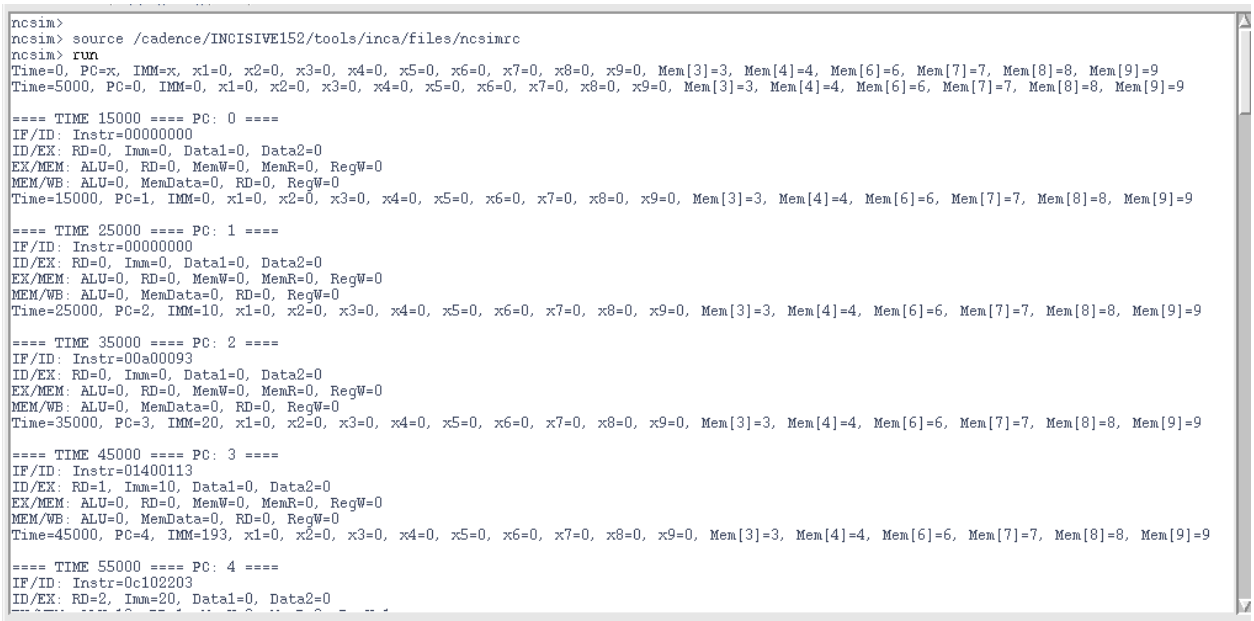
Simulation

Test Instructions

```
// Initialize instruction memory
initial begin
    instruction_memory[0] = 32'b000000001010_00000_000_00001_0010011; // ADDI x1, x0, 10
    instruction_memory[1] = 32'b000000010100_00000_000_00010_0010011; // ADDI x2, x0, 20
    instruction_memory[2] = 32'b000011000001_00000_010_00100_0000011; // LW x4, 193(x0)
    instruction_memory[3] = 32'b000000100110_00000_010_00101_0000011; // LW x5, 38(x0)
    instruction_memory[4] = 32'b0000000_00010_00001_000_00011_0110011; // ADD x3, x1, x2
    instruction_memory[5] = 32'b0100000_00001_00010_000_00110_0110011; // SUB x6, x2, x1
    instruction_memory[6] = 32'b0000000_00010_00001_100_00111_0110011; // XOR x7, x1, x2
    instruction_memory[7] = 32'b0000000_00010_00001_110_01000_0110011; // OR x8, x1, x2
    instruction_memory[8] = 32'b0000000_00010_00001_111_01001_0110011; // AND x9, x1, x2
    instruction_memory[9] = 32'b0000000_00011_00000_010_00011_0100011; // SW x3, 3(x0)
    instruction_memory[10] = 32'b0000000_00011_00000_010_00100_0100011; // SW x3, 4(x0)
    instruction_memory[11] = 32'b0000000_00110_00000_010_00110_0100011; // SW x6, 6(x0)
    instruction_memory[12] = 32'b0000000_00111_00000_010_00111_0100011; // SW x7, 7(x0)
    instruction_memory[13] = 32'b0000000_01000_00000_010_01000_0100011; // SW x8, 8(x0)
    instruction_memory[14] = 32'b0000000_01001_00000_010_01001_0100011; // SW x9, 9(x0)
    instruction_memory[15] = 32'b0; // NOP
end
```

Testbench Output

The simulation of the verilog code works as expected.



```
ncsim>
ncsim> source /cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> run
Time=0, PC=x, IMM=x, x1=0, x2=0, x3=0, x4=0, x5=0, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9
Time=5000, PC=0, IMM=0, x1=0, x2=0, x3=0, x4=0, x5=0, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9

==== TIME 15000 ==== PC: 0 ====
IF/ID: Instr=00000000
ID/EX: RD=0, Imm=0, Data1=0, Data2=0
EX/MEM: ALU=0, RD=0, MemW=0, MemR=0, RegW=0
MEM/WB: ALU=0, MemData=0, RD=0, RegW=0
Time=15000, PC=1, IMM=0, x1=0, x2=0, x3=0, x4=0, x5=0, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9

==== TIME 25000 ==== PC: 1 ====
IF/ID: Instr=00000000
ID/EX: RD=0, Imm=0, Data1=0, Data2=0
EX/MEM: ALU=0, RD=0, MemW=0, MemR=0, RegW=0
MEM/WB: ALU=0, MemData=0, RD=0, RegW=0
Time=25000, PC=2, IMM=10, x1=0, x2=0, x3=0, x4=0, x5=0, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9

==== TIME 35000 ==== PC: 2 ====
IF/ID: Instr=00a00093
ID/EX: RD=0, Imm=0, Data1=0, Data2=0
EX/MEM: ALU=0, RD=0, MemW=0, MemR=0, RegW=0
MEM/WB: ALU=0, MemData=0, RD=0, RegW=0
Time=35000, PC=3, IMM=20, x1=0, x2=0, x3=0, x4=0, x5=0, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9

==== TIME 45000 ==== PC: 3 ====
IF/ID: Instr=01400113
ID/EX: RD=1, Imm=10, Data1=0, Data2=0
EX/MEM: ALU=0, RD=0, MemW=0, MemR=0, RegW=0
MEM/WB: ALU=0, MemData=0, RD=0, RegW=0
Time=45000, PC=4, IMM=193, x1=0, x2=0, x3=0, x4=0, x5=0, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9

==== TIME 55000 ==== PC: 4 ====
IF/ID: Instr=0c102203
ID/EX: RD=2, Imm=20, Data1=0, Data2=0
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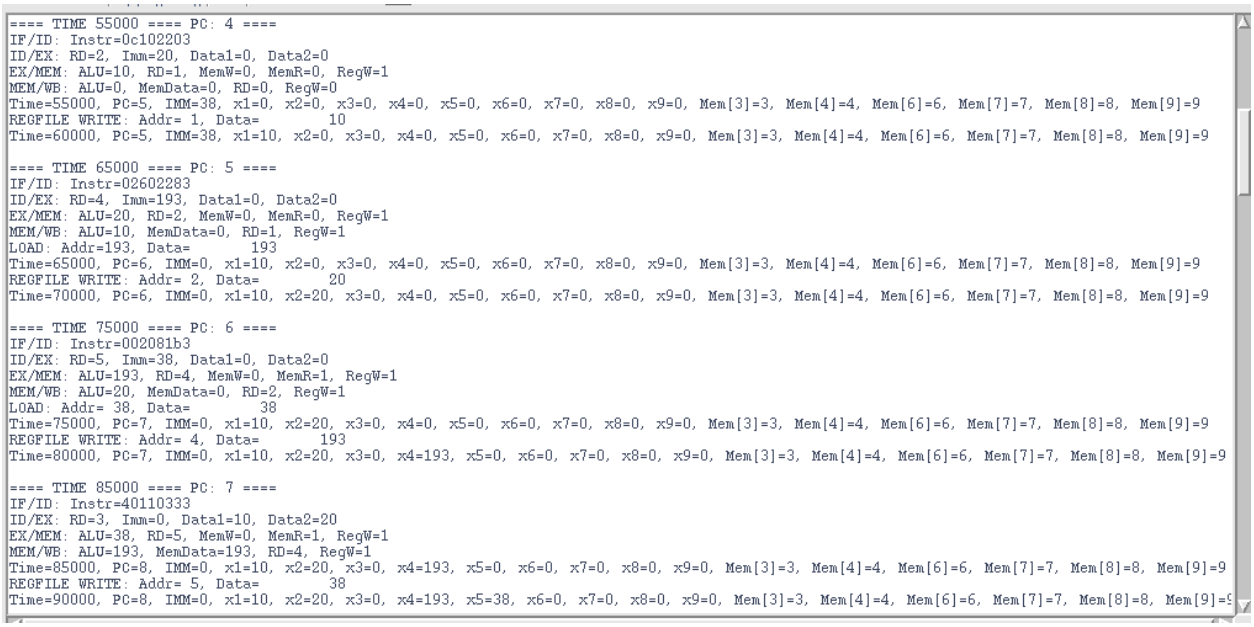

```
==== TIME 55000 ==== PC: 4 ====
IF/ID: Instr=0c102203
ID/EX: RD=2, Imm=20, Data1=0, Data2=0
EX/MEM: ALU=10, RD=1, MemW=0, MemR=0, RegW=1
MEM/WB: ALU=0, MemData=0, RD=0, RegW=0
Time=55000, PC=5, IMM=38, x1=0, x2=0, x3=0, x4=0, x5=0, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9
REGFILE WRITE: Addr= 1, Data=        10
Time=60000, PC=5, IMM=38, x1=10, x2=0, x3=0, x4=0, x5=0, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9

==== TIME 65000 ==== PC: 5 ====
IF/ID: Instr=02602283
ID/EX: RD=4, Imm=193, Data1=0, Data2=0
EX/MEM: ALU=20, RD=2, MemW=0, MemR=0, RegW=1
MEM/WB: ALU=10, MemData=0, RD=1, RegW=1
LOAD: Addr=193, Data=       193
Time=65000, PC=6, IMM=0, x1=10, x2=0, x3=0, x4=0, x5=0, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9
REGFILE WRITE: Addr= 2, Data=        20
Time=70000, PC=6, IMM=0, x1=10, x2=20, x3=0, x4=0, x5=0, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9

==== TIME 75000 ==== PC: 6 ====
IF/ID: Instr=002081b3
ID/EX: RD=5, Imm=38, Data1=0, Data2=0
EX/MEM: ALU=193, RD=4, MemW=0, MemR=1, RegW=1
MEM/WB: ALU=20, MemData=0, RD=2, RegW=1
LOAD: Addr= 38, Data=        38
Time=75000, PC=7, IMM=0, x1=10, x2=20, x3=0, x4=0, x5=0, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9
REGFILE WRITE: Addr= 4, Data=       193
Time=80000, PC=7, IMM=0, x1=10, x2=20, x3=0, x4=193, x5=0, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9

==== TIME 85000 ==== PC: 7 ====
IF/ID: Instr=40110333
ID/EX: RD=3, Imm=0, Data1=10, Data2=20
EX/MEM: ALU=38, RD=5, MemW=0, MemR=1, RegW=1
MEM/WB: ALU=193, MemData=193, RD=4, RegW=1
Time=85000, PC=8, IMM=0, x1=10, x2=20, x3=0, x4=193, x5=0, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9
REGFILE WRITE: Addr= 5, Data=        38
Time=90000, PC=8, IMM=0, x1=10, x2=20, x3=0, x4=193, x5=38, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9
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REGFILE WRITE: Addr= 5, Data=        38
Time=90000, PC=8, IMM=0, x1=10, x2=20, x3=0, x4=193, x5=38, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9

==== TIME 95000 ==== PC: 8 ====
IF/ID: Instr=0020c3b3
ID/EX: RD=6, Imm=0, Data1=20, Data2=10
EX/MEM: ALU=30, RD=3, MemW=0, MemR=0, RegW=1
MEM/WB: ALU=38, MemData=38, RD=5, RegW=1
Time=95000, PC=9, IMM=0, x1=10, x2=20, x3=0, x4=193, x5=38, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]=9
REGFILE WRITE: Addr= 3, Data=        30
Time=100000, PC=9, IMM=0, x1=10, x2=20, x3=30, x4=193, x5=38, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9]

==== TIME 105000 ==== PC: 9 ====
IF/ID: Instr=0020e433
ID/EX: RD=7, Imm=0, Data1=10, Data2=20
EX/MEM: ALU=10, RD=6, MemW=0, MemR=0, RegW=1
MEM/WB: ALU=30, MemData=38, RD=3, RegW=1
Time=105000, PC=10, IMM=0, x1=10, x2=20, x3=30, x4=193, x5=38, x6=0, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[9
REGFILE WRITE: Addr= 6, Data=        10
Time=110000, PC=10, IMM=0, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[

==== TIME 115000 ==== PC: 10 ====
IF/ID: Instr=0020f4b3
ID/EX: RD=8, Imm=0, Data1=10, Data2=20
EX/MEM: ALU=30, RD=7, MemW=0, MemR=0, RegW=1
MEM/WB: ALU=10, MemData=38, RD=6, RegW=1
Time=115000, PC=11, IMM=3, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=0, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem[
REGFILE WRITE: Addr= 7, Data=        30
Time=120000, PC=11, IMM=3, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem

==== TIME 125000 ==== PC: 11 ====
IF/ID: Instr=003021a3
ID/EX: RD=9, Imm=0, Data1=10, Data2=20
EX/MEM: ALU=30, RD=8, MemW=0, MemR=0, RegW=1
MEM/WB: ALU=30, MemData=38, RD=7, RegW=1
Time=125000, PC=12, IMM=4, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem
REGFILE WRITE: Addr= 8, Data=        30
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==== TIME 125000 ==== PC: 11 ====
IF/ID: Instr=003021a3
ID/EX: RD=9, Imm=0, Data1=10, Data2=20
EX/MEM: ALU=30, RD=8, MemW=0, MemR=0, RegW=1
MEM/WB: ALU=30, MemData=38, RD=7, RegW=1
Time=125000, PC=12, IMM=4, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=0, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Mem
REGFILE WRITE: Addr= 8, Data=        30
Time=130000, PC=12, IMM=4, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Me

==== TIME 135000 ==== PC: 12 ====
IF/ID: Instr=00302223
ID/EX: RD=3, Imm=3, Data1=0, Data2=30
EX/MEM: ALU=0, RD=9, MemW=0, MemR=0, RegW=1
MEM/WB: ALU=30, MemData=38, RD=8, RegW=1
Time=135000, PC=13, IMM=6, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=3, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, Me
STORE: Addr=  3, Data=        30
REGFILE WRITE: Addr= 9, Data=         0
Time=140000, PC=13, IMM=6, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, M

==== TIME 145000 ==== PC: 13 ====
IF/ID: Instr=00602323
ID/EX: RD=4, Imm=4, Data1=0, Data2=30
EX/MEM: ALU=3, RD=3, MemW=1, MemR=0, RegW=0
MEM/WB: ALU=0, MemData=38, RD=9, RegW=1
Time=145000, PC=14, IMM=7, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=4, Mem[6]=6, Mem[7]=7, Mem[8]=8, M
STORE: Addr=  4, Data=        30
Time=150000, PC=14, IMM=7, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=6, Mem[7]=7, Mem[8]=8,

==== TIME 155000 ==== PC: 14 ====
IF/ID: Instr=007023a3
ID/EX: RD=6, Imm=6, Data1=0, Data2=10
EX/MEM: ALU=4, RD=4, MemW=1, MemR=0, RegW=0
MEM/WB: ALU=3, MemData=38, RD=3, RegW=0
Time=155000, PC=15, IMM=8, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=6, Mem[7]=7, Mem[8]=8,
STORE: Addr=  6, Data=        10
Time=160000, PC=15, IMM=8, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=10, Mem[7]=7, Mem[8]=8,
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==== TIME 155000 ==== PC: 14 ====
IF/ID: Instr=007023a3
ID/EX: RD=6, Imm=6, Data1=0, Data2=10
EX/MEM: ALU=4, RD=4, MemW=1, MemR=0, RegW=0
MEM/WB: ALU=3, MemData=38, RD=3, RegW=0
Time=155000, PC=15, IMM=8, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=6, Mem[7]=7, Mem[8]=8,
STORE: Addr=  6, Data=        10
Time=160000, PC=15, IMM=8, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=10, Mem[7]=7, Mem[8]=8,

==== TIME 165000 ==== PC: 15 ====
IF/ID: Instr=00802423
ID/EX: RD=7, Imm=7, Data1=0, Data2=30
EX/MEM: ALU=6, RD=6, MemW=1, MemR=0, RegW=0
MEM/WB: ALU=4, MemData=38, RD=4, RegW=0
Time=165000, PC=16, IMM=9, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=10, Mem[7]=7, Mem[8]=8,
STORE: Addr=  7, Data=        30
Time=170000, PC=16, IMM=9, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=10, Mem[7]=30, Mem[8]=8

==== TIME 175000 ==== PC: 16 ====
IF/ID: Instr=009024a3
ID/EX: RD=8, Imm=8, Data1=0, Data2=30
EX/MEM: ALU=7, RD=7, MemW=1, MemR=0, RegW=0
MEM/WB: ALU=6, MemData=38, RD=6, RegW=0
Time=175000, PC=17, IMM=0, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=10, Mem[7]=30, Mem[8]=8
STORE: Addr=  8, Data=        30
Time=180000, PC=17, IMM=0, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=10, Mem[7]=30, Mem[8]=3

==== TIME 185000 ==== PC: 17 ====
IF/ID: Instr=00000000
ID/EX: RD=9, Imm=9, Data1=0, Data2=0
EX/MEM: ALU=8, RD=8, MemW=1, MemR=0, RegW=0
MEM/WB: ALU=7, MemData=38, RD=7, RegW=0
Time=185000, PC=18, IMM=0, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=10, Mem[7]=30, Mem[8]=3
STORE: Addr=  9, Data=         0
Time=190000, PC=18, IMM=0, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=10, Mem[7]=30, Mem[8]=3

==== TIME 195000 ==== PC: 18 ====
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==== TIME 195000 ==== PC: 18 ====
IF/ID: Instr=xxxxxxxx
ID/EX: RD=0, Imm=0, Data1=0, Data2=0
EX/MEM: ALU=9, RD=9, MemW=1, MemR=0, RegW=0
MEM/WB: ALU=8, MemData=38, RD=8, RegW=0
Time=195000, PC=19, IMM=0, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=10, Mem[7]=30, Mem[8]=3

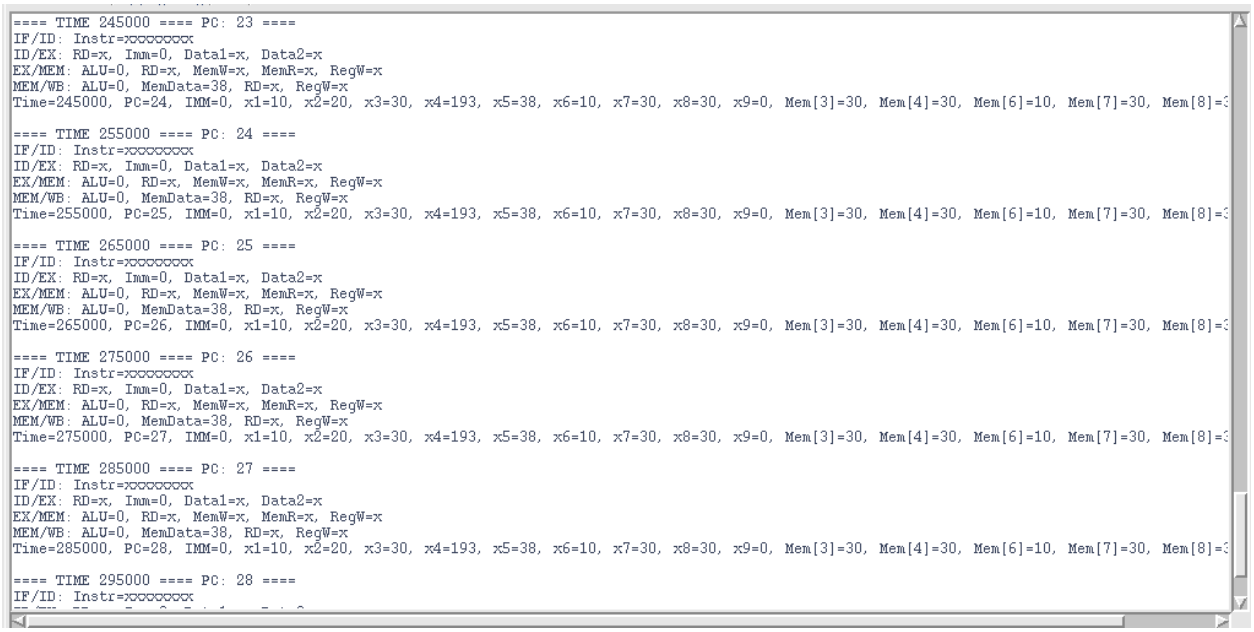
==== TIME 205000 ==== PC: 19 ====
IF/ID: Instr=xxxxxxxx
ID/EX: RD=x, Imm=0, Data1=x, Data2=x
EX/MEM: ALU=0, RD=0, MemW=0, MemR=0, RegW=0
MEM/WB: ALU=9, MemData=38, RD=9, RegW=0
Time=205000, PC=20, IMM=0, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=10, Mem[7]=30, Mem[8]=3

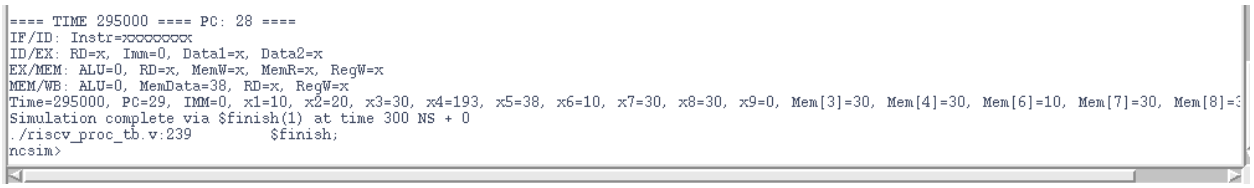
==== TIME 215000 ==== PC: 20 ====
IF/ID: Instr=xxxxxxxx
ID/EX: RD=x, Imm=0, Data1=x, Data2=x
EX/MEM: ALU=0, RD=x, MemW=x, MemR=x, RegW=x
MEM/WB: ALU=0, MemData=38, RD=0, RegW=0
Time=215000, PC=21, IMM=0, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=10, Mem[7]=30, Mem[8]=3

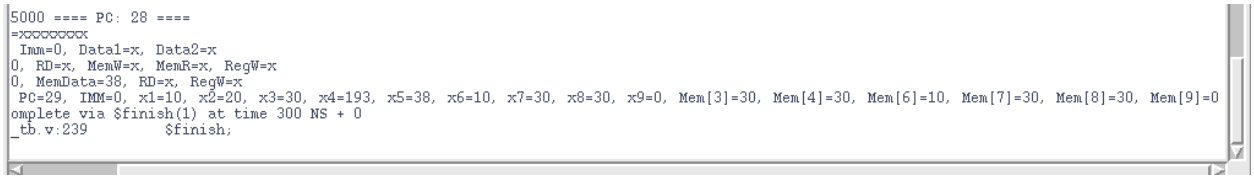
==== TIME 225000 ==== PC: 21 ====
IF/ID: Instr=xxxxxxxx
ID/EX: RD=x, Imm=0, Data1=x, Data2=x
EX/MEM: ALU=0, RD=x, MemW=x, MemR=x, RegW=x
MEM/WB: ALU=0, MemData=38, RD=x, RegW=x
Time=225000, PC=22, IMM=0, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=10, Mem[7]=30, Mem[8]=3

==== TIME 235000 ==== PC: 22 ====
IF/ID: Instr=xxxxxxxx
ID/EX: RD=x, Imm=0, Data1=x, Data2=x
EX/MEM: ALU=0, RD=x, MemW=x, MemR=x, RegW=x
MEM/WB: ALU=0, MemData=38, RD=x, RegW=x
Time=235000, PC=23, IMM=0, x1=10, x2=20, x3=30, x4=193, x5=38, x6=10, x7=30, x8=30, x9=0, Mem[3]=30, Mem[4]=30, Mem[6]=10, Mem[7]=30, Mem[8]=3

==== TIME 245000 ==== PC: 23 ====
IF/ID: Instr=xxxxxxxx
```







The final results should be:

x1 = 0 + 10 = 10

x2 = 0 + 20 = 20

x4 = 193

x5 = 38

x3 = x1 + x2 = 30

x6 = x2 - x1 = 10

x7 = x1 xor x2 = 30

x8 = x1 or x2 = 30

x9 = x1 and x2 = 0

mem[3] = x3 = 30

mem[4] = x3 = 30

mem[6] = x6 = 10

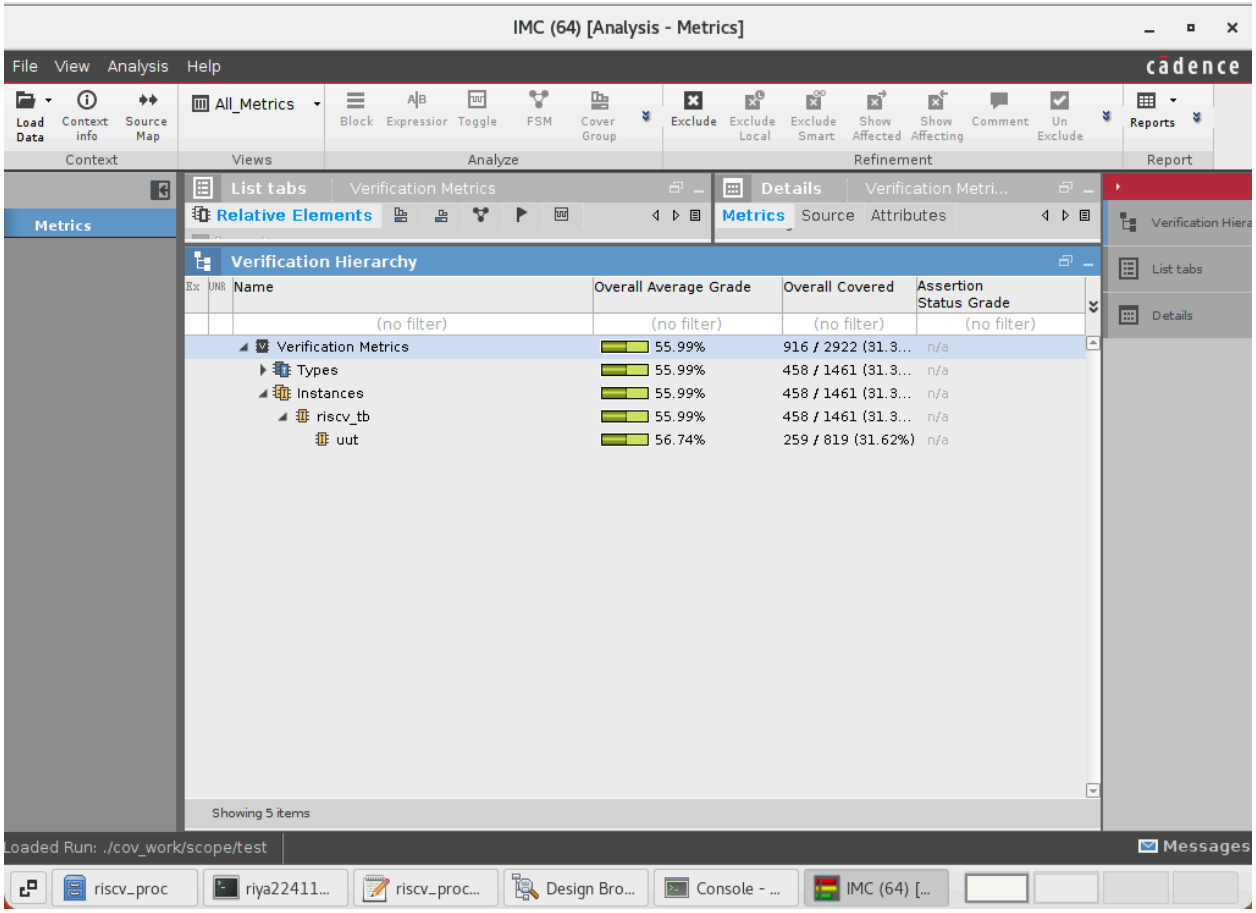
mem[7] = x7 = 30

mem[8] = x8 = 30

mem[9] = x9 = 0

Coverage Report

The coverage is low because all variables in the design are 32 bit long but for testing purposes, they were assigned small numbers (max 193, 8 bits). The upper bits remain unused.



Synthesis

The register for immediate value (ID_EX_imm) is directed to not optimize unused flip flops. There is one unconnected pin in the synthesized netlist, which is suspected to be in the Program Counter design.

The timing intent results are as expected.

```
Lint summary
 Unconnected/logic driven clocks                                  0
 Sequential data pins driven by a clock signal                    0
 Sequential clock pins without clock waveform                     0
 Sequential clock pins with multiple clock waveforms              0
 Generated clocks without clock waveform                          0
 Generated clocks with incompatible options                       0
 Generated clocks with multi-master clock                         0
 Paths constrained with different clocks                          0
 Loop-breaking cells for combinational feedback                   0
 Nets with multiple drivers                                       0
 Timing exceptions with no effect                                 0
 Suspicious multi_cycle exceptions                                0
 Pins/ports with conflicting case constants                       0
 Inputs without clocked external delays                           0
 Outputs without clocked external delays                          0
 Inputs without external driver/transition                        0
 Outputs without external load                                    0
 Exceptions with invalid timing start-/endpoints                  0

                                                    Total:        0
```

The post-synthesis power report is as follows:

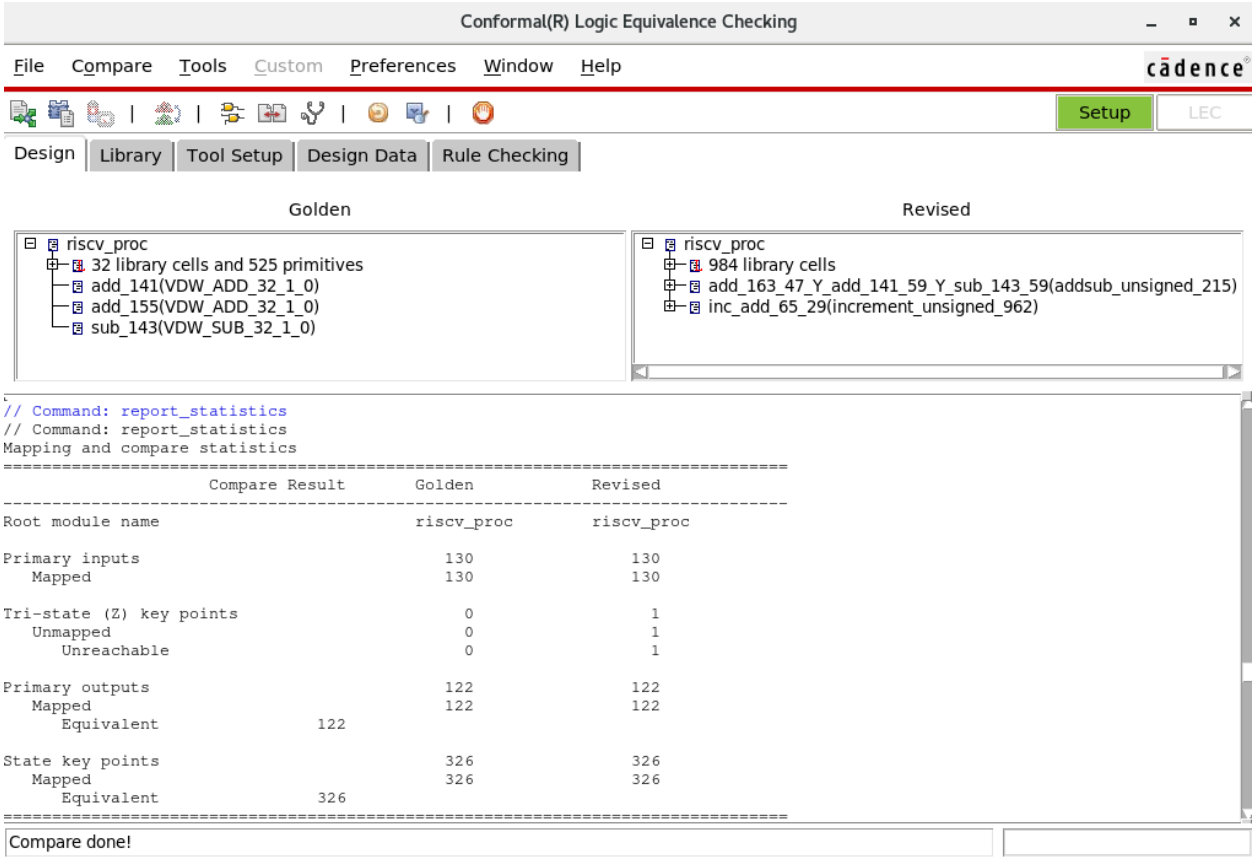
```
Instance: /riscv_proc
Power Unit: W
PDB Frames: /stim#0/frame#0
  ---------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ---------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     9.74239e-07  2.78994e-05  1.96768e-06  3.08413e-05  59.40%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     6.26996e-07  4.63482e-06  3.27926e-06  8.54108e-06  16.45%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     0.00000e+00  0.00000e+00  1.25376e-05  1.25376e-05  24.15%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ---------------------------------------------------------------------------
    Subtotal     1.60123e-06  3.25342e-05  1.77845e-05  5.19200e-05 100.00%
  Percentage           3.08%       62.66%       34.25%      100.00% 100.00%
  ---------------------------------------------------------------------------
```

The post-synthesis area report is as follows:

Type	Instances	Area	Area %
sequential	326	1682.716	60.8
inverter	110	61.446	2.2
buffer	1	0.798	0.0
logic	910	1024.898	37.0
physical_cells	0	0.000	0.0
total	1347	2769.858	100.0

Logical Equivalence Check

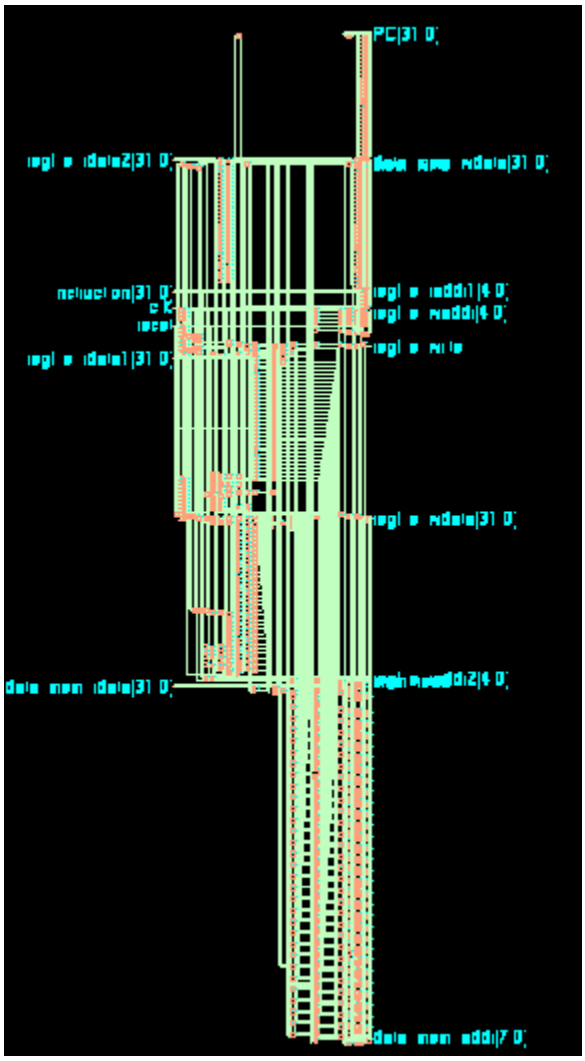
The verilog code and the netlist are equivalent except one Z pin in the netlist which was not present in the original design.



Static Timing Analysis (before DFT)

Schematic

The pre-DFT schematic is as follows:



Graph Based Analysis

The setup and hold slacks are positive.

```
Path 1: MET Setup Check with Pin EX_MEM_alu_result_reg[31]/CK
Endpoint:   EX_MEM_alu_result_reg[31]/D (v) checked with  leading edge of 'clk'
Beginpoint: ID_EX_funct7_reg[1]/Q       (v) triggered by  leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time          0.600
- Setup                         0.824
+ Phase Shift                  15.000
- Uncertainty                   0.020
= Required Time                14.756
- Arrival Time                 14.749
= Slack Time                    0.007
     Clock Rise Edge                0.000
     + Clock Network Latency (Ideal) 0.600
     = Beginpoint Arrival Time      0.600
      ------------------------------------------------------------------------------------------
      Instance                                  Arc           Cell       Delay  Arrival  Required
                                                                          Time     Time
      ------------------------------------------------------------------------------------------
      ID_EX_funct7_reg[1]                       CK ^          -          -      0.600    0.607
      ID_EX_funct7_reg[1]                       CK ^ -> Q v   DFF_X2     1.326  1.926    1.933
      g3442                                     A3 v -> ZN ^  NOR3_X1    0.431  2.357    2.364
      g3405                                     A3 ^ -> ZN v  NAND4_X1   0.375  2.732    2.739
      g3403                                     A v -> ZN ^   INV_X32    0.423  3.155    3.162
      add_163_47_Y_add_141_59_Y_sub_143_59/g1121  B ^ -> Z ^    XOR2_X2    0.629  3.783    3.790
      add_163_47_Y_add_141_59_Y_sub_143_59/g1057  A1 ^ -> ZN v  AOI22_X1   0.250  4.033    4.040
      add_163_47_Y_add_141_59_Y_sub_143_59/g1038  B2 v -> ZN ^  OAI21_X2   0.444  4.477    4.484
      add_163_47_Y_add_141_59_Y_sub_143_59/g1036  A1 ^ -> ZN v  AOI22_X1   0.237  4.713    4.720
      add_163_47_Y_add_141_59_Y_sub_143_59/g1033  B1 v -> ZN ^  OAI21_X1   0.442  5.155    5.162
      add_163_47_Y_add_141_59_Y_sub_143_59/g1031  A1 ^ -> ZN v  AOI22_X1   0.233  5.388    5.395
      add_163_47_Y_add_141_59_Y_sub_143_59/g1028  B1 v -> ZN ^  OAI21_X1   0.432  5.820    5.827
      add_163_47_Y_add_141_59_Y_sub_143_59/g1026  A1 ^ -> ZN v  AOI22_X1   0.234  6.054    6.061
      add_163_47_Y_add_141_59_Y_sub_143_59/g1023  B2 v -> ZN ^  OAI21_X2   0.460  6.514    6.520
```

```
Path 1: MET Hold Check with Pin IF_ID_instr_reg[19]/CK
Endpoint:   IF_ID_instr_reg[19]/D (v) checked with  leading edge of 'clk'
Beginpoint: instruction[19]       (v) triggered by  leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time          0.600
+ Hold                          0.073
+ Phase Shift                   0.000
+ Uncertainty                   0.020
= Required Time                 0.693
  Arrival Time                  1.092
  Slack Time                    0.399
     Clock Rise Edge                     0.000
     + Input Delay                       0.300
     + Drive Adjustment                  0.005
     + Source Insertion Delay            0.600
     = Beginpoint Arrival Time           0.905
      ------------------------------------------------------------------------
      Instance            Arc               Cell     Delay  Arrival  Required
                                                             Time     Time
      ------------------------------------------------------------------------
      -                   instruction[19] v  -        -      0.905    0.506
      g7280               A2 v -> ZN v       AND2_X1  0.187  1.092    0.693
      IF_ID_instr_reg[19]  D v               DFF_X1   0.000  1.092    0.693
      ------------------------------------------------------------------------
```

There are no timing violations but there are some untested paths.

TIMING CHECK COVERAGE SUMMARY

Check Type	No. of Checks	Met	Violated	Untested
ExternalDelay (Early)	122	122 (100%)	0 (0%)	0 (0%)
ExternalDelay (Late)	122	122 (100%)	0 (0%)	0 (0%)
Hold	328	328 (100%)	0 (0%)	0 (0%)
PulseWidth	662	652 (98%)	0 (0%)	10 (1%)
Recovery	10	0 (0%)	0 (0%)	10 (100%)
Removal	10	0 (0%)	0 (0%)	10 (100%)
Setup	328	328 (100%)	0 (0%)	0 (0%)

Path Based Analysis

The setup and hold slacks are positive.

```
Path 1: MET Setup Check with Pin EX_MEM_alu_result_reg[31]/CK
Endpoint:   EX_MEM_alu_result_reg[31]/D (v) checked with  leading edge of 'clk'
Beginpoint: ID_EX_funct7_reg[1]/Q       (v) triggered by  leading edge of 'clk'
Path Groups: {clk}
Retime Analysis { Data Path-Slew }
Other End Arrival Time          0.600
- Setup                         0.808
+ Phase Shift                  15.000
- Uncertainty                   0.020
= Required Time                14.772
- Arrival Time                 14.342
= Slack Time                    0.430
= Slack Time(original)          0.007
     Clock Rise Edge                 0.000
     + Clock Network Latency (Ideal) 0.600
     = Beginpoint Arrival Time       0.600
      ------------------------------------------------------------------------------------------
      Instance                                  Arc           Cell       Retime  Arrival  Required
                                                                         Delay   Time     Time
      ------------------------------------------------------------------------------------------
      ID_EX_funct7_reg[1]                       CK ^          -          -       0.600    1.030
      ID_EX_funct7_reg[1]                       CK ^ -> Q v   DFF_X2     1.326   1.926    2.356
      g3442                                     -             NOR3_X1    0.000   1.926    2.356
      g3442                                     A3 v -> ZN ^  NOR3_X1    0.431   2.357    2.787
      g3405                                     -             NAND4_X1   0.000   2.357    2.787
      g3405                                     A3 ^ -> ZN v  NAND4_X1   0.375   2.732    3.162
      g3403                                     -             INV_X32    0.000   2.732    3.162
      g3403                                     A v -> ZN ^   INV_X32    0.409   3.141    3.571
      add_163_47_Y_add_141_59_Y_sub_143_59/g1121  -           XOR2_X2    0.000   3.141    3.571
      add_163_47_Y_add_141_59_Y_sub_143_59/g1121  B ^ -> Z ^   XOR2_X2    0.628   3.769    4.199
      add_163_47_Y_add_141_59_Y_sub_143_59/g1057  -           AOI22_X1   0.000   3.769    4.199
      add_163_47_Y_add_141_59_Y_sub_143_59/g1057  A1 ^ -> ZN v  AOI22_X1   0.249   4.017    4.447
      add_163_47_Y_add_141_59_Y_sub_143_59/g1038  -           OAI21_X2   0.000   4.017    4.447
```

```
Path 1: MET Hold Check with Pin IF_ID_instr_reg[19]/CK
Endpoint:   IF_ID_instr_reg[19]/D (v) checked with  leading edge of 'clk'
Beginpoint: instruction[19]       (v) triggered by  leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time          0.600
+ Hold                          0.073
+ Phase Shift                   0.000
+ Uncertainty                   0.020
= Required Time                 0.693
  Arrival Time                  1.092
  Slack Time                    0.399
     Clock Rise Edge                     0.000
     + Input Delay                       0.300
     + Drive Adjustment                  0.005
     + Source Insertion Delay            0.600
     = Beginpoint Arrival Time           0.905
      ------------------------------------------------------------------------
      Instance             Arc                Cell     Delay  Arrival  Required
                                                           Time     Time
      ------------------------------------------------------------------------
      -                    instruction[19] v  -        -      0.905    0.506
      g7280                A2 v -> ZN v       AND2_X1  0.187  1.092    0.693
      IF_ID_instr_reg[19]  D v                DFF_X1   0.000  1.092    0.693
      ------------------------------------------------------------------------
```

There are no timing violations but there are some untested paths.

TIMING CHECK COVERAGE SUMMARY

Check Type	No. of Checks	Met	Violated	Untested
ExternalDelay (Early)	122	122 (100%)	0 (0%)	0 (0%)
ExternalDelay (Late)	122	122 (100%)	0 (0%)	0 (0%)
Hold	328	328 (100%)	0 (0%)	0 (0%)
PulseWidth	662	652 (98%)	0 (0%)	10 (1%)
Recovery	10	0 (0%)	0 (0%)	10 (100%)
Removal	10	0 (0%)	0 (0%)	10 (100%)
Setup	328	328 (100%)	0 (0%)	0 (0%)

Design For Test

All 306 flip flops pass the DFT rule check and are mapped to scan cells.

```
Detected 0 DFT rule violation(s)
        Summary of check_dft_rules
        **************************
        Number of usable scan cells: 4
Clock Rule Violations:
---------------------
          Internally driven clock net: 0
              Tied constant clock net: 0
                   Undriven clock net: 0
        Conflicting async & clock net: 0
                      Misc. clock net: 0

Async. set/reset Rule Violations:
--------------------------------
        Internally driven async net: 0
              Tied active async net: 0
                 Undriven async net: 0
                    Misc. async net: 0

   Total number of DFT violations: 0

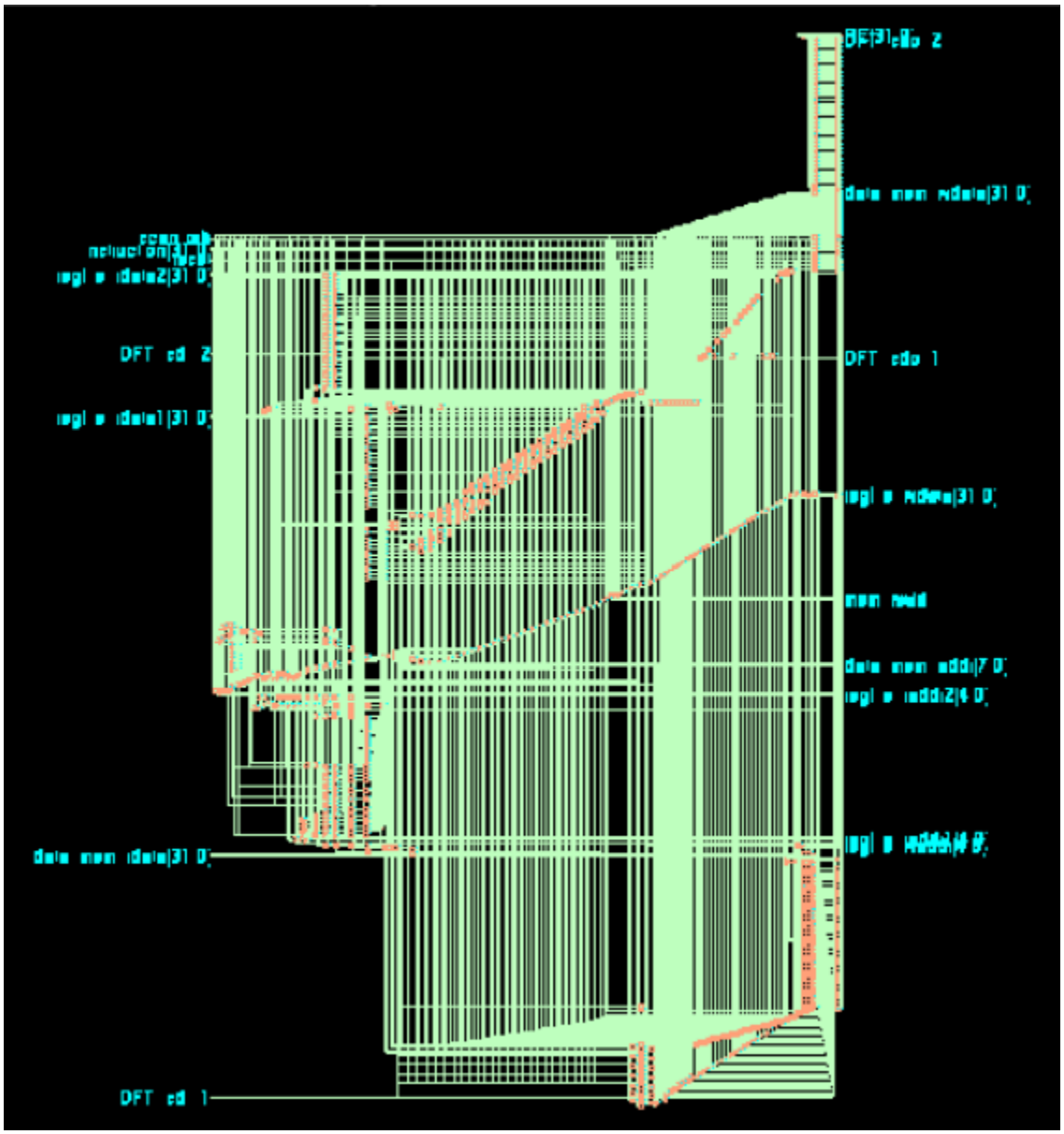
Total number of Test Clock Domains: 1
  DFT Test Clock Domain: clk
        Test Clock 'clk' (Positive edge) has 306 registers
Number of user specified non-Scan registers:   0
    Number of registers that fail DFT rules:   0
    Number of registers that pass DFT rules: 306
Percentage of total registers that are scannable: 100%
```

```
Scan mapping status report
==========================
    Scan mapping: converting flip-flops that pass TDRC.
    Scan mapping done: 306 flip-flops mapped to scan.
    Category                                 Number    Percentage
    -------------------------------------------------------------
    Scan flip-flops mapped for DFT              306        100.00%
    Flip-flops not mapped for DFT
         flip-flops not scan replaceable          0          0.00%
         flip-flops not targeted for DFT          0          0.00%
    -------------------------------------------------------------
                                   Totals        306        100.00%
```

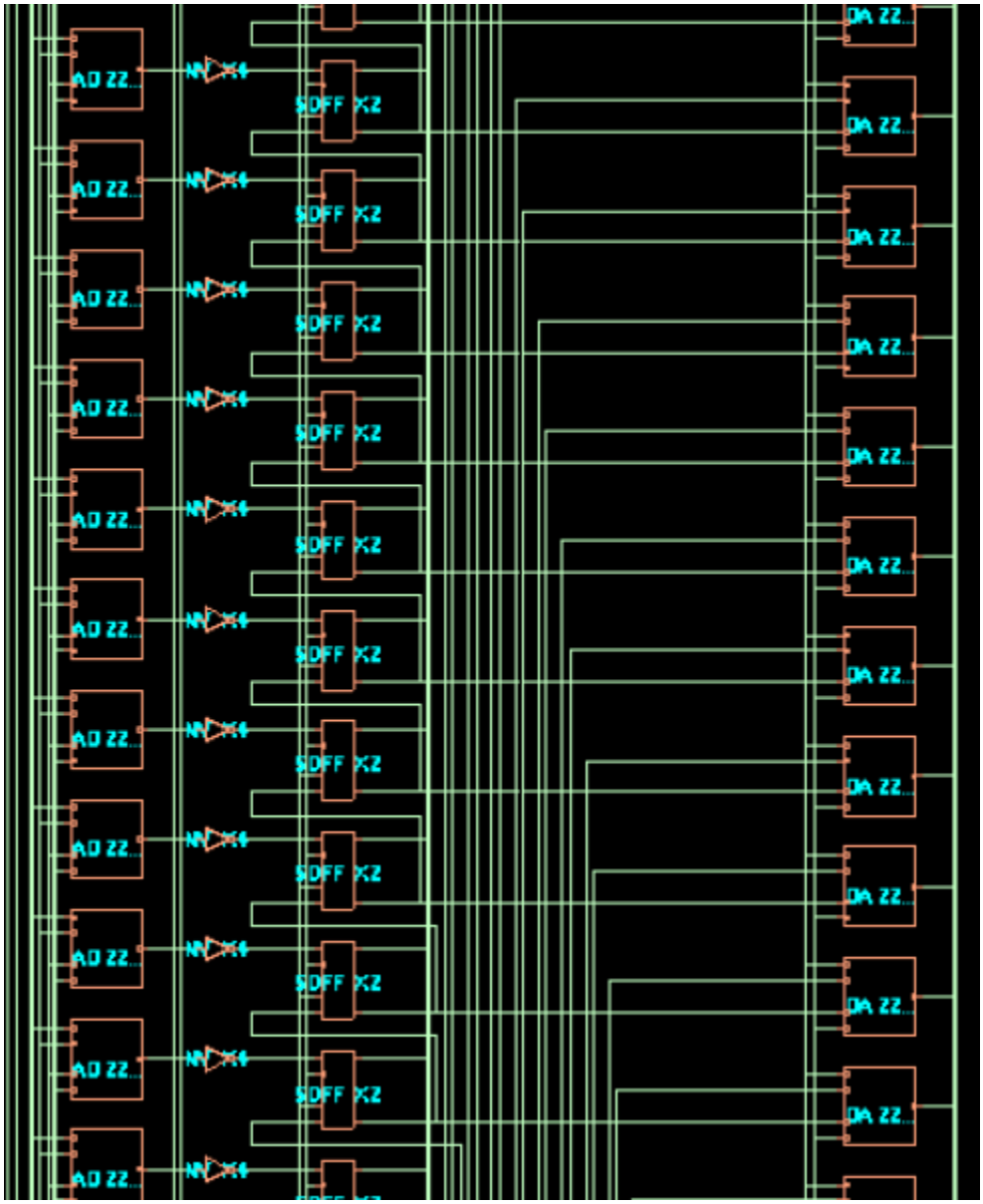
Static Timing Analysis (after DFT)

Schematic

In the post-DFT schematic, scan cells can be seen.



Zoomed section of schematic:



Graph Based Analysis

The hold slack is positive but the setup slack is negative. This design requires more optimization or a lower clock frequency (around 25 ns time period).

```
Path 1: VIOLATED Setup Check with Pin ID_EX_opcode_reg[6]/CK
Endpoint:   ID_EX_opcode_reg[6]/SE (^) checked with  leading edge of 'clk'
Beginpoint: scan_en                (^) triggered by  leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time          0.500
- Setup                         4.355
+ Phase Shift                  10.000
- Uncertainty                   0.020
= Required Time                 6.125
- Arrival Time                 13.091
= Slack Time                   -6.966
     Clock Rise Edge                      0.000
     + Input Delay                        0.300
     + Drive Adjustment                  12.291
     + Source Insertion Delay             0.500
     = Beginpoint Arrival Time           13.091
      ------------------------------------------------------------------
      Instance             Arc        Cell     Delay  Arrival  Required
                                                      Time     Time
      ------------------------------------------------------------------
      -                    scan_en ^  -        -      13.091   6.125
      ID_EX_opcode_reg[6]  SE ^       SDFF_X1  0.000  13.091   6.125
      ------------------------------------------------------------------
```

```
Path 1: MET Hold Check with Pin EX_MEM_alu_result_reg[0]/CK
Endpoint:   EX_MEM_alu_result_reg[0]/SI (^) checked with  leading edge of 'clk'
Beginpoint: DFT_sdi_1                   (^) triggered by  leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time          0.500
+ Hold                          0.015
+ Phase Shift                   0.000
+ Uncertainty                   0.020
= Required Time                 0.535
  Arrival Time                  0.839
  Slack Time                    0.304
     Clock Rise Edge                      0.000
     + Input Delay                        0.300
     + Drive Adjustment                   0.039
     + Source Insertion Delay             0.500
     = Beginpoint Arrival Time            0.839
      ------------------------------------------------------------------------
      Instance                 Arc          Cell     Delay  Arrival  Required
                                                             Time     Time
      ------------------------------------------------------------------------
      -                        DFT_sdi_1 ^  -        -      0.839    0.535
      EX_MEM_alu_result_reg[0] SI ^         SDFF_X2  0.000  0.839    0.535
      ------------------------------------------------------------------------
```

There are many setup violations but there are no untested paths.

TIMING CHECK COVERAGE SUMMARY

Check Type	No. of Checks	Met	Violated	Untested
ExternalDelay (Early)	124	124 (100%)	0 (0%)	0 (0%)
ExternalDelay (Late)	124	124 (100%)	0 (0%)	0 (0%)
Hold	918	918 (100%)	0 (0%)	0 (0%)
PulseWidth	612	612 (100%)	0 (0%)	0 (0%)
Setup	918	592 (64%)	326 (35%)	0 (0%)

Path Based Analysis

The hold slack is positive but the setup slack is negative. This design requires more optimization or a lower clock frequency (around 25 ns time period).

```
Path 1: VIOLATED Setup Check with Pin ID_EX_opcode_reg[6]/CK
Endpoint:   ID_EX_opcode_reg[6]/SE (^) checked with  leading edge of 'clk'
Beginpoint: scan_en                (^) triggered by  leading edge of 'clk'
Path Groups: {clk}
Retime Analysis { Data Path-Slew }
Other End Arrival Time          0.500
- Setup                         4.355
+ Phase Shift                  10.000
- Uncertainty                   0.020
= Required Time                 6.125
- Arrival Time                 13.091
= Slack Time                   -6.966
= Slack Time(original)         -6.966
     Clock Rise Edge                     0.000
     + Input Delay                       0.300
     + Drive Adjustment                 12.291
     + Source Insertion Delay            0.500
     = Beginpoint Arrival Time          13.091
      ------------------------------------------------------------------
      Instance             Arc        Cell     Retime  Arrival  Required
                                                Delay   Time     Time
      ------------------------------------------------------------------
      -                    scan_en ^  -        -       13.091   6.125
      ID_EX_opcode_reg[6]  -          SDFF_X1  0.000   13.091   6.125
      ------------------------------------------------------------------
```

```
Path 1: MET Hold Check with Pin EX_MEM_alu_result_reg[0]/CK
Endpoint:   EX_MEM_alu_result_reg[0]/SI (^) checked with  leading edge of 'clk'
Beginpoint: DFT_sdi_1                   (^) triggered by  leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time          0.500
+ Hold                          0.015
+ Phase Shift                   0.000
+ Uncertainty                   0.020
= Required Time                 0.535
  Arrival Time                  0.839
  Slack Time                    0.304
     Clock Rise Edge                     0.000
     + Input Delay                       0.300
     + Drive Adjustment                  0.039
     + Source Insertion Delay            0.500
     = Beginpoint Arrival Time           0.839
      ------------------------------------------------------------------------
      Instance                   Arc          Cell     Delay  Arrival  Required
                                                           Time     Time
      ------------------------------------------------------------------------
      -                          DFT_sdi_1 ^  -        -      0.839    0.535
      EX_MEM_alu_result_reg[0]   SI ^         SDFF_X2  0.000  0.839    0.535
      ------------------------------------------------------------------------
```

There are many setup violations but there are no untested paths.

TIMING CHECK COVERAGE SUMMARY

Check Type	No. of Checks	Met	Violated	Untested
ExternalDelay (Early)	124	124 (100%)	0 (0%)	0 (0%)
ExternalDelay (Late)	124	124 (100%)	0 (0%)	0 (0%)
Hold	918	918 (100%)	0 (0%)	0 (0%)
PulseWidth	612	612 (100%)	0 (0%)	0 (0%)
Setup	918	592 (64%)	326 (35%)	0 (0%)

Issues and Learnings

- In verilog code, arrays are not synthesizable and should be replaced with address and data ports.
- Asynchronous inputs should not be constrained with respect to the clock.
- Using root and instance attributes to avoid optimizing parts of the design.
- When using slow.lib, the area of all instances and cells is reported as 0.
- There are differences in the timing analysis done by genus and tempus. Genus does not report setup violations whereas tempus does.
- In the conformal script generated during synthesis, the command **set_analyze_option -auto -report_map** has to be commented out. It does not work in my version of the tool. Also, the **exit -f** command at the end has to be replaced by **pause**, otherwise the conformal window closes immediately after running the do file.
- Correcting unconnected pins in a design.
- To perform PBA instead of GBA, add flag -retime path_slew_propagation to report_timing command.
- A new constraint file needs to be created for DFT to include the new test mode and shift enable ports.
- DFT (in my version of the tool) requires the command **replace_scan** before **connect_scan_chains.** Otherwise, flip-flops are marked as non-scannable. Also, DFT only works for FreePDK45_lib_v1.0_typical_scan.lib and not for slow.lib (in my case).
- This design requires more optimization and a high clock period.