

LAPORAN UAS ELEKTRONIKA DAYA



Disusun oleh:

Nama : Rizal Kurniawan Saputra

Program Studi : Teknik Elektro

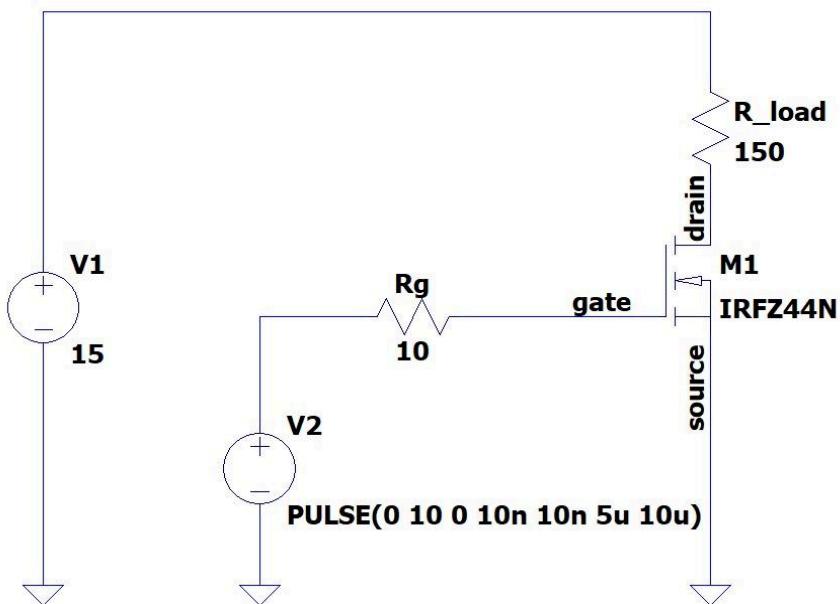
NIM : 22/496542/TK/54416

**DEPARTEMEN TEKNIK ELEKTRO & TEKNOLOGI INFORMASI
FAKULTAS TEKNIK UNIVERSITAS GADJAH MADA
YOGYAKARTA**

2025

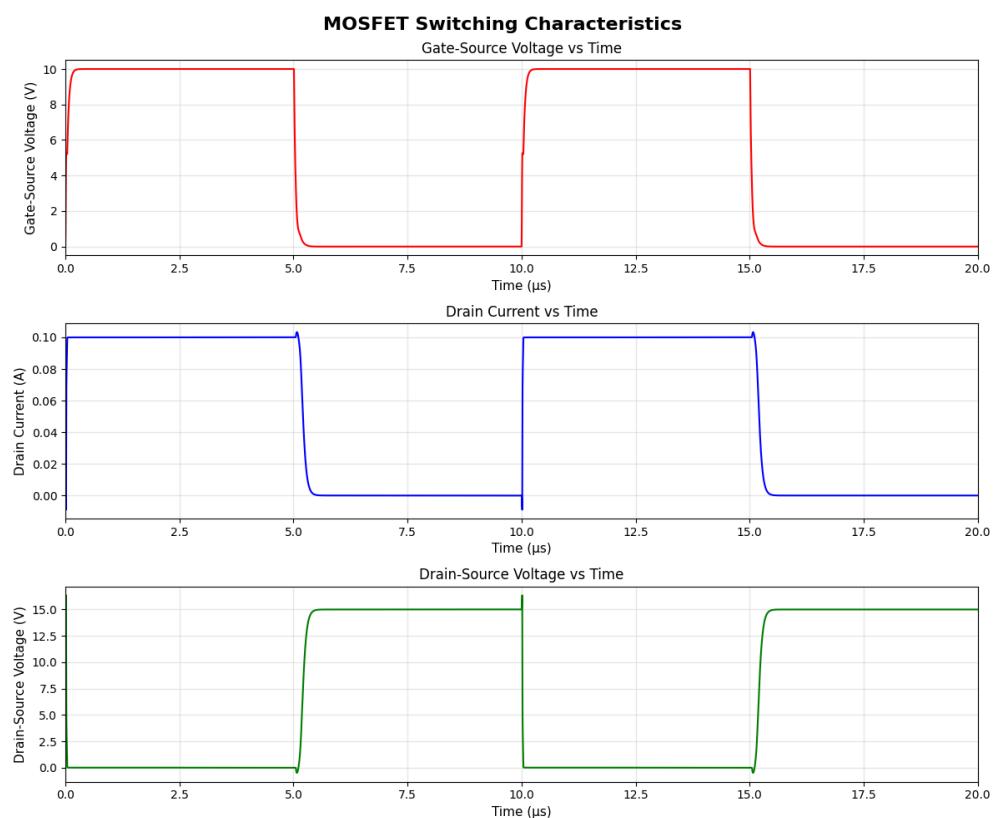
Task 1

a. Schematic Low Side Driving

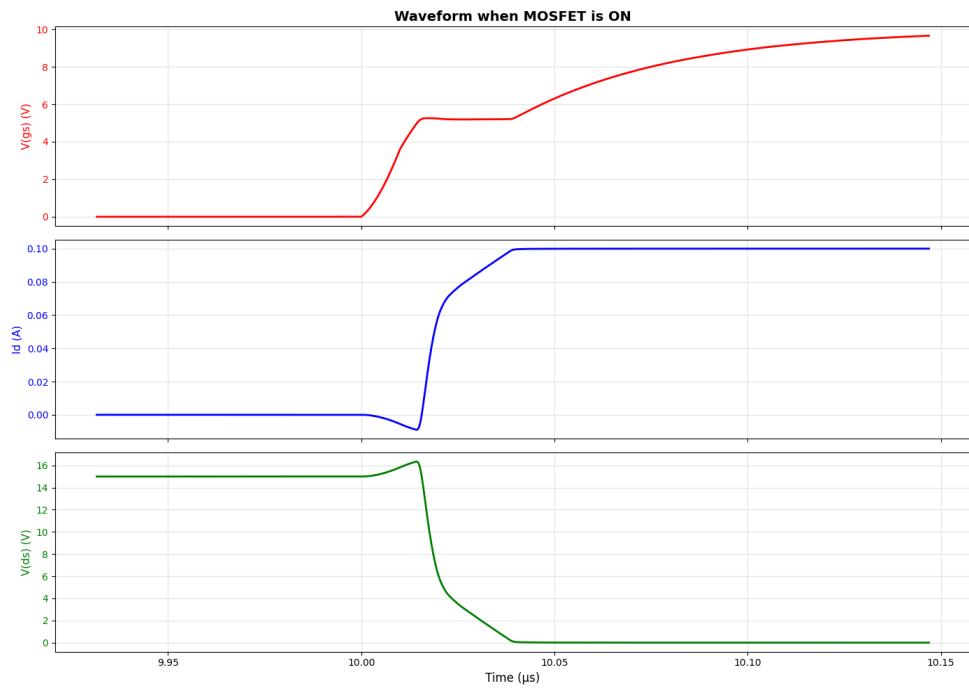


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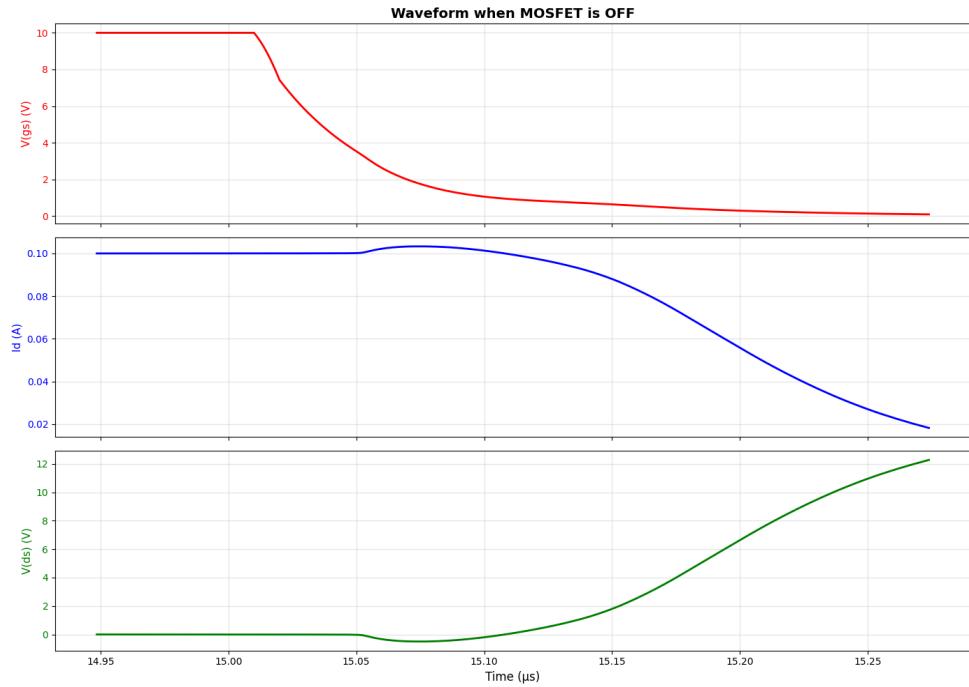
Simulation Results:



- Waveform when the MOSFET is ON

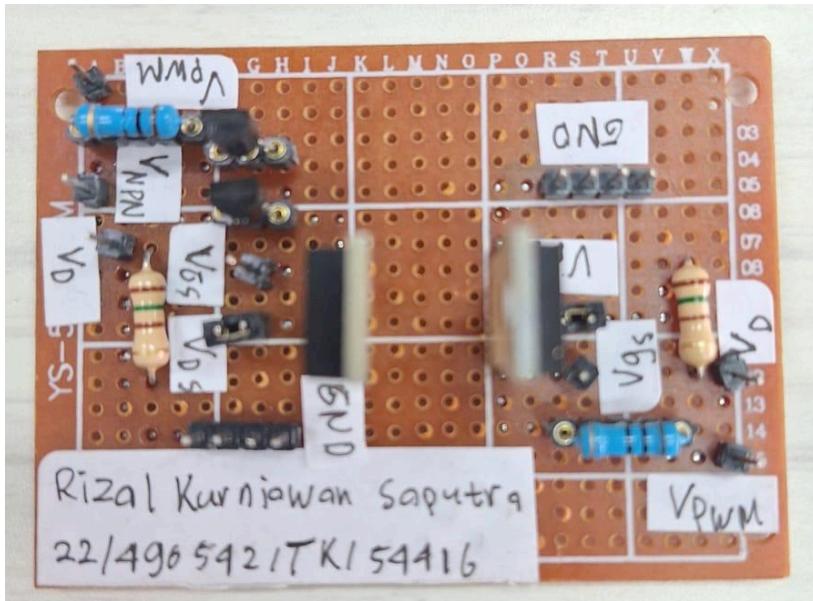


- Waveform when the MOSFET is OFF



Experiments Results:

- Hardware



- Waveform Experiment

Yellow line : V_{GS}

Blue line : V_{DS}



$$R_g = 10 \Omega$$

$$R_g = 100 \Omega$$

- Waveform when the MOSFET is ON and OFF

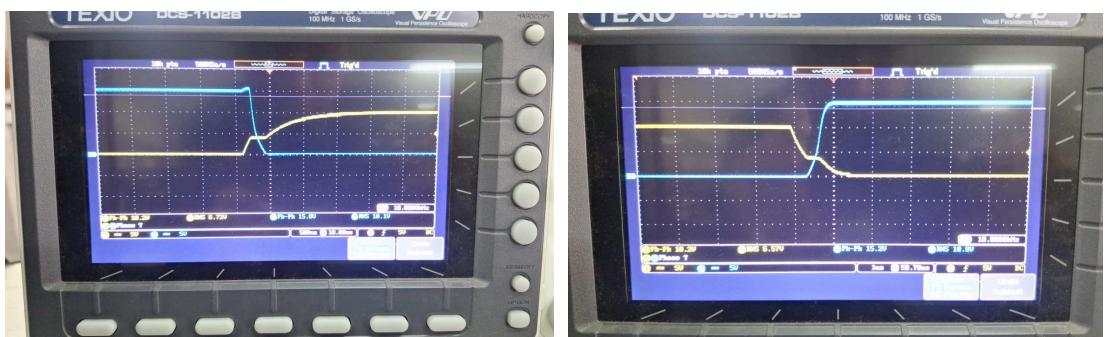
Yellow line : V_{GS}

Blue line : V_{DS}



ON ($R_g = 10 \Omega$)

OFF ($R_g = 10 \Omega$)



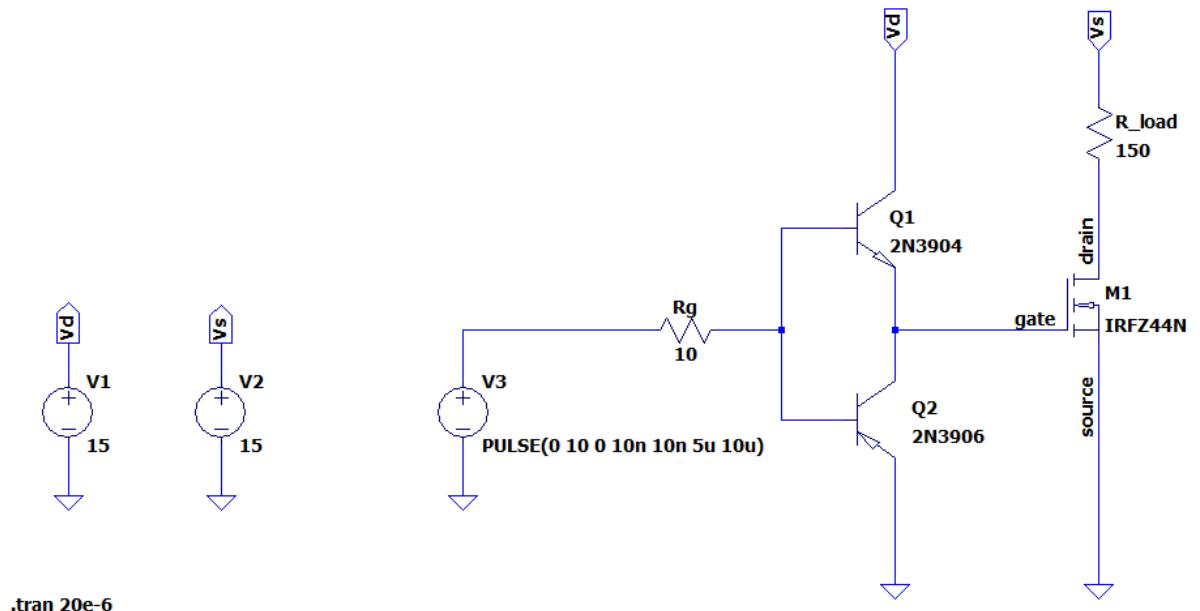
ON ($R_g = 100 \Omega$)

OFF ($R_g = 100 \Omega$)

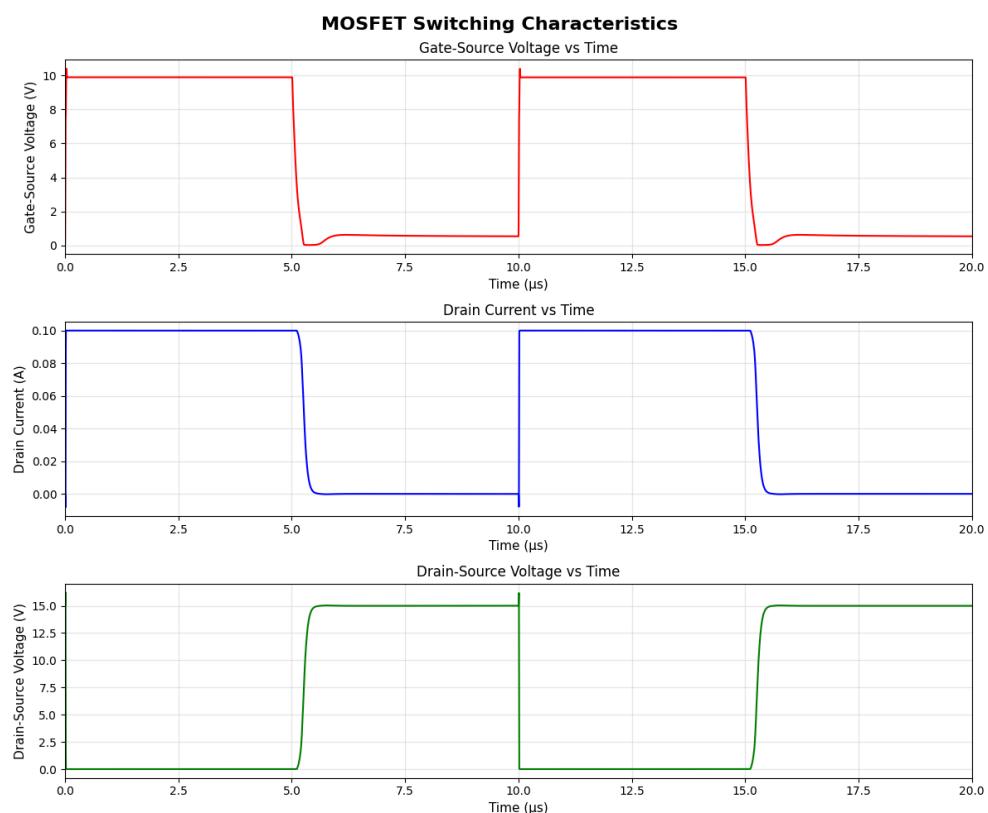
- Analysis Experiment

Based on the experimental results, the gate resistance value significantly affects the switching speed of the MOSFET. As the value of R_g increases, the duration of the Miller Plateau becomes longer, whereas a smaller R_g results in a shorter Miller Plateau. This behavior can be clearly observed by comparing the results for $R_g=10 \Omega$ and $R_g=100 \Omega$. A longer Miller Plateau leads to a longer switching transition time, which consequently increases the switching losses.

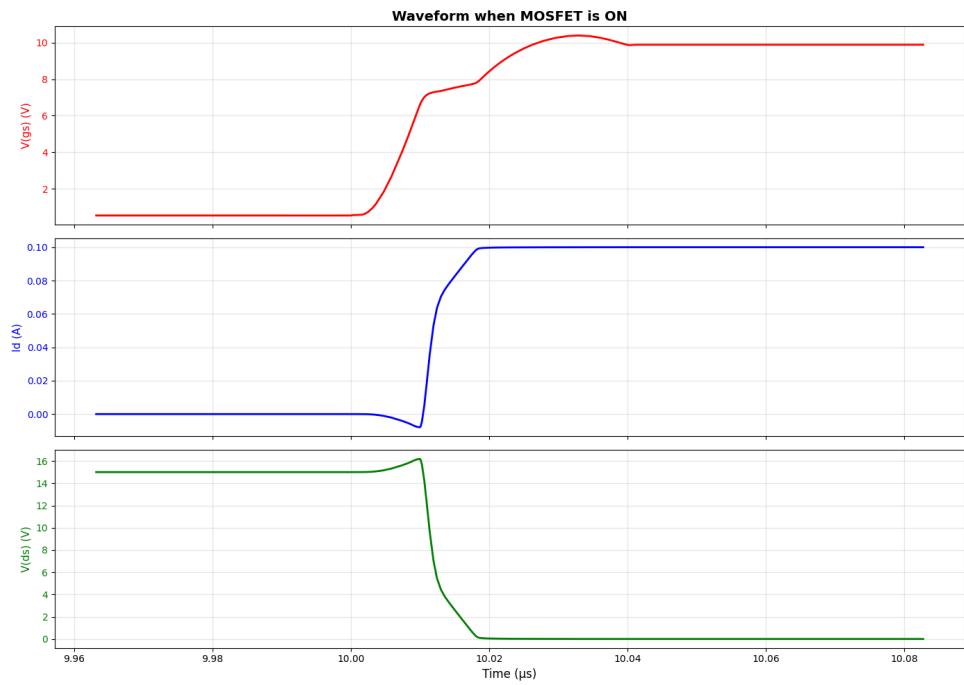
b. Schematic Low-Side Totem Pole



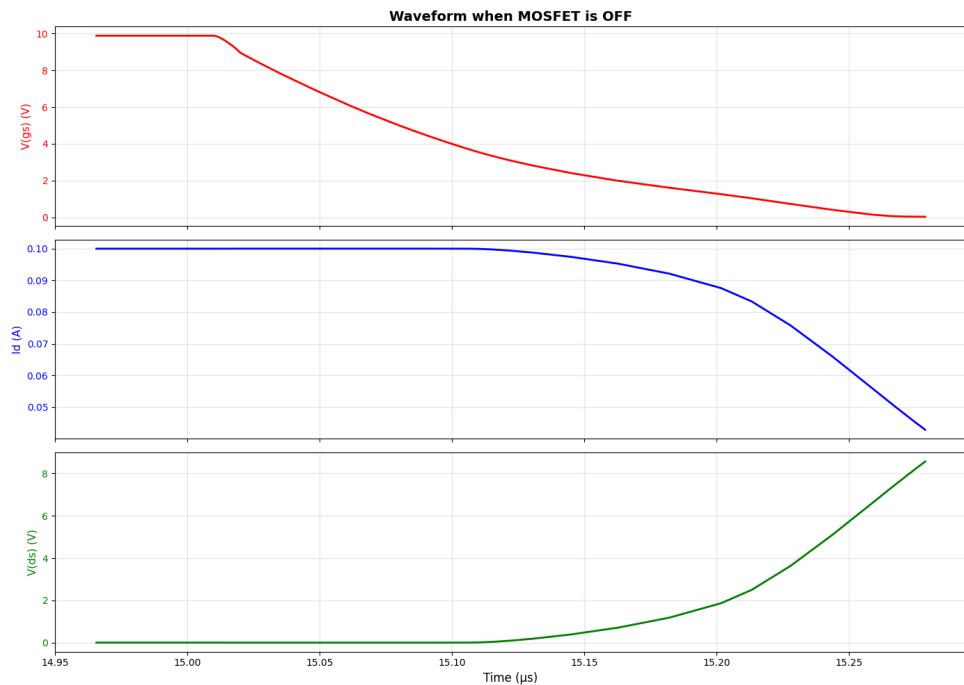
Simulation Results:



- Waveform when the MOSFET is ON



- Waveform when the MOSFET is OFF

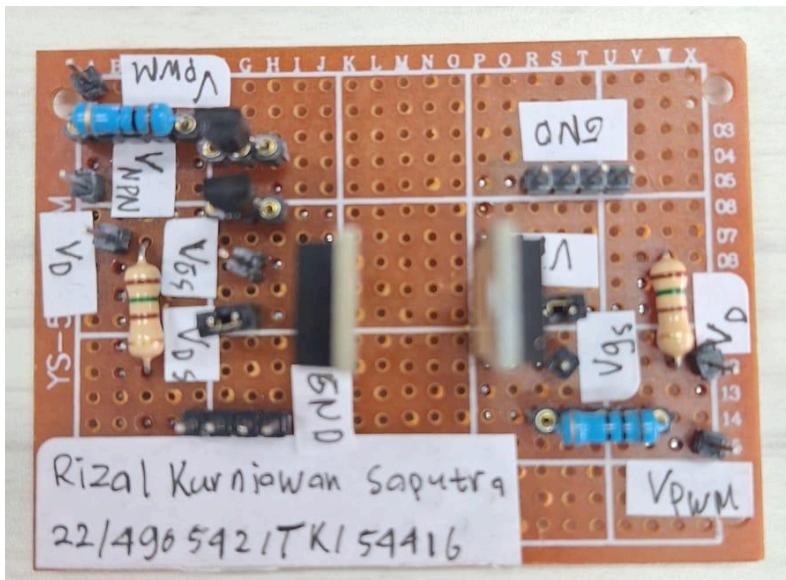


Experiment Results:

- Switching Characteristic of Totem-Pole at $R_g = 10 \Omega$

Rise time	10 ns
Turn on plateau time	13.4 ns
Fall time	23.55 ns
Turn off plateau time	25 ns
Overshoot Experiment ($R_g = 10 \Omega$)	3.8 V
Overshoot Experiment ($R_g = 1 k\Omega$)	3.5 V
Overshoot Experiment ($R_g = 3.3 k\Omega$)	2.4 V

- Hardware



- Waveform Experiment

Yellow line : V_{GS}

Blue line : V_{DS}



$R_g = 10 \Omega$



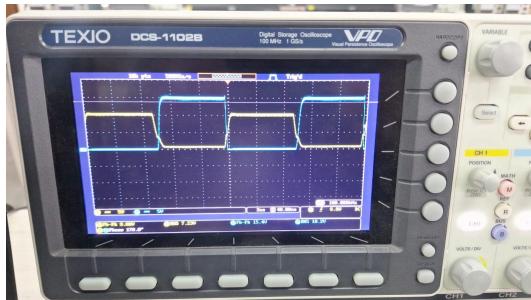
$R_g = 100 \Omega$



$R_g = 1 k\Omega$



$R_g = 3.3 k\Omega$



$R_g = 10 k\Omega$

- Waveform when the MOSFET is ON and OFF

Yellow line : V_{GS}

Blue line : V_{DS}



ON ($R_g = 10 \Omega$)

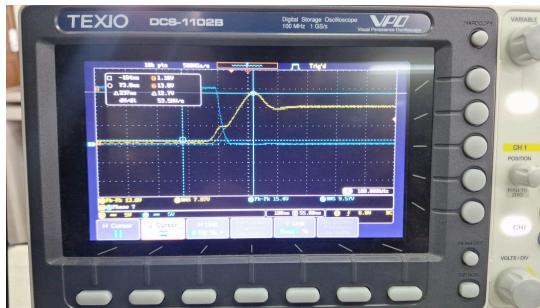


OFF ($R_g = 10 \Omega$)

- Overshoot V_{gs}

Yellow line : V_{GS}

Blue line : V_{DS}



$$R_g = 10 \Omega$$



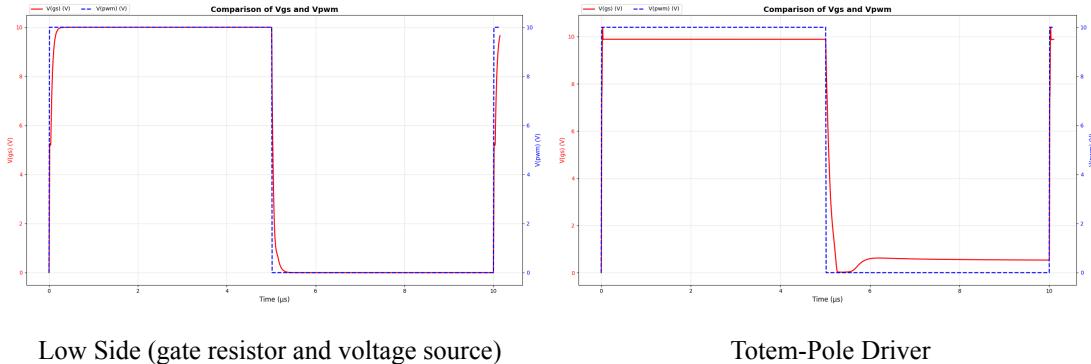
$$R_g = 3.3 \text{ k}\Omega$$

- Analysis Experiment:

Based on the experimental results, the gate resistance R_g affects the switching speed of the MOSFET in the Totem-Pole configuration. In addition, R_g acts as a damping element that suppresses resonant behavior caused by cable and circuit parasitic effects. As shown in the figure above, increasing R_g results in more heavily damped voltage and current oscillations. However, this oscillation damping involves a trade-off, as a higher R_g slows down the switching process and consequently increases the switching losses. Overall, the Totem-Pole configuration provides better switching performance compared to a simple gate resistor and voltage source configuration.

Analysis:

- How does the totem-pole driver improve MOSFET switching performance compared to using only a gate resistor and voltage source?



The Totem-Pole (Push-Pull) driver circuit consists of a complementary pair of transistors (NPN and PNP) configured as an emitter follower. The main advantage of this topology compared to the simple driving method (using only a gate resistor and a voltage source) lies in its very low output impedance, enabling two critical operating modes:

- Very Strong Current Source (via NPN): Capable of instantly injecting a large current into the MOSFET gate during the Turn-On process.
- Very Strong Current Sink (via PNP): Capable of drawing a large current from the MOSFET gate to ground during the Turn-Off process.

A MOSFET has intrinsic capacitance ($C_{iss} = C_{gs} + C_{gd}$) that must be charged for the MOSFET to turn on and discharged for it to turn off. According to the fundamental capacitor law:

$$I = C \frac{dV}{dt} \Rightarrow \frac{dV}{dt} = \frac{I}{C}$$

The rate of change of the gate voltage, $\frac{dV}{dt}$, which represents the switching speed, is directly proportional to the current I. In a simple low-side driver that relies solely on a gate resistor (R_g), the charging current is passively limited by Ohm's law

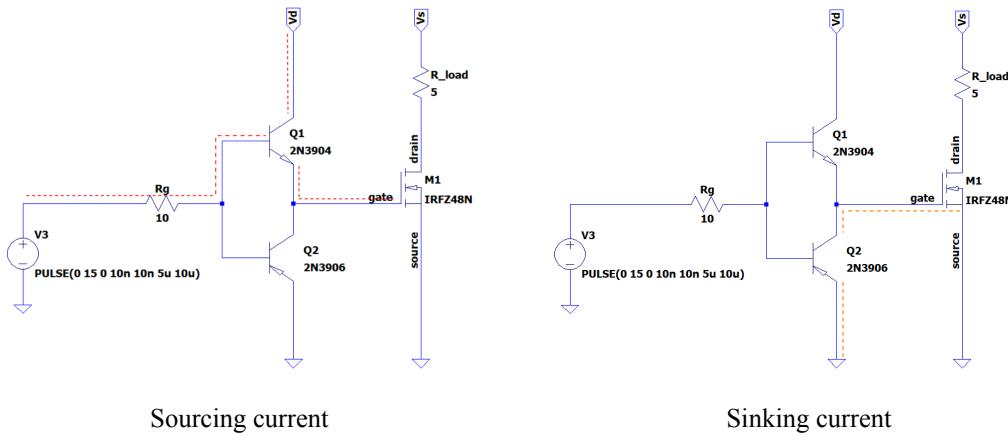
$$I_g = \frac{V_G - V_{GS}}{R_g}$$

In contrast, the Totem-Pole configuration acts as a current buffer. The NPN and PNP transistors provide extremely low-impedance paths, allowing much higher peak

currents to flow during the charging and discharging of C_{iss} (and to more effectively overcome the Miller effect on C_{rss}). As a result, the transition times (rise time and fall time) become significantly shorter, reducing switching losses and improving the overall system efficiency compared to the passive-resistor method.

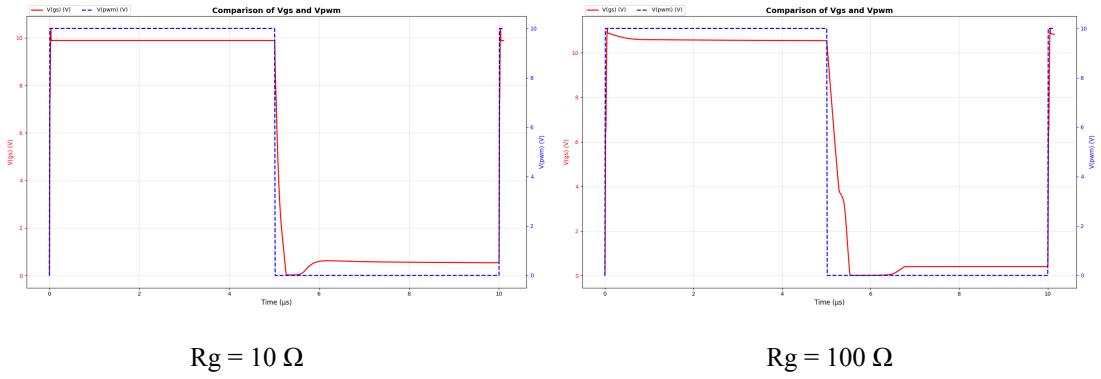
The difference in switching performance can be observed in the two figures above, where the Totem-Pole driver clearly demonstrates faster switching behavior compared to the low-side driver.

- Explain how the sourcing and sinking currents of the BJTs affect the switching speed.



The totem pole driver illustrated in the figure above as a push-pull current buffer designed to efficiently drive the power MOSFET (M1) using a complementary pair of Bipolar Junction Transistors. When the input pulse V_{gate} transitions to a high state, the NPN transistor (Q1) becomes forward-biased, creating a low-impedance path that sources current directly from the supply rail V_d into the MOSFET gate, as indicated by the red dashed line. This high sourcing current rapidly charges the MOSFET's internal gate capacitance, significantly reducing the rise time (t_r) and ensuring a fast turn-on. Conversely, when the input signal drops to zero, Q1 turns off and the PNP transistor (Q2) becomes active, providing a direct path to ground for the stored gate charge to drain, shown by the orange dashed line. This ability to sink current rapidly discharges the gate capacitance, minimizing the fall time (t_f) during turn-off. By maximizing both sourcing and sinking current capabilities, this topology effectively overcomes gate capacitance constraints, allowing the MOSFET to switch states quickly and minimizing power losses associated with the linear transition region.

- Analyze the effect of gate resistance R_g on:



(a) Switching speed

The gate resistance R_g determines the switching speed of a MOSFET. This is because R_g controls the magnitude of the current entering the gate according to Ohm's Law:

$$I_g = \frac{V_g - V_{GS}}{R_g}$$

When R_g is small, a larger current flows into the gate. This accelerates the charging and discharging of the input capacitance C_{iss} , resulting in faster switching times. Conversely, if R_g is large, it yields a smaller gate current, which slows down the switching process. The difference in switching performance can be observed in the two figures above. When $R_g = 100 \Omega$ is clearly demonstrates faster switching behavior compared to the $R_g = 10 \Omega$.

(b) dv/dt and di/dt

The time derivative of gate-source voltage is given by

$$\begin{aligned} I_g &= I_{gs} + I_{gd} \\ I_g &= C_{gs} \frac{dV_{GS}}{dt} + C_{gd} \frac{dV_{GS}}{dt} \\ I_g &= \frac{V_g - V_{GS}}{R_g} \\ \frac{dV_{GS}}{dt} &= \frac{V_g - V_{GS}}{R_g \times (C_{iss})} \end{aligned}$$

The time derivative of drain-current is summarized from [1]

$$\begin{aligned} I_D &= \frac{W\mu_0 C_{ox}}{2L} (V_{GS} - V_{TH})^2 (1 + \lambda(V_{GS} - V_{TH})) \\ \frac{dI_D}{dt} &= \frac{W\mu_0 C_{ox}}{2L} (V_{GS} - V_{TH}) (2 + 3\lambda(V_{GS} - V_{TH})) \frac{dV_{GS}}{dt} \\ V_{GS,off} &= V_{GG} e^{-t/(R_g C_{iss})} \end{aligned}$$

$$V_{GS,ON} = V_{GG} \left(1 - e^{-t/(R_g C_{iss})} \right)$$

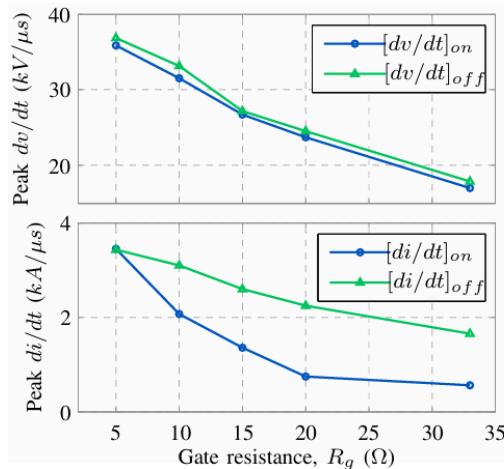
$$\frac{dI_{D,OFF}}{dt} = - \frac{W\mu_0 C_{OX} V_{GG}}{2LR_g C_{ISS}} x (2 + 3\lambda x) e^{-t/(R_g C_{iss})}$$

$$\frac{dI_{D,ON}}{dt} = \frac{W\mu_0 C_{OX} V_{GG}}{2LR_g C_{ISS}} y (2 + 3\lambda y) e^{-t/(R_g C_{iss})}$$

$$x = V_{GG} e^{-t/(R_g C_{iss})} - V_{TH}$$

$$y = V_{GG} \left(1 - e^{-t/(R_g C_{iss})} \right) - V_{TH}$$

Based on the equations above, the gate resistance has an inverse relationship with dv/dt and di/dt. When the gate resistance is increased, the rate of change of voltage and current decreases, resulting in slower switching behavior. This leads to higher switching voltage and current, which in turn increases the common-mode current and EMI generated in the system [High Switching Performance of 1700V, 50A SiC Power MOSFET over Si IGBT/BiMOSFET for Advanced Power Conversion Applications]. The characteristics of dv/dt and di/dt versus gate resistance are plotted in the figure below.



Turn OFF and Turn ON of dv/dt and di/dt of MOSFET in Variation of R_g [2]

(c) Switching energy/losses

Switching losses pada MOSFET umumnya disebabkan oleh switching losses dan conduction. Switching losses merupakan kerugian daya akibat switch ON OFF pada gate MOSFET. Sedangkan conduction losses merupakan kerugian daya akibat

MOSFET dalam keadaan conduct atau power MOSFET dalam kondisi ON.

The derivation of switching energy losses is summarized from [3]

- **Switching Losses**

$$E_{on} = \frac{1}{2}V_d I_o t_{on}$$

$$E_{off} = \frac{1}{2}V_d I_o t_{off}$$

Time period t_{on} and t_{off} are determined as,

$$t_{on} = \frac{Q}{I_{Gon}}$$

$$t_{off} = \frac{Q}{I_{Goff}}$$

And gate current when MOSFET ON OFF are determined as,,

$$I_{Gon} = \frac{V_{gs} - V_{PL}}{R_G}$$

$$I_{Goff} = \frac{V_{PL}}{R_G}$$

- **Conduction Losses**

$$E_{C_{ds}} = \frac{1}{2}C_{ds} V_d^2$$

- **Total Losses**

$$P_{sw} = \left(E_{on} + E_{off} + E_{C_{ds}} \right) \cdot f_{sw}$$

$$P_{sw} = \left(\frac{1}{2}V_d I_o \frac{R_G Q}{V_{gs} - V_{PL}} + \frac{1}{2}V_d I_o \frac{R_G Q}{V_{PL}} + \frac{1}{2}C_{ds} V_d^2 \right) \cdot f_{sw}$$

$$Q = Q_{gs} + Q_g$$

From the equation above, the gate resistance has a direct relationship with the switching energy losses. Increasing the gate resistance leads to higher switching energy losses, whereas reducing the gate resistance results in lower switching energy losses.

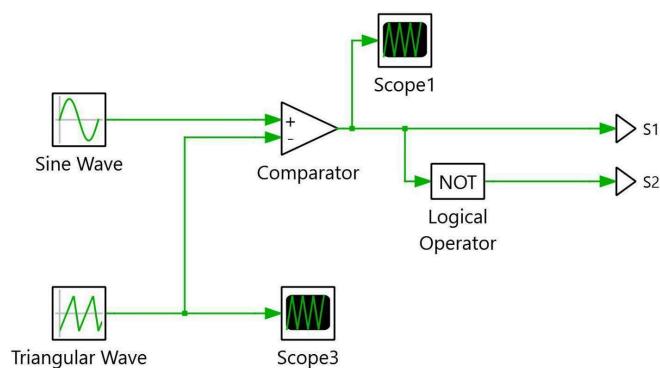
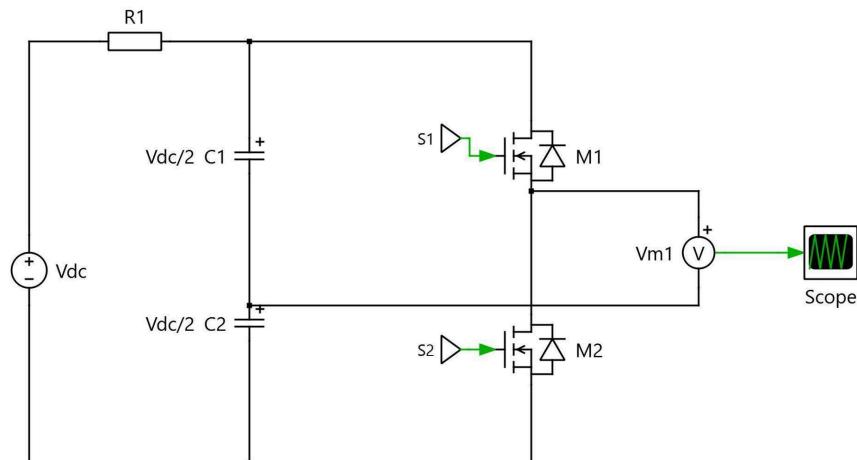
Task 2

- Plot Output Voltage in Time and Frequency Domains

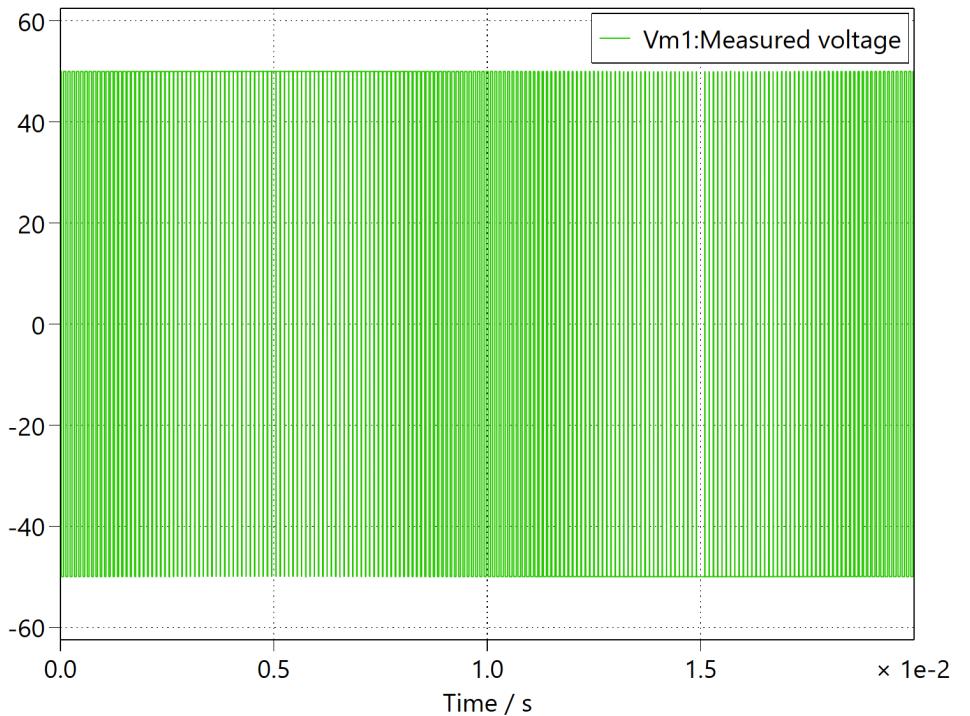
a. Half-bridge single-phase inverter

Specification:

Vdc	100 V
fsw	10 kHz
D	50 %
R	1 Ω
C1	1 μF
C2	1 μF
Vout	± 50 V

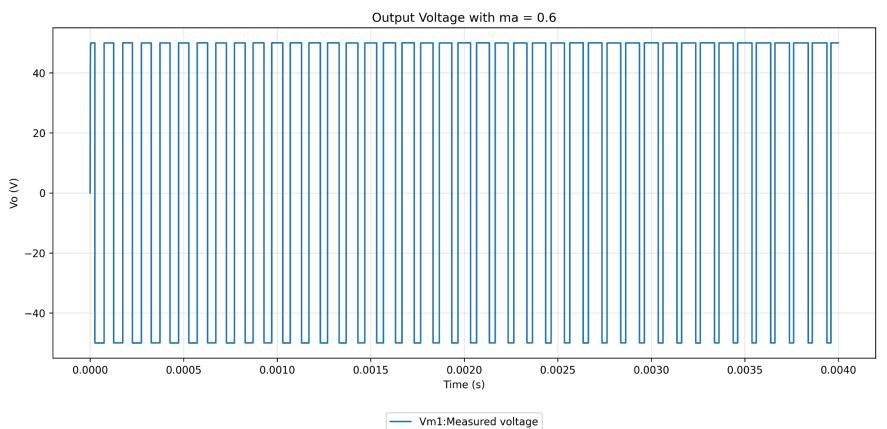


- 1) Generate the switching waveforms of the output voltage $v_o(t)$ using SPWM

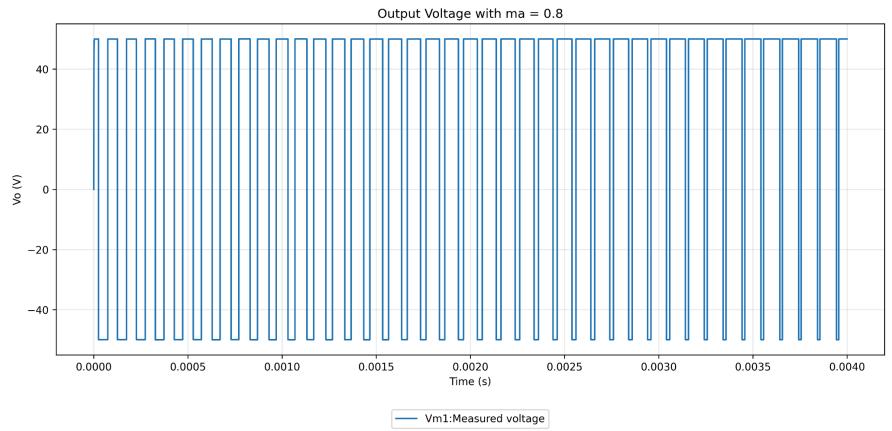


- 2) Plot the time-domain waveform of the output voltage at different modulation indices ma (e.g., 0.6, 0.8, 1.0)

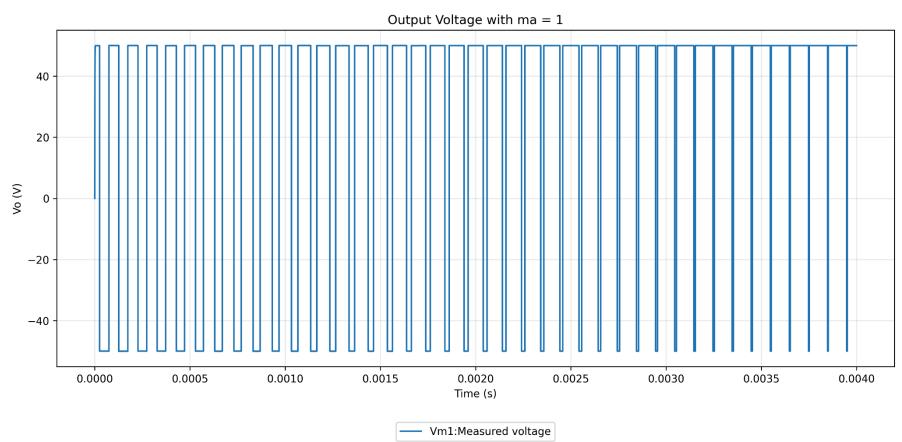
- $ma = 0.6$



- $ma = 0.8$

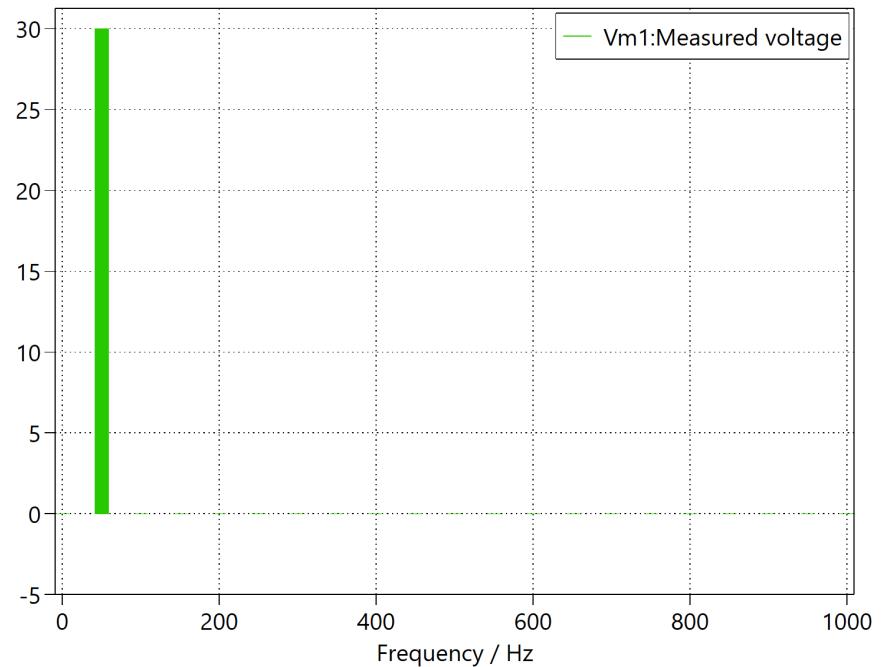


- $ma = 1$

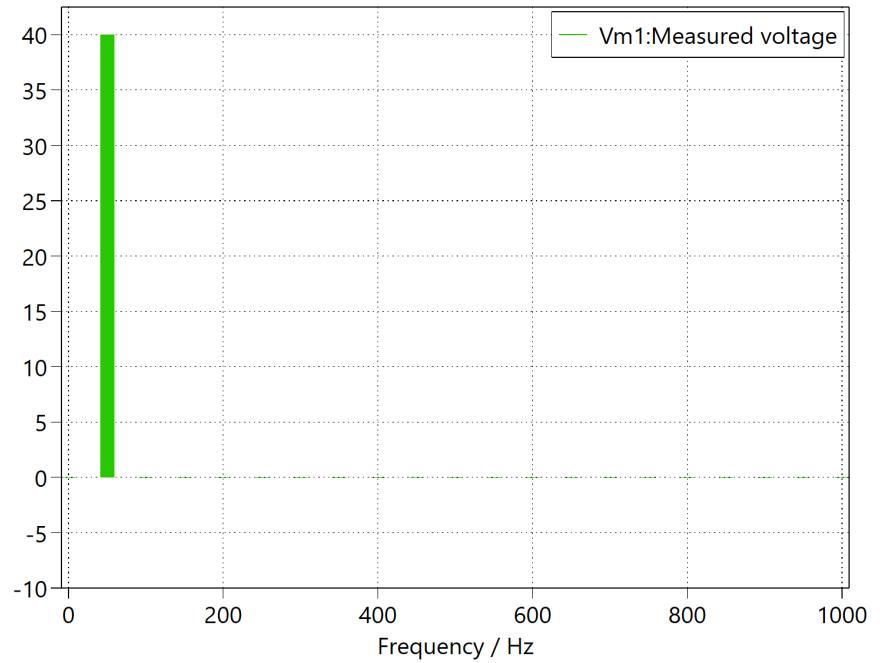


3) Obtain the frequency-domain representation using FFT

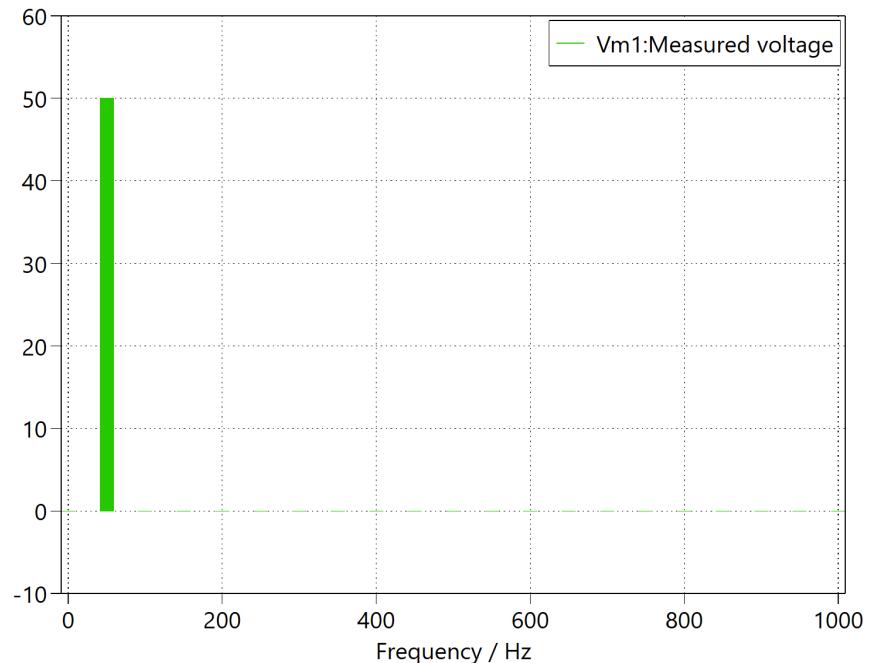
- $ma = 0.6$



- $ma = 0.8$



- $ma = 1$

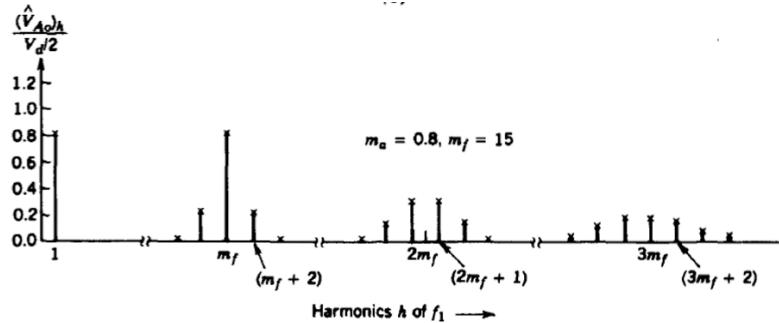


- Fundamental component: The fundamental component is located at the first harmonic, which corresponds to a frequency of 50 Hz. The value of this fundamental component represents by

$$(V_o) = ma (V_d/2)$$

with $ma = \frac{V_{control}}{V_{tri}} = \frac{\text{peak amplitude of the control signal}}{\text{peak amplitude of the triangular signal}}$

- Dominant switching harmonics:



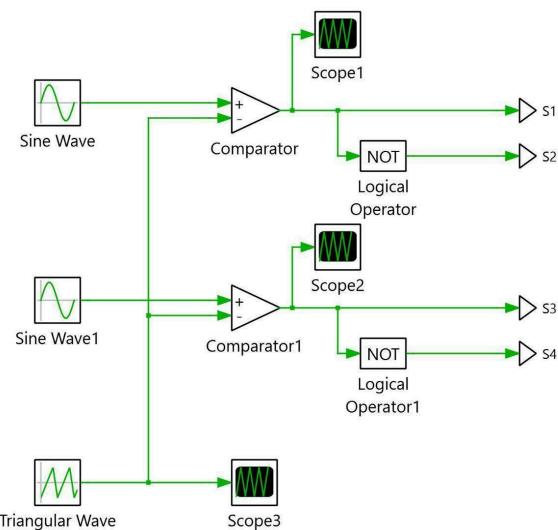
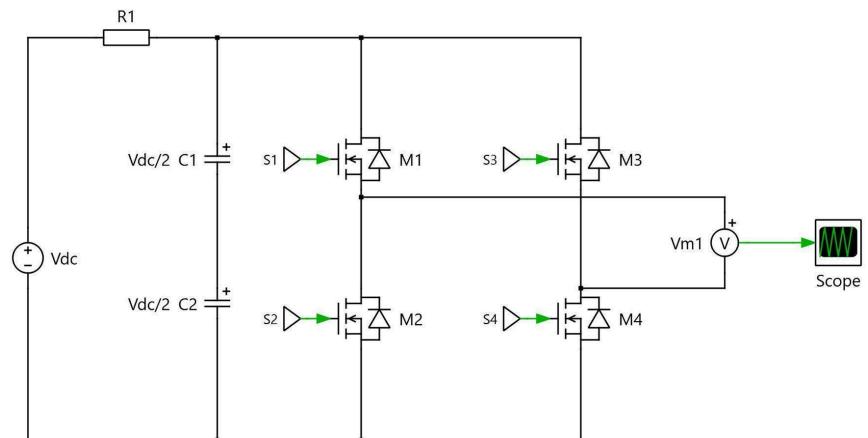
Dominant switching harmonics appear at the switching (or modulation) frequency and in the frequency range surrounding it. In addition, significant harmonic components also occur at the multiples of the switching frequency (m_f , $2m_f+1$, $3m_f$, $3m_f+2$ and so on), which can be seen from the figure above.

with $m_f = \frac{f_{sw}}{f_1} = \frac{\text{switching or carrier frequency}}{\text{fundamental frequency}}$

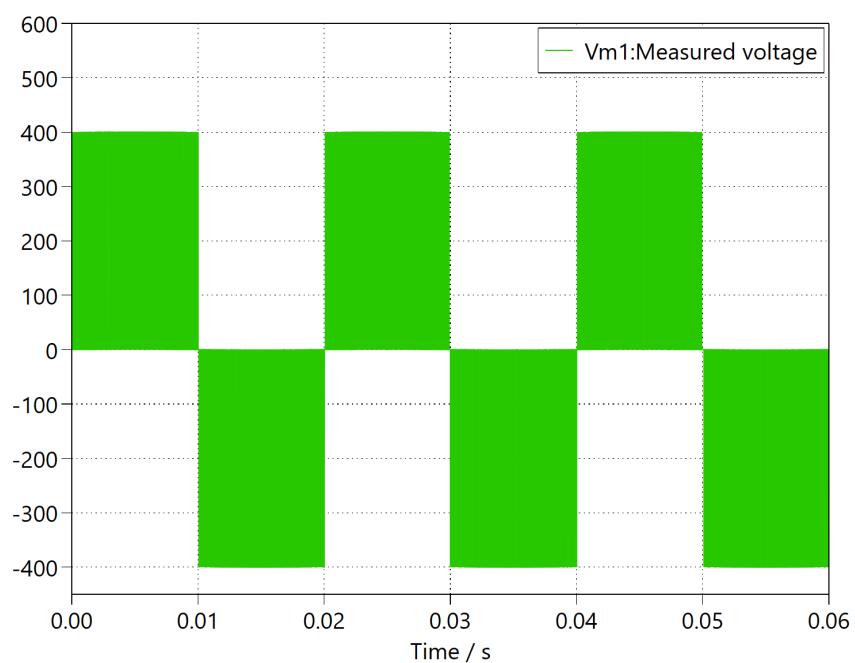
b. Full-bridge single-phase inverter

Specification:

Vdc	400 V
fsw	10 kHz
D	50 %
R	1 Ω
C1	1 μF
C2	1 μF
Vout	± 400 V

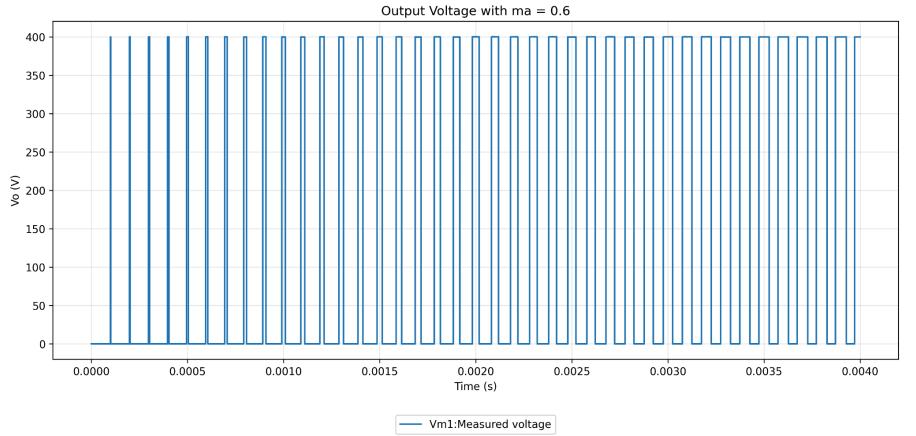


- 1) Generate the switching waveforms of the output voltage $v_o(t)$ using SPWM

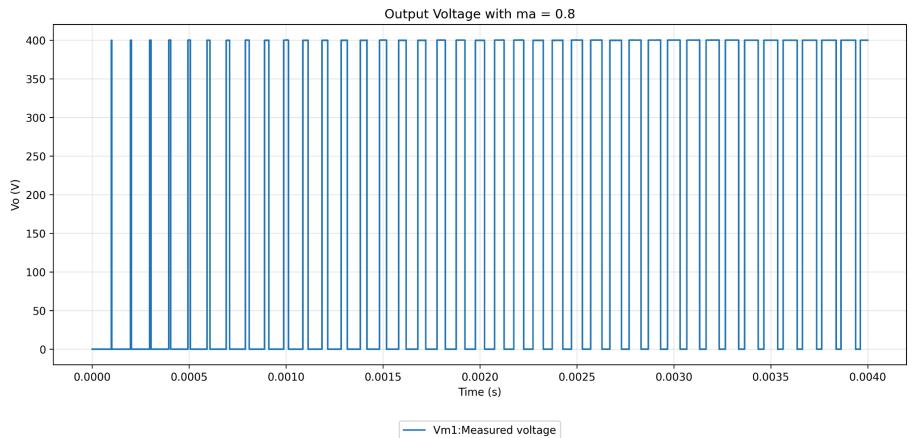


- 2) Plot the time-domain waveform of the output voltage at different modulation indices ma (e.g., 0.6, 0.8, 1.0)

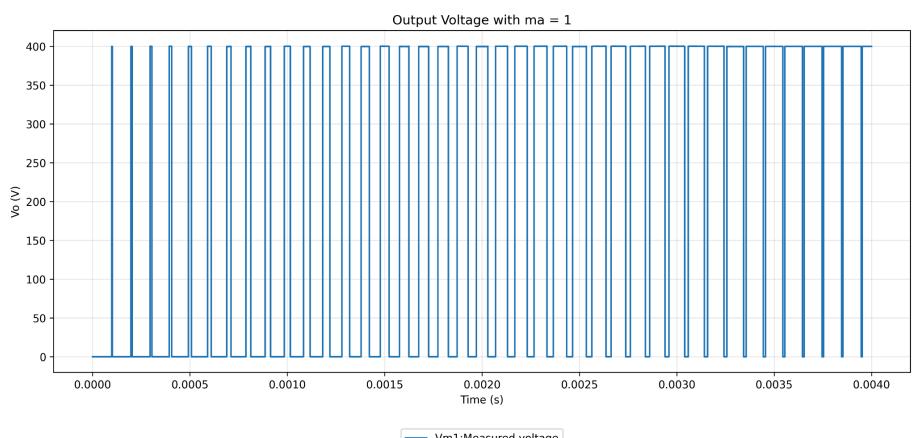
- $ma = 0.6$



- $ma = 0.8$

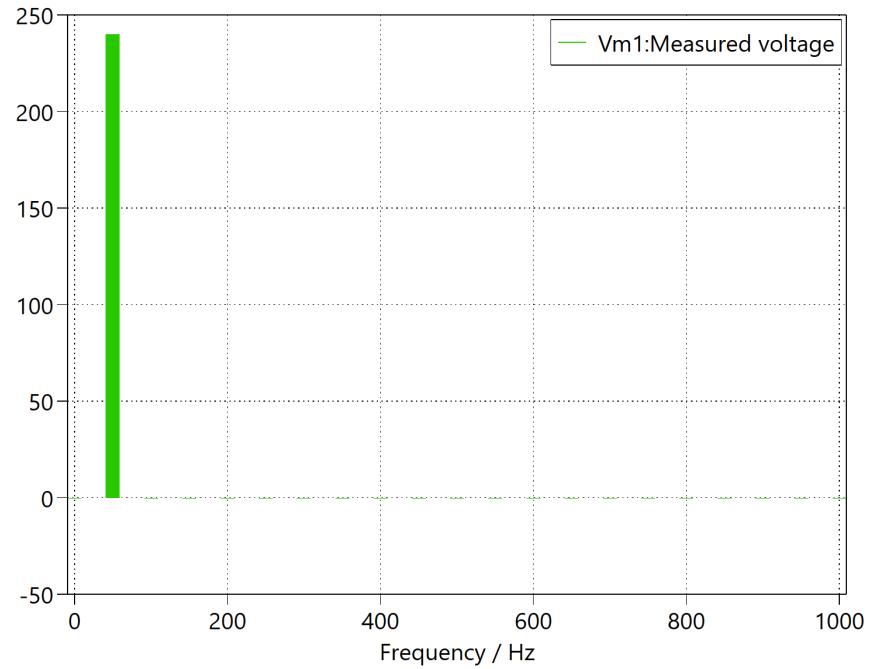


- $ma = 1$

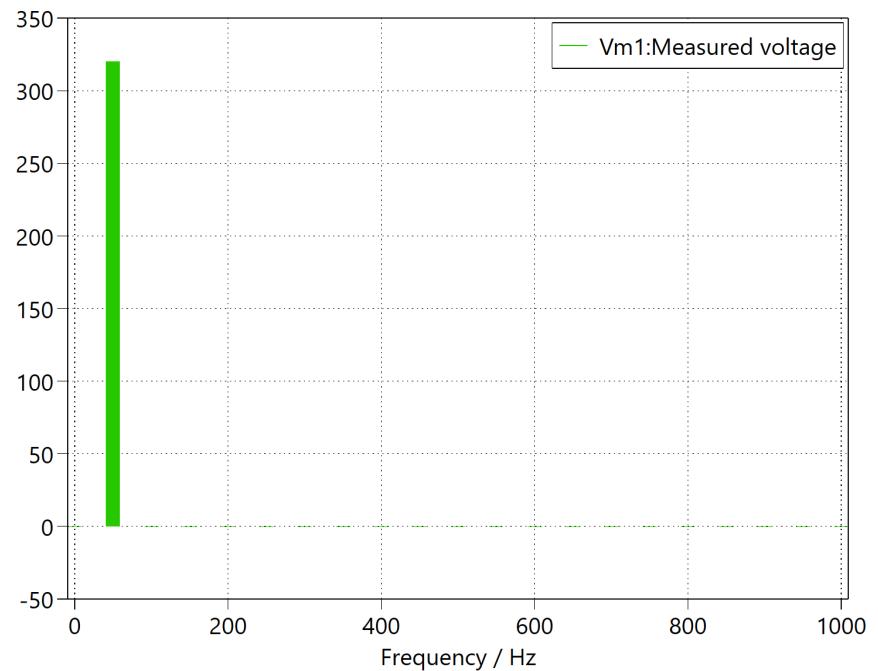


- 3) Obtain the frequency-domain representation using FFT

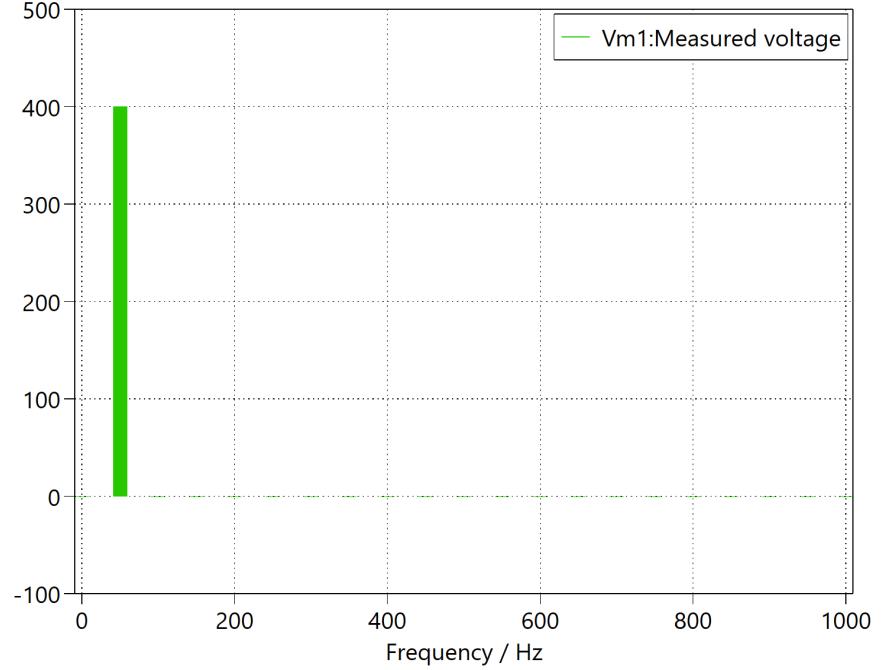
- $ma = 0.6$



- $ma = 0.8$



- $ma = 1$

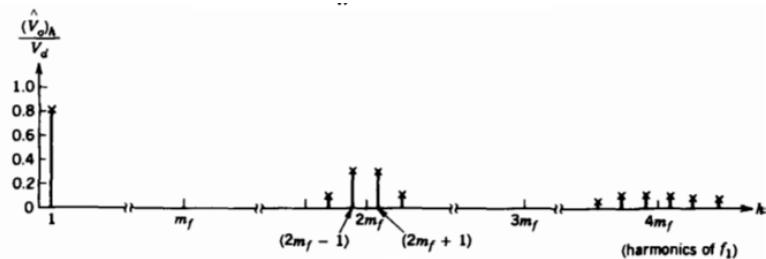


- Fundamental component: The fundamental component is located at the first harmonic, which corresponds to a frequency of 50 Hz. The value of this fundamental component represents by

$$(V_o) = ma (V_d)$$

with $ma = \frac{V_{control}}{V_{tri}} = \frac{\text{peak amplitude of the control signal}}{\text{peak amplitude of the triangular signal}}$

- Dominant switching harmonics:



Dominant switching harmonics appear at the switching (or modulation) frequency and in the frequency range surrounding it. In addition, significant harmonic components also occur at the multiples of the switching frequency ($2mf-1$, $2mf+1$,

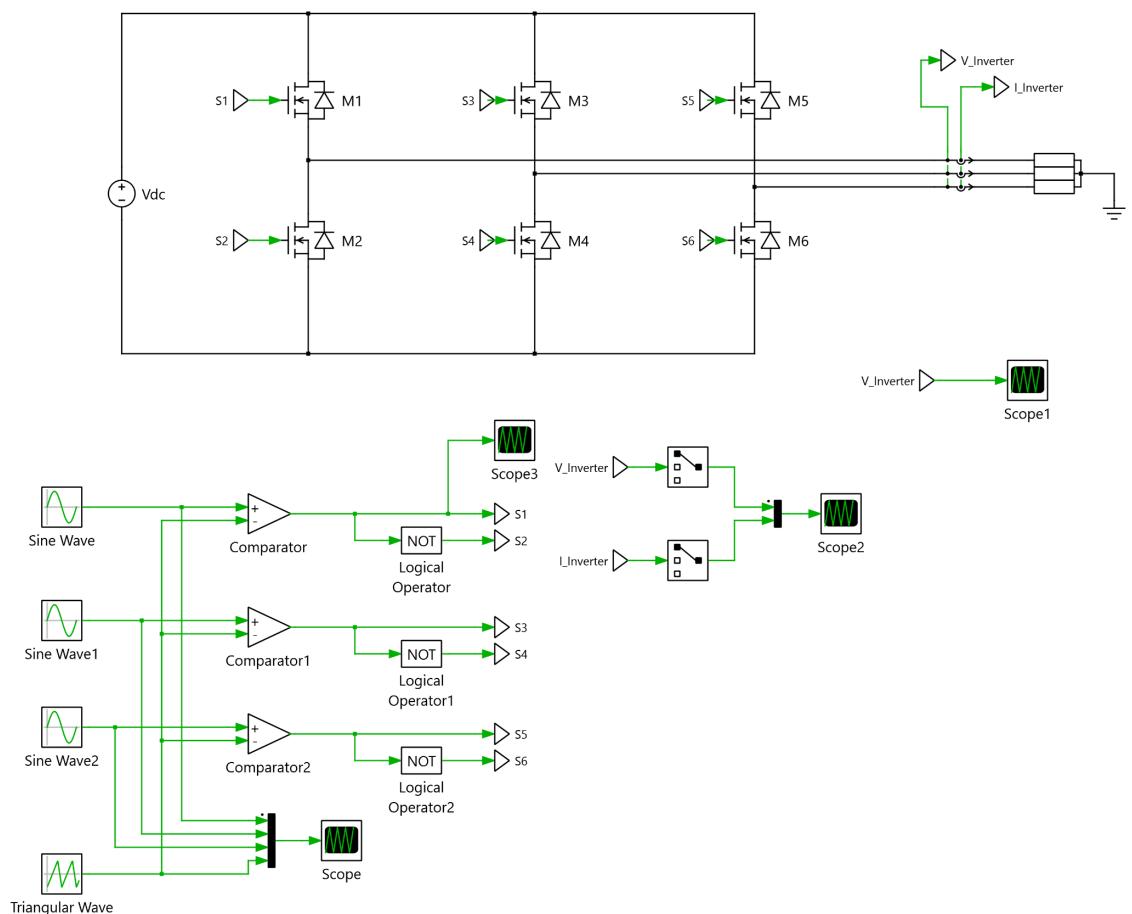
$4mf+1$, and so on), which can be seen from the figure above.

$$\text{with } mf = \frac{f_{sw}}{f_1} = \frac{\text{switching or carrier frequency}}{\text{fundamental frequency}}$$

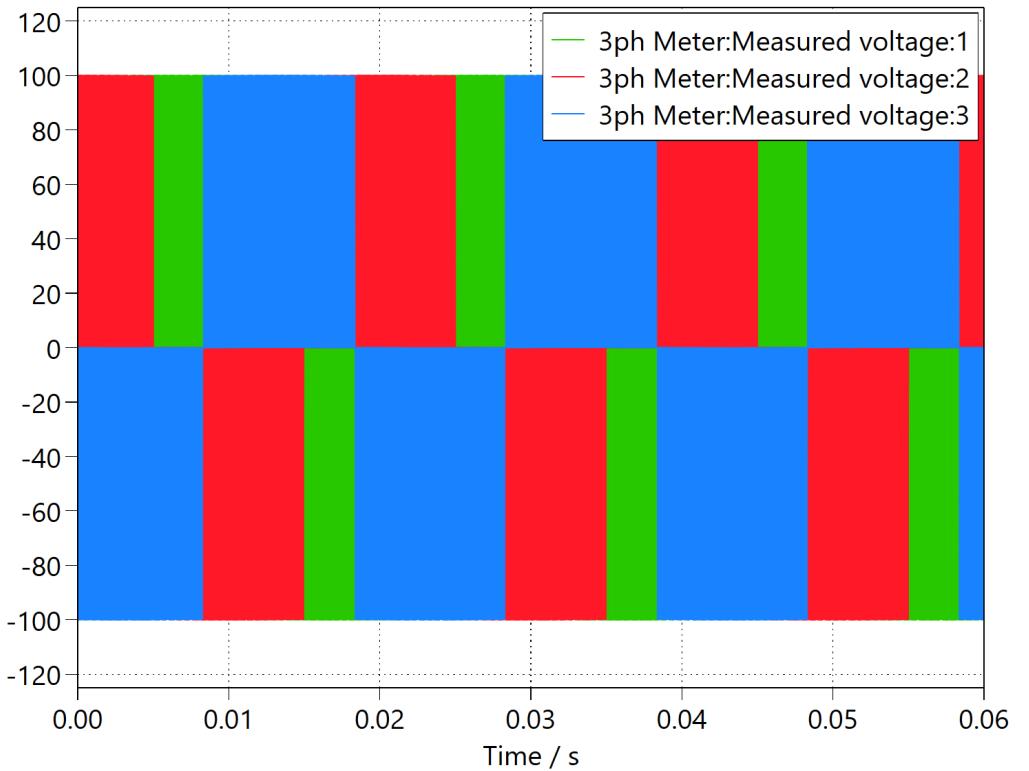
c. Three-phase inverter

Specification:

Vdc	100 V
fsw	10 kHz
D	50 %
Vout	± 100 V

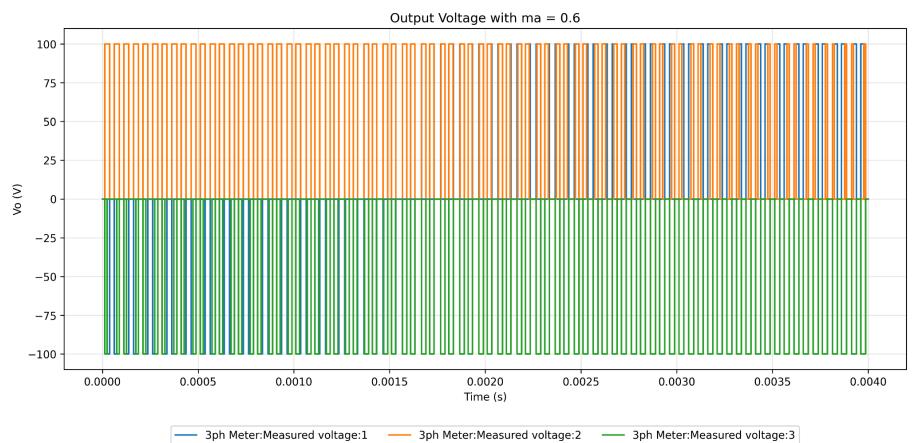


- 1) Generate the switching waveforms of the output voltage $v_o(t)$ using SPWM

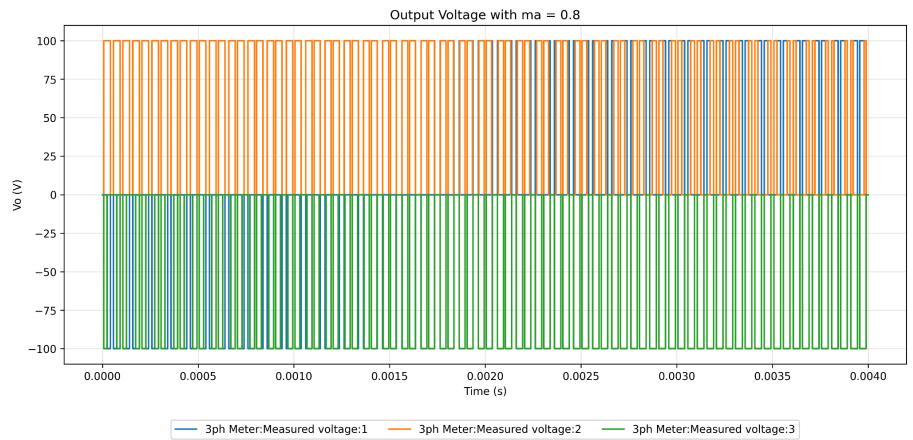


- 2) Plot the time-domain waveform of the output voltage at different modulation indices ma (e.g., 0.6, 0.8, 1.0)

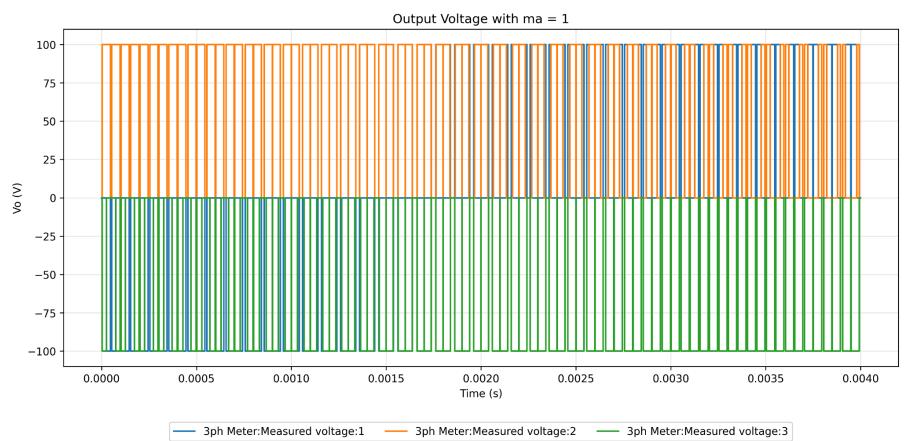
- $ma = 0.6$



- $ma = 0.8$

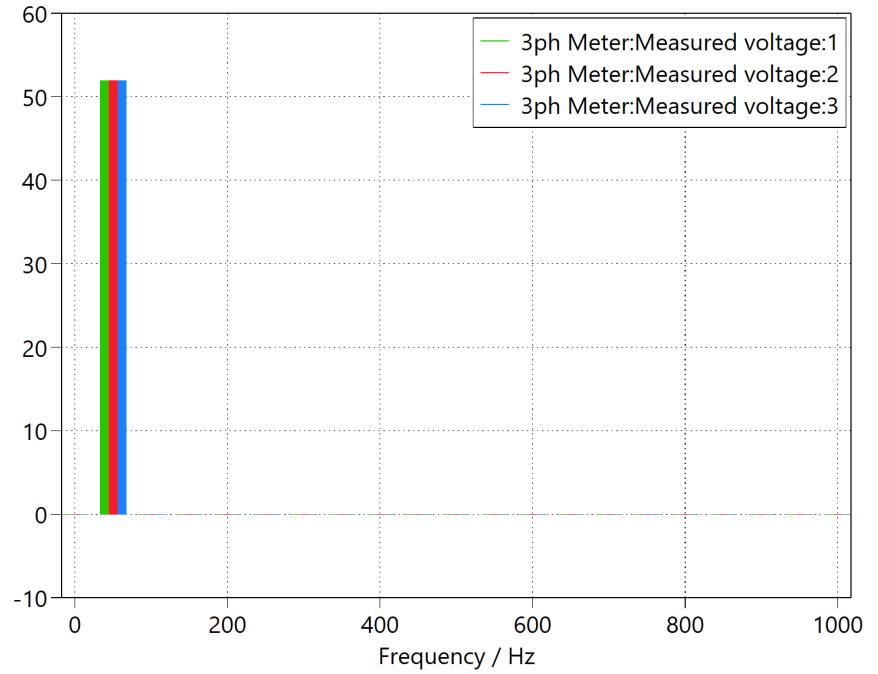


- $ma = 1$

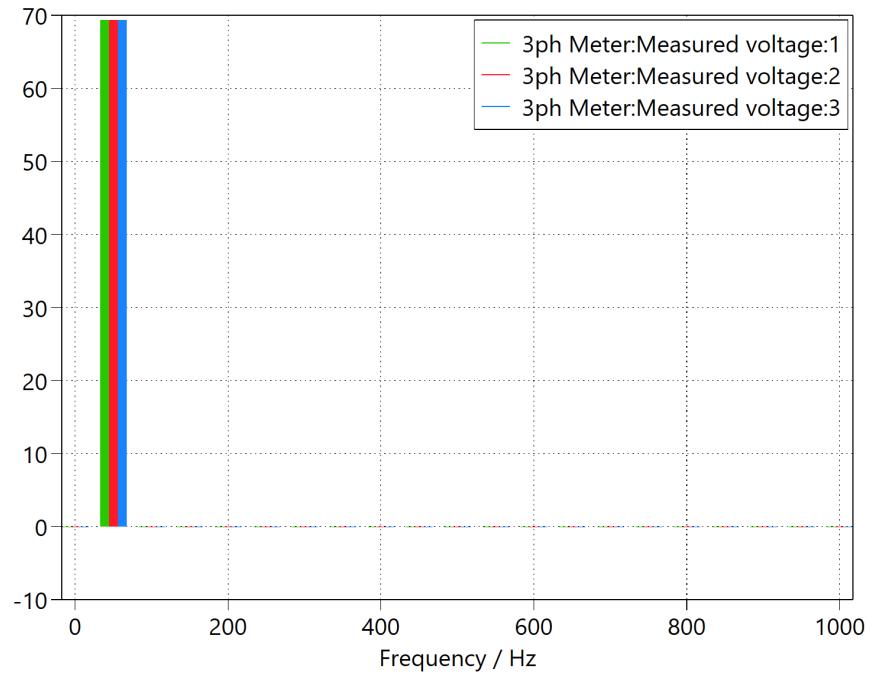


3) Obtain the frequency-domain representation using FFT

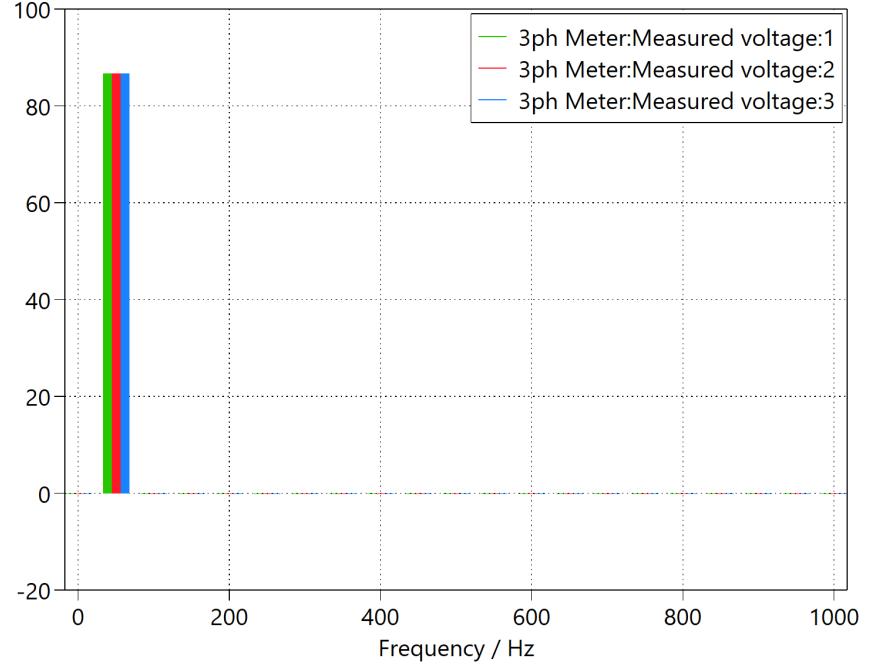
- $ma = 0.6$



- $ma = 0.8$



- $ma = 1$

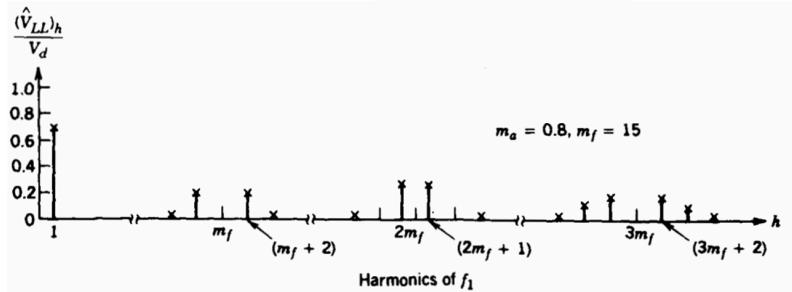


- Fundamental component: The fundamental component is located at the first harmonic, which corresponds to a frequency of 50 Hz. The value of this fundamental component represents by

$$(V_{LL}) = 0.612 ma (Vd)$$

with $ma = \frac{V_{control}}{V_{tri}} = \frac{\text{peak amplitude of the control signal}}{\text{peak amplitude of the triangular signal}}$

- Dominant switching harmonics:

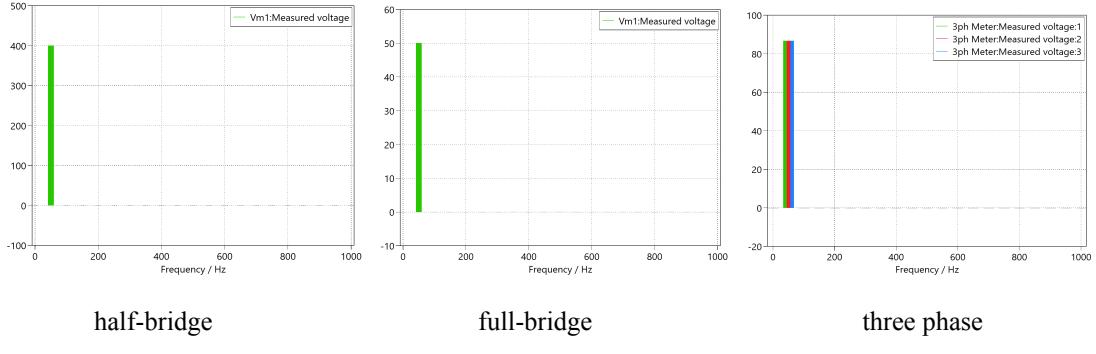


Dominant switching harmonics of line to line voltage appear at the switching (or modulation) frequency and in the frequency range surrounding it. In addition, significant harmonic components also occur at the multiples of the switching

frequency ($mf+2$, $mf-2$ $2mf+1$, $3mf+2$, and so on), which can be seen from the figure above.

$$\text{with } mf = \frac{f_{sw}}{f_1} = \frac{\text{switching or carrier frequency}}{\text{fundamental frequency}}$$

Compare harmonic spectra among the three converter types:



Based on the harmonic spectrum analysis of the three converters above, the effectiveness of employing Sinusoidal Pulse Width Modulation (SPWM) techniques is evident. Unlike conventional square wave modulation, which naturally generates significant low-order odd harmonic components (such as the 3rd, 5th, 7th, 9th, etc.), SPWM effectively minimizes these distortions in the low-frequency range. Rather than being eliminated, these harmonic components are shifted to higher frequencies, specifically around the sidebands of the switching frequency. This phenomenon explains why the harmonic spectrum appears remarkably clean within the fundamental range, effectively suppressing lower-order noise. Beyond these spectral characteristics, the specific circuit topology of each converter directly impacts the resulting output voltage amplitude, even when utilizing the same DC voltage source (V_d) and amplitude modulation (ma). The voltage relationships for each topology are defined as follows:

The output voltage of half-bridge inverter:

$$(V_o) = ma (V_d/2)$$

The output voltage of full-bridge inverter:

$$(V_o) = ma (V_d)$$

The line-to-line voltage of three-phase inverter is expressed as:

$$(V_{LL}) = 0.612 ma (V_d)$$

2. Design a second-order output filter

a. Design LC filter

Specification Full-Bridge Single-Phase Inverter

Vdc	400 V
fsw	10 kHz
D	50 %
R	1 Ω
C1	1 μF
C2	1 μF
Vmax	311 V
Vmin	-311 V
Vrms	220 V
fc	1 kHz
Imax	5 A
Irms	3.53 A

The design of the LC filter is obtained from [4], serving as the primary reference for parameter selection, mathematical formulation, and implementation considerations.

$$2\pi f_s L I_{Lmax} \leq 0.03 V_o$$

$$L \leq \frac{0.03 V_{rms}}{2\pi f_s I_{Lmax}}$$

$$C = \frac{1}{(2\pi f_c)^2 L}$$

The value of inductance is

$$L = \frac{0.03 V_{rms}}{2\pi f_s I_{Lmax}}$$

$$L = \frac{0.03 * 220}{2\pi * 50 * 3.53}$$

$$L = 5.9 \text{ mH}$$

The value of capacitance is

$$C = \frac{1}{(2\pi f_c)^2 L}$$

$$C = \frac{1}{(2\pi * 50)^2 * 0.0059}$$

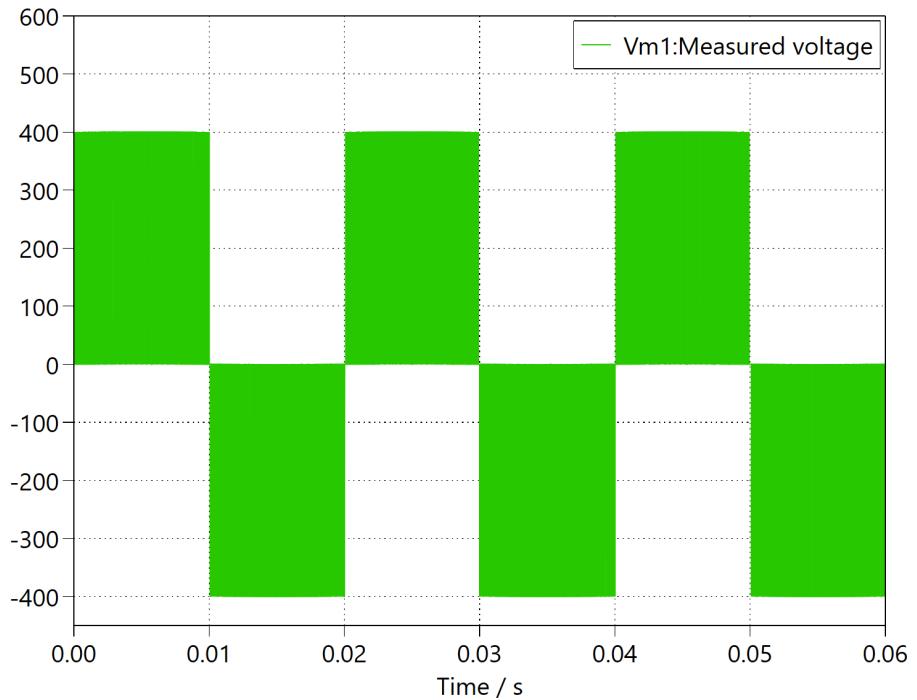
$$C = 4.26 \mu F$$

b. Limitations and Trade-Off of Design Filter

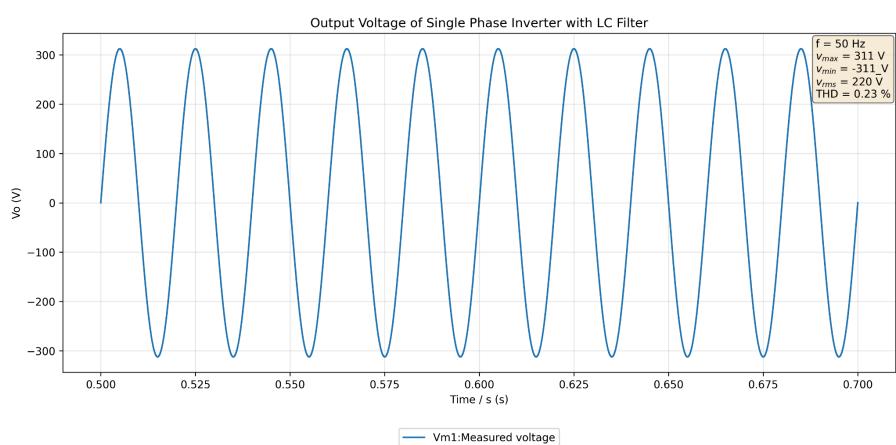
The LC filter design employed in this work may not be fully optimal when voltage ripple and current ripple are considered as primary design constraints in inverter applications. This design approach primarily focuses on eliminating or significantly attenuating harmonic components generated by the switching frequency. As a result, the selection of the filter parameters is driven by harmonic suppression requirements rather than ripple minimization at the output. Consequently, a trade-off arises between harmonic attenuation and ripple performance, where prioritizing the reduction of switching harmonics may lead to less stringent control of voltage and current ripple under certain operating conditions. In addition, emphasizing harmonic filtering can result in relatively larger passive components, which may increase system size, cost, and dynamic response limitations. Therefore, while the proposed filter design is effective in improving output waveform quality by suppressing switching harmonics, it presents limitations in applications where tight voltage and current ripple specifications, fast transient response, or compact system design are critical requirements.

c. Filtered output voltage waveform

- Time Domain Response

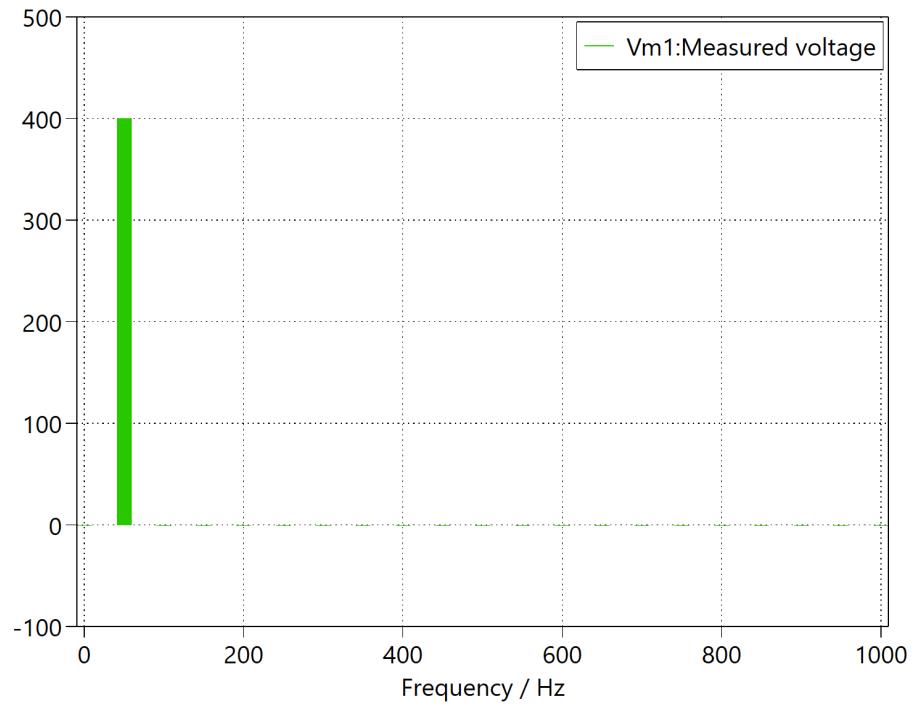


Output voltage before filter

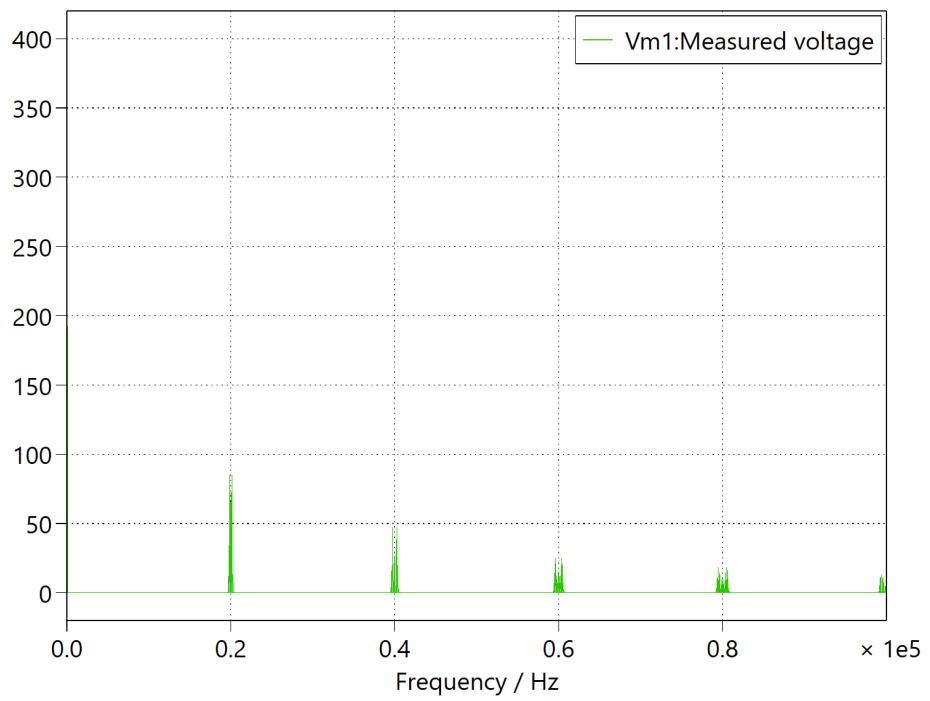


Output voltage After filter

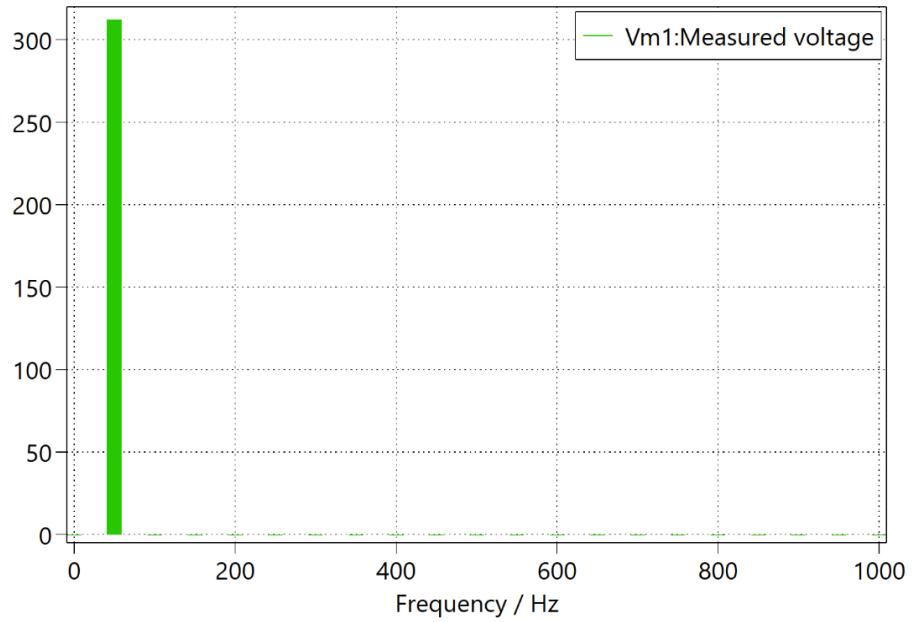
- Frequency Domain Response



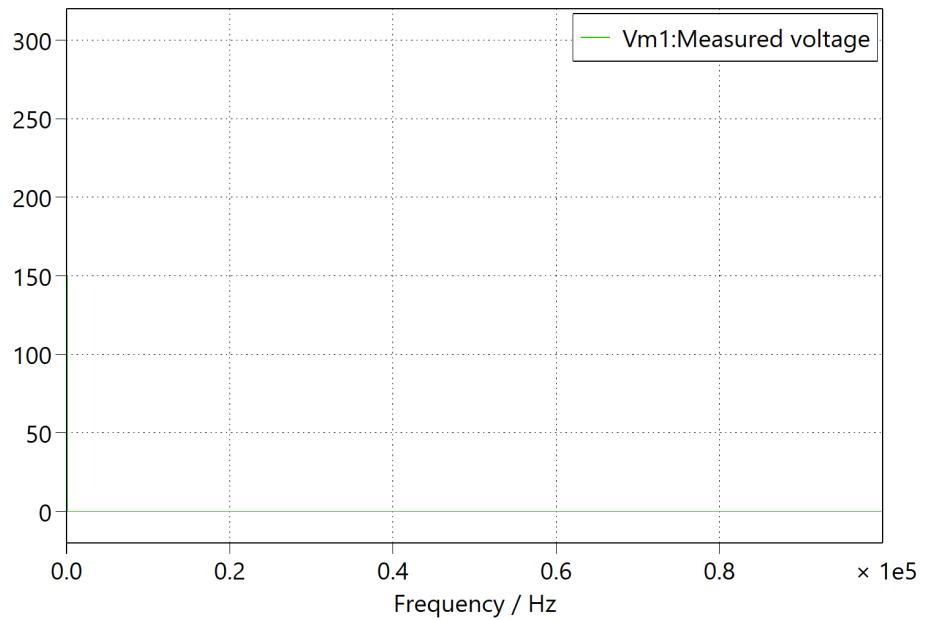
Spectrum Frequency Before Filter (1)



Spectrum Frequency Before Filter (2)



Spectrum Frequency After Filter (1)



Spectrum Frequency After Filter (2)

d. Analysis:

The output signal of the filter is an AC signal with a voltage of 220 Vrms and a fundamental frequency of 50 Hz. Based on the frequency spectrum plot shown above, it can be observed that the filter effectively passes the fundamental component while significantly attenuating the harmonic components generated by the switching process in the unipolar single-phase

full-bridge inverter. This indicates that the filter performs well in improving the quality of the output waveform. The total harmonic distortion (THD) of the output signal is 0.23%, which is below the standard THD limit of 5%, therefore the output power quality meets the required standards.

REFERENCES

- [1] H. Li, X. Liao, Y. Hu, Z. Zeng, E. Song, and H. Xiao, “Analysis of SiC MOSFET dI/dt and its temperature dependence,” *IET Power Electronics*, vol. 11, no. 3, pp. 491–500, Mar. 2018, doi: 10.1049/iet-pel.2017.0203.
- [2] S. Hazra *et al.*, “High Switching Performance of 1700-V, 50-A SiC Power MOSFET over Si IGBT/BiMOSFET for Advanced Power Conversion Applications,” *IEEE Trans Power Electron*, vol. 31, no. 7, pp. 4742–4754, Jul. 2016, doi: 10.1109/TPEL.2015.2432012.
- [3] E. O. Prado, P. C. Bolsi, H. C. Sartori, and J. R. Pinheiro, “Simple analytical model for accurate switching loss calculation in power MOSFETs using non-linearities of Miller capacitance,” *IET Power Electronics*, vol. 15, no. 7, pp. 594–604, May 2022, doi: 10.1049/pel2.12252.
- [4] N. R. Kudithi and S. Somkun, “Single Phase Power Generation System from Fuel Cell,” *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 9, no. 4, pp. 1676–1684, 2018, doi: 10.11591/ijped.s.v9n4.pp1676-1684.