Martin Haubenwallner

# Finding and Analyzing Undocumented Model-Specific Registers on x86_64

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Graz University of Technology

Institute for Applied Information Processing and Communications

Advisor: Michael Schwarz

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# Abstract

Model-specific registers (MSRs) are a fundamental part of the x86_64 instruction set architecture. They are used, among others, to toggle CPU features, debugging, and monitoring. As an example, the IA32_LSTAR MSR shall be noted. It contains the instruction pointer of the system-call handler, that is executed by the `syscall` instruction. Model-specific in this context means that each micro-architecture may have a different set of MSRs. Both AMD and Intel provide a substantial list of documented MSRs as part of their developer manuals.

However, already conducted research has shown that undocumented MSRs may provide security-critical information or functionality, for example, enabling debugging modes or reading CPU internal states [6]. On Linux, a toolset is available for working with MSRs, consisting of the `msr` kernel module and the relating msr-tools which can be used for reading from and writing to MSRs from userspace. Unfortunately, there was no high-performance scanning tool to find undocumented MSRs and no tools for analyzing data from dynamic MSRs.

In this thesis, we lay the foundation for further research of both undocumented and documented model-specific registers (MSRs) on x86_64 systems. We first design and then implement software to find and analyze both documented and undocumented MSRs. In the next step, we scan for and find undocumented MSRs on various x86_64 CPUs (Intel and AMD). We then statistically analyze the found static undocumented MSRs and formulate a hypothesis based on the found anomalies in the data. Using our sampling and analyzing tools, we then monitor the found dynamic MSRs and conclude as to what their purpose might be and what their data might mean.

**Keywords:** MSR, Model-Specific Register, Undocumented, x86_64, x64, Intel, AMD, Scanning

# Contents

# Chapter 1

# Introduction

Developing highly sophisticated devices such as modern x86_64 CPUs is a very complicated task that requires an immense amount of testing to make sure all parts with their respective features work reliable and correct. Documents such as the errata sheets of various vendors, e.g. Intel or AMD, show that despite thorough testing, bugs still happen.

A fundamental tool for testing these processors during development are so-called model-specific registers or MSRs for short. These special registers are used, for example, for monitoring CPU states, and enabling and disabling CPU features [9]. Each microarchitecture has its own set of MSRs.

x86_64 CPU developers such as Intel or AMD document a lot of their CPU's MSRs. However, previous experiments, such as the one by Christopher Domas [6], have shown that there are also undocumented ones. In software development, we can see that debug functionality, that is not removed before the product is released, often leads to security vulnerabilities [23]. As it may very well be that the same is true for hardware, undocumented MSRs will become of high interest for information security researchers since undocumented MSRs may give further insight into the inner workings of CPUs, or even pose security vulnerabilities themselves.

To lay a foundation for more efficient research in the field of MSRs, we develop a software toolset that allows easy and efficient scanning for MSRs that are present on an x86_64 system. Additionally, we conduct initial analytical experiments and present first methods to categorize undocumented MSRs. We conduct all of our experiments on multiple x86_64 microarchitectures from two manufacturers, namely Intel and AMD. We discuss the different behavior and techniques of these manufacturers we observed as well as the found undocumented dynamic MSRs and their respective properties we discovered.

Due to the very complex nature of CPUs, this thesis mainly focuses on undocumented dynamic MSRs, which are undocumented MSRs that do not have fixed values but rather change over time. Undocumented static MSRs are statistically analyzed. Furthermore,

we discuss the various other aspects of MSRs as future work, such as reverse-engineering flags or monitoring CPU behavior when specific values are changed.

To summarize we make the following contributions:

- We design and implement a software toolset to find and analyze undocumented MSRs.
- We analyze four Intel CPUs and one AMD CPU and find 5880 undocumented MSRs.
- We statistically analyze the undocumented static MSRs on four Intel CPUs and one AMD CPU and find unexpected anomalies.
- We present techniques on how to categorize undocumented dynamic MSRs and apply these to our found MSRs.

# Chapter 2

# Background

In this chapter, we give a basic introduction to microarchitectures, model-specific registers, CPU privilege rings, and other topics needed to understand the work done in this thesis.

## 2.1 Microarchitectures

Each microarchitecture is based on a so-called instruction set architecture (ISA) such as x86_64. ISAs define in an abstract way how the CPU works [7]. Specifically, they define the available instructions, registers, and addressing formats, to name a few. A specific implementation of such an ISA is called a microarchitecture. There may be multiple microarchitectures implementing the same ISA. As a consequence, all microarchitectures based on the same ISA can execute the same binaries. Additionally, it does not make a difference for programmers on which microarchitecture of a certain ISA they are working on as long as they do not wish to use microarchitecture specific extensions. However, there may be some differences between microarchitectures that are allowed by the ISA. For instance, there are model-specific registers which may be different on each microarchitecture [9].

## 2.2 CPU Rings

x86_64 CPUs implement four different privilege levels, so-called rings. These rings are implemented to increase security. For example, they prevent potentially malicious user programs which are running in ring three, which is the least privileged ring, from executing potentially harmful instructions such as `hlt`, which halts the CPU. Rings three to one are for user-mode, whereas ring zero is for kernel-mode. While ring zero has full privileges and can thus execute all instructions, rings three to one can only use certain subsets of the instruction set [9]. In theory, ring three is for user-mode, ring two is for system-mode, ring one is for drivers, and ring zero is for kernel-mode. In practice, only

ring three and zero are used with the operating system kernel running in ring zero and the user programs running in ring three.

Ring zero is usually referred to as kernelspace, while ring three is commonly referred to as userspace.

## 2.3 Model-Specific Registers (MSRs)

CPUs tend to get more and more complex, embedding more and more features and functionality. With this rising complexity, there arises a need to control and monitor these features. x86_64, leverages model-specific registers, which are 64-bit wide registers with a 32-bit address. As can be seen in CPU manufacturer documentations, these registers are used, among others, for toggling CPU features, monitoring system performance, and debugging [1,9]. "Model-specific" describes the fact that each microarchitecture may have its own set of MSRs, each with their individual addresses and functionalities. Though the address-functionality-mapping usually correlates between microarchitectures, this is not necessarily the case [9].

Christopher Domas [6] has shown that there exist undocumented MSRs which may expose security-critical functionality or information.

There are over one thousand different documented MSRs that provide hundreds of different functions and settings on Intel processors alone [9].

### 2.3.1 Instructions for Modifying MSRs

x86_64 offers two instructions, `rdmsr` and `wrmsr`, to read from and write to MSRs respectively. These instructions can be executed either in real mode or protected mode [9]. In protected mode, these instructions are only available in ring 0 and thus require kernel privileges to execute.

For both instructions, the address of the target MSR is specified in the RCX register, whereas the higher 32 bits are ignored [9]. `rdmsr` reads the values of the respective MSR into the registers RDX:RAX with RDX storing the higher 32 bits and RAX storing the lower 32 bits of the 64-bit MSR value. The higher 32 bits of the RDX and RAX registers are cleared. `wrmsr` writes the value in RDX to the higher 32 bits and the value in RAX to the lower 32 bits of the MSR. The higher 32 bits of both RDX and RAX are ignored.

If one executes either of the two instructions on an MSR that is reserved or unimplemented, the CPU generates a General Protection (GP) exception [9]. Additionally, a GP is generated if `wrmsr` would change reserved bits in an implemented MSR.

## 2.4 Syscall

As described in Section 2.2, there are two primary privilege levels, or rings, on modern x86_64 CPUs (namely three and zero). To escalate from ring three to ring zero, the

`syscall` instruction is used [9]. This instruction invokes a system handler that was previously defined by the operating system by loading the respective address from the IA32_LSTAR MSR (0xc0000084) into the instruction pointer register (RIP) and setting the privilege level to zero. This way, the operating system can provide necessary privileged services, such as reading from a file or writing to a network socket, to unprivileged user-processes in a safe way. Once the operating system served the request of the user-process it deescalates back to ring three via the `iret` instruction and the user-process resumes right after the `syscall` instruction [9].

## 2.5 Linux Kernel Module

As stated above, the `wrmsr` and `rdmsr` instructions cannot be executed in userspace as they require kernelspace privileges. With Linux kernel modules, Linux offers a way to dynamically extend the Linux kernel at runtime. In principle, a Linux kernel module (LKM) is a program that is compiled to a kernel object, which may then be loaded into the Linux kernel and is executed in ring 0. Usually, the programming language of choice for creating an LKM is C.

## 2.6 Input/Output Control (ioctl)

On Linux, the number of syscalls has already exceeded 330 [32]. Adding a new syscall is usually discouraged as it requires it to be implemented in every architecture the kernel supports and is less flexible than ioctls [22]. Instead, it is recommended to create a character device and implement ioctl calls. The abbreviation ioctl stands for **i**nput/**o**utput **c**on**t**ro**l** and was added to manipulate the parameters of the underlying device [18]. It is basically a way to implement device-specific "syscalls" that are called ioctl calls. In short, a handler for the unlocked ioctl operation [5] on the respective device is added, which gets invoked when an ioctl syscall with an open file descriptor to the underlying device as a parameter is made. With this technology, it is possible to implement dynamic driver-specific syscall-like services that are executed in ring zero. This means that it is possible for kernel modules to provide syscall like interfaces to communicate with the driver.

**Listing 2.1:** The ioctl call function signature [18]

```
int ioctl(int fd, unsigned long request, ...);
```

The function signature of the ioctl call can be seen in Listing 2.1. It has to contain a valid file descriptor to the respective desired device, a request number, as well as an untyped pointer to memory [18].

## 2.7 Misc Device

In Linux, each device driver has a major number assigned to it [21]. Each individual device of this device driver gets a minor number assigned and can thus be identified by the major minor value pair. Allocating a major device number makes sense when the driver has multiple devices and thus entry points. Every action on an individual device falls back to the responsible device driver, which is the driver with the respective major number. As it is not feasible to allocate a new major number for each small service, Linux offers a simplified interface that allows for single devices to be registered. This interface is realized as the misc device driver, which has the major number 10 assigned [21]. It is possible to register a new device on this driver and then override all desired file operations of this device.

## 2.8 Exception Handling in the Linux Kernel

As described before, the `rdmsr` and `wrmsr` instructions may throw different exceptions during execution. Unhandled exceptions in an LKM usually cause the executing process to be killed. Fortunately, there exists a way to handle exceptions in the Linux kernel that has similar semantics to try/catch of higher-level languages like C++ or Python [16]. One of the key differences is that this mechanism works on the assembly level instead of being accessible through a higher level language like C itself.

To achieve try-catch behavior on certain instructions an entry containing the address of the respective instruction that may generate an exception, the address of the fixup code, and the address of the handler function that shall be executed when an exception is thrown is added to the __ex_table section. The so-called fixup code is stored in the "fixup" section and is called by the handler if an exception is raised on the specific instruction specified in the __ex_table. As this fixup code is called in the interrupt context, it should be as performant as possible. The handler has to have the function type depicted in Listing 2.2.

**Listing 2.2:** The ex_handler_t type [31]

```
typedef bool (*ex_handler_t)(
const struct exception_table_entry *,
struct pt_regs *,
int,
unsigned long,
unsigned long);
```

As one might expect, this kind of exception handling is often used in the Linux kernel, and thus, there are convenient macros that make working with this mechanism easier. Listing 2.3 shows the macro that creates the entry in the __ex_table. The `from` parameter specifies the address at which an exception might be thrown. The `to` parameter specifies

the location of the fixup code. The `handler` parameter specifies the location of the handler that shall be called to handle exceptions.

**Listing 2.3:** The _ASM_EXTABLE_HANDLE macro [31]

```
#define _ASM_EXTABLE_HANDLE(from, to, handler)    \
.pushsection "__ex_table","a" ;                   \
.balign 4 ;                                       \
.long (from) - . ;                                \
.long (to) - . ;                                  \
.long (handler) - . ;                             \
.popsection
```

There already exists a default handler, that calls the corresponding fixup code when an exception was generated, and a respective extable macro, see Listings 2.4 and 2.5.

**Listing 2.4:** The ex_handler_default function [31]

```
__visible bool ex_handler_default(
const struct exception_table_entry *fixup,
struct pt_regs *regs,
int trapnr,
unsigned long error_code,
unsigned long fault_addr)
{
regs->ip = ex_fixup_addr(fixup);
return true;
}
```

**Listing 2.5:** The _ASM_EXTABLE macro [31]

```
# define _ASM_EXTABLE(from, to)   \
_ASM_EXTABLE_HANDLE(from, to, ex_handler_default)
```

## 2.9 `rdmsr_safe` and `wrmsr_safe`

With the building blocks described in Section 2.8 it is trivial to create a safe version of both `rdmsr` and `wrmsr`. As reading from and writing to MSRs is a quite common task to perform for an x86_64 operating system these functions have already been written and merged into the kernel upstream [31], see Listings 2.6 and 2.7. These implementations provide an error value that can be used to check if the respective read or write operation was successful or whether an exception was generated.

**Listing 2.6:** The native_read_msr_safe function [31]

```
static inline unsigned long long native_read_msr_safe(
unsigned int msr, int *err)
```

```
{
DECLARE_ARGS(val, low, high);

asm volatile("2: rdmsr ; xor %[err],%[err]\n"
"1:\n\t"
".section .fixup,\"ax\"\n\t"
"3: mov %[fault],%[err]\n\t"
"xorl %%eax, %%eax\n\t"
"xorl %%edx, %%edx\n\t"
"jmp 1b\n\t"
".previous\n\t"
_ASM_EXTABLE(2b, 3b)
: [err] "=r" (*err), EAX_EDX_RET(val, low, high)
: "c" (msr), [fault] "i" (-EIO));
if (msr_tracepoint_active(__tracepoint_read_msr))
do_trace_read_msr(msr, EAX_EDX_VAL(val, low, high),
*err);
return EAX_EDX_VAL(val, low, high);
}
```

**Listing 2.7:** The native_write_msr_safe function [31]

```
static inline int notrace
native_write_msr_safe(unsigned int msr, u32 low, u32 high)
{
int err;

asm volatile("2: wrmsr ; xor %[err],%[err]\n"
"1:\n\t"
".section .fixup,\"ax\"\n\t"
"3: mov %[fault],%[err] ; jmp 1b\n\t"
".previous\n\t"
_ASM_EXTABLE(2b, 3b)
: [err] "=a" (err)
: "c" (msr), "0" (low), "d" (high),
[fault] "i" (-EIO)
: "memory");
if (msr_tracepoint_active(__tracepoint_write_msr))
do_trace_write_msr(msr, ((u64)high << 32 | low),
err);
return err;
}
```

## 2.10 Pearson and Spearman Correlation Coefficients

For this section, let two variables $X$ and $Y$ be defined as:

$$X = \{x_1, x_2, x_3, ..., x_n\} \tag{2.1}$$

$$Y = \{y_1, y_2, y_3, ..., y_n\} \tag{2.2}$$

With $x_i$ and $y_i$ each denoting the $i$th data sample.

As Xu and Deng describe in their paper [33], the Pearson correlation coefficient is used to determine the correlation of two normal continuous variables. It yields a value $r$ in the interval [-1, 1]. The meaning of $r$ for two variables $X$ and $Y$ can be expressed with the following function:

$$\text{Meaning of } r = \begin{cases} \text{X and Y have a complete positive correlation} & \text{if } r = 1 \\ \text{X and Y have a positive correlation} & \text{if } 0 < r < 1 \\ \text{X and Y have no obvious correlation} & \text{if } r = 0 \\ \text{X and Y have a negative correlation} & \text{if } -1 < r < 0 \\ \text{X and Y have a complete negative correlation} & \text{if } r = -1 \end{cases} \tag{2.3}$$

The Spearman rank correlation coefficient is described by Chok in his thesis [3] as a rank-based version of the Pearson correlation coefficient. Similarly to Pearson's correlation coefficient, the Spearman rank correlation coefficient yields a value $r_s$ for two variables X and Y in the interval [-1, 1]. The meaning of $r_s$ can be expressed through the same function as the result of Pearson, see Equation 2.3. Chok further notes, that Spearman's coefficient can not only find complete correlations for linearly related variables but also for variables that are related in a non-linear monotonic way. However, Spearman's correlation coefficient can still be 0 for variables that have a non-monotonic relationship.

As the Pearson correlation coefficient is more outlier sensitive than the Spearman correlation coefficient, Pearson seems to better reflect the overall concordance if there are only a few outliers [3]. Both of these coefficients are used in this thesis and the resulting framework to offer more conclusive results.

# Chapter 3

# Design

To fulfill our goal of templating undocumented MSRs, we develope a software toolset that is split into two main parts, the kernel part, and the userspace part, which are explained in this chapter. For an abstract visualization of this software toolset see Figure 3.1.

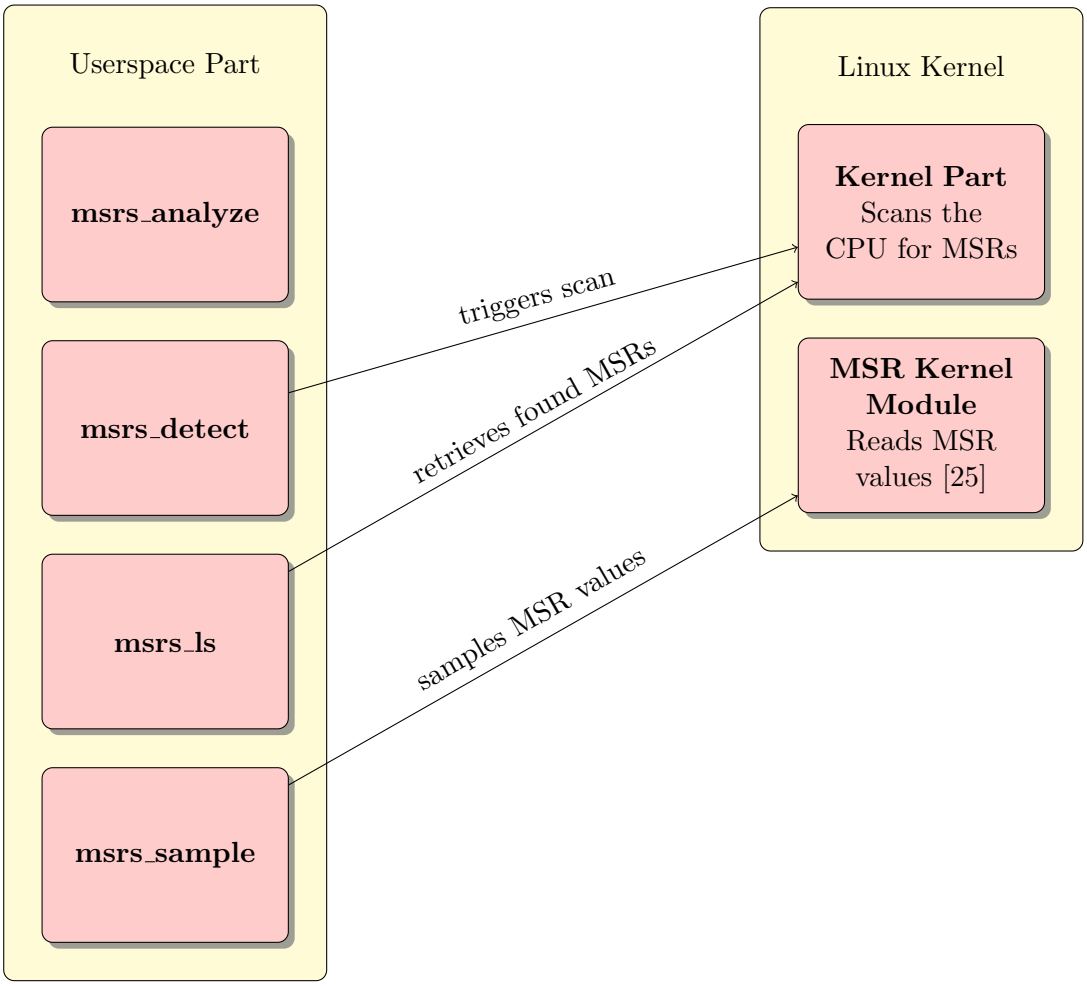



**Figure 3.1:** This figure shows an abstract visualization of the software toolset.

## 3.1 Overview

Fulfilling our main goal of finding undocumented MSRs and analyzing the dynamic ones requires multiple steps:

1. Get a list of the MSRs that exist on the respective CPU.
2. Extract all undocumented MSRs from this list.
3. Check for each MSR if it is static or dynamic.
4. Analyze the dynamic MSRs.

## 3.2 Kernel Part

MSRs can only be read from and written to in ring zero. Hence, the scanning for MSRs has to be done in kernelspace.

The kernel part is responsible for two things:

**scanning** scan the whole range of possible MSRs

**exposing** expose a list of the found MSRs to userspace

The platform of choice for the toolset is Linux due to it being open-source and easily modifiable. There are two ways to extend the functionality of the Linux kernel. One can either create a custom kernel, thus actually modifying the kernel itself by extending the functionality, or one can create a kernel module that can be loaded into the kernel at runtime. Creating a custom kernel comes with the upside of having all functions of the kernel available but with the downside of being far less flexible as each user of the toolset would have to install and boot the custom kernel. Additionally, a custom kernel would come with a far more significant maintenance overhead as all upstream changes of the Linux kernel would have to be implemented into the custom kernel if one does not want it to go severely out of date quite quickly. A kernel module is far more flexible as it can be loaded into and out of the running kernel and poses less maintenance overhead. However, it needs to be recompiled for each new kernel version as APIs may have changed. Due to the nature of our application being a tool and the anticipated maintenance overhead, we decide to implement the functionality via a kernel module.

The whole scanning process is carried out solely in kernelspace in order to gain performance by avoiding costly and, in this case, unnecessary inconveniences like context switches.

To achieve even more performance, the scanning is carried out multithreaded. While this poses a quite high CPU load on multiple cores, it also drastically decreases the run time.

Linux offers multiple ways to communicate between kernelspace and userspace, including sockets, procfs, sysfs, syscalls, and ioctls [31]. We decide to use ioctls as it poses the least overhead and is quite easy to implement. Our kernel module creates a misc device that allows triggering a scan via ioctl and reading the list of found MSRs via the pread syscall [26]. As there already exists an in-tree kernel module for reading and writing from and to MSRs, called simply msr [25], we decide against implementing this feature.

## 3.3 Userspace Part

We also need a set of userspace tools that enable us to communicate with our kernel module, sample MSRs, as well as analyze the collected data.

The needed functionality is split into four tools: msrs_detect, msrs_ls, msrs_sample, and msrs_analyze.

### 3.3.1 msrs_detect

msrs_detect is a simple program that triggers a new scan with a user-defined number of workers via an ioctl call.

### 3.3.2 msrs_ls

msrs_ls prints all MSRs that were found by the module.

### 3.3.3 msrs_sample

msrs_sample samples MSRs specified by the user on all available cores for a user-specified amount of time and prints the results to stdout. All values are represented in hexadecimal notation without a prefix or postfix. Lines starting with # are comments and do not denote a sample value. The output format is described in Table 3.1.

**Table 3.1:** The format of the output generated by msrs_sample.

| Line | Description | Example |
|---|---|---|
| 1 | The list of sampled CPUs separated by a comma. | f,e,d,c,b,a,9,8,7,6,5,4,3,2,1,0 |
| 2 | The list of sampled MSRs separated by a comma. | 102,108,10a,110,118,11f |
| 3 | The sampling time. | 12c |
| 4 - N | Each line represents one read. Each individual line, or read, contains a list of MSR values per CPU, which are separated by a comma, separated by a semicolon. The order of MSRs as well as CPUs is the same as in the respective lines 1 and 2. | MSR102_CPU0,MSR102_CPU1, ...,MSR102_CPUf;MSR108_CPU0, ...,MSR108_CPUf;...;MSR11f_CPU0, ...,MSR11f_CPUf\n |

### 3.3.4 msrs_analyze

msrs_analyze is a tool to analyze the data samples generated by msrs_sample. For this purpose, it provides the two main functions "plot" and "corr".

The "plot" function checks, per MSR, for changes on each CPU and plots the data of all CPUs in a single line plot. If data changes are present on a CPU, the tool additionally generates a line plot containing only the data of this specific CPU, a bit heatmap, that shows the bit changes of all reads, as well as a line plot which shows the data changes as well as the reverse data changes.

The "corr" function calculates the Pearson as well as the Spearman correlation coefficients, see Section 2.10, between a specified MSR and other MSRs in the individual sample file on the raw sample data as well as on the data changes. If a user-defined similarity threshold is reached, the tool creates a plot visualizing the similarity.

The "changes" function analyzes the values of each MSR per CPU and looks for changes in the sampled values. Changes means that there are different values read from the same MSR over time. If changes are found the address of the respective MSR is printed on stdout.

# Chapter 4

# Implementation

In this chapter, we will discuss the various implementation details of the kernel module and the userspace tools.

## 4.1 Kernel Module (msrs)

The kernel module is written in C. Multithreading is implemented by using a concurrency managed workqueue [8]. For communication purposes with the userspace, a misc device, see Section 2.7, with the name `msrs` is created. The path to the driver device file is `/dev/msrs`. This device implements four file operations as shown in Table 4.1.

**Table 4.1:** Implemented file operations.

| Operation | Description |
|---|---|
| open | Used by the `open` [27] syscall. This call will lock the device preventing it being opened multiple times at the same time. |
| read | Used by the `pread` [26] syscall. It is used to receive the found MSRs by reading from the device. Each 64-bit value represents an MSR address that was found. |
| unlocked_ioctl | Used for `ioctl` calls. `unlocked_ioctl` [5] does, in contrast to an `ioctl` call, not run under the Big Kernel Lock (BKL) [4]. |
| release | Used to release the device. It is used by the `close` [28] syscall. Unlocks the device. |

The `ioctl` interface provides one call, which has to be provided with an integer that specifies how many workers to use for starting an MSR scan. To avoid race conditions, only one process at a time is allowed to have a valid open file descriptor of the driver device file. If a process attempts to open the device file while another process already

holds an open file descriptor, the device will return -EBUSY indicating that the resource is busy [30].

## 4.2 Userspace

Except for the msrs_analyze tool, which is written in Python 3, all other userspace tools are written in C++17.

### 4.2.1 msrs_detect

**Listing 4.1:** Usage of msrs_detect

```
./msrs_detect thread_count
```

Listing 4.1 shows the usage of the msrs_detect tool. All arguments are described in the table 4.2.

**Table 4.2:** Command line arguments of msrs_detect.

| Argument | Description |
|---|---|
| thread_count | This mandatory positional argument specifies the number of workers to be used for the scanning process. The value has to be in $\{n \in \mathbb{N} \mid n \leq \text{UINT\_MAX}\}$. A thread_count too high may cause the system to freeze. |

### 4.2.2 msrs_ls

**Listing 4.2:** Usage of msrs_ls

```
./msrs_ls
```

Listing 4.2 shows the usage of the msrs_ls tool. It takes no arguments but directly reads all found MSR addresses and prints them, separated by a `\n`, in hexadecimal format to the standard output.

### 4.2.3 msrs_sample

**Listing 4.3:** Usage of msrs_sample

```
./msrs_sample duration msr [msr]...
```

Listing 4.3 shows the usage of the msrs_sample tool. All arguments are described in Table 4.3. The tool prints the sample data in the format described in Section 3.3.3 to the standard output. As all values are printed in hexadecimal, neither prefix, as for example `0x`, nor a postfix, as for example `H`, is added to the values.

**Table 4.3:** Command line arguments of msrs_sample.

| Argument | Description |
|---|---|
| duration | This mandatory positional argument specifies the number of seconds the tool shall sample the specified MSRs. It has to be provided in decimal. The time value has to be in $\{n \in \mathbb{N} \mid n < 2^{32}\}$. |
| msr [msr]... | At least one MSR has to be specified. Additional MSRs may be specified. The MSR addresses may be provided in decimal, octal (prefix: 0), or hexadecimal (prefix: 0x). Each provided MSR value has to be in $\{n \in \mathbb{N} \cup \{0\} \mid n < 2^{32}\}$. |

### 4.2.4 msrs_analyze

As noted above, this tool is written in Python 3. The reason for this is that Python offers a large variety of libraries for scientifically analyzing and plotting data, like NumPy [19], SciPy [24], and matplotlib [29], and additionally has integrated support for unlimited range integers [20].

**Listing 4.4:** Usage of msrs_analyze

```
python3 msrs_analyze.py [-h] [-a ACTION] [-m MSR] [--msrs
    MSRS] [-s SIMILARITY_THRESHOLD] [-c CPUS] sample_file
```

Listing 4.4 shows the usage of the msrs_analyze tool. All arguments are described in Table 4.4.

**Table 4.4:** Command line arguments of msrs_analyze.

| **Argument** | **Description** |
|---|---|
| sample_file | This mandatory positional argument specifies the file containing the sampled data that shall be analyzed. |
| -h, –help | Shows help information. |
| -a, –action | Specifies the action to execute (one of: plot, corr, changes). The default is plot. |
| –m, –msr | Specifies the main MSR used for comparison. Mandatory for action "corr". |
| –msrs | Specifies the MSRs that shall be used for the selected action. The default is: "all". |
| -s, –similarity-threshold | Specifies the similarity threshold which is a value between 0 and 1 with 0 being no connection at all and 1 stating complete equality, see also Section 2.10. This threshold has to be reached for the tool to generate a plot. The default is: 0.75 |
| -c, –cpus | Specifies the CPUs that shall be used for the selected action. The default is "all". |

# Chapter 5

# Fundamental Assessment

In this chapter, we lay the needed foundation for our experiments. We specify the experimentation setup, gather information, and conduct first fundamental experiments that provide us with the necessary data needed for more specialized experiments and the final general assessment of this thesis.

## 5.1 Experimentation Setup

In Table 5.1, the CPUs used for experimentation are depicted.

**Table 5.1:** Table of x86_64 CPUs used for experimentation.

| CPU | Manufacturer | Microarchitecture |
|---|---|---|
| Ryzen Threadripper 1920X [2] | AMD | Zen |
| Core i7-6700K [11] | Intel | Skylake |
| Core i7-8700K [12] | Intel | Coffee Lake |
| Core i9-9900K [13] | Intel | Coffee Lake |
| Xeon Silver 4208 [15] | Intel | Cascade Lake |

## 5.2 MSR Scans

We use the tools described before to scan for MSRs on each CPU depicted in Table 5.1. For each individual CPU, all documented MSRs are extracted from the respective Intel [9] and AMD [1] manuals. Please note that for AMD, we exclusively take into account the documented MSRs and not the specified ranges they provide in their document. We use this data to determine which found MSRs are documented and which are undocumented.

The extraction of the undocumented MSRs is done in a semi-automatic way using the tools described in Chapter 3, as well as basic command line tools such as `comm`. On our

CPUs the MSR scans took between 1 minute 19 seconds (AMD Ryzen Threadripper 1920X) and 8 minutes 43 seconds (Intel Core i7-6700K with hyper-threading disabled). Based on the results of multiple scans conducted on each CPU the scans seem to be fully deterministic, thus yield the same results each time. A summary of the results of this first scan can be found in Table 5.2.

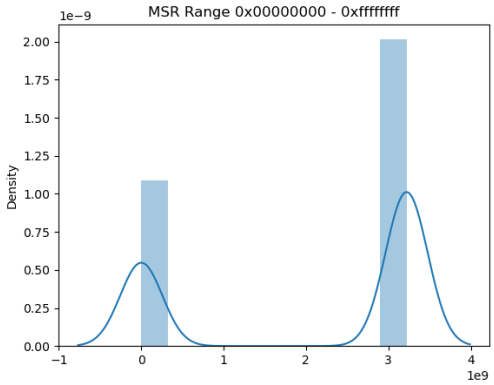
**Table 5.2:** Summarized results of the fundamental scan.

| CPU | Number of Found MSRs | Number of Undocumented MSRs |
|---|---|---|
| Ryzen Threadripper 1920X [2] | 5240 | 4875 (93.03%) |
| Core i7-6700K [11] | 477 | 104 (21.80%) |
| Core i7-8700K [12] | 520 | 124 (23.85%) |
| Core i9-9900K [13] | 532 | 134 (25.19%) |
| Xeon Silver 4208 [15] | 1098 | 643 (58.56%) |

A list of all detected MSRs can be found in the appendix in Section 10.1.

### 5.2.1 MSR Ranges

**Figure 5.1:** The distribution of MSRs over the whole range.




Based on the combined results of the found MSRs on all analyzed CPUs we found that there are apparently three used value ranges which we call $R_1$, $R_2$, and $R_3$ . They are defined as follows:

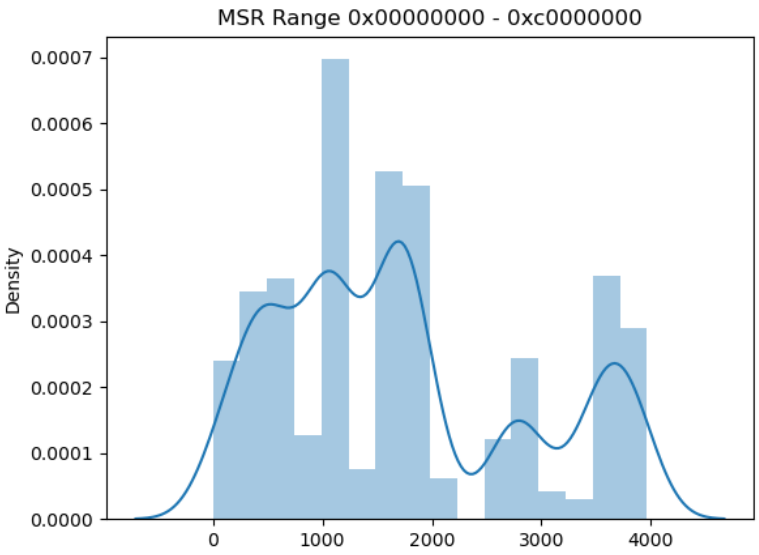
$$R_1 = \{n \in \mathbb{N} \cup \{0\} \,|n < 0xc0000000\} \tag{5.1}$$

$$R_2 = \{n \in \mathbb{N} \cup \{0\} \,|0xc0000000 \leq n < 0xc0010000\} \tag{5.2}$$

$$R_3 = \{n \in \mathbb{N} \cup \{0\} \,|n \geq 0xc0010000\} \tag{5.3}$$

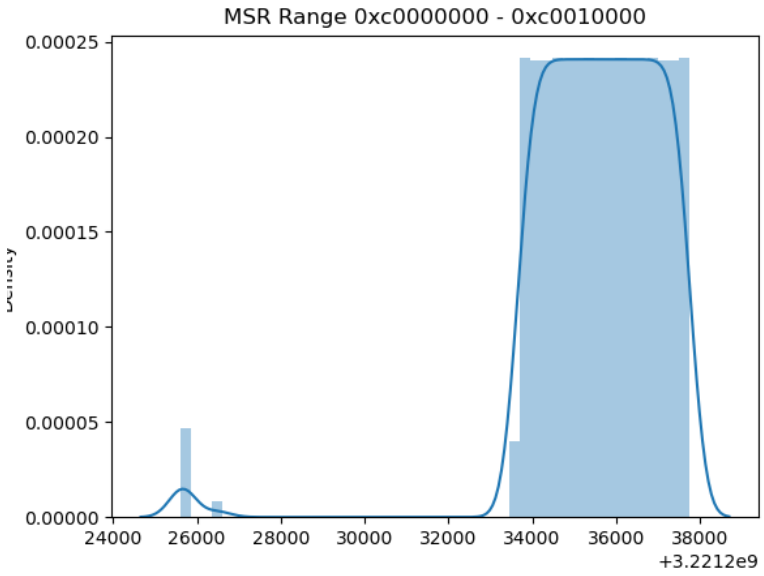
Empirically, using the actually existing MSRs on our CPUs, we found the ranges $R_1^{emp}$, $R_2^{emp}$, and $R_2^{emp}$, see the respective Figures 5.2, 5.3, and 5.4, on our machines to be:

**Figure 5.2:** The distribution of MSRs in $R_1^{emp}$.



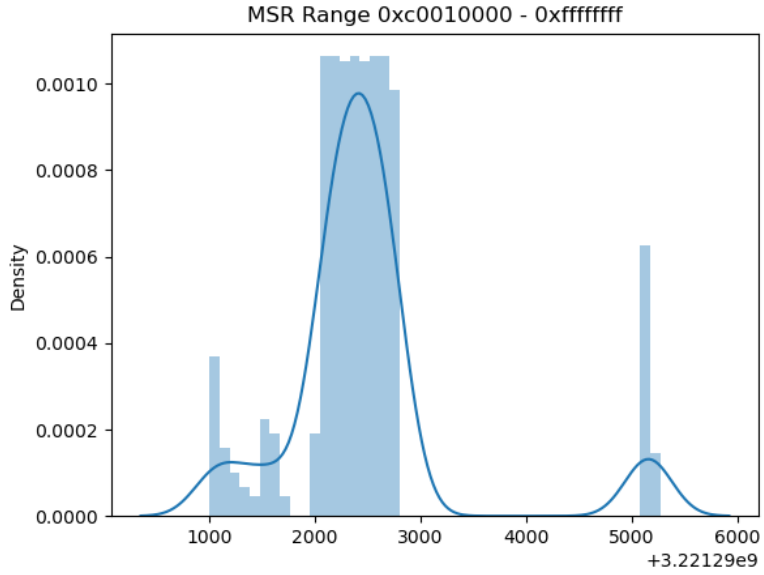

$$R_1^{emp} = \{n \in \mathbb{N} \cup \{0\} \,|n \leq 0xf7b\} \tag{5.4}$$

**Figure 5.3:** The distribution of MSRs in $R_2^{emp}$.




$$R_2^{emp} = \{n \in \mathbb{N} | 0xc0000080 \leq n \leq 0xc0002fff\} \tag{5.5}$$

**Figure 5.4:** The distribution of MSRs in $R_3^{emp}$.



$$R_3^{emp} = \{n \in \mathbb{N} | 0xc0010000 \leq n \leq 0xc00110a2\} \tag{5.6}$$

## 5.3 Differences AMD and Intel

We see a vast difference in the number of existing MSRs with the AMD CPU which has with 5240 MSRs nearly five times as many MSRs as the Intel processor with the most MSRs in our setup, which is the Intel Xeon Silver 4208 with 1098 MSRs. When comparing the number of existing MSRs divided into two groups, specifically documented and undocumented we see that our scanned AMD and Intel processors do not differ significantly in terms of existing documented MSRs but differ significantly in terms of existing undocumented MSRs. In numbers this means that the AMD CPU has 4875 undocumented MSRs whereas the Intel CPU with the most undocumented MSRs, which is again the Intel Xeon Silver 4208, has only 643 undocumented MSRs. For a detailed overview see Table 5.2.

# Chapter 6

# Analyzing Statistical Parameters of Static Undocumented MSRs

In this chapter we evaluate statistical parameters of the static undocumented MSRs that we found on the tested CPUs and discuss potential anomalies.

## 6.1 AMD Ryzen Threadripper 1920X

As we can see in Table 6.1 all 12 CPUs, except for CPU 0 and CPU 6, have 4852 undocumented static MSRs that are zero and 21 undocumented static MSRs that are non-zero. CPUs 0 and 6 have 4804 undocumented static MSRs with the value zero and 69 undocumented static MSRs that are non-zero as can be seen in Table 6.2. In Table 6.2 we can additionally see that at least 19 of the 48 additional MSRs have the value d01a000000000000. This is also visible when comparing Figures 6.1 and 6.2.

**Table 6.1:** Static MSRs with value zero compared to static MSRs with a non-zero value on the AMD Ryzen Threadripper 1920X.

| CPU | Number of Zero MSRs | Number of Non-Zero MSRs |
|---|---|---|
| 0 | 4804 | 69 (0.014%) |
| 1 | 4852 | 21 (0.004%) |
| 2 | 4852 | 21 (0.004%) |
| 3 | 4852 | 21 (0.004%) |
| 4 | 4852 | 21 (0.004%) |
| 5 | 4852 | 21 (0.004%) |
| 6 | 4804 | 69 (0.014%) |
| 7 | 4852 | 21 (0.004%) |
| 8 | 4852 | 21 (0.004%) |
| 9 | 4852 | 21 (0.004%) |
| 10 | 4852 | 21 (0.004%) |
| 11 | 4852 | 21 (0.004%) |

**Table 6.2:** Statistical parameters of static non-zero MSRs on the AMD Ryzen Threadripper 1920X.

| CPU | Minimum | Maximum | Median | Mode |
|---|---|---|---|---|
| 0 | 0000000000000001 | d400005d51505800 | 00000000feb00000 | d01a000000000000 (x20) |
| 1 | 0000000000000001 | d400005d51505800 | 000000001808cc17 | 0000000000000001 (x1) |
| 2 | 0000000000000001 | d400005d51505800 | 000000001808cc17 | 0000000000000001 (x1) |
| 3 | 0000000000000001 | d400005d51505800 | 000000001808cc17 | 0000000000000001 (x1) |
| 4 | 0000000000000001 | d400005d51505800 | 000000001808cc17 | 0000000000000001 (x1) |
| 5 | 0000000000000001 | d400005d51505800 | 000000001808cc17 | 0000000000000001 (x1) |
| 6 | 0000000000000001 | d400005d51505800 | 00000000feb00000 | d01a000000000000 (x20) |
| 7 | 0000000000000001 | d400005d51505800 | 000000001808cc17 | 0000000000000001 (x1) |
| 8 | 0000000000000001 | d400005d51505800 | 000000001808cc17 | 0000000000000001 (x1) |
| 9 | 0000000000000001 | d400005d51505800 | 000000001808cc17 | 0000000000000001 (x1) |
| 10 | 0000000000000001 | d400005d51505800 | 000000001808cc17 | 0000000000000001 (x1) |
| 11 | 0000000000000001 | d400005d51505800 | 000000001808cc17 | 0000000000000001 (x1) |

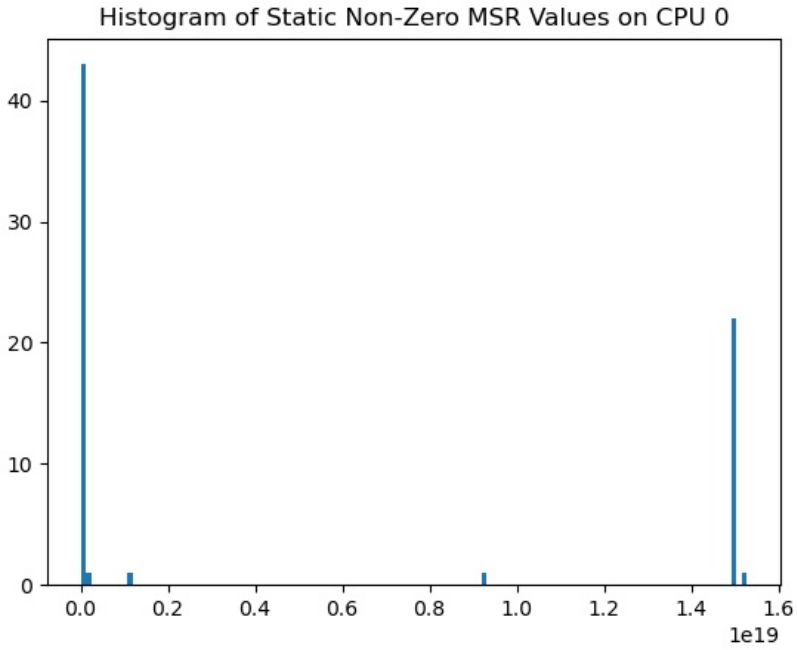



**Figure 6.1:** Histogram of the static non-zero MSR values on the AMD Ryzen Threadripper 1920X on CPU 0.

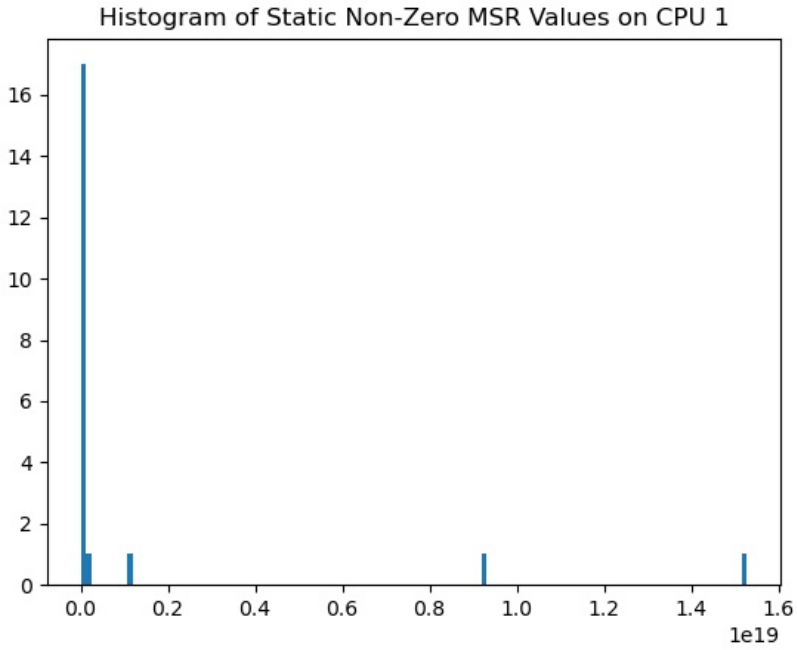



**Figure 6.2:** Histogram of the static non-zero MSR values on the AMD Ryzen Threadripper 1920X on CPU 1.

## 6.2 Intel Core i7-6700K

The Intel Core i7-6700K has a total of 70 undocumented static MSRs that are zero and 29 that are non-zero, see Table 6.3. In Table 6.4 can be seen that the most common value among the undocumented static non-zero MSRs is the same as the minimum, namely 1. The histogram of the non-zero values can be found in Figure 6.3.

**Table 6.3:** Static MSRs with value zero compared to static MSRs with a non-zero value on the Intel Core i7-6700K.

| CPU | Number of Zero MSRs | Number of Non-Zero MSRs |
|---|---|---|
| 0 | 70 | 29 (0.414%) |
| 1 | 70 | 29 (0.414%) |
| 2 | 70 | 29 (0.414%) |
| 3 | 70 | 29 (0.414%) |

**Table 6.4:** Statistical parameters of static non-zero MSRs on the Intel Core i7-6700K.

| CPU | Minimum | Maximum | Median | Mode |
|---|---|---|---|---|
| 0 | 0000000000000001 | fd0cd1679876a800 | 0000000000401cc0 | 0000000000000001 (x6) |
| 1 | 0000000000000001 | fd0cd1679876a800 | 0000000000401cc0 | 0000000000000001 (x6) |
| 2 | 0000000000000001 | fd0cd1679876a800 | 0000000000401cc0 | 0000000000000001 (x6) |
| 3 | 0000000000000001 | fd0cd1679876a800 | 0000000000401cc0 | 0000000000000001 (x6) |

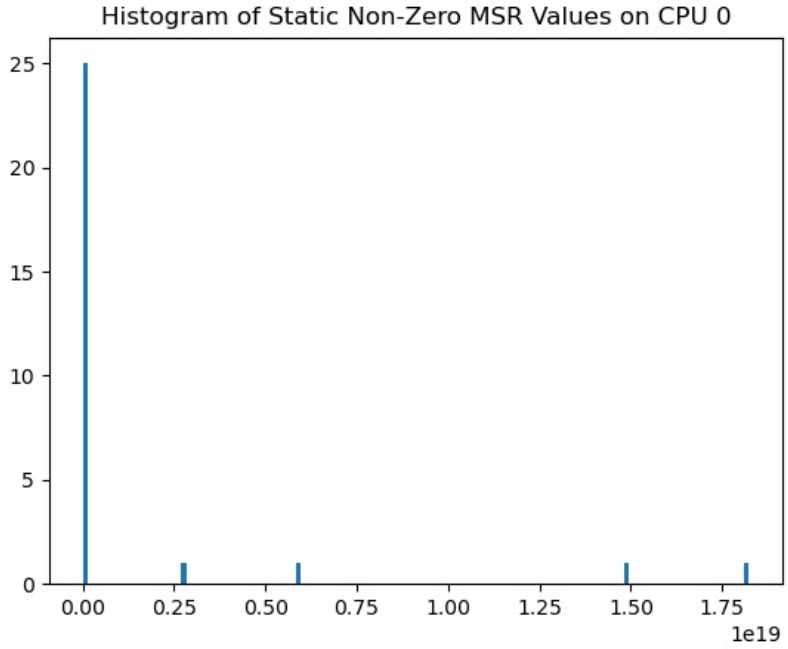



**Figure 6.3:** Histogram of the static non-zero MSR values on the Intel Core i7-6700K on CPU 0.

## 6.3 Intel Core i7-8700K

The Intel Core i7-8700K has a total of 89 undocumented static MSRs that are zero and 32 that are non-zero, see Table 6.5. In Table 6.6 can be seen that the most common value among the undocumented static non-zero MSRs is the same as the minimum, namely 1. The histogram of the non-zero values can be found in Figure 6.4.

**Table 6.5:** Static MSRs with value zero compared to static MSRs with a non-zero value on the Intel Core i7-8700K.

| CPU | Number of Zero MSRs | Number of Non-Zero MSRs |
|---|---|---|
| 0 | 89 | 32 (0.360%) |
| 1 | 89 | 32 (0.360%) |
| 2 | 89 | 32 (0.360%) |
| 3 | 89 | 32 (0.360%) |
| 4 | 89 | 32 (0.360%) |
| 5 | 89 | 32 (0.360%) |
| 6 | 89 | 32 (0.360%) |
| 7 | 89 | 32 (0.360%) |
| 8 | 89 | 32 (0.360%) |
| 9 | 89 | 32 (0.360%) |
| 10 | 89 | 32 (0.360%) |
| 11 | 89 | 32 (0.360%) |

**Table 6.6:** Statistical parameters of static non-zero MSRs on the Intel Core i7-8700K.

| CPU | Minimum | Maximum | Median | Mode |
|---|---|---|---|---|
| 0 | 0000000000000001 | fd0cd1679876a800 | 000000000003c362 | 0000000000000001 (x6) |
| 1 | 0000000000000001 | fd0cd1679876a800 | 000000000003c362 | 0000000000000001 (x6) |
| 2 | 0000000000000001 | fd0cd1679876a800 | 000000000003c362 | 0000000000000001 (x6) |
| 3 | 0000000000000001 | fd0cd1679876a800 | 000000000003c362 | 0000000000000001 (x6) |
| 4 | 0000000000000001 | fd0cd1679876a800 | 000000000003c362 | 0000000000000001 (x6) |
| 5 | 0000000000000001 | fd0cd1679876a800 | 000000000003c362 | 0000000000000001 (x6) |
| 6 | 0000000000000001 | fd0cd1679876a800 | 000000000003c362 | 0000000000000001 (x6) |
| 7 | 0000000000000001 | fd0cd1679876a800 | 000000000003c362 | 0000000000000001 (x6) |
| 8 | 0000000000000001 | fd0cd1679876a800 | 000000000003c362 | 0000000000000001 (x6) |
| 9 | 0000000000000001 | fd0cd1679876a800 | 000000000003c362 | 0000000000000001 (x6) |
| 10 | 0000000000000001 | fd0cd1679876a800 | 000000000003c362 | 0000000000000001 (x6) |
| 11 | 0000000000000001 | fd0cd1679876a800 | 000000000003c362 | 0000000000000001 (x6) |

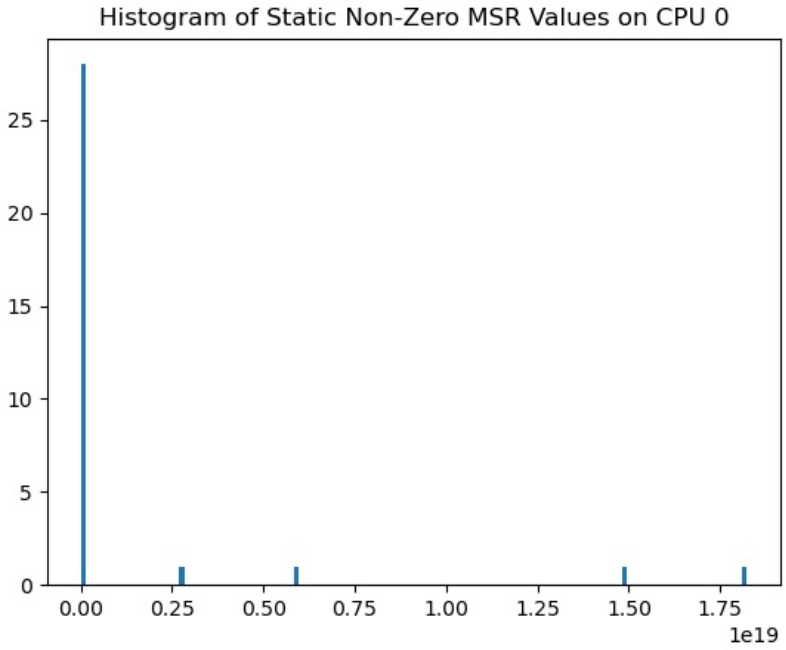



**Figure 6.4:** Histogram of the static non-zero MSR values on the Intel Core i7-8700K on CPU 0.

## 6.4 Intel Core i9-9900K

The Intel Core i9-9900K has a total of 99 undocumented static MSRs that are zero and 33 that are non-zero, see Table 6.7. In Table 6.8 can be seen that the most common value among the undocumented static non-zero MSRs is the same as the minimum, namely 1. The histogram of the non-zero values can be found in Figure 6.5.

**Table 6.7:** Static MSRs with value zero compared to static MSRs with a non-zero value on the Intel Core i9-9900K.

| CPU | Number of Zero MSRs | Number of Non-Zero MSRs |
|---|---|---|
| 0 | 99 | 33 (0.333%) |
| 1 | 99 | 33 (0.333%) |
| 2 | 99 | 33 (0.333%) |
| 3 | 99 | 33 (0.333%) |
| 4 | 99 | 33 (0.333%) |
| 5 | 99 | 33 (0.333%) |
| 6 | 99 | 33 (0.333%) |
| 7 | 99 | 33 (0.333%) |
| 8 | 99 | 33 (0.333%) |
| 9 | 99 | 33 (0.333%) |
| 10 | 99 | 33 (0.333%) |
| 11 | 99 | 33 (0.333%) |
| 12 | 99 | 33 (0.333%) |
| 13 | 99 | 33 (0.333%) |
| 14 | 99 | 33 (0.333%) |
| 15 | 99 | 33 (0.333%) |

**Table 6.8:** Statistical parameters of static non-zero MSRs on the Intel Core i9-9900K.

| CPU | Minimum | Maximum | Median | Mode |
|---|---|---|---|---|
| 0 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |
| 1 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |
| 2 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |
| 3 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |
| 4 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |
| 5 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |
| 6 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |
| 7 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |
| 8 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |
| 9 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |
| 10 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |
| 11 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |
| 12 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |
| 13 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |
| 14 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |
| 15 | 0000000000000001 | fd0cd1679876a800 | 00000000000187ad | 0000000000000001 (x6) |

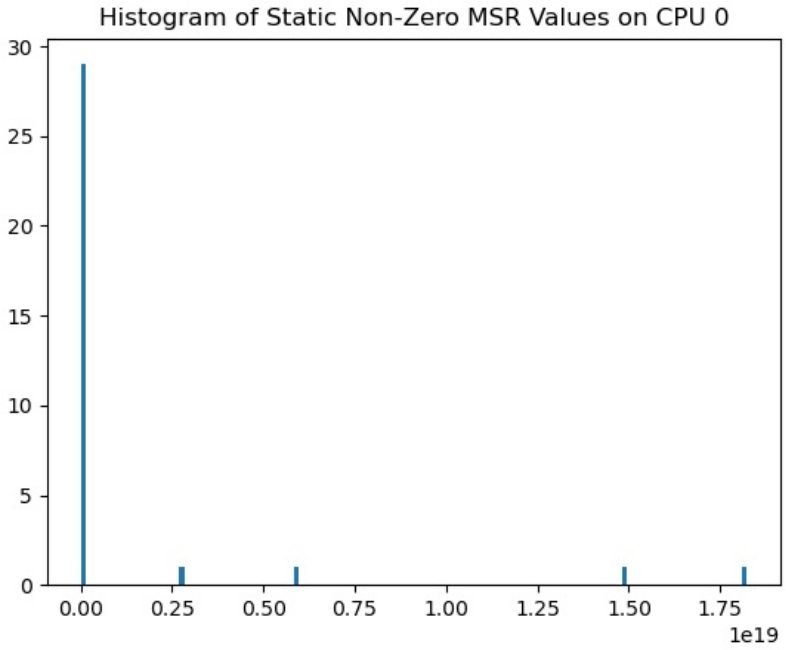



**Figure 6.5:** Histogram of the static non-zero MSR values on the Intel Core i9-9900K on CPU 0.

## 6.5 Intel Xeon Silver 4208

As we can see in Table 6.9 from the 16 CPUs total, 1 CPU has 490 undocumented static MSRs with value zero and 111 non-zero MSRs, 10 CPUs have 488 undocumented static MSRs with value zero and 113 non-zero MSRs, and 5 CPUs have 489 undocumented static MSRs with value zero and 112 non-zero MSRs. Even though there are quite a few irregularities in respect to the amount of zero and non-zero undocumented static MSRs between the different CPUs on the Intel Xeon Silver 4208 the statistical parameters minimum, maximum, median, and mode are the same on all 16 CPUs, see Table 6.10. Figures 6.6, 6.7, and 6.8 are representative histograms of the three different zero to non-zero undocumented static MSR value correlations.

**Table 6.9:** Static MSRs with value zero compared to static MSRs with a non-zero value on the Intel Xeon Silver 4208.

| CPU | Number of Zero MSRs | Number of Non-Zero MSRs |
|---|---|---|
| 0 | 490 | 111 (0.227%) |
| 1 | 488 | 113 (0.232%) |
| 2 | 488 | 113 (0.232%) |
| 3 | 488 | 113 (0.232%) |
| 4 | 488 | 113 (0.232%) |
| 5 | 489 | 112 (0.229%) |
| 6 | 488 | 113 (0.232%) |
| 7 | 488 | 113 (0.232%) |
| 8 | 488 | 113 (0.232%) |
| 9 | 488 | 113 (0.232%) |
| 10 | 489 | 112 (0.229%) |
| 11 | 489 | 112 (0.229%) |
| 12 | 489 | 112 (0.229%) |
| 13 | 489 | 112 (0.229%) |
| 14 | 488 | 113 (0.232%) |
| 15 | 488 | 113 (0.232%) |

**Table 6.10:** Statistical parameters of static non-zero MSRs on the Intel Xeon Silver 4208.

| CPU | Minimum | Maximum | Median | Mode |
|---|---|---|---|---|
| 0 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |
| 1 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |
| 2 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |
| 3 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |
| 4 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |
| 5 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |
| 6 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |
| 7 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |
| 8 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |
| 9 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |
| 10 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |
| 11 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |
| 12 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |
| 13 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |
| 14 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |
| 15 | 0000000000000001 | d7aac184a9664800 | 0000000000030000 | 0000000000030000 (x18) |

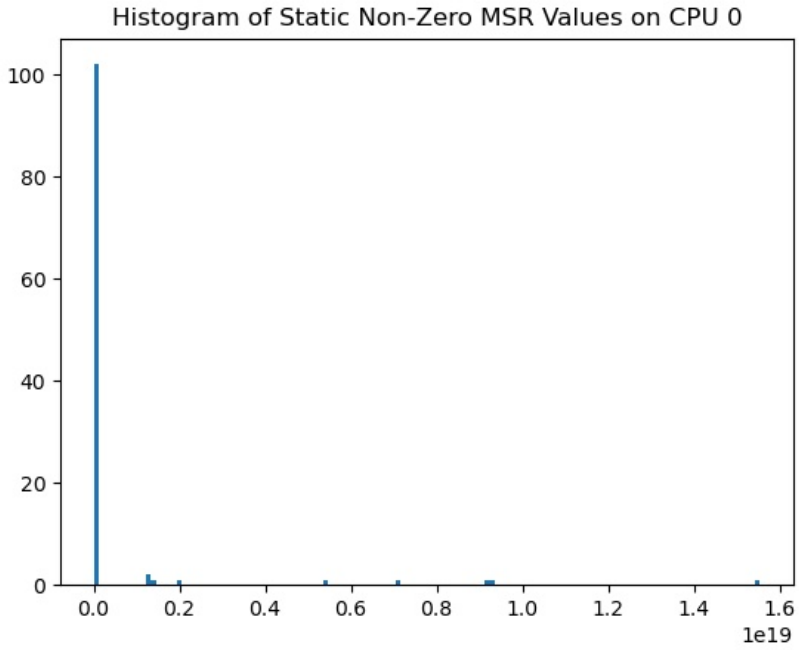



**Figure 6.6:** Histogram of the static non-zero MSR values on the Intel Xeon Silver 4208 on CPU 0.

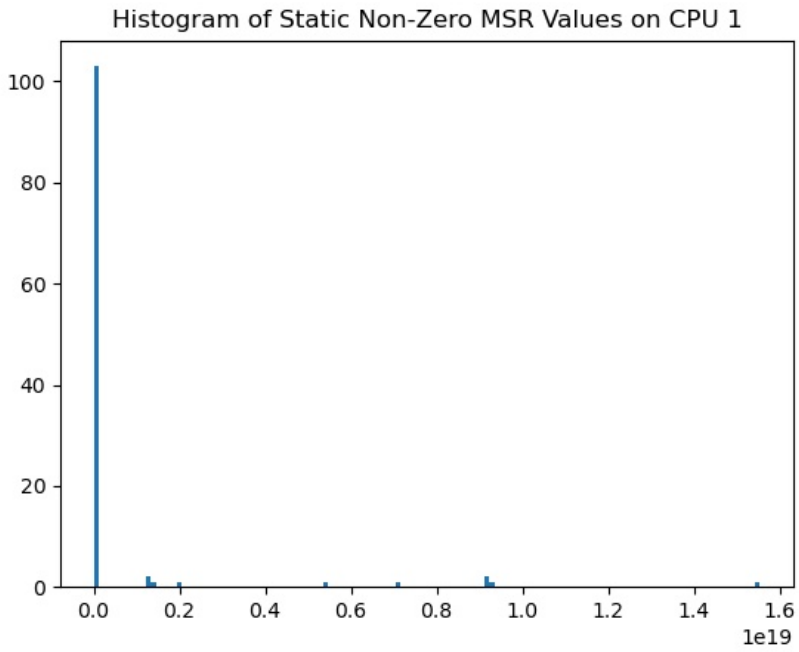



**Figure 6.7:** Histogram of the static non-zero MSR values on the Intel Xeon Silver 4208 on CPU 1.

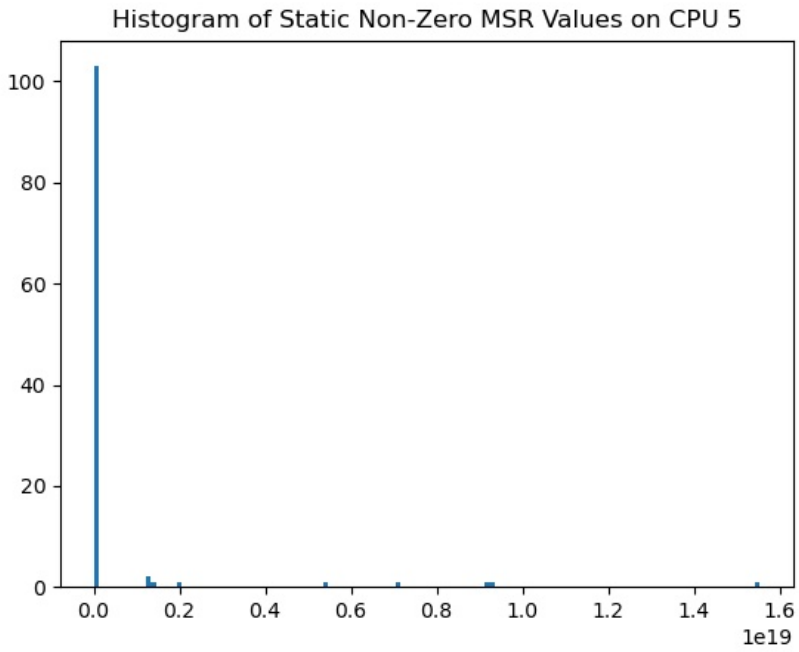



**Figure 6.8:** Histogram of the static non-zero MSR values on the Intel Xeon Silver 4208 on CPU 5.

## 6.6 Findings

The tested Intel Core series CPUs do not have any anomalies in the evaluated statistical parameters. However, the tested Intel Xeon Silver 4208 and the tested AMD Ryzen Threadripper 1920X show certain irregularities when it comes to the amount of zero and non-zero values of their undocumented static MSRs. The AMD Ryzen Threadripper 1920X even shows irregularities in the statistical parameters of it's non-zero undocumented static MSR values. These differences might indicate that the individual CPUs may not have the exact same properties or may even have differences on the transistor layer.

# Chapter 7

# Analysis of Undocumented Dynamic MSRs

In this chapter, we will explore all undocumented MSRs with dynamic values and draw conclusions from the data we gather.

## 7.1 Initial Data Gathering

To find out which MSRs are dynamic, we sample, per CPU, all undocumented MSRs at once for 180 seconds. We then filter for MSRs, which yielded different values during the scan by using the changes function of msrs_analyze. The results can be found in Table 7.1.

Although the AMD Ryzen CPU has the most undocumented MSRs, 4875 in total, it has only two undocumented MSRs with dynamic values, which is a similar number as the tested Intel Core series CPUs implement (2 to 4). It is quite notable that the undocumented dynamic MSRs of the tested Intel Core series CPUs seem to be a subset of the undocumented dynamic MSRs of the Intel Core i7-6700K CPU. By far the most undocumented dynamic MSRs, 42 to be exact, are implemented in the Intel Xeon Silver 4208 server CPU.

**Table 7.1:** Summarized results of the search for dynamic MSRs.

| CPU | Number of Undocumented MSRs | Number of Undocumented Dynamic MSRs | Undocumented Dynamic MSRs |
|---|---|---|---|
| Ryzen Threadripper 1920X [2] | 4875 | 2 (0.0004%) | c0010293<br>c0011083 |
| Core i7-6700K [11] | 104 | 4 (0.0385%) | 4e2<br>1a1<br>621<br>637 |
| Core i7-8700K [12] | 124 | 3 (0.0242%) | 1a1<br>621<br>637 |
| Core i9-9900K [13] | 134 | 2 (0.0149%) | 1a1<br>637 |
| Xeon Silver 4208 [15] | 643 | 42 (0.0653%) | see appendix<br>Section 10.2 |

## 7.2 Cross Correlation

From the addresses of the documented and undocumented dynamic MSRs, we draw conclusions from their values by correlating them to documented dynamic MSRs. For this, we sample all documented and undocumented dynamic MSRs together for 60 seconds. During the sampling, we execute a CPU stress test that spins on a square root function for a few seconds, which will, among others, trigger spikes in electricity and temperature sensor readings, which in turn makes the correlation between such registers more clear.

## 7.3 Intel Core CPUs

As mentioned in Section 7.1, we found that the tested Intel Core processors share addresses of undocumented dynamic MSRs. We found that they seem to have the same functionality, although some have different value offsets. In this section, we analyze them in more detail.

### 7.3.1 A Package Thermal Margin MSR (0x1a1)

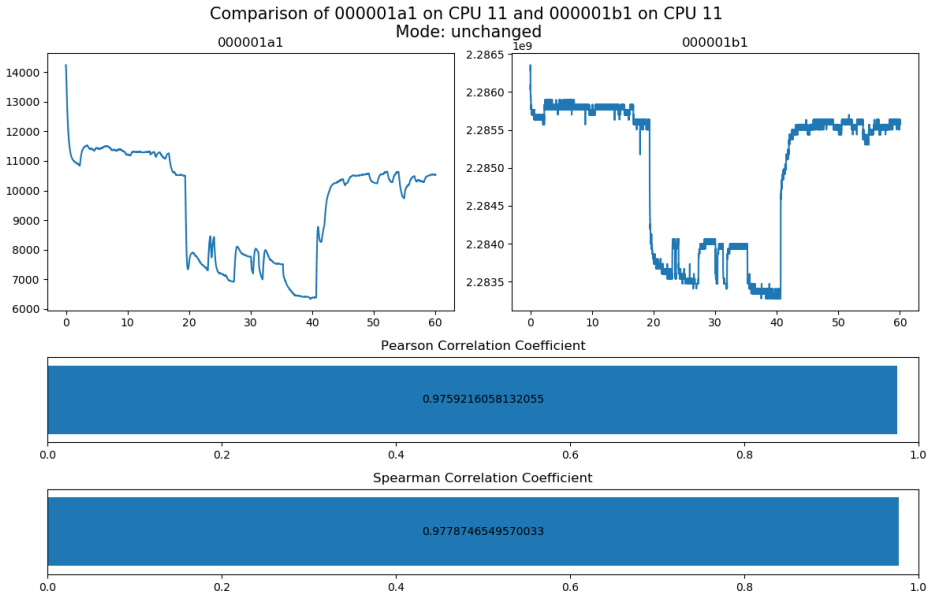



**Figure 7.1:** Correlation of MSR 0x1a1 and the IA32_PACKAGE_THERM_STATUS MSR (0x1b1) on the Intel Core i7-8700K.

The MSR 0x1a1 has an obvious correlation with the IA32_PACKAGE_THERM_STATUS MSR (0x1b1) on all tested CPUs as shown in Figure 7.1 and Appendix Section 10.3.2. Additionally, we observe other, less strong, correlations to thermally, and performance-related MSRs on different Intel Core CPUs such as IA32_PERF_STATUS (0x198) on the Core i7-6700K, and IA32_THERM_STATUS (0x19c) on the Core i7-8700K. We can, therefore, conclude that the 0x1a1 MSR is affected by thermal changes within the CPU. However, it does not seem to be a direct temperature sensor reading as the value decreases when the CPU load increases and the CPU generates more heat. This conclusion matches a statement made in an Intel forum post [34] claiming the 0x1a1 register being the IA32_PACKAGE_THERM_MARGIN MSR.

### 7.3.2 A State Register (0x621)

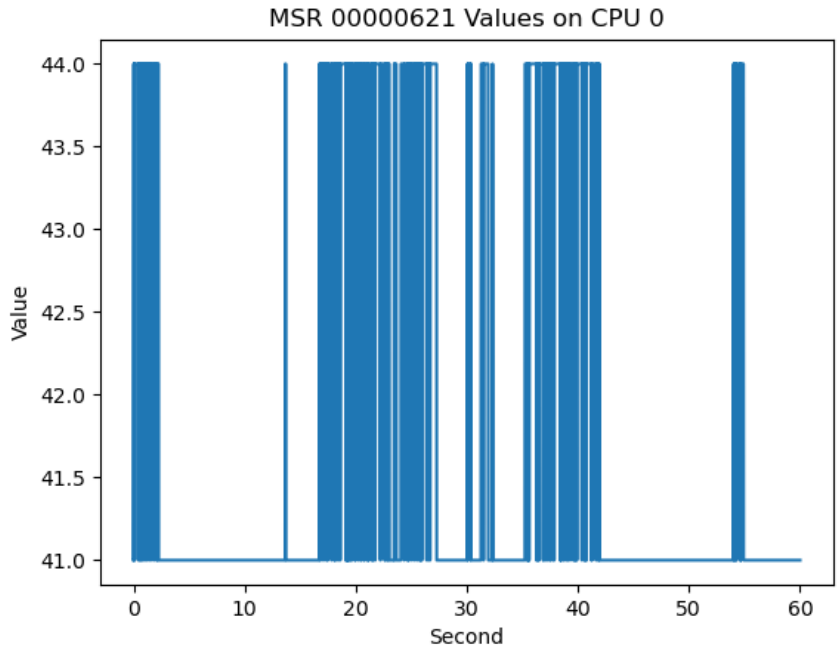



**Figure 7.2:** Values of MSR 0x621 on the Intel Core i7-8700K.

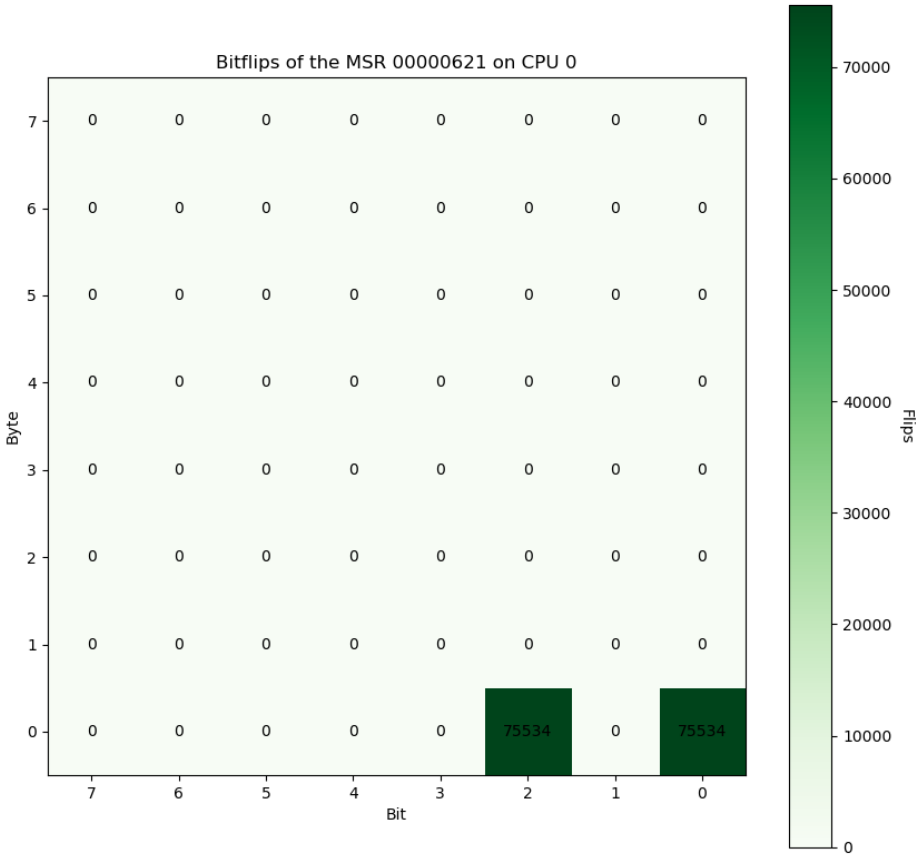



**Figure 7.3:** Bit-flip map of MSR 0x621 on the Intel Core i7-8700K.

MSR 0x621 correlates with two performance counter state registers, but only on Core i7-8700K. The correlation with MSR_RING_PERF_LIMIT_REASONS (0x6b1) is nearly a complete negative. The second correlation with MSR_PERF_STATUS (0x198) is weaker but still above 71% for Pearson and above 82% for Spearman. In Figure 7.2 we can see that the sampled values of MSR 0x621 alternate between 41 and 44, indicating alternating bit flips of bit zero and bit two, see Figure 7.3. This behavior suggests that this register represents at least two states that are mutually exclusive.

### 7.3.3 A RAPL or Performance Counter MSR (0x637)

MSR 0x637 correlates very strongly with the same nine documented MSRs on all Intel Core CPUs: MSR 0x10, MSR 0x659, MSR 0x619, MSR 0x658, MSR 0x611, MSR 0x639, MSR 0xe7, MSR 0xe8, and MSR 0x64e. For a full set of correlations with these MSRs on all tested Intel Core CPUs see Section 10.3.2 in the appendix. On the Core i7-9900K, it

additionally correlates with MSR IA32_FIXED_CTR1 (0x30a), which is a performance counter, see figure 7.5. Out of these nine MSRs, six are performance counters, and three are RAPL (Running Average Power Limit) registers [9]. We can see, for example, in Figure 7.4 that the curve has the same spike as the RAPL registers when the stress test begins and thus power consumption increases. For this reason, we think that this register is a RAPL register instead of a performance counter. However, we do not have any evidence of this register not being a performance counter.

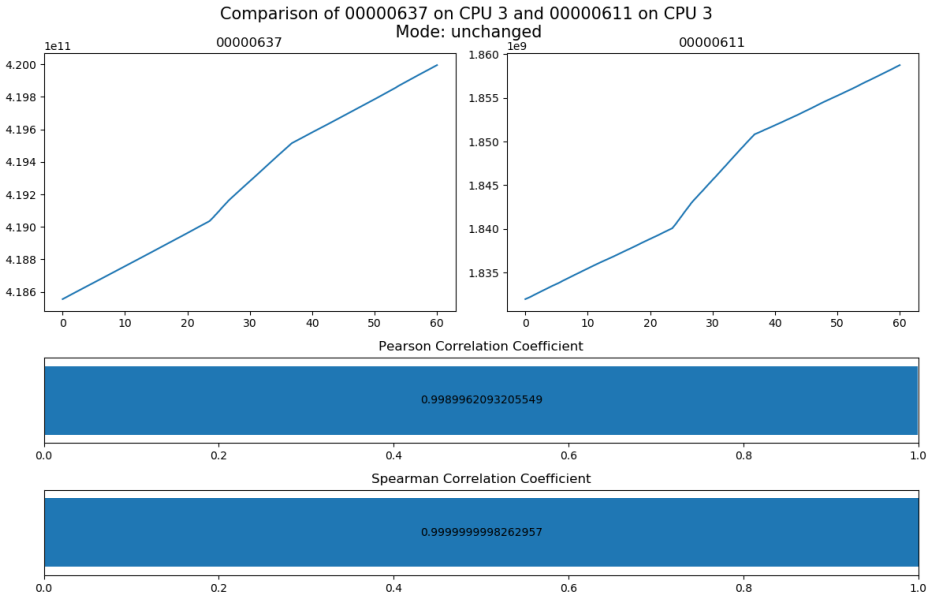



**Figure 7.4:** Correlation of MSR 0x637 and MSR_PKG_ENERGY_STATUS (0x611) on the Intel Core i7-6700K.

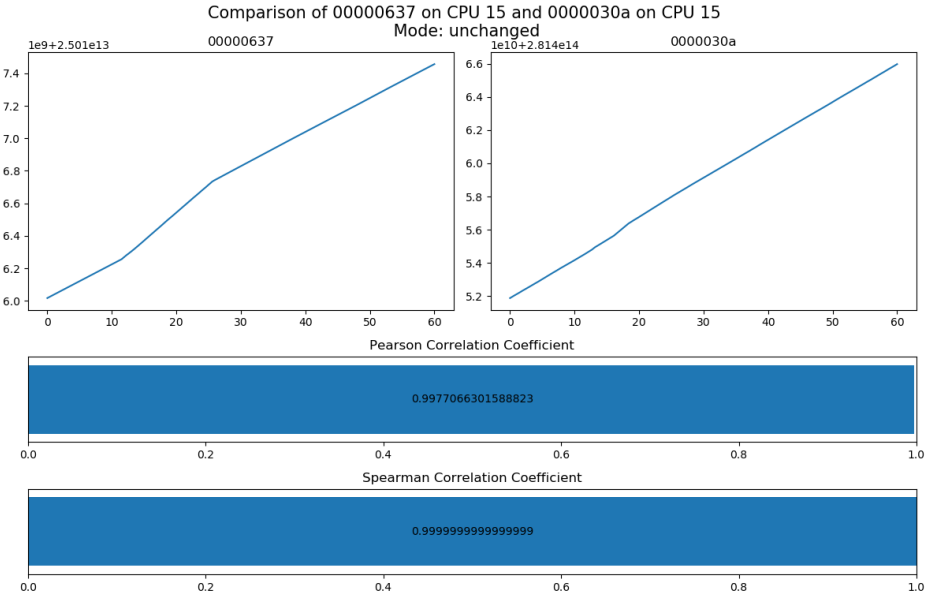



**Figure 7.5:** Correlation of MSR 0x637 and MSR IA32_FIXED_CTR1 (0x30a).

### 7.3.4 A System Management Mode MSR (0x4e2)?

On the Intel Core i7-6700K, we found a dynamic MSR that has no notable correlation to other MSRs. As of the Intel manual [9], the family of this particular CPU, specifically with the DisplayFamily_DisplayModel signatures of 06_5EH, has its documented MSRs, besides the architectural MSRs, listed in Tables 2-20, 2-21, 2-25, 2-29, 2-35, 2-39, and 2-40 [9]. The only occurrence of 0x4e2, however, is in Tables 2-12 [9] and 2-30 [9], thus it is only documented for other microarchitectures. It is also mentioned in Section 34.17.2 SMI Delivery Delay Reporting of the Intel manual [9]. In these occurrences, the register is described as being a state indicator if the servicing of a system management interrupt is delayed. It is further noted that this register may only be queried in system management mode, and attempts to query it outside of system management mode will result in a general protection fault.

In the Plots 7.6, 7.7, and 7.8 we see that we have bit flips of the lowest four bits which correspond to the logical cores of the system, as hyper-threading was disabled in the BIOS during the sampling. This behavior matches the register's description for other microarchitectures, except that it is accessible from kernelspace. To verify that this undocumented MSR is indeed the MSR_SMM_DELAYED described in the Intel manual [9], further experiments are needed that would be beyond the scope of this thesis.

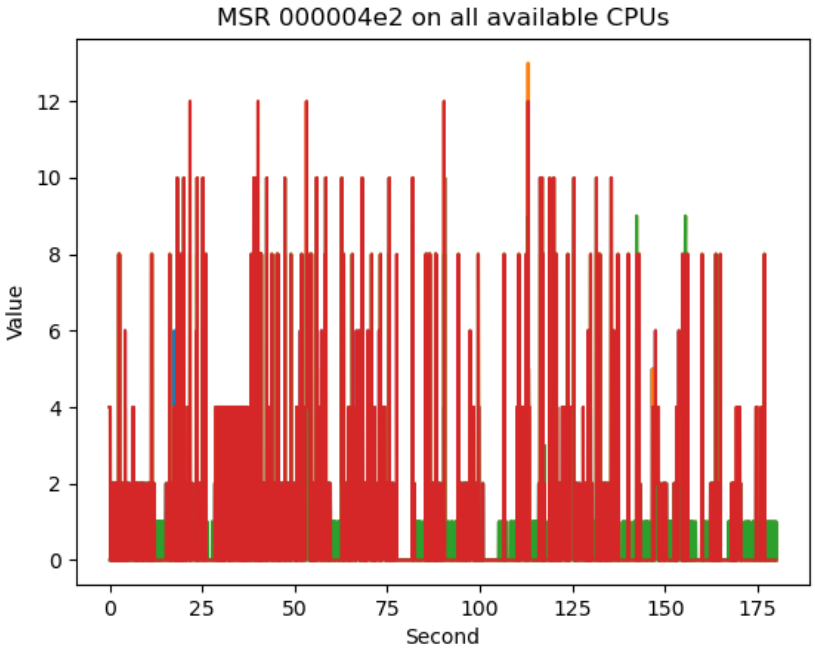



**Figure 7.6:** Values of MSR 0x4e2 on the Intel Core i7-6700K. Please note that at the time of sampling hyper-threading was deactivated in BIOS and thus this experiment was conducted only on the 4 physical cores of this CPU.

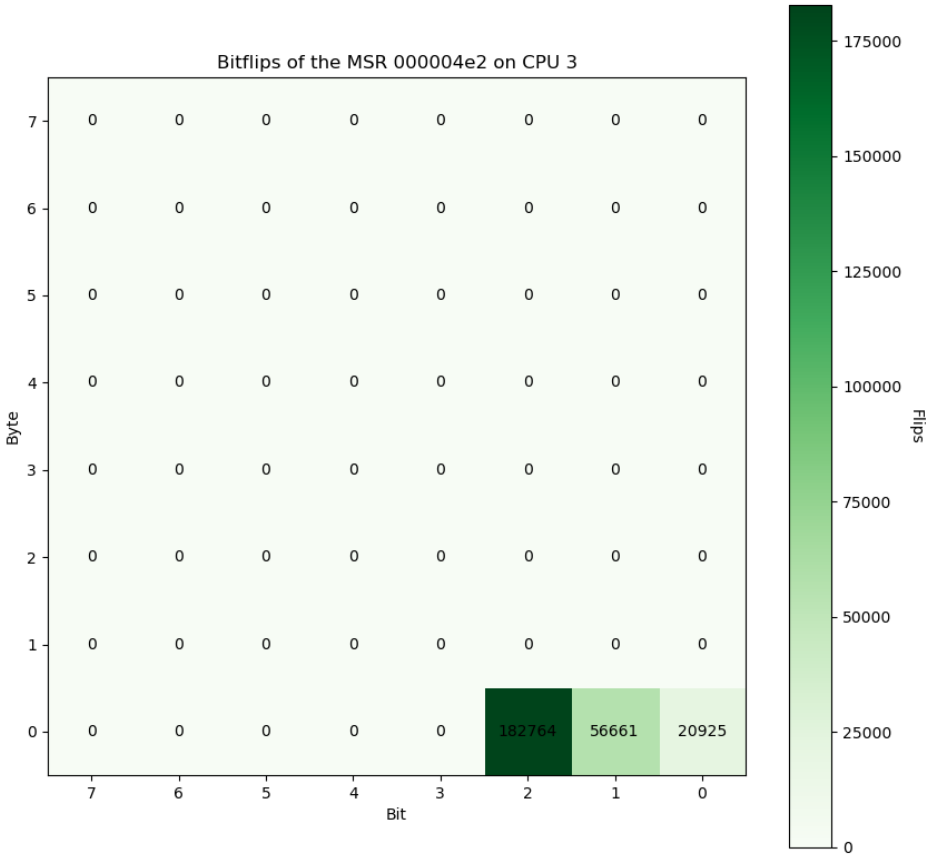



**Figure 7.7:** Bit-flip map of MSR 0x64e2 on the Intel Core i7-6700K on CPU 3. Please note that at the time of sampling hyper-threading was deactivated in BIOS and thus this experiment was conducted only on the 4 physical cores of this CPU.

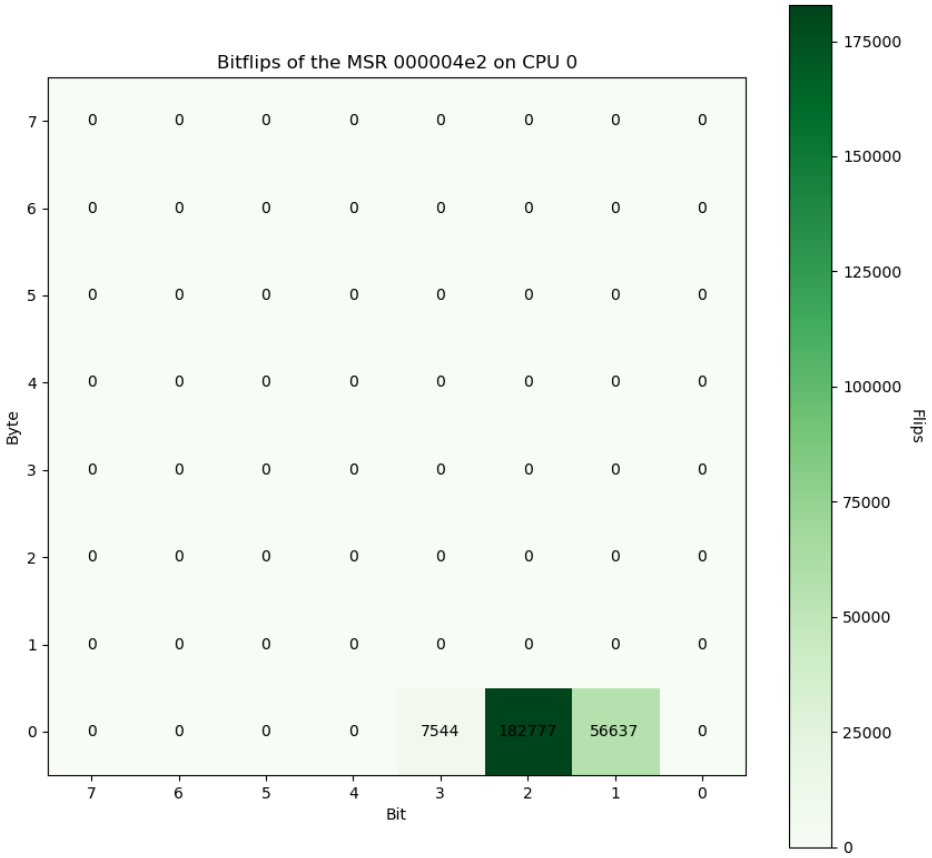



**Figure 7.8:** Bit-flip map of MSR 0x64e2 on the Intel Core i7-6700K on CPU 0. Please note that at the time of sampling hyper-threading was deactivated in BIOS and thus this experiment was conducted only on the 4 physical cores of this CPU.

## 7.4 Intel Xeon Silver 4208

As can be seen in Table 7.1, our Xeon CPU, the Xeon Silver 4208, has 42 undocumented dynamic MSRs which is, compared to the other tested CPUs, by far the most. When looking at its registers, we can see that it shares some undocumented dynamic MSRs with the Intel Core CPUs. Specifically 0x1a1, and 0x637. These MSRs share the same properties, which means the assumed classification of these MSRs from Section 7.3 holds for the Intel Xeon Silver 4208 as well. In this section, we will examine these registers in more detail.

### 7.4.1 Another Thermally Related MSR (0x1a3)

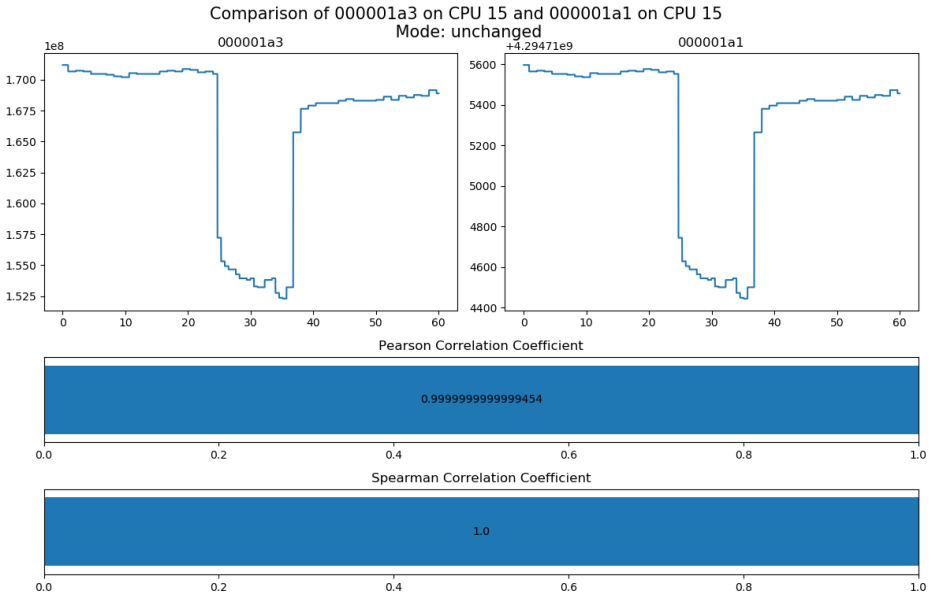



**Figure 7.9:** Correlation of MSR 0x1a3 and 0x1a1.

Interestingly, we found an undocumented dynamic MSR, 0x1a3 to be specific, that yielded the exact same output curve as the register 0x1a1, see Figure 7.9. The difference only being the offset as well as the scaling. From the plot, we can further deduce that MSR 0x1a3 reads the data from the same sensor as MSR 0x1a1 does but transforms them in a specific way.

### 7.4.2 40 RAPL or Performance Counter MSRs

The remaining 40 dynamic undocumented MSRs, including 0x637, all correlate with each other. Except for 0xb05, the correlations are nearly complete for both Spearman as well as Pearson, see Figure 7.10 for an example, which means that the conclusions we draw for 0x637 in Section 7.3 still hold for these 40 registers.

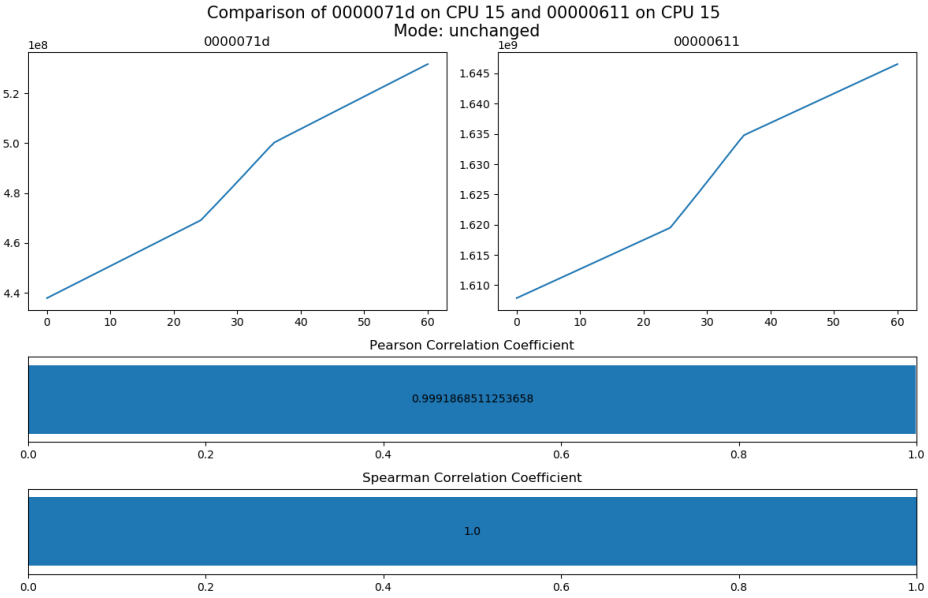



**Figure 7.10:** Correlation of MSR 0x71d and 0x611.

As the correlation between 0xb05 and 0x637 is still very strong, see Figure 7.11, with $r > 0.977$ for Pearson and $r > 0.999$ for Spearman, we conclude that 0xb05 is also a RAPL or Performance Counter MSR as 0x637.

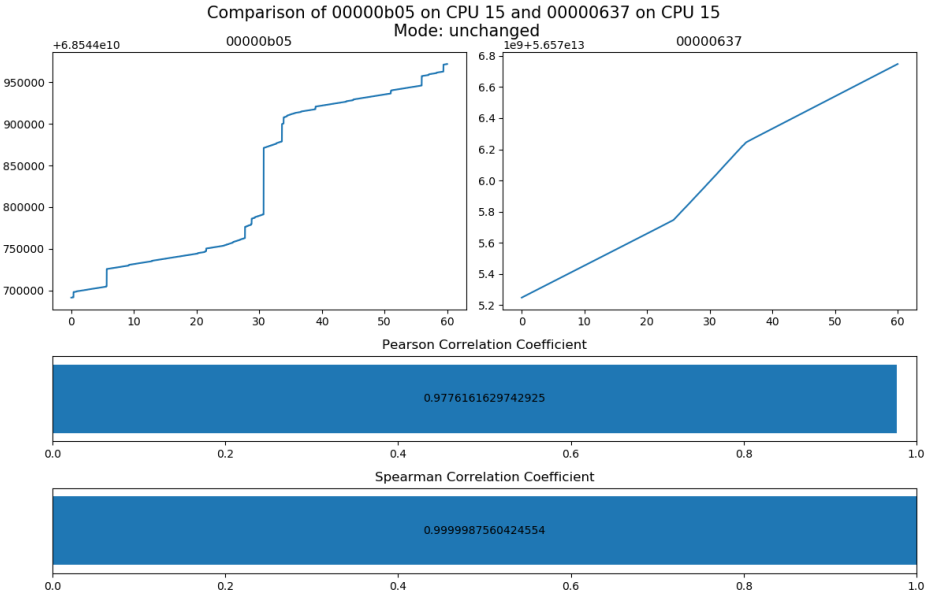



**Figure 7.11:** Correlation of MSR 0xb05 and 0x637.

A full set of relevant, i.e. ($r \geq 0.75$), correlations of MSR 0x637, which includes all other 39 MSRs discussed in this subsection, can be found in the appendix in Section 10.3.1.

## 7.5 AMD Ryzen 7 CPU

On our Ryzen 7 CPU, we found only two undocumented dynamic MSRs that do not correlate with any documented MSR, namely 0xc0010293 and 0xc0011083. For more information on these MSRs see Figures 7.12, 7.13, 7.14, and 7.15 respectively.

Further research, that would be beyond the scope of this thesis, is needed to reverse engineer these registers.

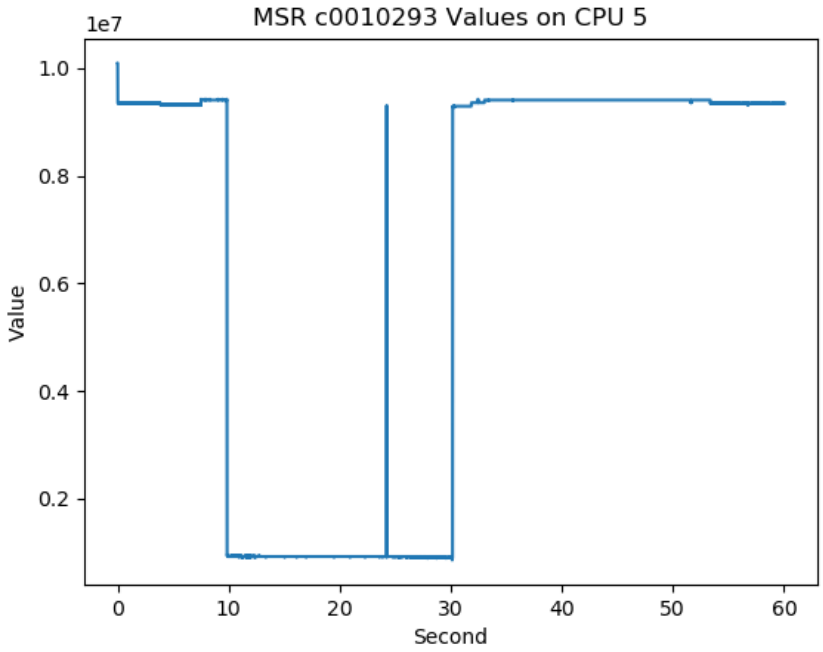



**Figure 7.12:** Value curve of MSR 0xc0010293 on the AMD Ryzen Threadripper 1920X on CPU 5.

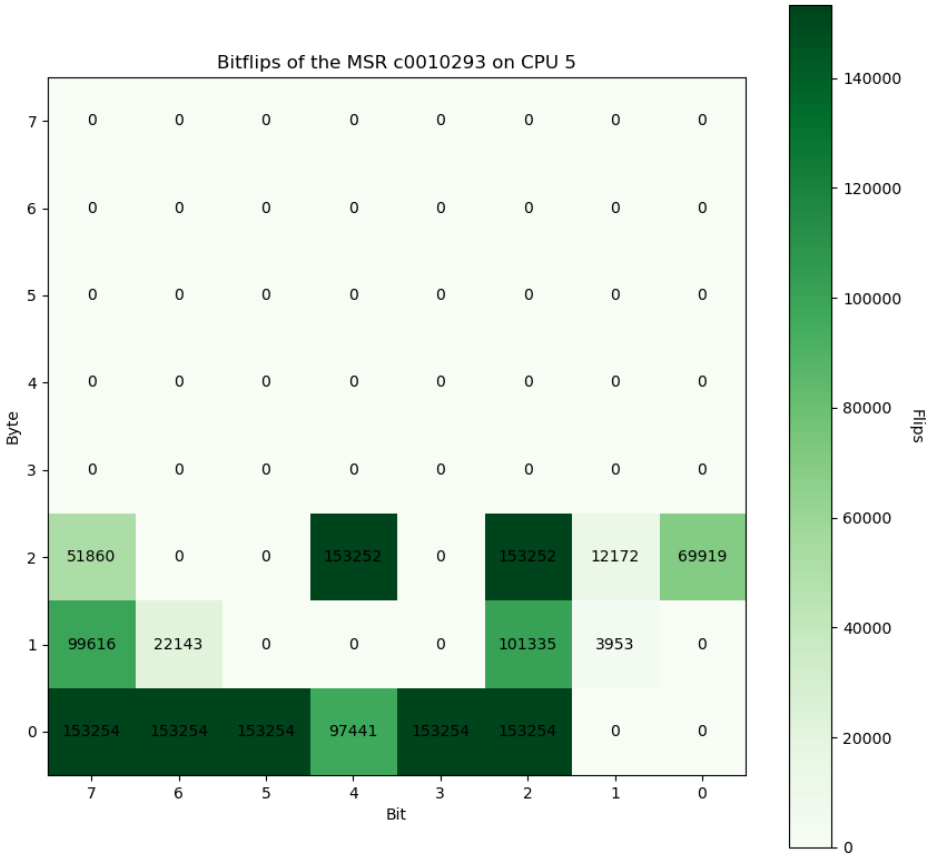



**Figure 7.13:** Bit-flip map of MSR 0xc0010293 on the AMD Ryzen Threadripper 1920X on CPU 5.

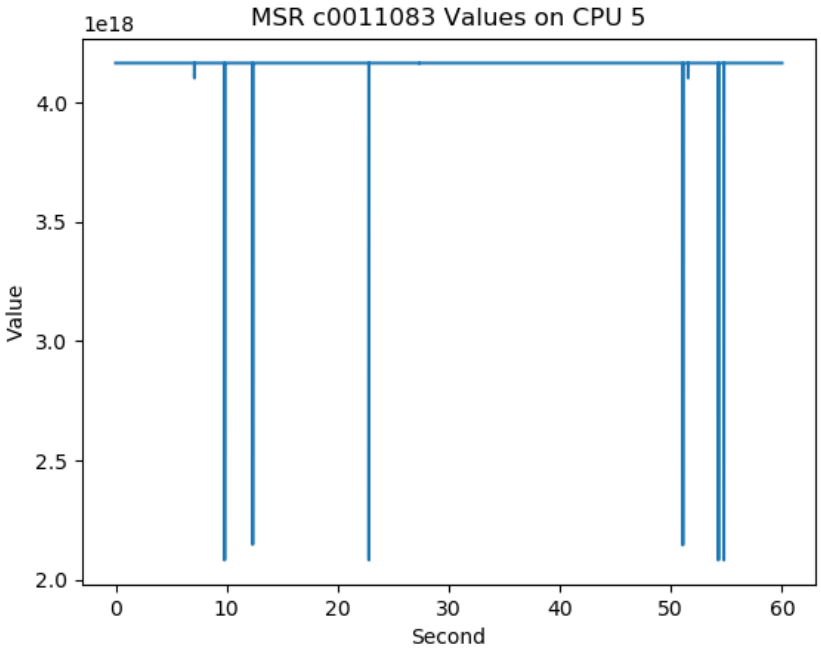



**Figure 7.14:** Value curve of MSR 0xc0011083 on the AMD Ryzen Threadripper 1920X on CPU 5.

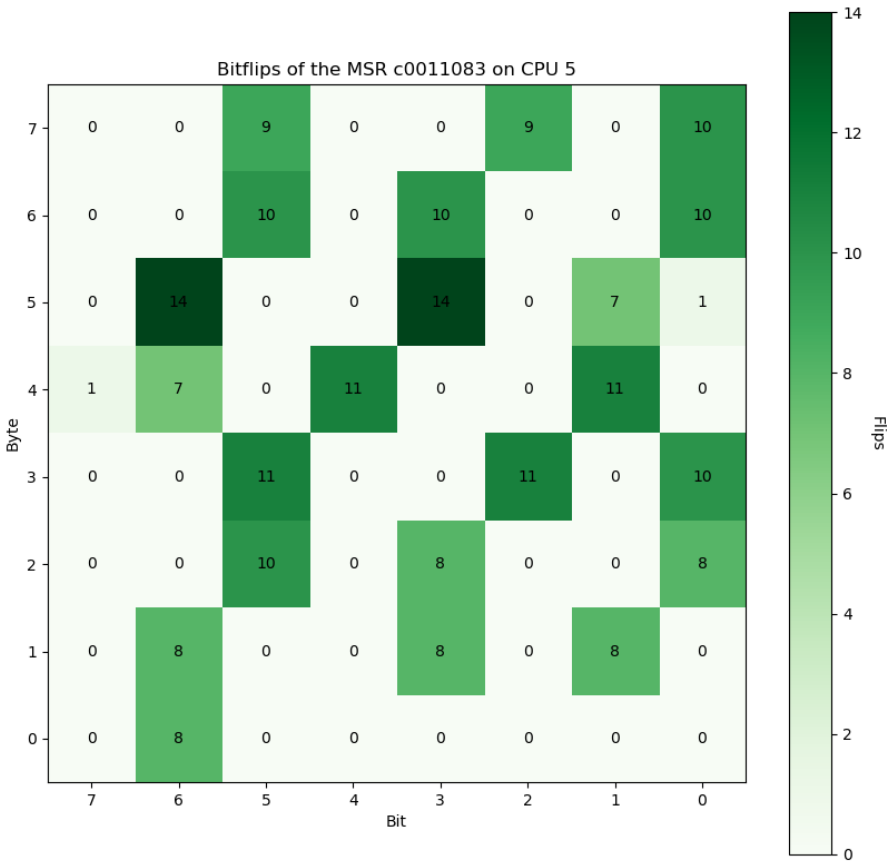



**Figure 7.15:** Bit-flip map of MSR 0xc0011083 on the AMD Ryzen Threadripper 1920X on CPU 5.

# Chapter 8

# Future Work

Simplified, MSRs can be used to read values, for example, of a sensor or states, enable or disable CPU features via individual bits, or configure CPU features. MSRs may even combine multiple categories. For example, they can have a 63 bit counter of some sort and one bit that can be used to reset the counter. In this thesis, we covered a part of the **read values** category, specifically the part of undocumented dynamic MSRs, which means that there is a wide range of unresearched categories of MSRs that we discuss in detail below.

## 8.1 Nomenclature

To make things easier, we decided to name the found categories described above.

- **Value-MSRs** these are MSRs that hold values. These values can either be dynamic or static. They can describe various things, such as readings or initialization values.
- **Flag-MSRs** these are MSRs that contain one or more bits that enable or disable CPU features.
- **Hybrid-MSRs** these are MSRs that combine Value-MSRs and Flag-MSRs

## 8.2 Value-MSRs

We found 53 undocumented dynamic MSRs on the CPUs we conducted our experiments on and determined their correlation and thus possible purpose. However, further research is needed to reverse-engineer what exactly these registers are there for.

Research also has to be conducted in the direction of static Value-MSRs.

## 8.3 Flag-MSRs

Flag-MSRs can be quite interesting for researchers working with microarchitectures as they might enable or disable certain CPU features that allow for faster, more efficient, more accurate, or even new research. As an example, there may be bits that disable certain pre-fetchers or security checks. Such bits may be hidden within the undocumented/reserved bits of documented MSRs or in entirely undocumented MSRs. A documented example is bit 9 of MSR 0x1a0 that can be used to disable the hardware prefetcher. This MSR is documented in Table 2-2 in Chapter 2 of Volume 4 of the Intel manual [9].

## 8.4 Hybrid-MSRs

Future research should note that MSRs may not strictly be Flag-MSRs or Value-MSRs but may very well be Hybrid-MSRs, which are a mixture of the two.

# Chapter 9

# Conclusion

In this thesis, we successfully developed a software toolset laying the foundation for future undocumented MSR based research. Furthermore, we conducted first experiments, foundational data gathering, and present techniques on how to categorize undocumented dynamic MSRs via cross-correlation. To summarize, we found 5880 undocumented MSRs with a share of 53 dynamic MSRs. We were able to categorize 43 dynamic MSRs and draw conclusions for them as to what their data tells us. On the AMD Ryzen Threadripper 1920X and the Intel Xeon Silver 4208 we found irregularities in the examined statistical parameters of the undocumented static MSRs that are the base for our hypothesis that there may be physical differences between the individual CPUs. As a last point, we discussed possible future work based on the findings and results of this thesis.

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# Chapter 10

# Appendix

## 10.1 Found Undocumented MSRs

### 10.1.1 AMD Ryzen Threadripper 1920X

| | | | | | |
|---|---|---|---|---|---|
| 401 | 402 | 410 | 411 | 424 | 42b |
| 420 | 421 | 422 | 423 | 42a | 431 |
| 426 | 427 | 428 | 429 | 430 | 437 |
| 42c | 42d | 42e | 42f | 436 | 441 |
| 432 | 433 | 434 | 435 | 440 | 447 |
| 438 | 439 | 43a | 43b | 446 | 455 |
| 442 | 443 | 444 | 445 | 454 | 45f |
| 448 | 449 | 44a | 44b | 45e | 465 |
| 456 | 457 | 45c | 45d | 464 | 46b |
| 460 | 461 | 462 | 463 | 46a | 471 |
| 466 | 467 | 468 | 469 | 470 | 477 |
| 46c | 46d | 46e | 46f | 476 | 47d |
| 472 | 473 | 474 | 475 | 47c | c000040a |
| 478 | 479 | 47a | 47b | c0000409 | c0002007 |
| 47e | 47f | da0 | c0000408 | c000040f | c000200f |
| c000040b | c000040c | c000040d | c000040e | c000200e | c000201c |
| c000200a | c000200b | c000200c | c000200d | c000201b | c000202b |
| c0002017 | c0002018 | c0002019 | c000201a | c000202a | c0002038 |
| c000201d | c000201e | c000201f | c0002027 | c0002037 | c000203e |
| c000202c | c000202d | c000202e | c000202f | c000203d | c0002044 |
| c0002039 | c000203a | c000203b | c000203c | c0002043 | c000204a |
| c000203f | c0002040 | c0002041 | c0002042 | c0002049 | c0002057 |
| c0002045 | c0002046 | c0002047 | c0002048 | c000204f | c000205d |
| c000204b | c000204c | c000204d | c000204e | c000205c | c000206a |
| c0002058 | c0002059 | c000205a | c000205b | c0002069 | c0002070 |

| | | | | | |
|---|---|---|---|---|---|
| c000205e | c000205f | c0002067 | c0002068 | c000206f | c000207b |
| c000206b | c000206c | c000206d | c000206e | c000207a | c0002081 |
| c0002071 | c0002072 | c0002073 | c0002077 | c0002080 | c000208c |
| c000207c | c000207d | c000207e | c000207f | c000208b | c0002092 |
| c0002082 | c0002083 | c0002087 | c000208a | c0002091 | c000209d |
| c000208d | c000208e | c000208f | c0002090 | c000209c | c00020a3 |
| c0002093 | c0002097 | c000209a | c000209b | c00020a2 | c00020ae |
| c000209e | c000209f | c00020a0 | c00020a1 | c00020ad | c00020b7 |
| c00020a7 | c00020aa | c00020ab | c00020ac | c00020b3 | c00020bf |
| c00020af | c00020b0 | c00020b1 | c00020b2 | c00020be | c00020ca |
| c00020ba | c00020bb | c00020bc | c00020bd | c00020c7 | c00020d0 |
| c00020c0 | c00020c1 | c00020c2 | c00020c3 | c00020cf | c00020db |
| c00020cb | c00020cc | c00020cd | c00020ce | c00020da | c00020ea |
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| c001059a | c001059b | c001059c | c001059d | c00105a4 | c00105ab |
| c00105a0 | c00105a1 | c00105a2 | c00105a3 | c00105aa | c00105b1 |
| c00105a6 | c00105a7 | c00105a8 | c00105a9 | c00105b0 | c00105b7 |
| c00105ac | c00105ad | c00105ae | c00105af | c00105b6 | c00105bd |
| c00105b2 | c00105b3 | c00105b4 | c00105b5 | c00105bc | c00105c3 |
| c00105b8 | c00105b9 | c00105ba | c00105bb | c00105c2 | c00105c9 |
| c00105be | c00105bf | c00105c0 | c00105c1 | c00105c8 | c00105cf |
| c00105c4 | c00105c5 | c00105c6 | c00105c7 | c00105ce | c00105d5 |
| c00105ca | c00105cb | c00105cc | c00105cd | c00105d4 | c00105db |
| c00105d0 | c00105d1 | c00105d2 | c00105d3 | c00105da | c00105e1 |
| c00105d6 | c00105d7 | c00105d8 | c00105d9 | c00105e0 | c00105e7 |

| | | | | | |
|---|---|---|---|---|---|
| c00105dc | c00105dd | c00105de | c00105df | c00105e6 | c00105ed |
| c00105e2 | c00105e3 | c00105e4 | c00105e5 | c00105ec | c00105f3 |
| c00105e8 | c00105e9 | c00105ea | c00105eb | c00105f2 | c00105f9 |
| c00105ee | c00105ef | c00105f0 | c00105f1 | c00105f8 | c00105ff |
| c00105f4 | c00105f5 | c00105f6 | c00105f7 | c00105fe | c0010605 |
| c00105fa | c00105fb | c00105fc | c00105fd | c0010604 | c001060b |
| c0010600 | c0010601 | c0010602 | c0010603 | c001060a | c0010611 |
| c0010606 | c0010607 | c0010608 | c0010609 | c0010610 | c0010617 |
| c001060c | c001060d | c001060e | c001060f | c0010616 | c001061d |
| c0010612 | c0010613 | c0010614 | c0010615 | c001061c | c0010623 |
| c0010618 | c0010619 | c001061a | c001061b | c0010622 | c0010629 |
| c001061e | c001061f | c0010620 | c0010621 | c0010628 | c001062f |
| c0010624 | c0010625 | c0010626 | c0010627 | c001062e | c0010635 |
| c001062a | c001062b | c001062c | c001062d | c0010634 | c001063b |
| c0010630 | c0010631 | c0010632 | c0010633 | c001063a | c0010641 |
| c0010636 | c0010637 | c0010638 | c0010639 | c0010640 | c0010647 |
| c001063c | c001063d | c001063e | c001063f | c0010646 | c001064d |
| c0010642 | c0010643 | c0010644 | c0010645 | c001064c | c0010653 |
| c0010648 | c0010649 | c001064a | c001064b | c0010652 | c0010659 |
| c001064e | c001064f | c0010650 | c0010651 | c0010658 | c001065f |
| c0010654 | c0010655 | c0010656 | c0010657 | c001065e | c0010665 |
| c001065a | c001065b | c001065c | c001065d | c0010664 | c001066b |
| c0010660 | c0010661 | c0010662 | c0010663 | c001066a | c0010671 |
| c0010666 | c0010667 | c0010668 | c0010669 | c0010670 | c0010677 |
| c001066c | c001066d | c001066e | c001066f | c0010676 | c001067d |
| c0010672 | c0010673 | c0010674 | c0010675 | c001067c | c0010683 |
| c0010678 | c0010679 | c001067a | c001067b | c0010682 | c0010689 |
| c001067e | c001067f | c0010680 | c0010681 | c0010688 | c001068f |
| c0010684 | c0010685 | c0010686 | c0010687 | c001068e | c0010695 |
| c001068a | c001068b | c001068c | c001068d | c0010694 | c001069b |
| c0010690 | c0010691 | c0010692 | c0010693 | c001069a | c00106a1 |
| c0010696 | c0010697 | c0010698 | c0010699 | c00106a0 | c00106a7 |
| c001069c | c001069d | c001069e | c001069f | c00106a6 | c00106ad |
| c00106a2 | c00106a3 | c00106a4 | c00106a5 | c00106ac | c00106b3 |
| c00106a8 | c00106a9 | c00106aa | c00106ab | c00106b2 | c00106b9 |
| c00106ae | c00106af | c00106b0 | c00106b1 | c00106b8 | c00106bf |
| c00106b4 | c00106b5 | c00106b6 | c00106b7 | c00106be | c00106c5 |
| c00106ba | c00106bb | c00106bc | c00106bd | c00106c4 | c00106cb |
| c00106c0 | c00106c1 | c00106c2 | c00106c3 | c00106ca | c00106d1 |
| c00106c6 | c00106c7 | c00106c8 | c00106c9 | c00106d0 | c00106d7 |
| c00106cc | c00106cd | c00106ce | c00106cf | c00106d6 | c00106dd |
| c00106d2 | c00106d3 | c00106d4 | c00106d5 | c00106dc | c00106e3 |
| c00106d8 | c00106d9 | c00106da | c00106db | c00106e2 | c00106e9 |

| | | | | | |
|---|---|---|---|---|---|
| c00106de | c00106df | c00106e0 | c00106e1 | c00106e8 | c00106ef |
| c00106e4 | c00106e5 | c00106e6 | c00106e7 | c00106ee | c00106f5 |
| c00106ea | c00106eb | c00106ec | c00106ed | c00106f4 | c00106fb |
| c00106f0 | c00106f1 | c00106f2 | c00106f3 | c00106fa | c0011001 |
| c00106f6 | c00106f7 | c00106f8 | c00106f9 | c0011000 | c001100b |
| c00106fc | c00106fd | c00106fe | c00106ff | c001100a | c0011014 |
| c0011006 | c0011007 | c0011008 | c0011009 | c0011011 | c0011021 |
| c001100c | c001100e | c001100f | c0011010 | c0011020 | c0011029 |
| c0011015 | c0011016 | c0011017 | c0011018 | c0011028 | c001102f |
| c0011022 | c0011024 | c0011025 | c0011026 | c001102e | c0011077 |
| c001102a | c001102b | c001102c | c001102d | c0011076 | c0011095 |
| c0011041 | c0011042 | c0011074 | c0011075 | c0011094 | |
| c0011078 | c0011083 | c0011092 | c0011093 | 413 | |
| c0011096 | c0011097 | c00110a2 | 412 | 425 | |

### 10.1.2 Intel Core i7-6700K

| | | | | | |
|---|---|---|---|---|---|
| 20 | 21 | 3e | 104 | 140 | 1da |
| 33 | 35 | 103 | 13d | 1c6 | 1f5 |
| 95 | 102 | 13a | 1aa | 1f4 | 302 |
| 11f | 121 | 1a8 | 1f0 | 2f5 | 4e3 |
| 19d | 1a1 | 1e0 | 2f4 | 4e2 | 609 |
| 1db | 1dc | 2e7 | 4e0 | 608 | 622 |
| 1fb | 2e0 | 397 | 607 | 621 | 634 |
| 305 | 393 | 603 | 620 | 633 | 704 |
| 503 | 601 | 61d | 632 | 703 | 714 |
| 615 | 618 | 631 | 702 | 713 | 724 |
| 623 | 630 | 637 | 712 | 723 | 734 |
| 635 | 636 | 709 | 722 | 733 | 742 |
| 705 | 708 | 719 | 732 | 741 | 748 |
| 715 | 718 | 729 | 740 | 747 | |
| 725 | 728 | 739 | 746 | 2e | |
| 735 | 738 | 745 | 2a | 80 | |
| 743 | 744 | 23 | 7a | 118 | |
| 749 | 22 | 59 | 110 | 150 | |

### 10.1.3 Intel Core i7-8700K

| | | | | | |
|---|---|---|---|---|---|
| 20 | 21 | 22 | 23 | 2a | 80 |
| 33 | 35 | 3e | 59 | 7a | 110 |
| 95 | 102 | 103 | 104 | 10f | 140 |
| 118 | 11f | 121 | 13a | 13d | 1c6 |
| 150 | 19d | 1a1 | 1a8 | 1aa | 1f4 |
| 1da | 1db | 1dc | 1e0 | 1f0 | 2f5 |
| 1f5 | 1fb | 2e0 | 2e7 | 2f4 | 4e2 |

| | | | | | |
|---|---|---|---|---|---|
| 302 | 305 | 393 | 397 | 4e0 | 608 |
| 4e3 | 503 | 601 | 603 | 607 | 621 |
| 609 | 615 | 618 | 61d | 620 | 633 |
| 622 | 623 | 630 | 631 | 632 | 703 |
| 634 | 635 | 636 | 637 | 702 | 713 |
| 704 | 705 | 708 | 709 | 712 | 723 |
| 714 | 715 | 718 | 719 | 722 | 733 |
| 724 | 725 | 728 | 729 | 732 | 741 |
| 734 | 735 | 738 | 739 | 740 | 747 |
| 742 | 743 | 744 | 745 | 746 | 753 |
| 748 | 749 | 750 | 751 | 752 | 759 |
| 754 | 755 | 756 | 757 | 758 | 765 |
| 760 | 761 | 762 | 763 | 764 | |
| 766 | 767 | 768 | 769 | 2e | |

### 10.1.4 Intel Core i9-9900K

| | | | | | |
|---|---|---|---|---|---|
| 20 | 21 | 22 | 59 | 10f | 140 |
| 33 | 35 | 3e | 104 | 13d | 1c6 |
| 95 | 102 | 103 | 13a | 1aa | 1f4 |
| 118 | 11f | 121 | 1a8 | 1f0 | 2f5 |
| 150 | 19d | 1a1 | 1e0 | 2f4 | 4e2 |
| 1da | 1db | 1dc | 2e7 | 4e0 | 608 |
| 1f5 | 1fb | 2e0 | 397 | 607 | 621 |
| 302 | 305 | 393 | 603 | 620 | 633 |
| 4e3 | 503 | 601 | 61d | 632 | 703 |
| 609 | 615 | 618 | 631 | 702 | 713 |
| 622 | 623 | 630 | 637 | 712 | 723 |
| 634 | 635 | 636 | 709 | 722 | 733 |
| 704 | 705 | 708 | 719 | 732 | 741 |
| 714 | 715 | 718 | 729 | 740 | 747 |
| 724 | 725 | 728 | 739 | 746 | 753 |
| 734 | 735 | 738 | 745 | 752 | 759 |
| 742 | 743 | 744 | 751 | 758 | 765 |
| 748 | 749 | 750 | 757 | 764 | f71 |
| 754 | 755 | 756 | 763 | f70 | f77 |
| 760 | 761 | 762 | 769 | f76 | |
| 766 | 767 | 768 | f75 | 2e | |
| f72 | f73 | f74 | 2a | 80 | |
| f78 | f79 | 23 | 7a | 110 | |

### 10.1.5 Intel Xeon Silver 4208

| | | | | | |
|---|---|---|---|---|---|
| 20 | 21 | 35 | 56 | 6b | 118 |
| 31 | 33 | 55 | 67 | 110 | 13a |

| | | | | | |
|---|---|---|---|---|---|
| 53 | 54 | 64 | 108 | 12a | 154 |
| 5f | 63 | 102 | 129 | 153 | 19d |
| af | e3 | 128 | 152 | 17f | 1ae |
| 11f | 122 | 150 | 178 | 1aa | 1e1 |
| 13d | 140 | 157 | 1a8 | 1e0 | 2e0 |
| 155 | 156 | 1a5 | 1dc | 1fb | 603 |
| 1a1 | 1a3 | 1db | 1f7 | 601 | 61c |
| 1c6 | 1da | 1f6 | 503 | 618 | 637 |
| 1e2 | 1f0 | 305 | 615 | 623 | 709 |
| 2e7 | 302 | 609 | 622 | 708 | 713 |
| 607 | 608 | 621 | 705 | 712 | 71b |
| 61d | 620 | 704 | 70d | 71a | a01 |
| 702 | 703 | 70c | 719 | a00 | a44 |
| 70a | 70b | 718 | 793 | a43 | a4b |
| 714 | 715 | 790 | a42 | a4a | a51 |
| 71c | 71d | a41 | a49 | a50 | a5b |
| a02 | a40 | a48 | a4f | a5a | a63 |
| a45 | a47 | a4e | a59 | a62 | a6a |
| a4c | a4d | a58 | a61 | a69 | a70 |
| a52 | a53 | a60 | a68 | a6f | a7a |
| a5c | a5f | a67 | a6e | a79 | a82 |
| a64 | a65 | a6d | a78 | a81 | a89 |
| a6b | a6c | a73 | a80 | a88 | a8f |
| a71 | a72 | a7f | a87 | a8e | a99 |
| a7b | a7c | a85 | a8d | a98 | aa1 |
| a83 | a84 | a8c | a93 | aa0 | aa8 |
| a8a | a8b | a92 | a9f | aa7 | aae |
| a90 | a91 | a9c | aa5 | aad | ab8 |
| a9a | a9b | aa4 | aac | ab3 | ac0 |
| aa2 | aa3 | aab | ab2 | abf | ac7 |
| aa9 | aaa | ab1 | abc | ac5 | acd |
| aaf | ab0 | abb | ac4 | acc | ad3 |
| ab9 | aba | ac3 | acb | ad2 | adf |
| ac1 | ac2 | aca | ad1 | adc | ae5 |
| ac8 | ac9 | ad0 | adb | ae4 | aec |
| ace | acf | ada | ae3 | aeb | af2 |
| ad8 | ad9 | ae2 | aea | af1 | afc |
| ae0 | ae1 | ae9 | af0 | afb | b04 |
| ae7 | ae8 | aef | afa | b03 | b0a |
| aed | aee | af9 | b02 | b09 | b10 |
| af3 | af8 | b01 | b08 | b0f | b16 |
| aff | b00 | b07 | b0e | b15 | b1c |
| b05 | b06 | b0d | b14 | b1b | b22 |

| | | | | | |
|---|---|---|---|---|---|
| b0b | b0c | b13 | b1a | b21 | b28 |
| b11 | b12 | b19 | b20 | b27 | b2e |
| b17 | b18 | b1f | b26 | b2d | b34 |
| b1d | b1e | b25 | b2c | b33 | b3a |
| b23 | b24 | b2b | b32 | b39 | b40 |
| b29 | b2a | b31 | b38 | b3f | b46 |
| b2f | b30 | b37 | b3e | b45 | b4c |
| b35 | b36 | b3d | b44 | b4b | b52 |
| b3b | b3c | b43 | b4a | b51 | b58 |
| b41 | b42 | b49 | b50 | b57 | b5e |
| b47 | b48 | b4f | b56 | b5d | e04 |
| b4d | b4e | b55 | b5c | e03 | e0a |
| b53 | b54 | b5b | e00 | e09 | e14 |
| b59 | b5a | c8c | e08 | e13 | e1a |
| b5f | c8b | e07 | e12 | e19 | e24 |
| e05 | e06 | e11 | e18 | e23 | e2a |
| e0b | e10 | e17 | e22 | e29 | e34 |
| e15 | e16 | e21 | e28 | e33 | e3a |
| e1b | e20 | e27 | e32 | e39 | e44 |
| e25 | e26 | e31 | e38 | e43 | e4a |
| e2b | e30 | e37 | e42 | e49 | e54 |
| e35 | e36 | e41 | e48 | e53 | e5a |
| e3b | e40 | e47 | e52 | e59 | e64 |
| e45 | e46 | e51 | e58 | e63 | e6a |
| e4b | e50 | e57 | e62 | e69 | e74 |
| e55 | e56 | e61 | e68 | e73 | e7a |
| e5b | e60 | e67 | e72 | e79 | e84 |
| e65 | e66 | e71 | e78 | e83 | e8a |
| e6b | e70 | e77 | e82 | e89 | e94 |
| e75 | e76 | e81 | e88 | e93 | e9a |
| e7b | e80 | e87 | e92 | e99 | ea4 |
| e85 | e86 | e91 | e98 | ea3 | eaa |
| e8b | e90 | e97 | ea2 | ea9 | eb4 |
| e95 | e96 | ea1 | ea8 | eb3 | eba |
| e9b | ea0 | ea7 | eb2 | eb9 | ec4 |
| ea5 | ea6 | eb1 | eb8 | ec3 | eca |
| eab | eb0 | eb7 | ec2 | ec9 | ed4 |
| eb5 | eb6 | ec1 | ec8 | ed3 | eda |
| ebb | ec0 | ec7 | ed2 | ed9 | ee4 |
| ec5 | ec6 | ed1 | ed8 | ee3 | eea |
| ecb | ed0 | ed7 | ee2 | ee9 | ef4 |
| ed5 | ed6 | ee1 | ee8 | ef3 | efa |
| edb | ee0 | ee7 | ef2 | ef9 | f04 |

| | | | | | |
|---|---|---|---|---|---|
| ee5 | ee6 | ef1 | ef8 | f03 | f0a |
| eeb | ef0 | ef7 | f02 | f09 | f14 |
| ef5 | ef6 | f01 | f08 | f13 | f1a |
| efb | f00 | f07 | f12 | f19 | f24 |
| f05 | f06 | f11 | f18 | f23 | f2a |
| f0b | f10 | f17 | f22 | f29 | f34 |
| f15 | f16 | f21 | f28 | f33 | f3a |
| f1b | f20 | f27 | f32 | f39 | f44 |
| f25 | f26 | f31 | f38 | f43 | f4a |
| f2b | f30 | f37 | f42 | f49 | f54 |
| f35 | f36 | f41 | f48 | f53 | f5a |
| f3b | f40 | f47 | f52 | f59 | f64 |
| f45 | f46 | f51 | f58 | f63 | f6a |
| f4b | f50 | f57 | f62 | f69 | f74 |
| f55 | f56 | f61 | f68 | f73 | f7a |
| f5b | f60 | f67 | f72 | f79 | |
| f65 | f66 | f71 | f78 | 2e | |
| f6b | f70 | f77 | 2a | 4f | |
| f75 | f76 | 23 | 4e | 5e | |
| f7b | 22 | 3e | 59 | 80 | |

## 10.2 Found Undocumented Dynamic MSRs on Intel Xeon Silver 4208

| | | | | | |
|---|---|---|---|---|---|
| 1a1 | 1a3 | 637 | 71d | a45 | a65 |
| a85 | aa5 | b01 | b05 | b08 | b09 |
| b0a | b0b | b0c | b0d | b0e | b0f |
| b18 | b19 | b1a | b1b | b1c | b1d |
| b1e | b1f | b28 | b29 | b2a | b2b |
| b2c | b2d | b2e | b2f | b38 | b39 |
| b3a | b3b | b3c | b3d | b3e | b3f |

## 10.3 Correlations

### 10.3.1 Undocumented Dynamic MSR Correlations on Intel Xeon Silver 4208

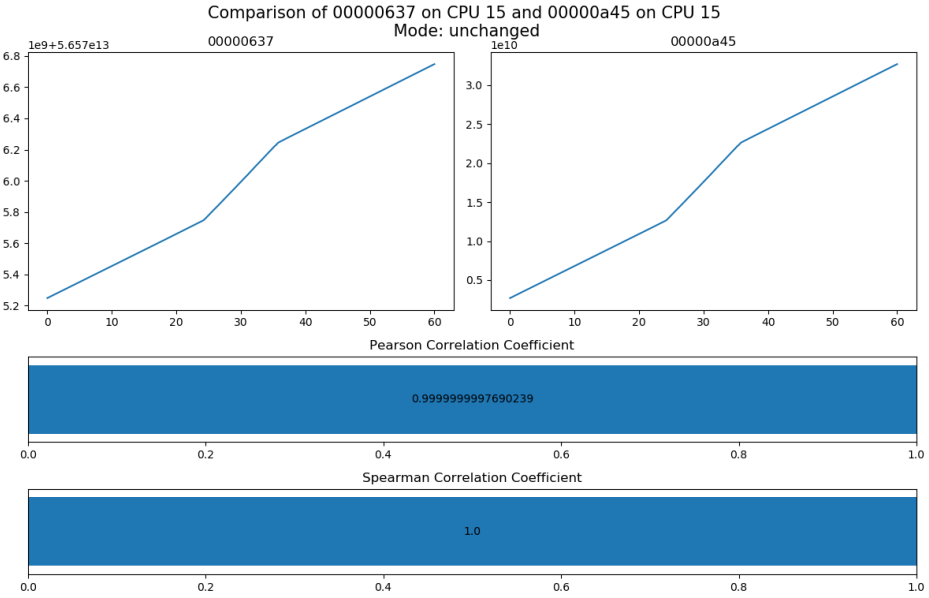


**Figure 10.1:** Correlation of MSR 0x637 and 0xa45.

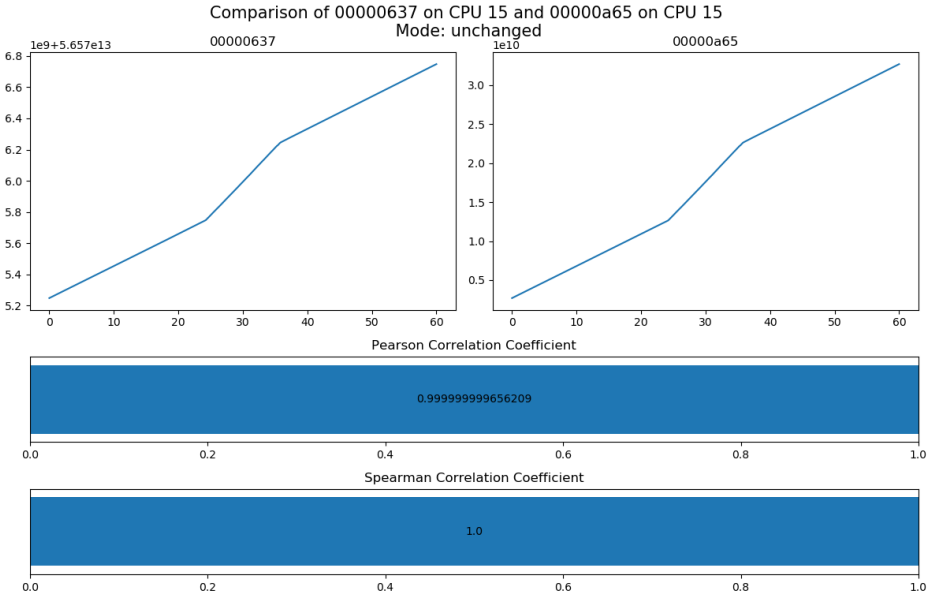


**Figure 10.2:** Correlation of MSR 0x637 and 0xa65.

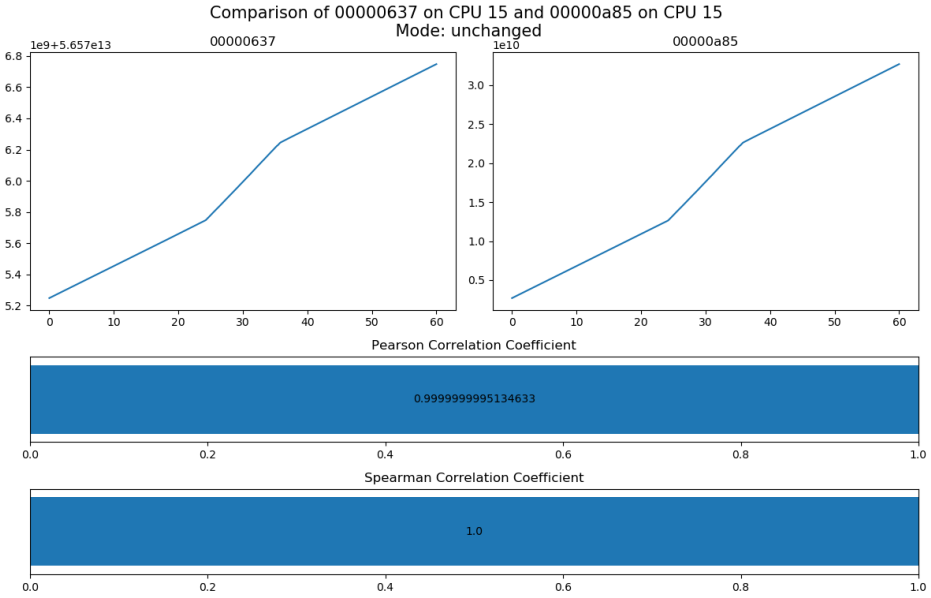


**Figure 10.3:** Correlation of MSR 0x637 and 0xa85.

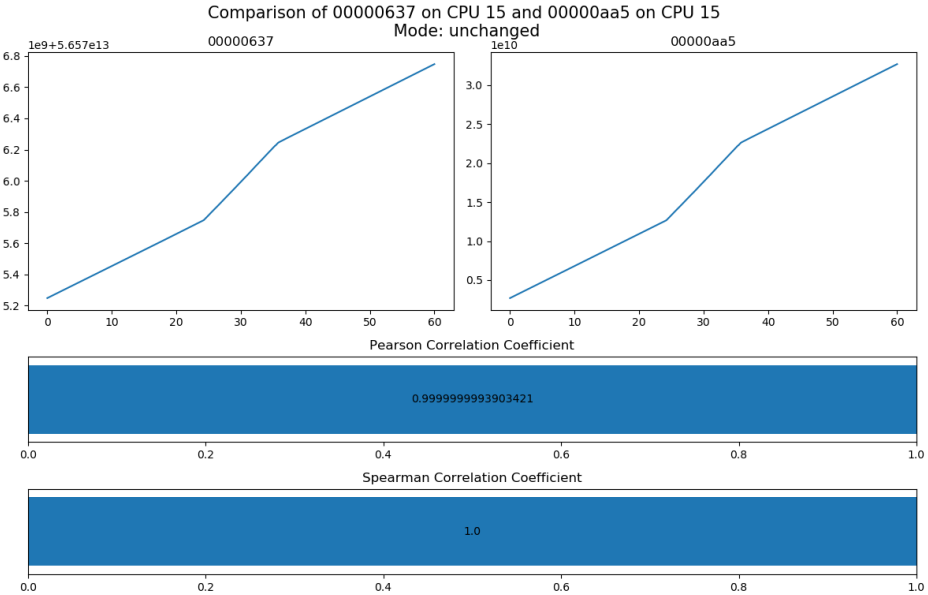


**Figure 10.4:** Correlation of MSR 0x637 and 0xaa5.

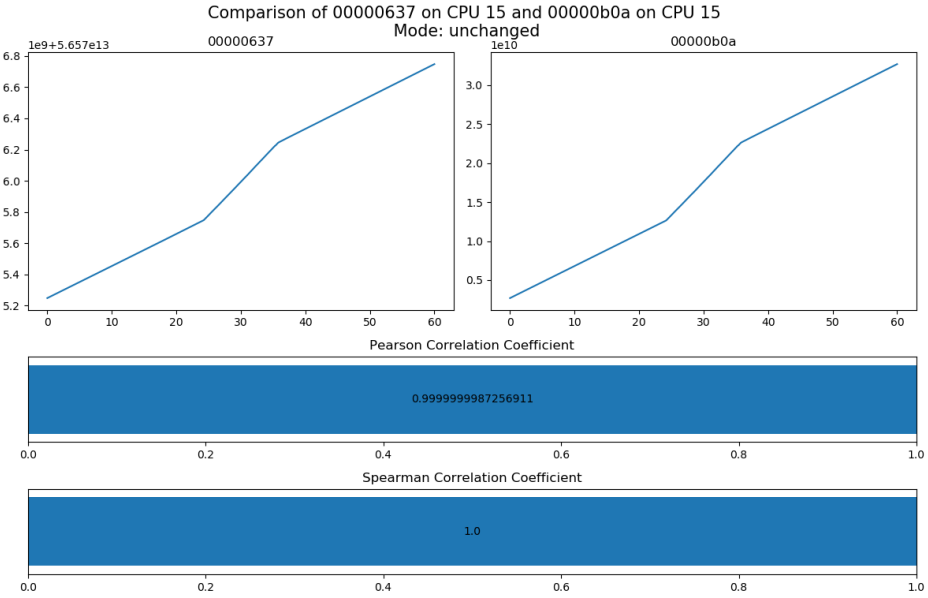


**Figure 10.5:** Correlation of MSR 0x637 and 0xb0a.

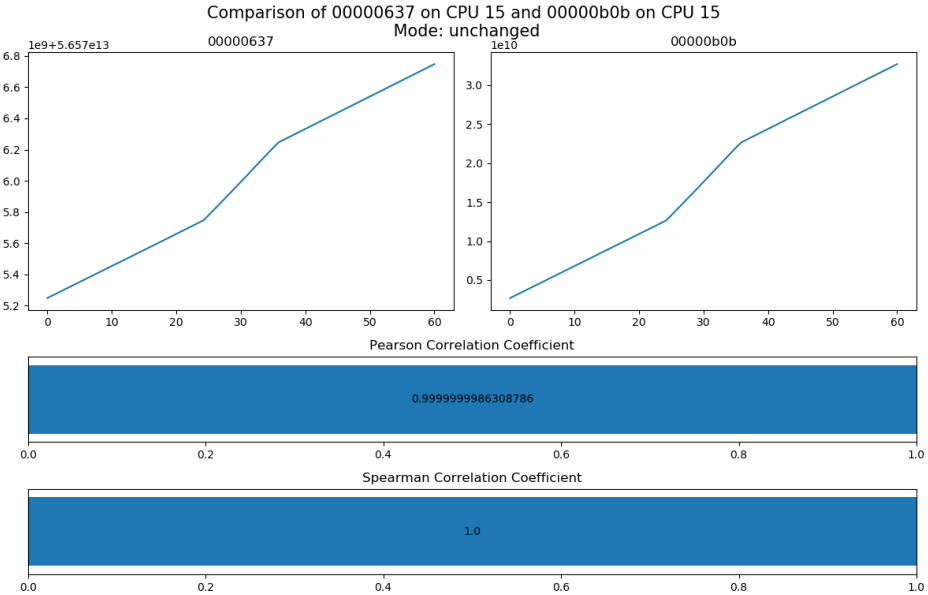


**Figure 10.6:** Correlation of MSR 0x637 and 0xb0b.

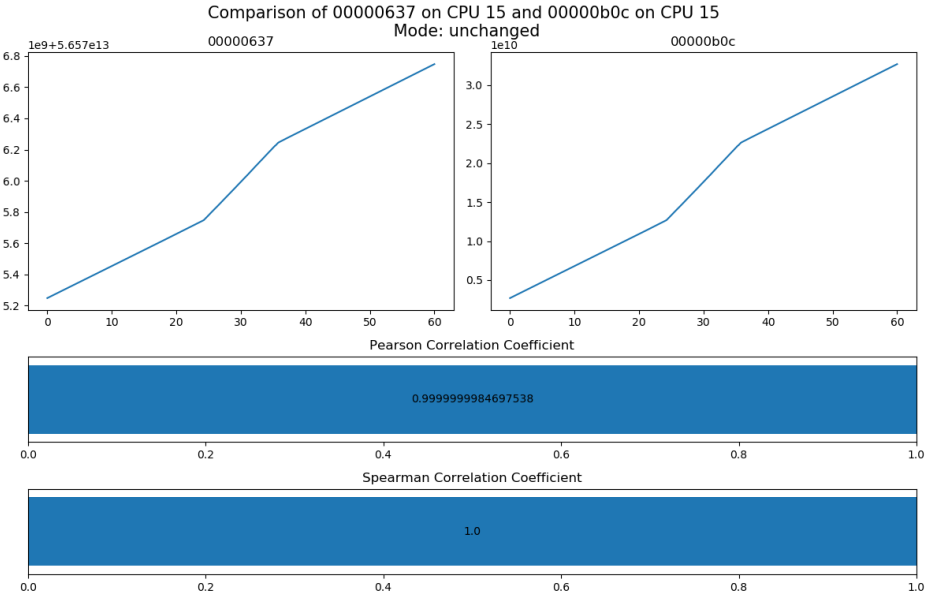


**Figure 10.7:** Correlation of MSR 0x637 and 0xb0c.

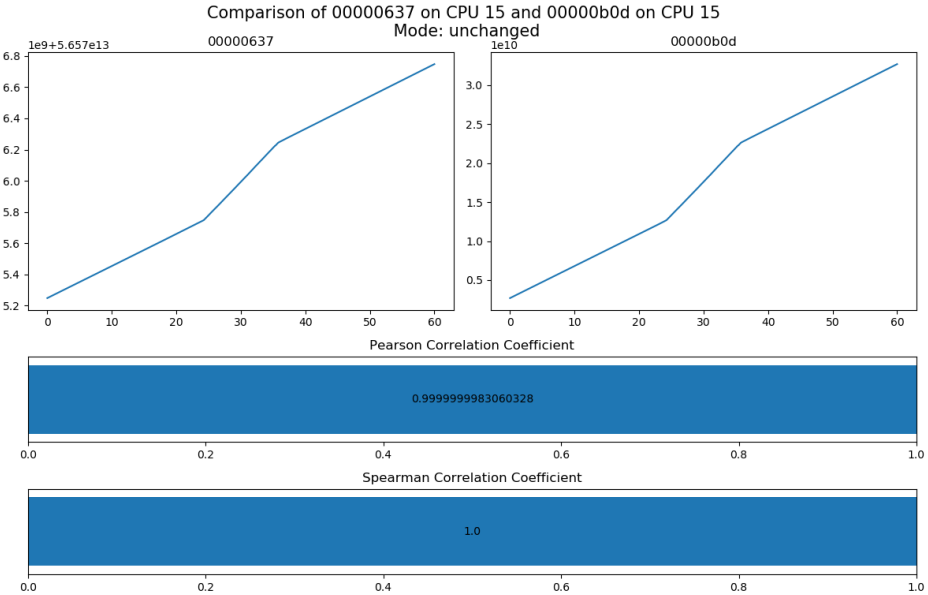


**Figure 10.8:** Correlation of MSR 0x637 and 0xb0d.

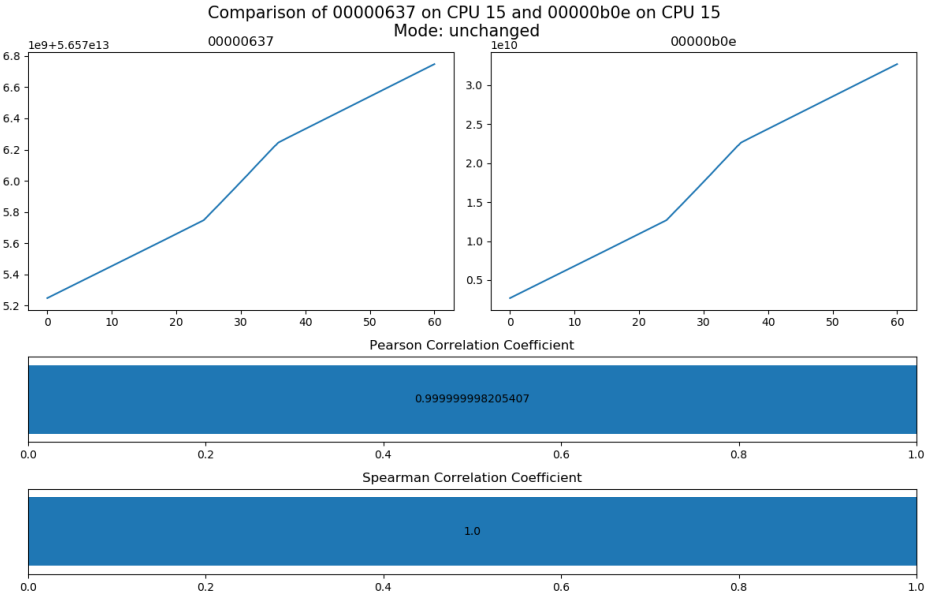


**Figure 10.9:** Correlation of MSR 0x637 and 0xb0e.

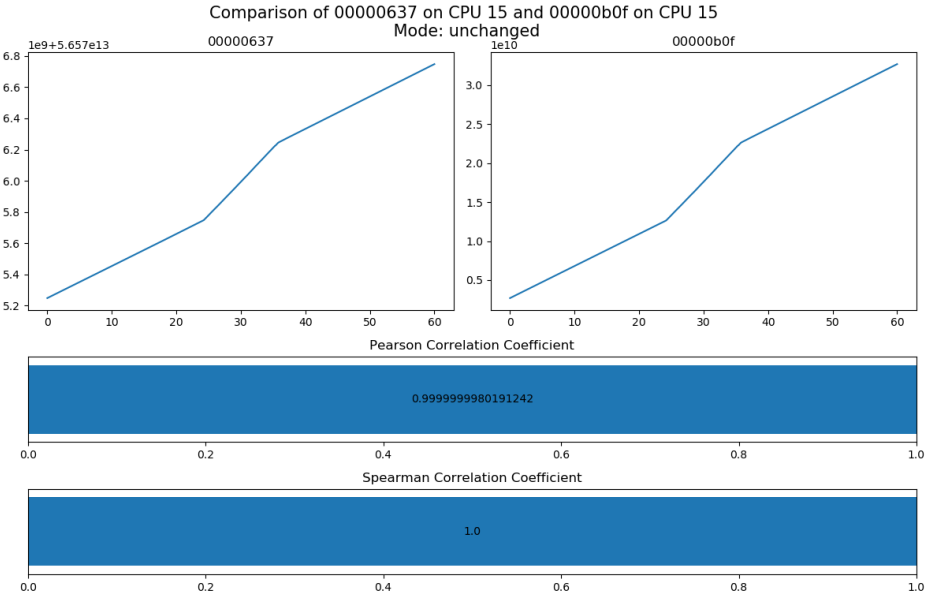


**Figure 10.10:** Correlation of MSR 0x637 and 0xb0f.

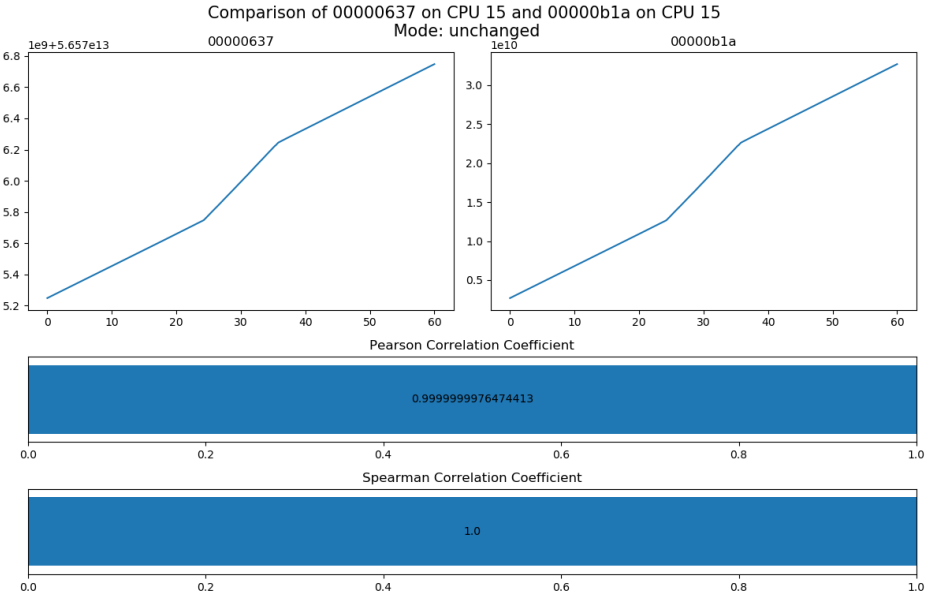


**Figure 10.11:** Correlation of MSR 0x637 and 0xb1a.

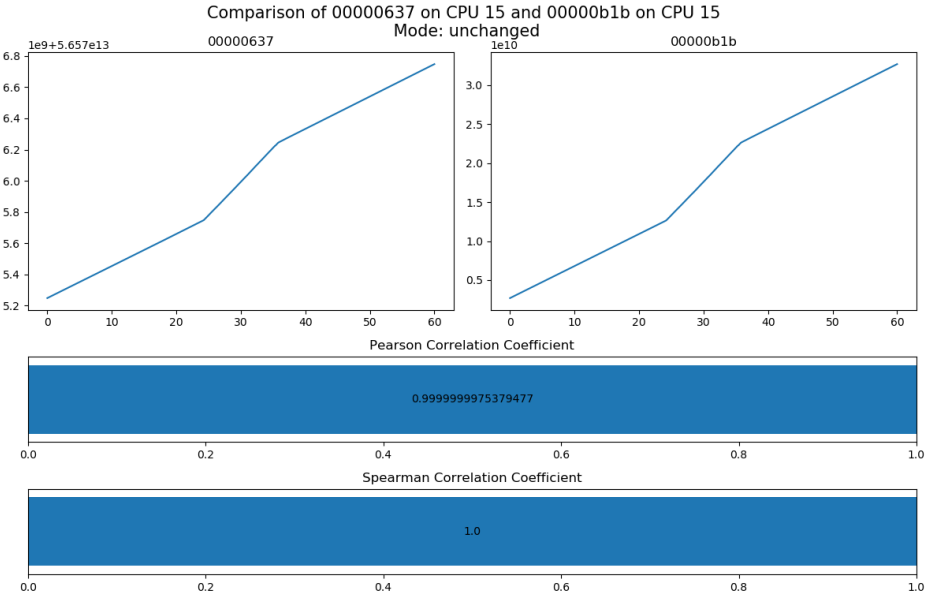


**Figure 10.12:** Correlation of MSR 0x637 and 0xb1b.

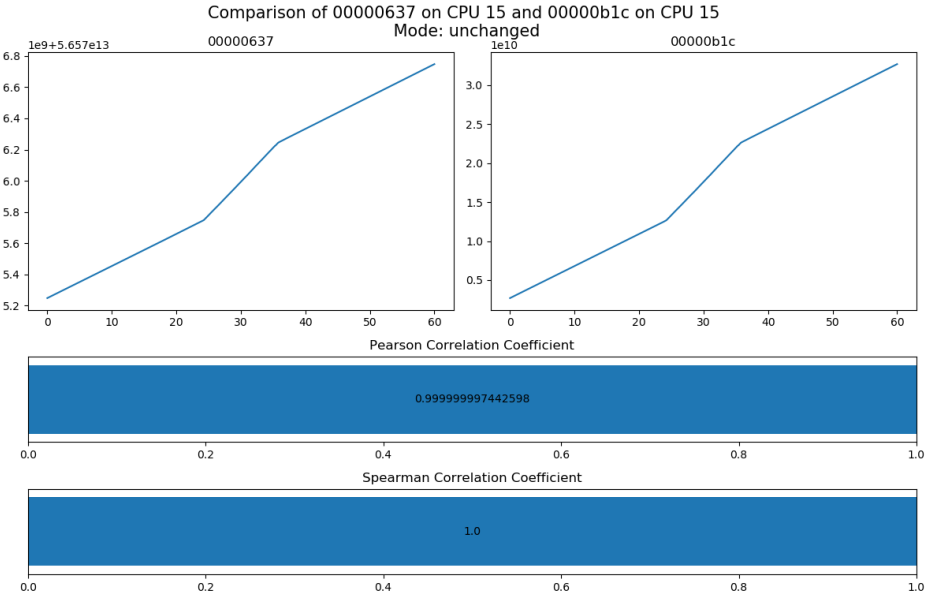


**Figure 10.13:** Correlation of MSR 0x637 and 0xb1c.

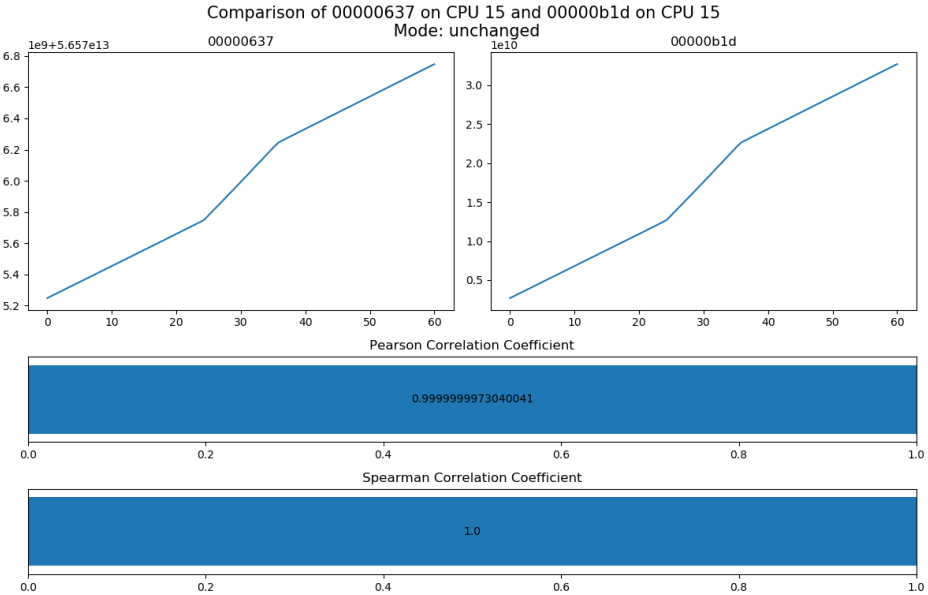


**Figure 10.14:** Correlation of MSR 0x637 and 0xb1d.

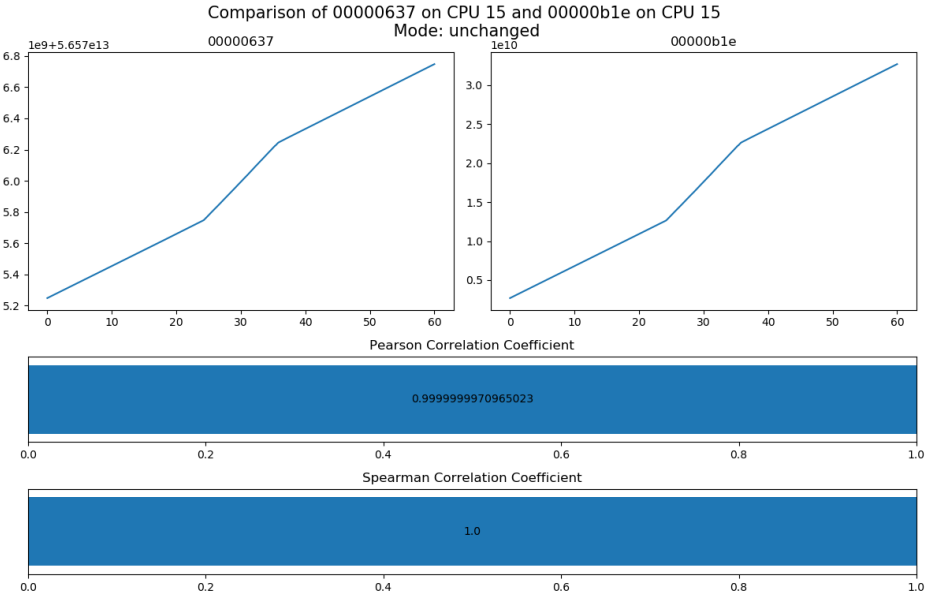


**Figure 10.15:** Correlation of MSR 0x637 and 0xb1e.

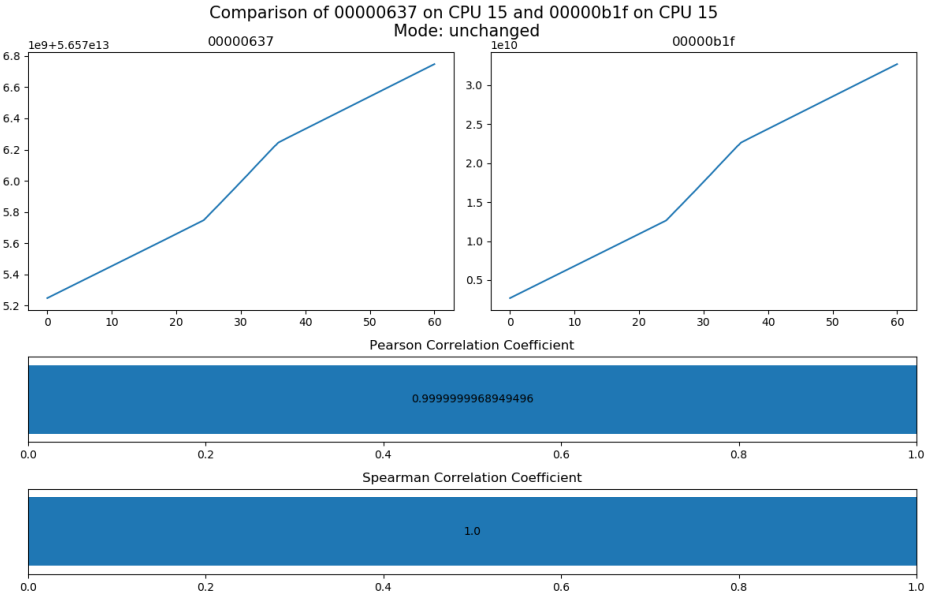


**Figure 10.16:** Correlation of MSR 0x637 and 0xb1f.

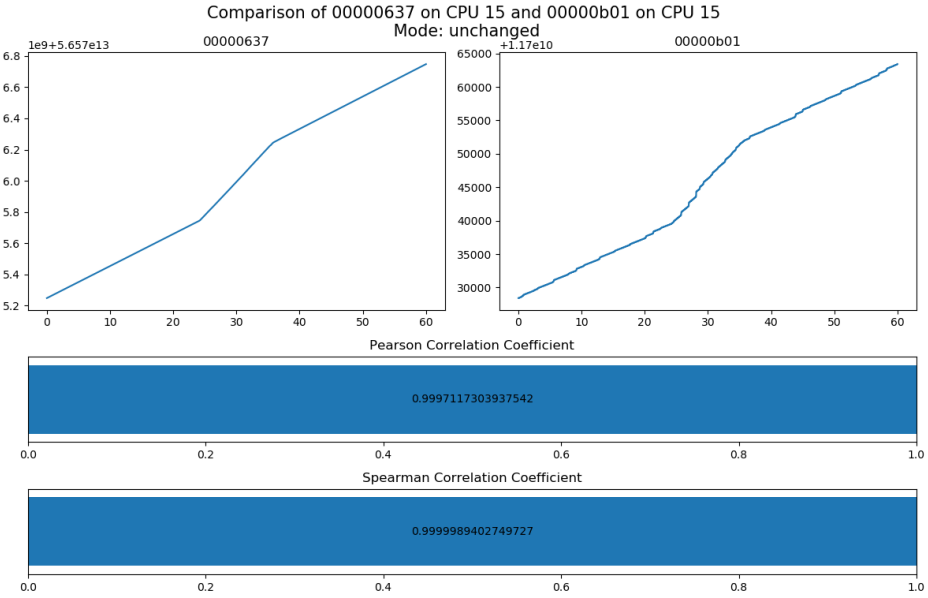


**Figure 10.17:** Correlation of MSR 0x637 and 0xb01.

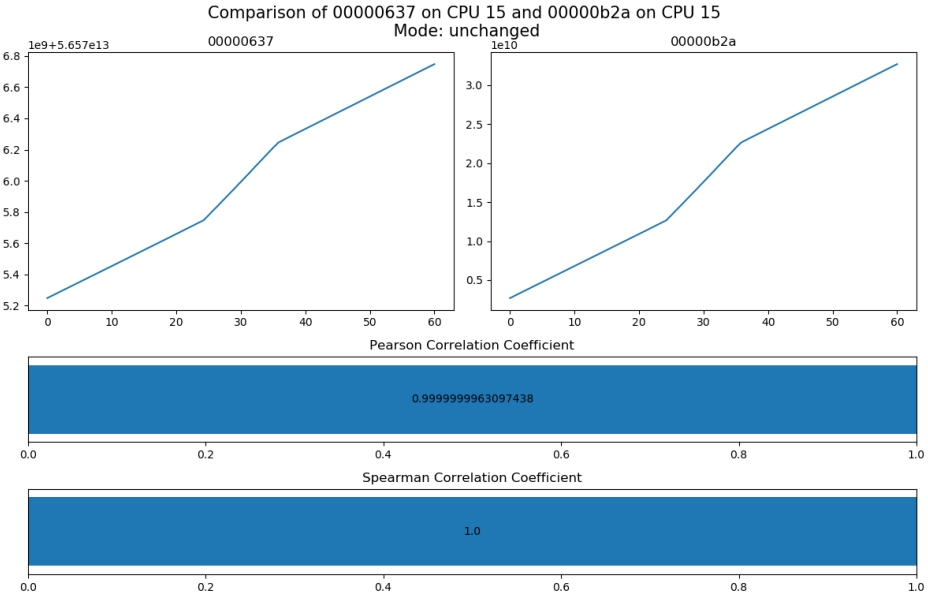


**Figure 10.18:** Correlation of MSR 0x637 and 0xb2a.

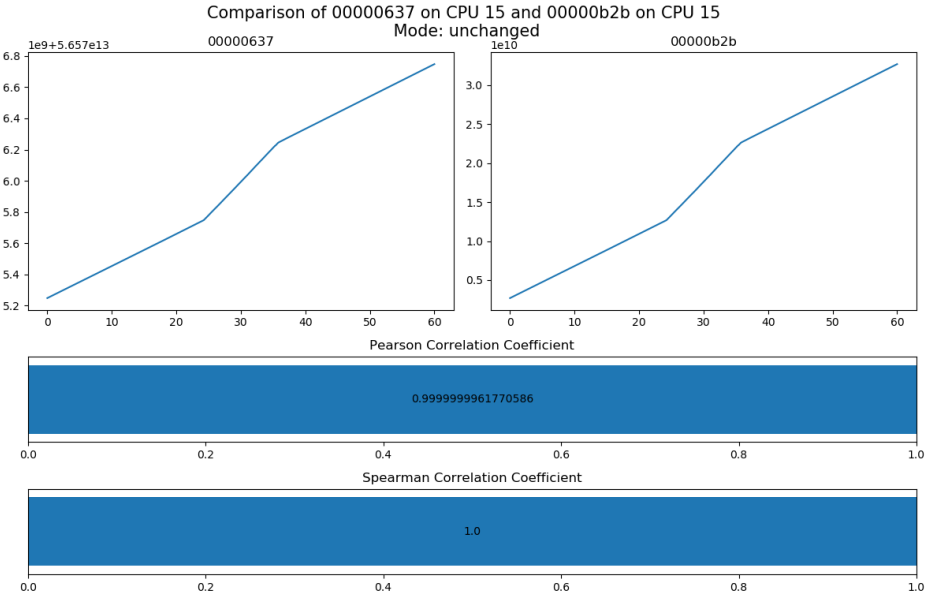


**Figure 10.19:** Correlation of MSR 0x637 and 0xb2b.

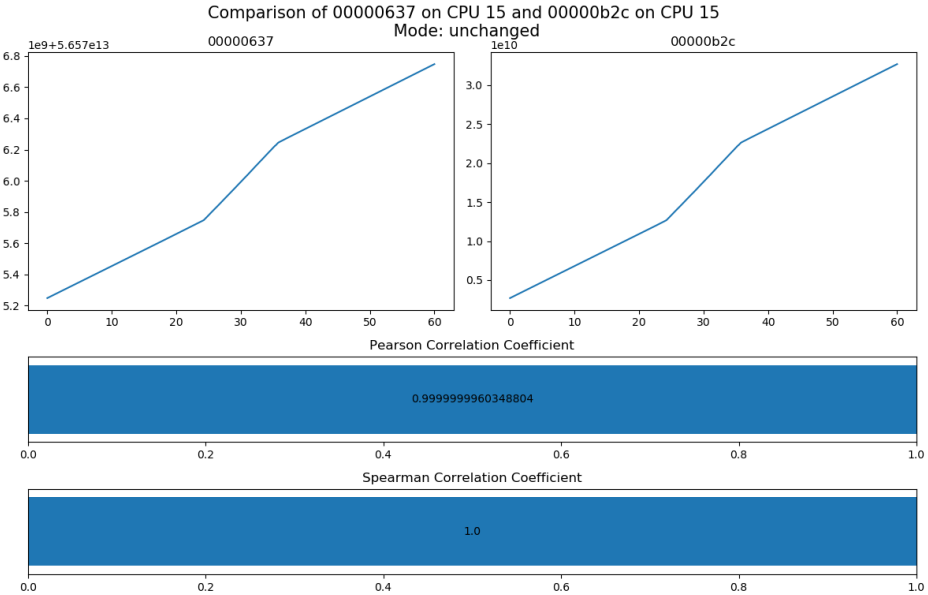


**Figure 10.20:** Correlation of MSR 0x637 and 0xb2c.

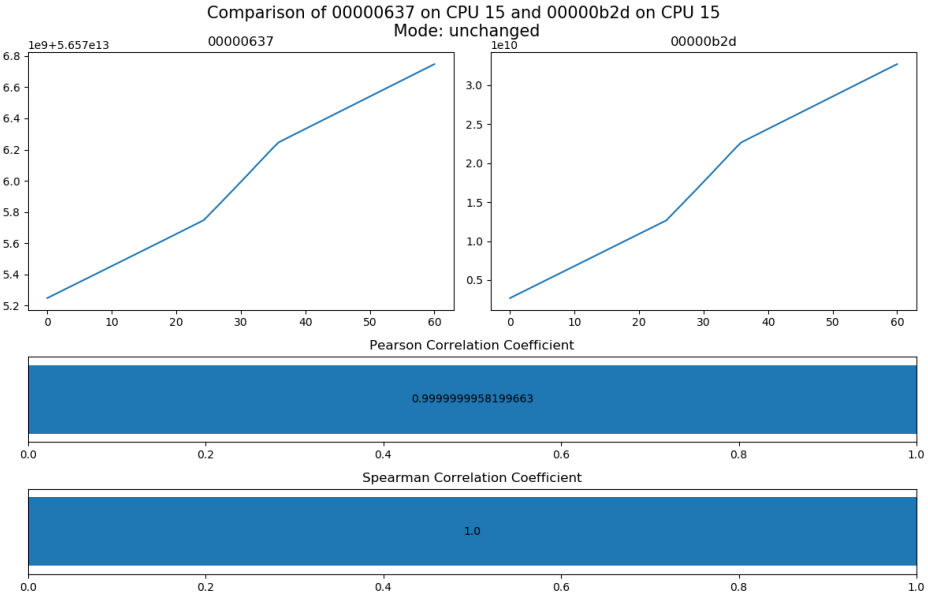


**Figure 10.21:** Correlation of MSR 0x637 and 0xb2d.

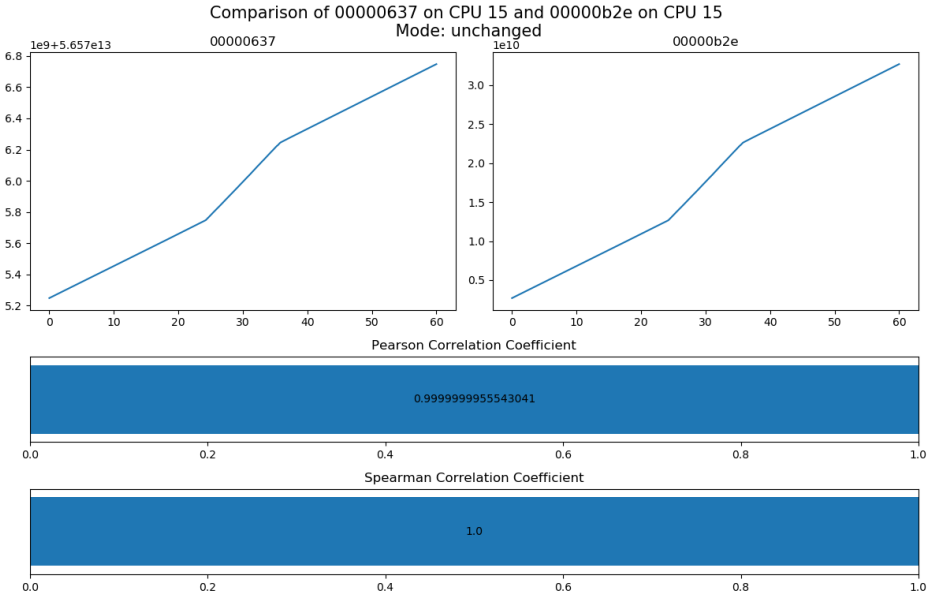


**Figure 10.22:** Correlation of MSR 0x637 and 0xb2e.

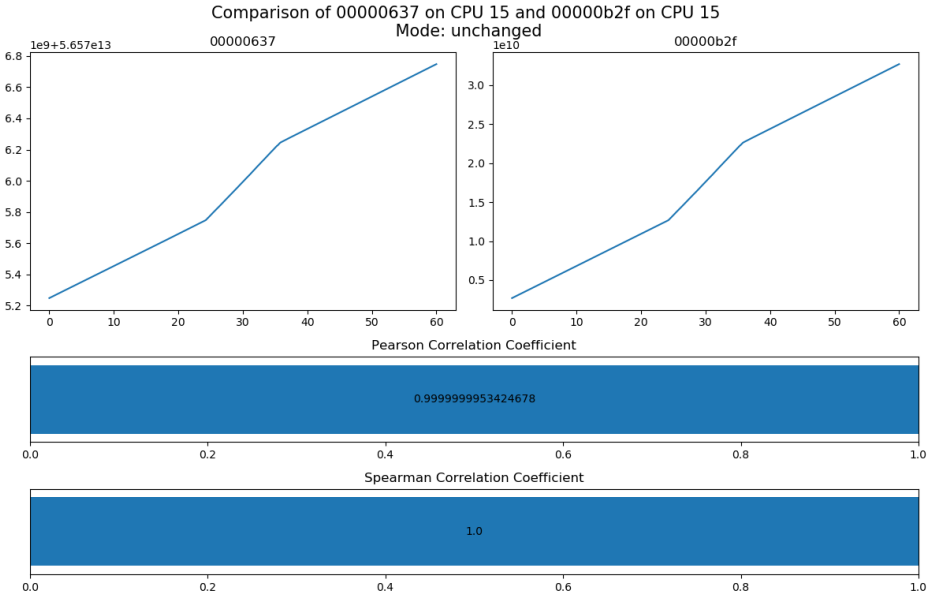


**Figure 10.23:** Correlation of MSR 0x637 and 0xb2f.

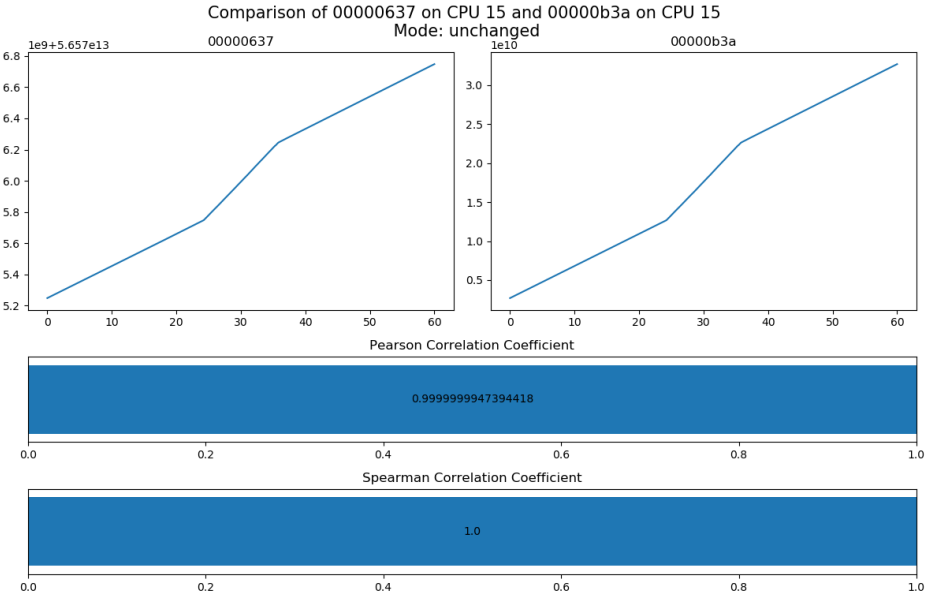


**Figure 10.24:** Correlation of MSR 0x637 and 0xb3a.

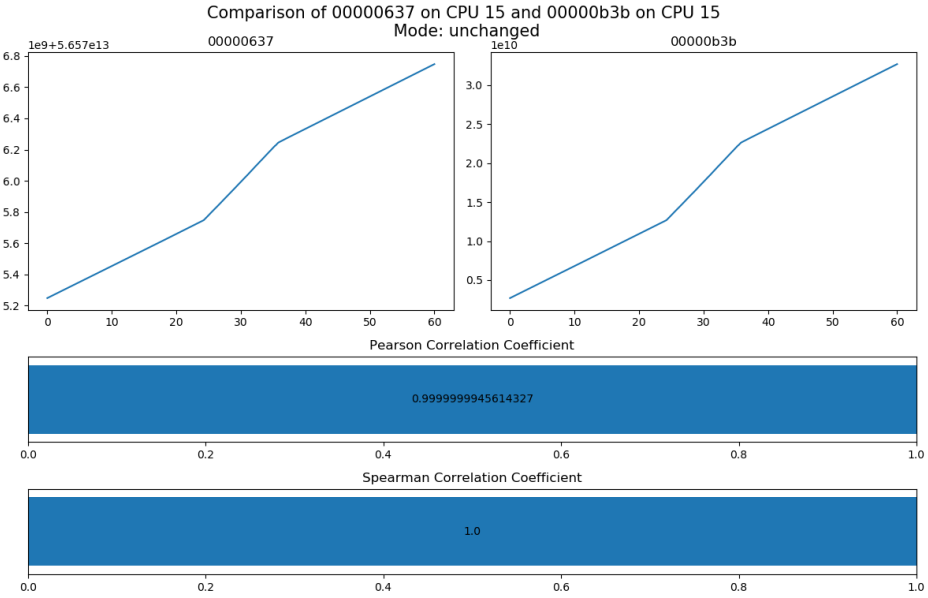


**Figure 10.25:** Correlation of MSR 0x637 and 0xb3b.

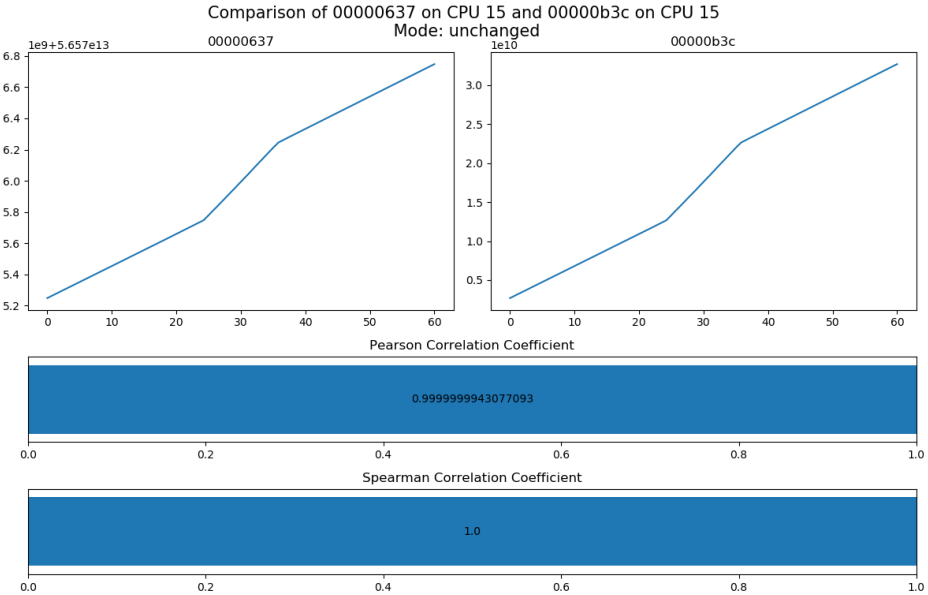


**Figure 10.26:** Correlation of MSR 0x637 and 0xb3c.

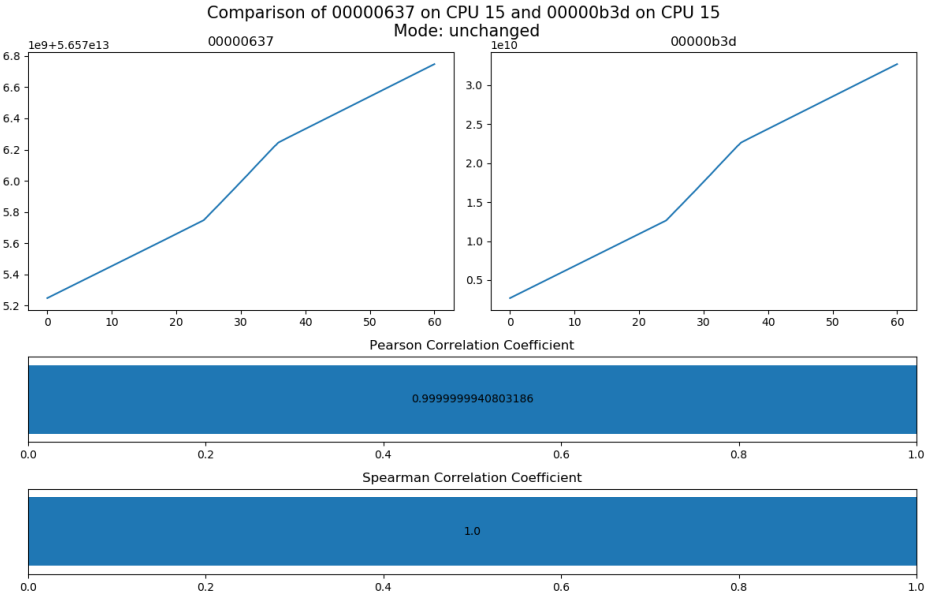


**Figure 10.27:** Correlation of MSR 0x637 and 0xb3d.

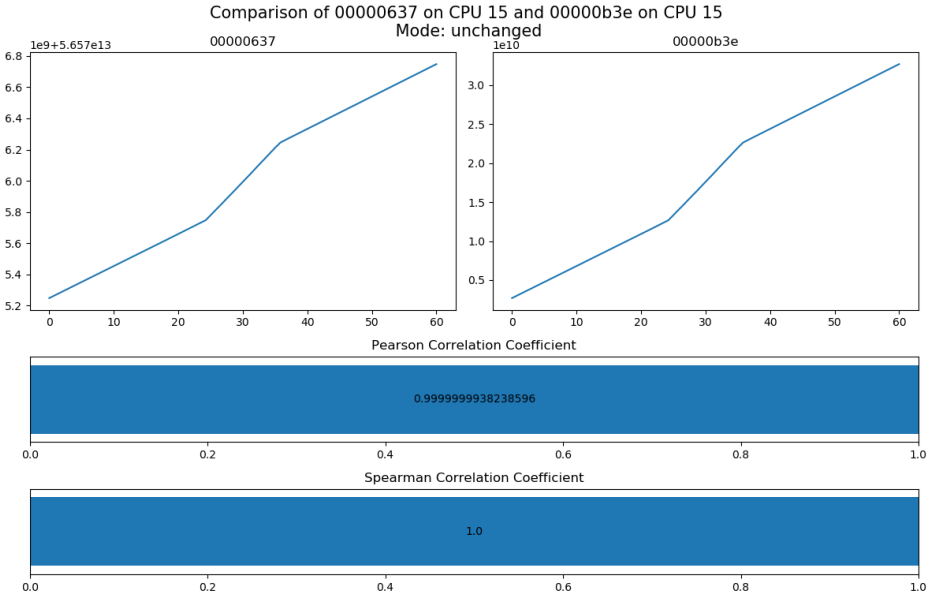


**Figure 10.28:** Correlation of MSR 0x637 and 0xb3e.

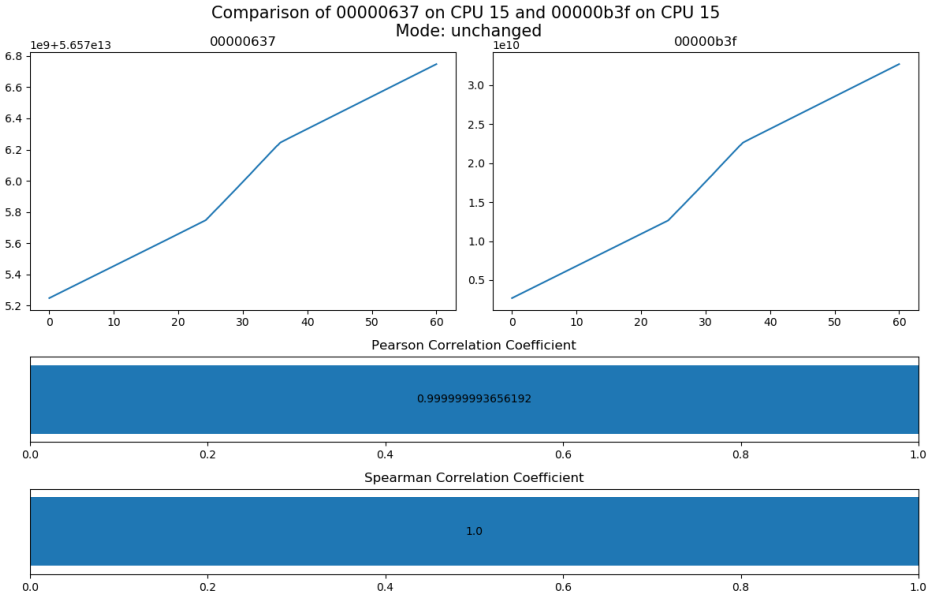


**Figure 10.29:** Correlation of MSR 0x637 and 0xb3f.

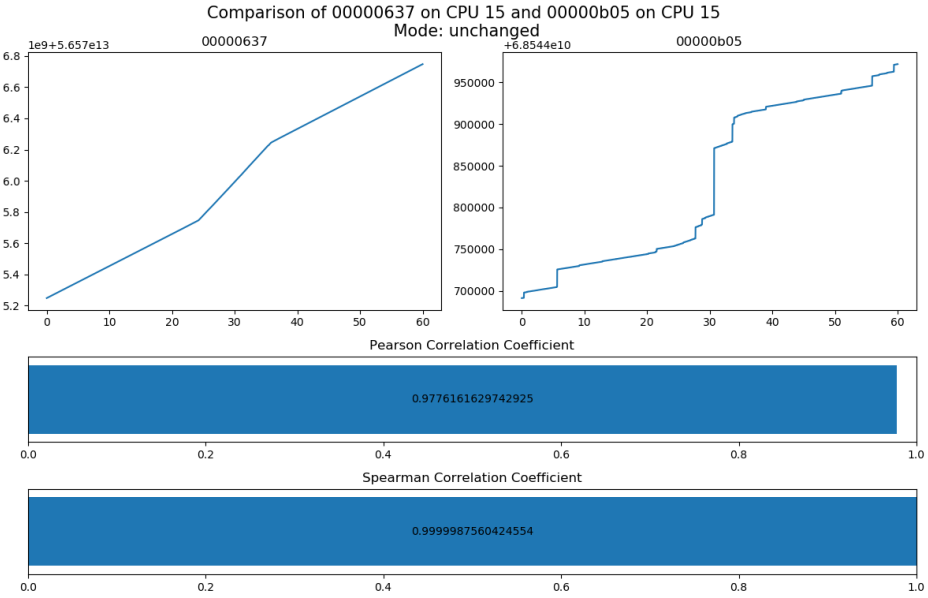


**Figure 10.30:** Correlation of MSR 0x637 and 0xb05.

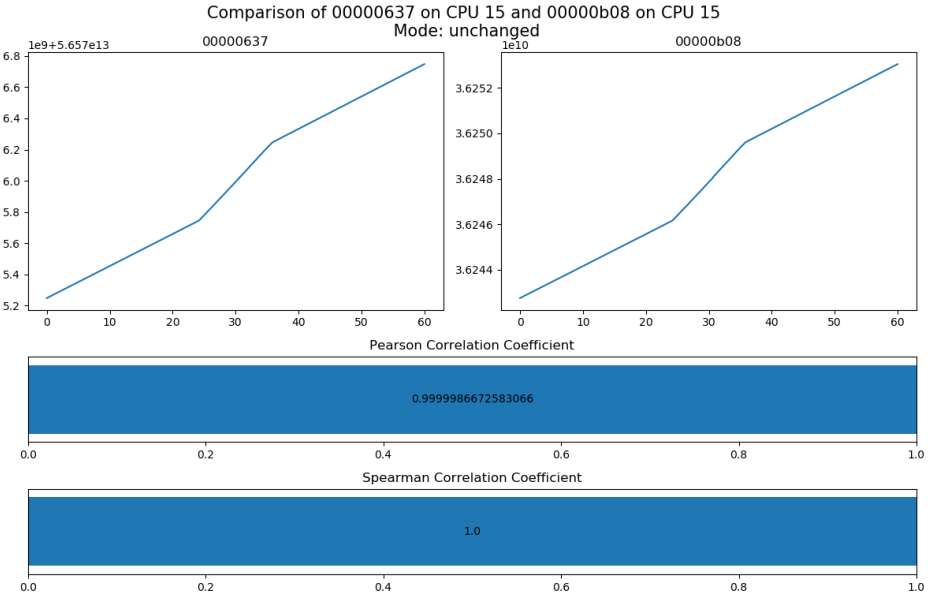


**Figure 10.31:** Correlation of MSR 0x637 and 0xb08.

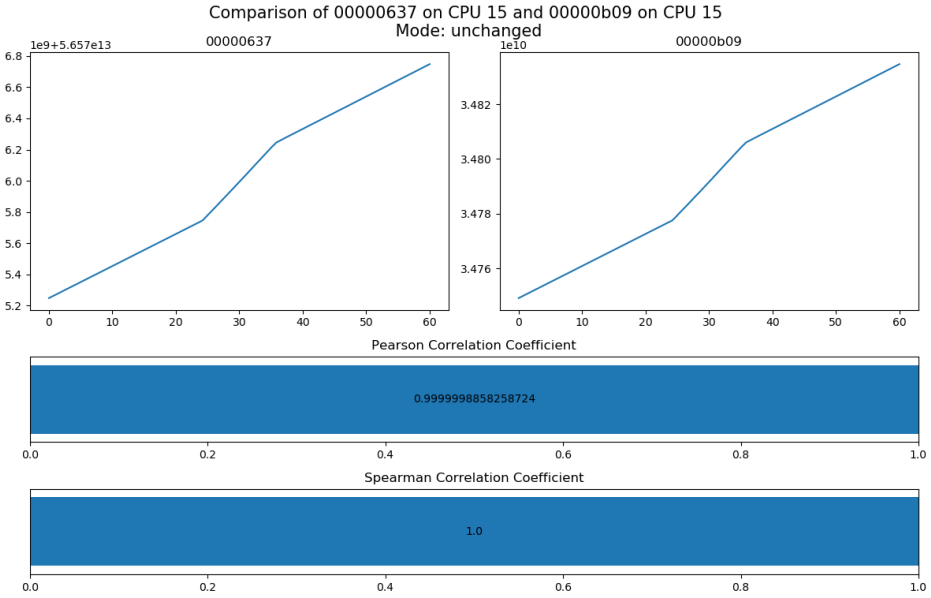


**Figure 10.32:** Correlation of MSR 0x637 and 0xb09.

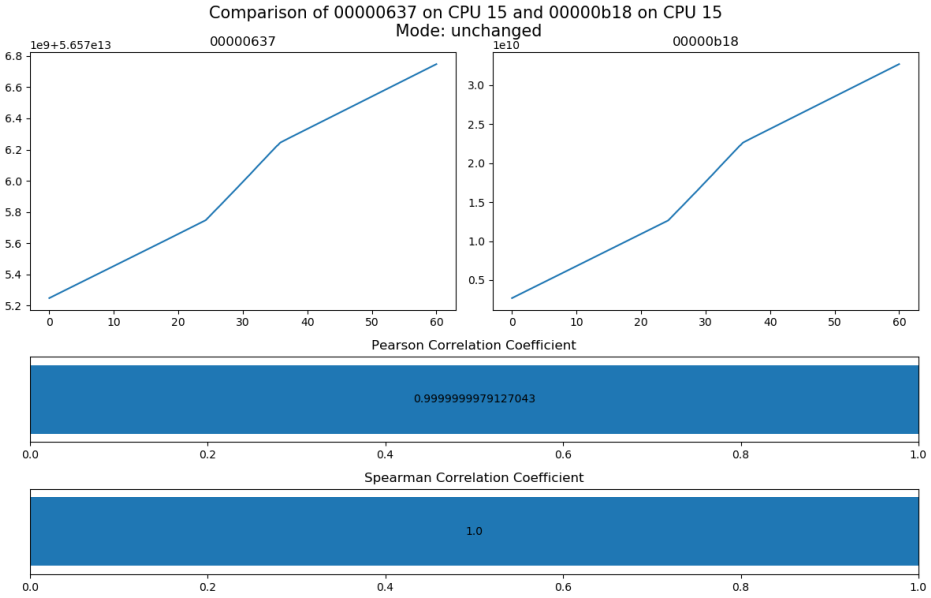


**Figure 10.33:** Correlation of MSR 0x637 and 0xb18.

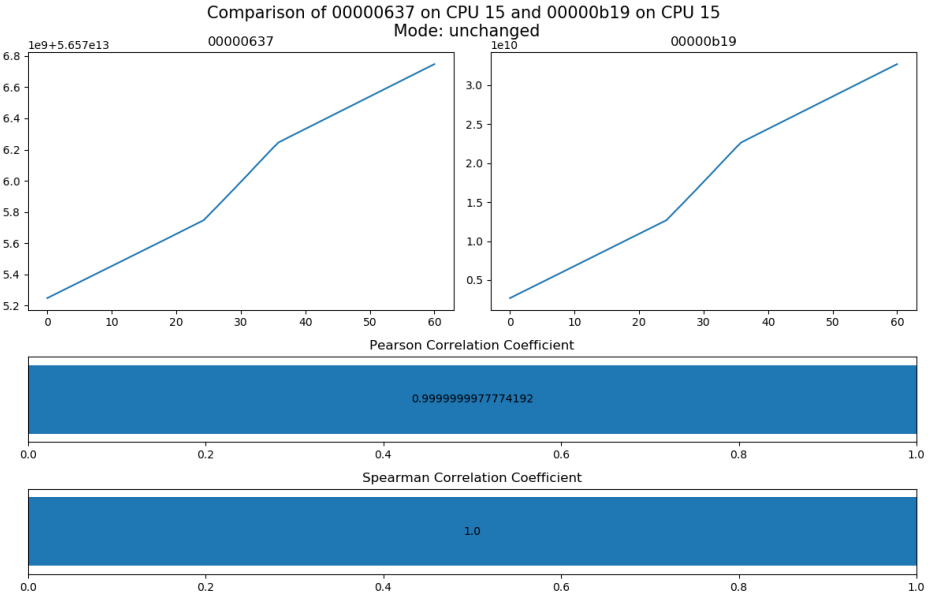


**Figure 10.34:** Correlation of MSR 0x637 and 0xb19.

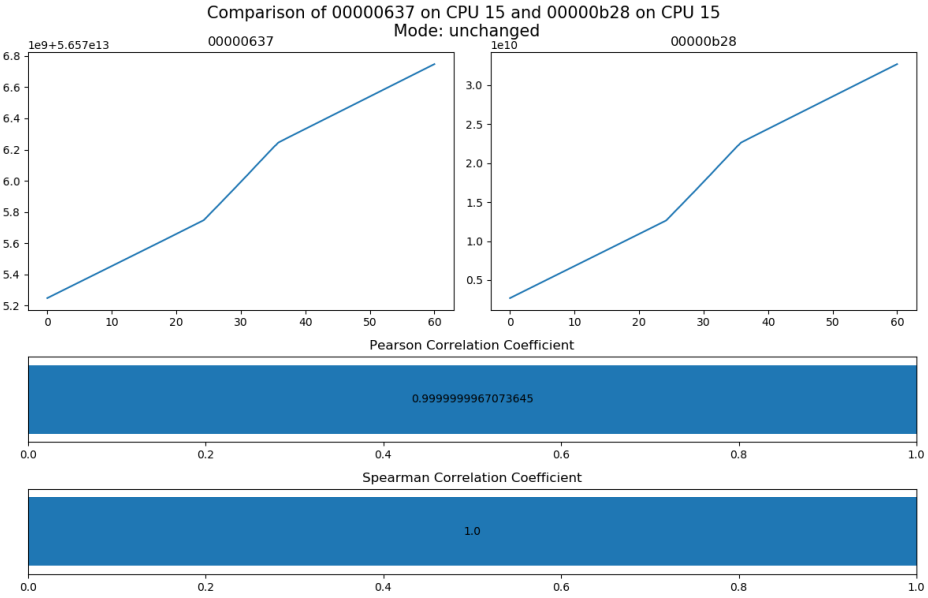


**Figure 10.35:** Correlation of MSR 0x637 and 0xb28.

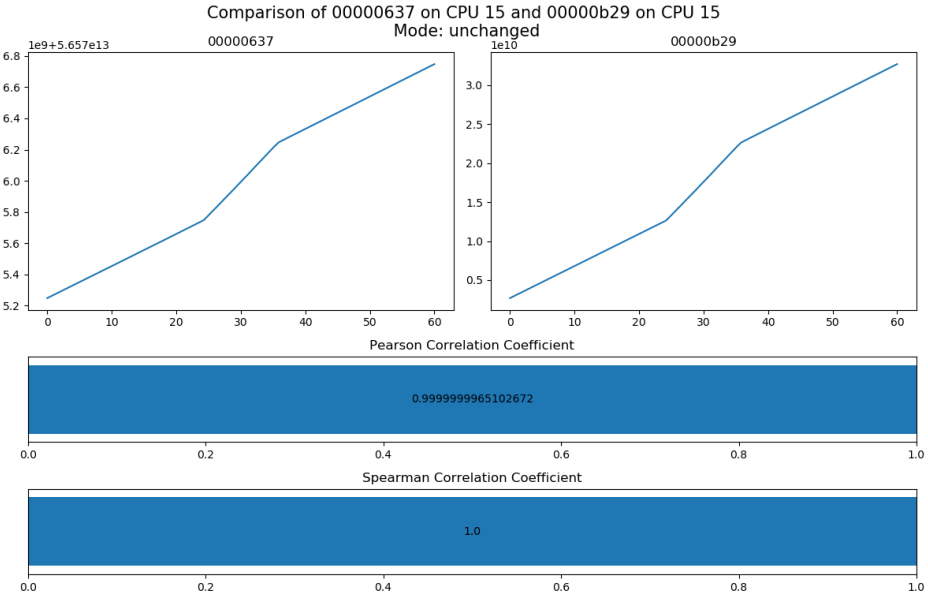


**Figure 10.36:** Correlation of MSR 0x637 and 0xb29.

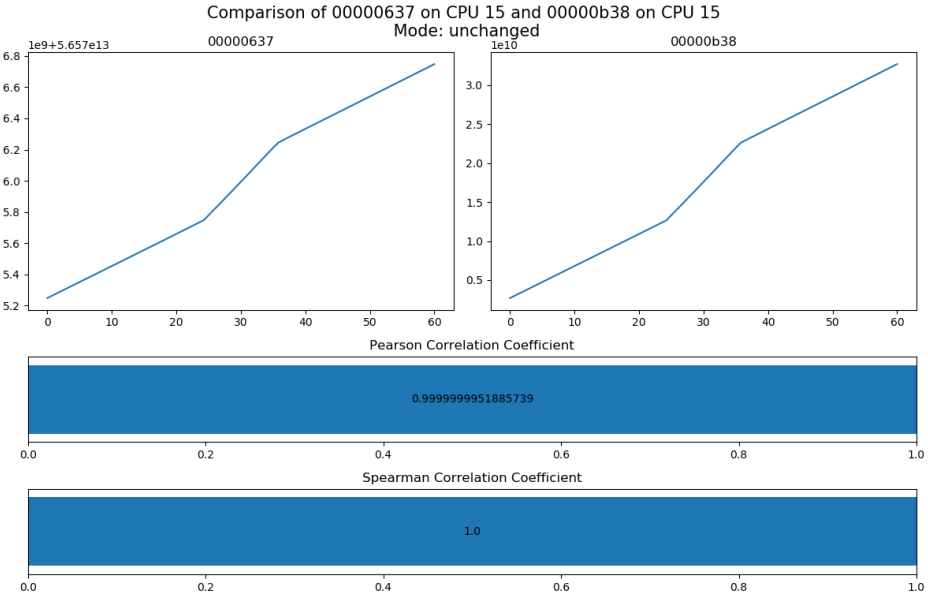


**Figure 10.37:** Correlation of MSR 0x637 and 0xb38.

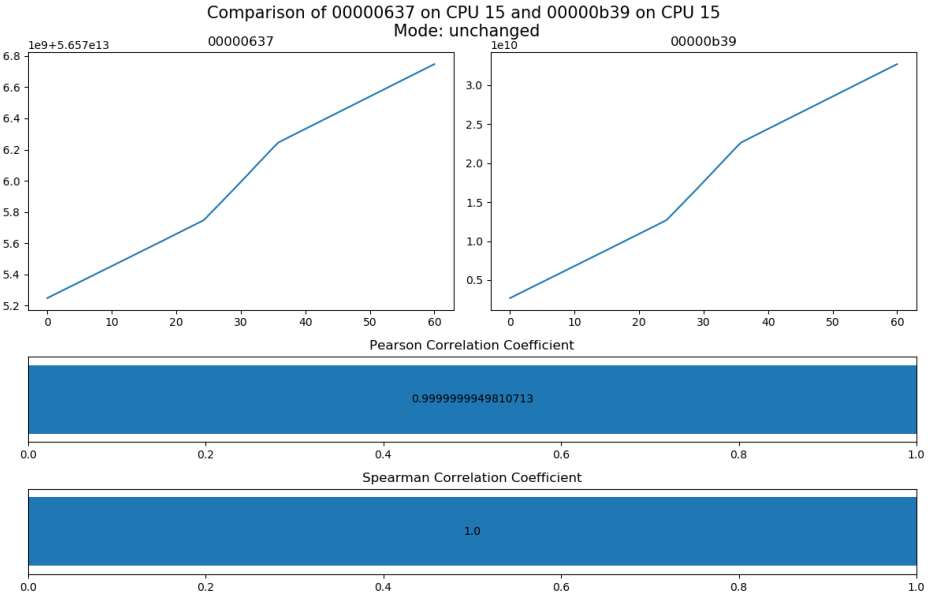


**Figure 10.38:** Correlation of MSR 0x637 and 0xb39.

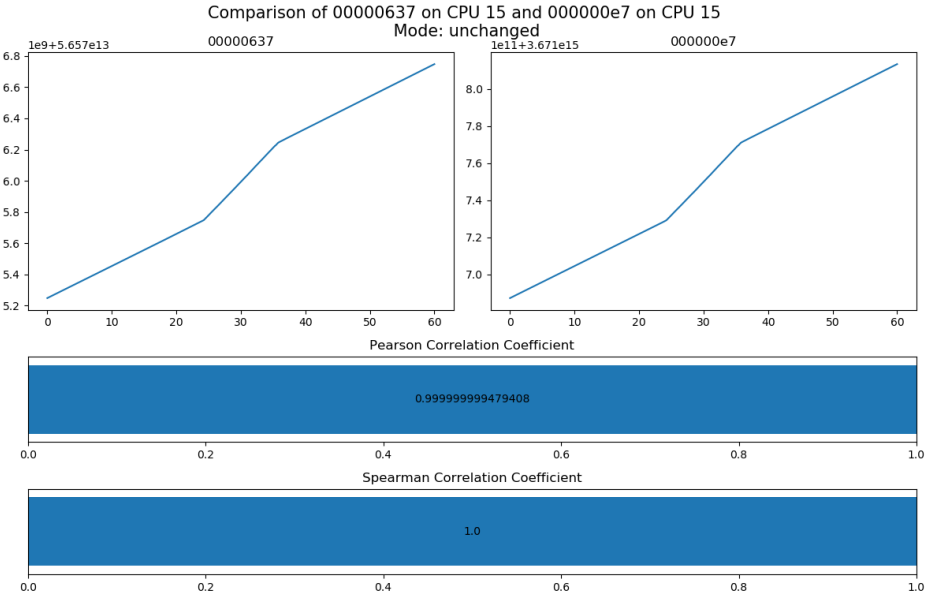


**Figure 10.39:** Correlation of MSR 0x637 and 0xe7.

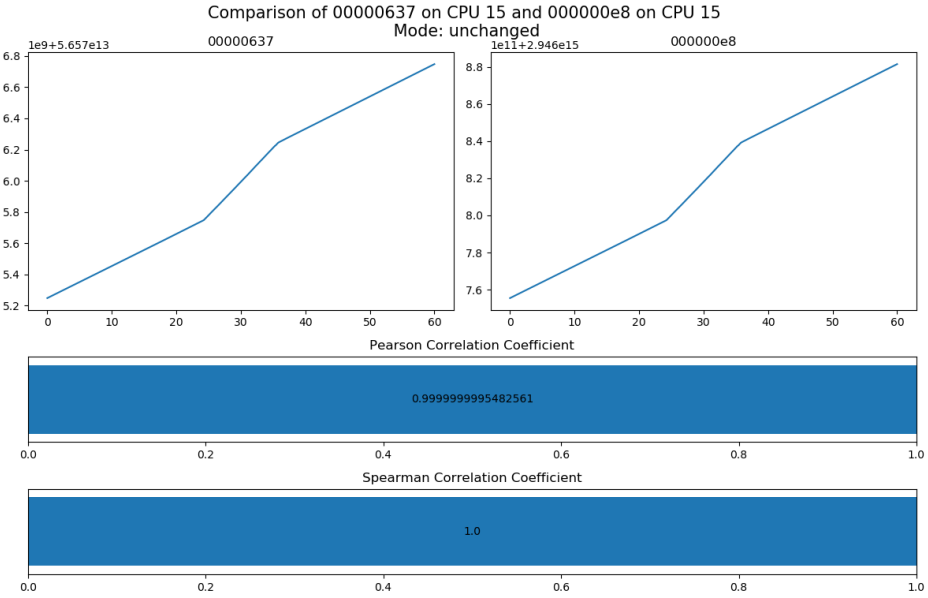


**Figure 10.40:** Correlation of MSR 0x637 and 0xe8.

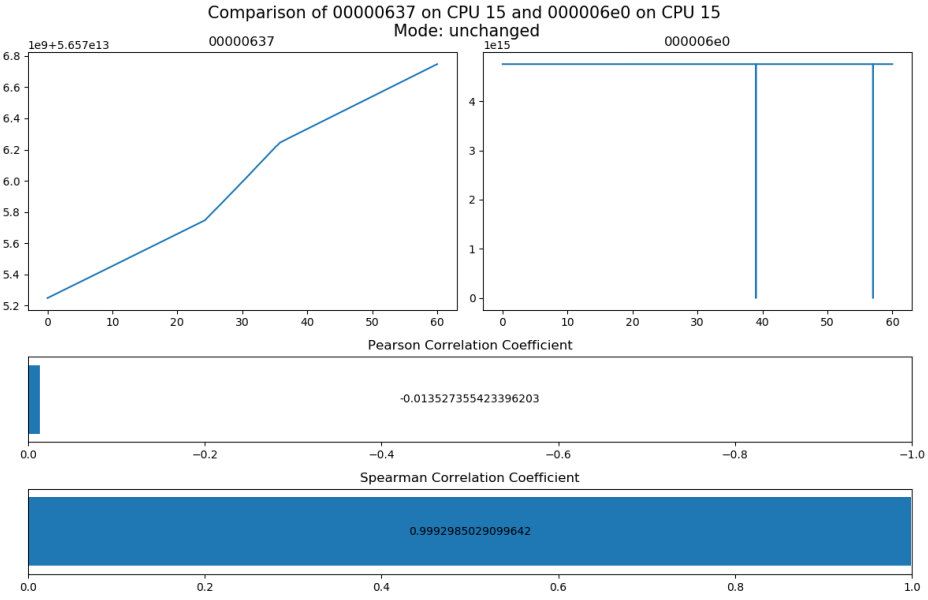


**Figure 10.41:** Correlation of MSR 0x637 and 0x6e0.

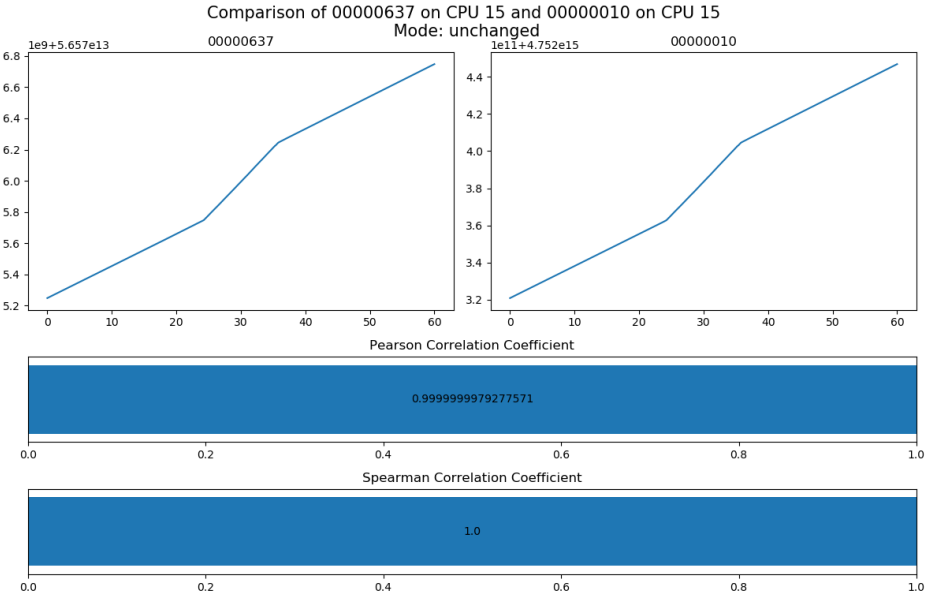


**Figure 10.42:** Correlation of MSR 0x637 and 0x10.

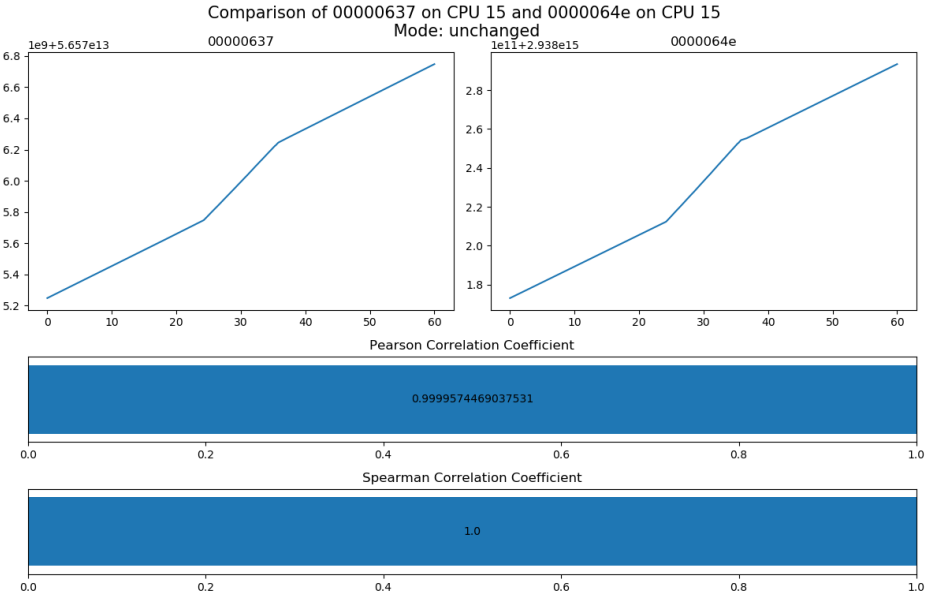


**Figure 10.43:** Correlation of MSR 0x637 and 0x64e.

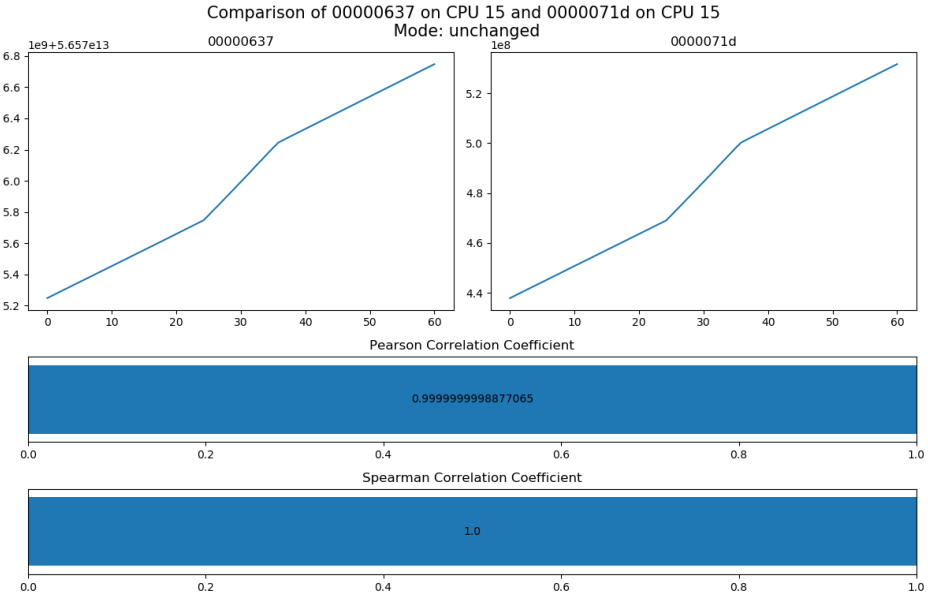


**Figure 10.44:** Correlation of MSR 0x637 and 0x71d.

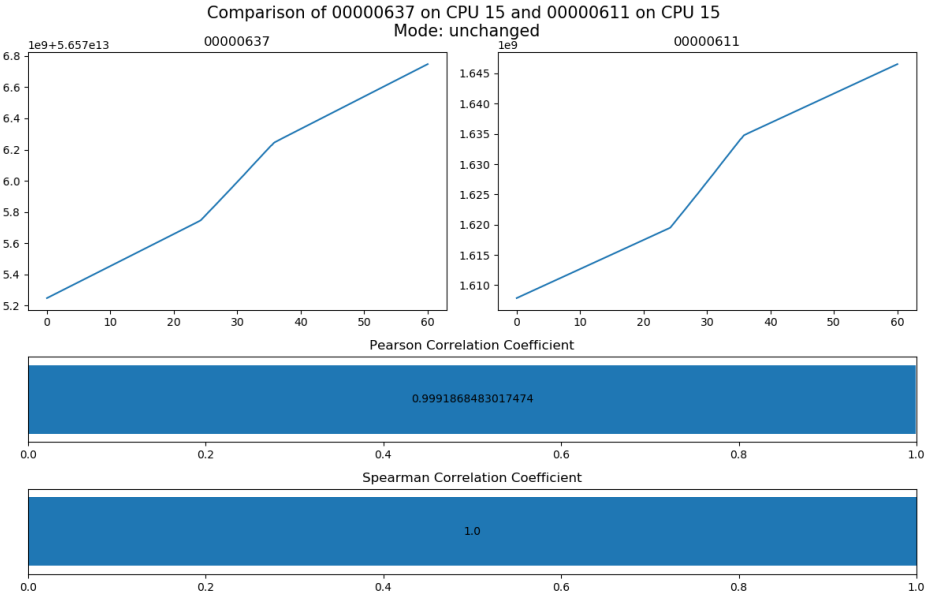


**Figure 10.45:** Correlation of MSR 0x637 and 0x611.

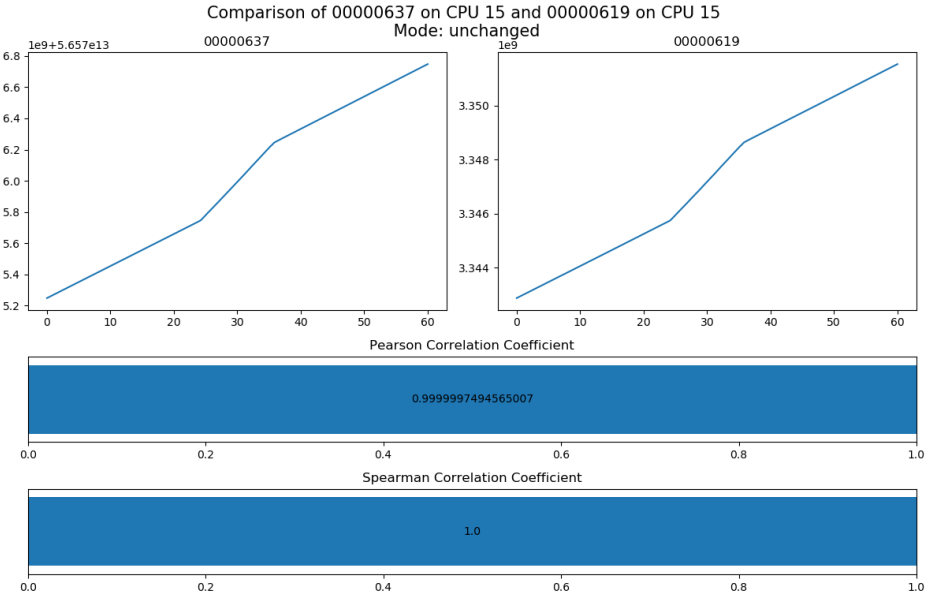


**Figure 10.46:** Correlation of MSR 0x637 and 0x619.

### 10.3.2 Correlations of MSR 0x1a1 with MSR IA32_PACKAGE_THERM_STATUS (0x1b1) on Intel Core CPUs

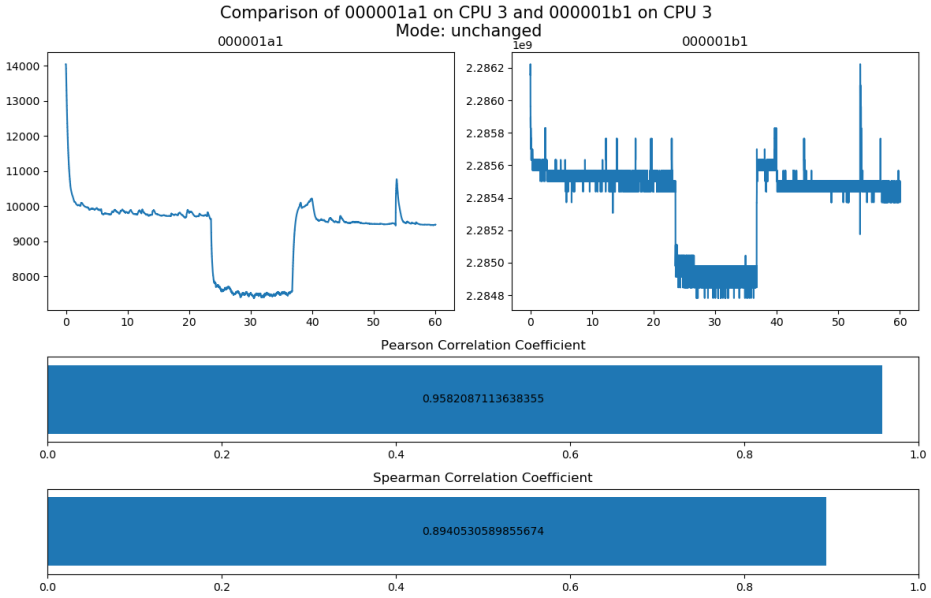


**Figure 10.47:** Correlation of MSR 0x1a1 and the IA32_PACKAGE_THERM_STATUS MSR (0x1b1) on the Intel Core i7-6700K

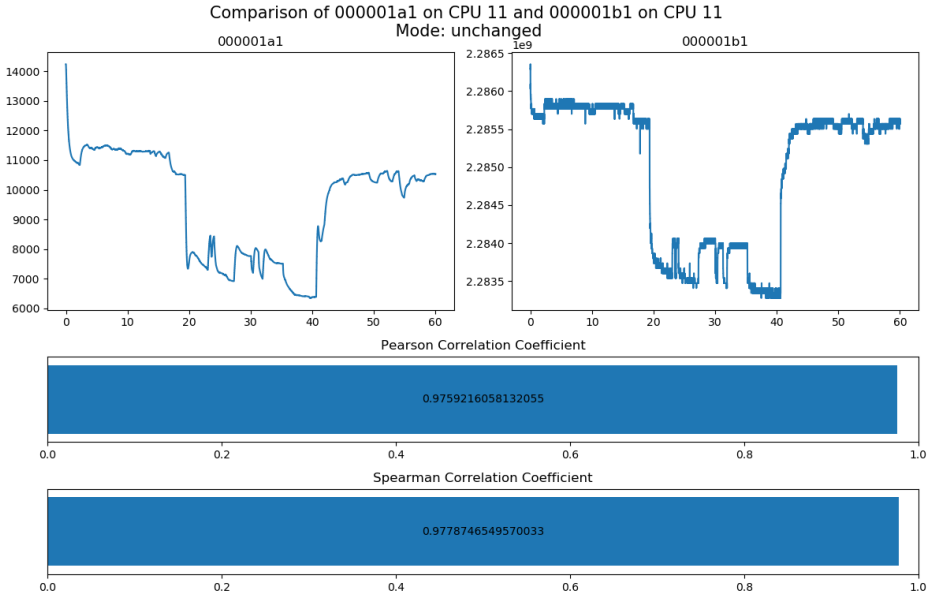


**Figure 10.48:** Correlation of MSR 0x1a1 and the IA32_PACKAGE_THERM_STATUS MSR (0x1b1) on the Intel Core i7-8700K

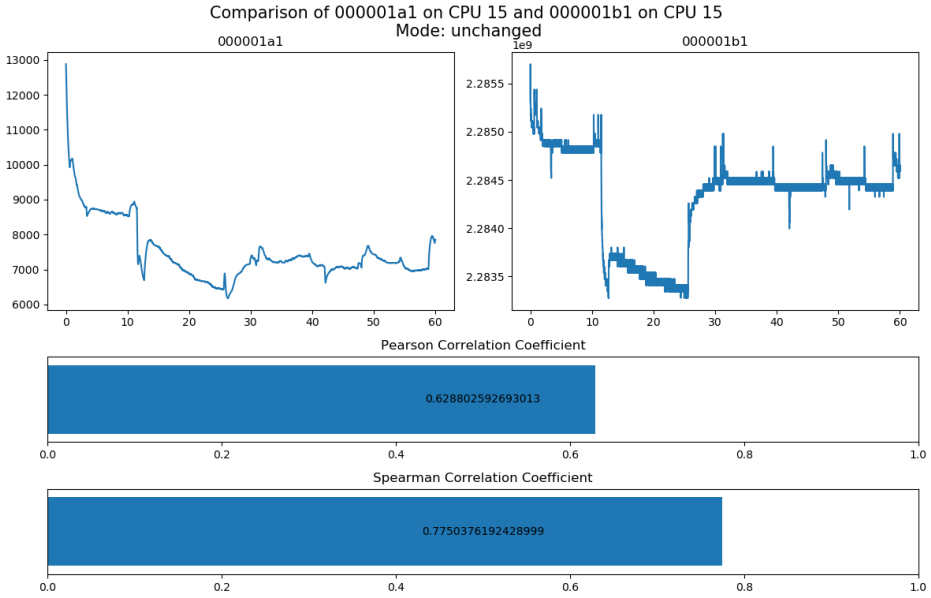


**Figure 10.49:** Correlation of MSR 0x1a1 and the IA32_PACKAGE_THERM_STATUS MSR (0x1b1) on the Intel Core i9-9900K

### 10.3.3 Strong correlations of 0x637 on all tested Intel Core CPUs

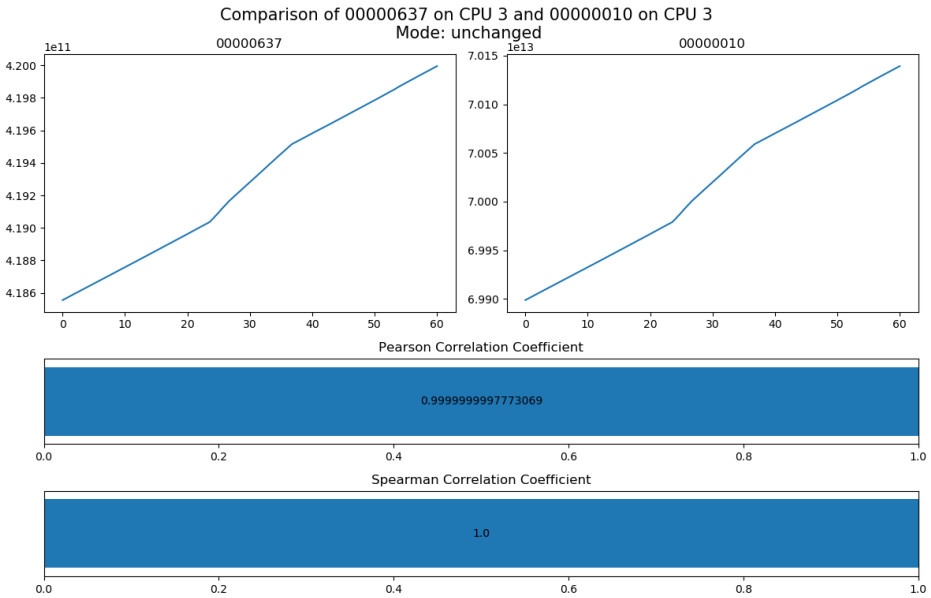


**Figure 10.50:** Correlation of MSR 0x637 and MSR 0x10 on the Intel Core i7-6700K.

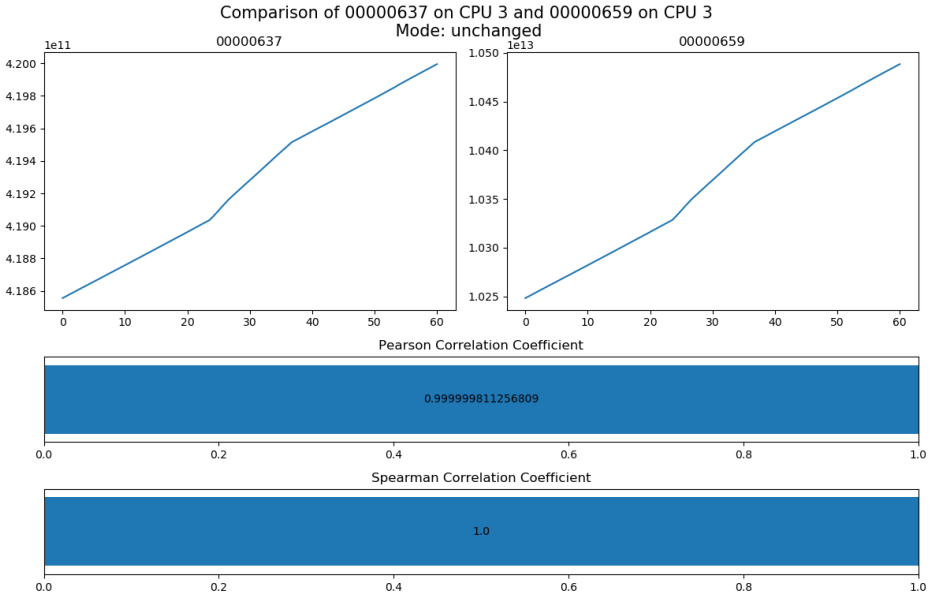


**Figure 10.51:** Correlation of MSR 0x637 and MSR 0x659 on the Intel Core i7-6700K.

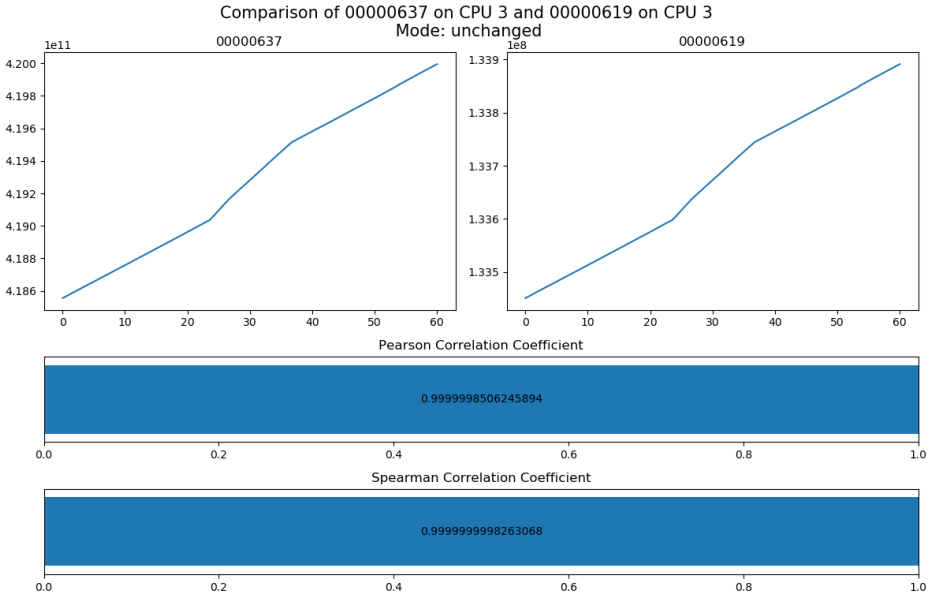


**Figure 10.52:** Correlation of MSR 0x637 and MSR 0x619 on the Intel Core i7-6700K.

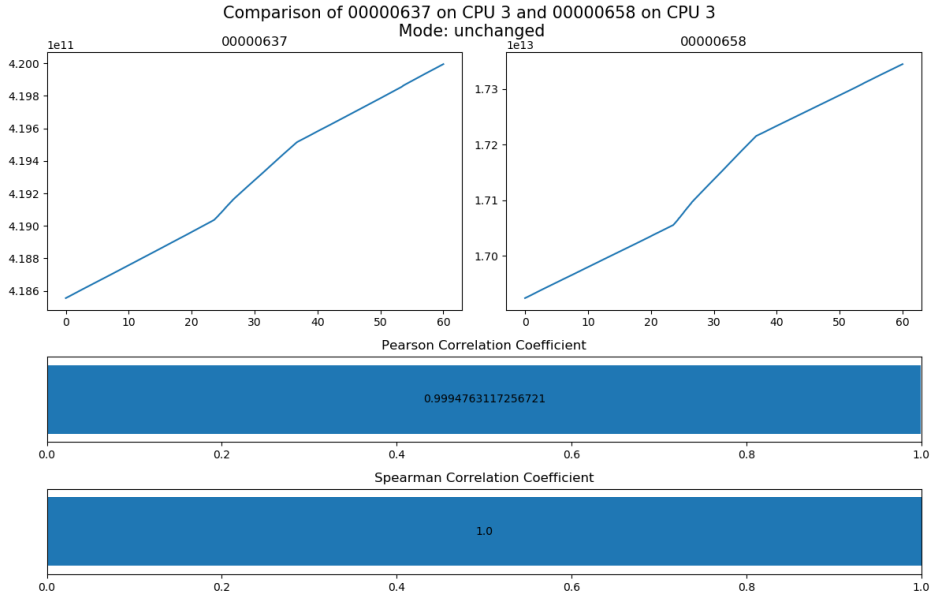


**Figure 10.53:** Correlation of MSR 0x637 and MSR 0x658 on the Intel Core i7-6700K.

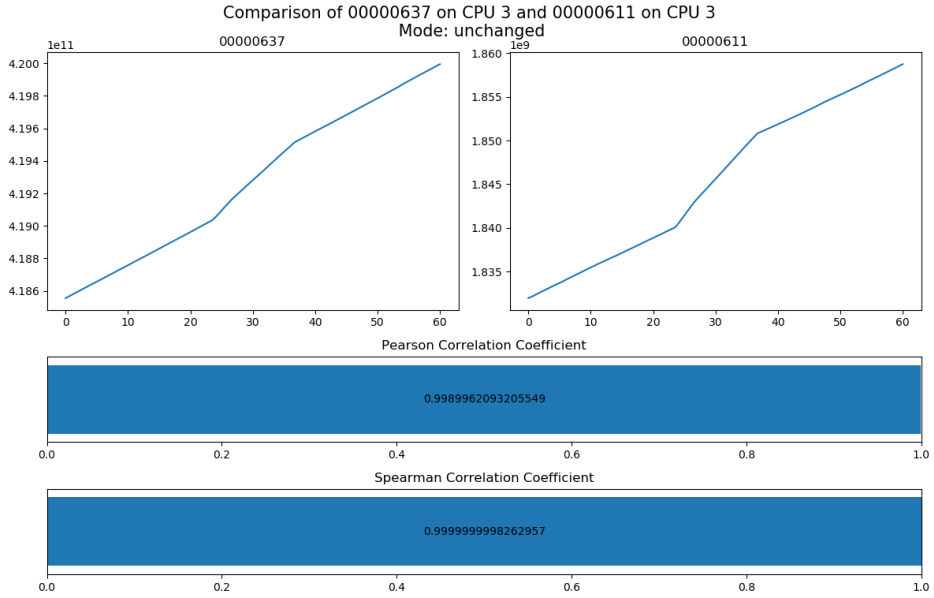


**Figure 10.54:** Correlation of MSR 0x637 and MSR 0x611 on the Intel Core i7-6700K.

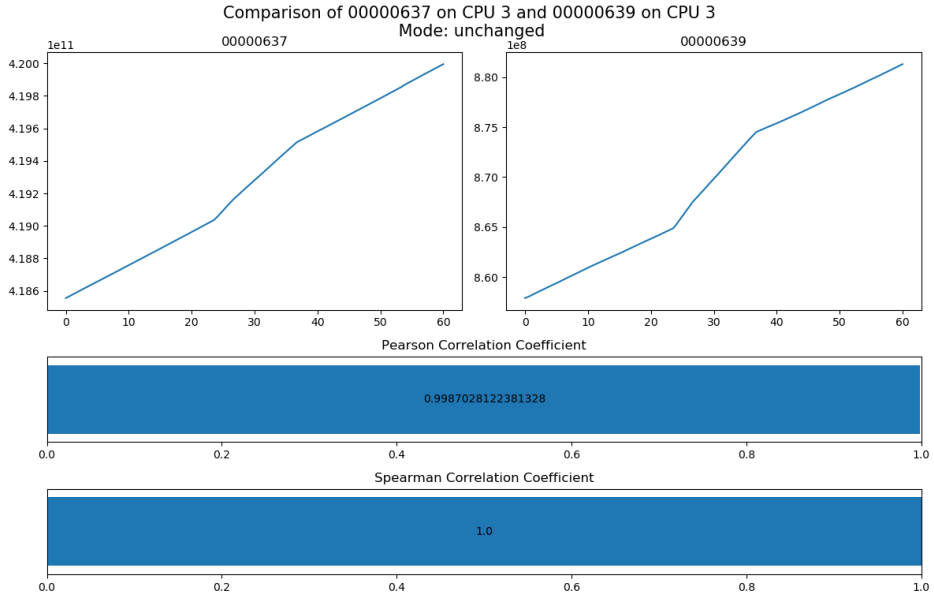


**Figure 10.55:** Correlation of MSR 0x637 and MSR 0x639 on the Intel Core i7-6700K.

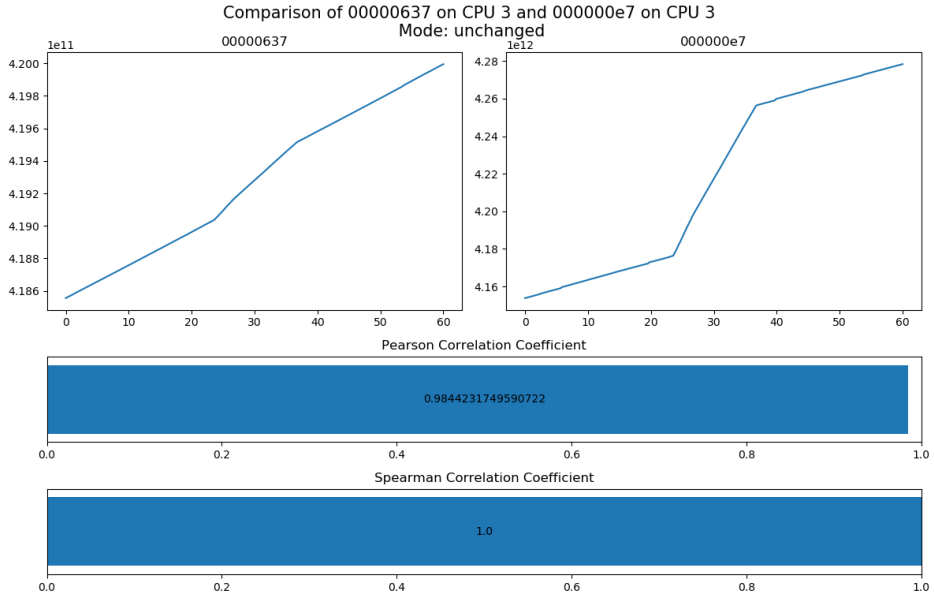


**Figure 10.56:** Correlation of MSR 0x637 and MSR 0xe7 on the Intel Core i7-6700K.

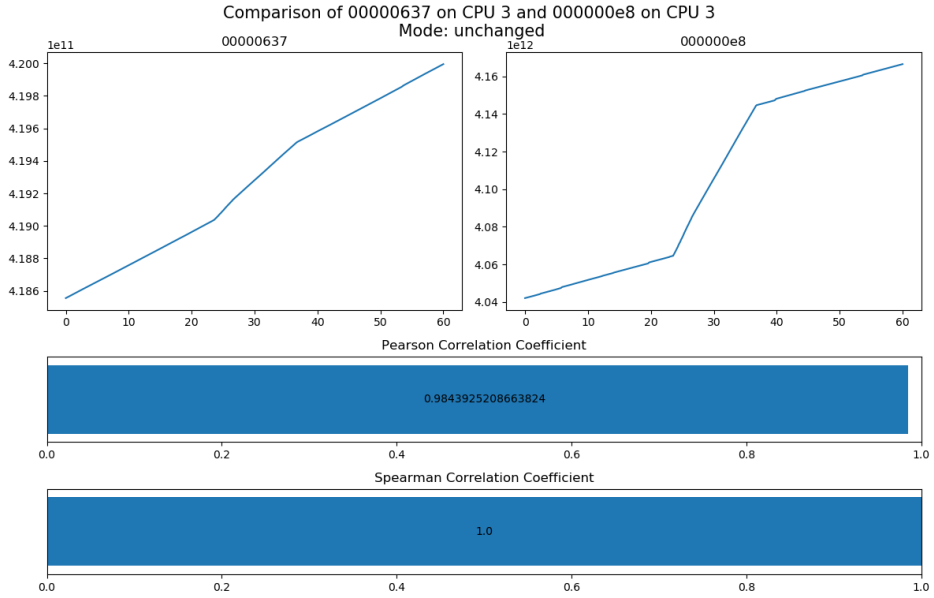


**Figure 10.57:** Correlation of MSR 0x637 and MSR 0xe8 on the Intel Core i7-6700K.

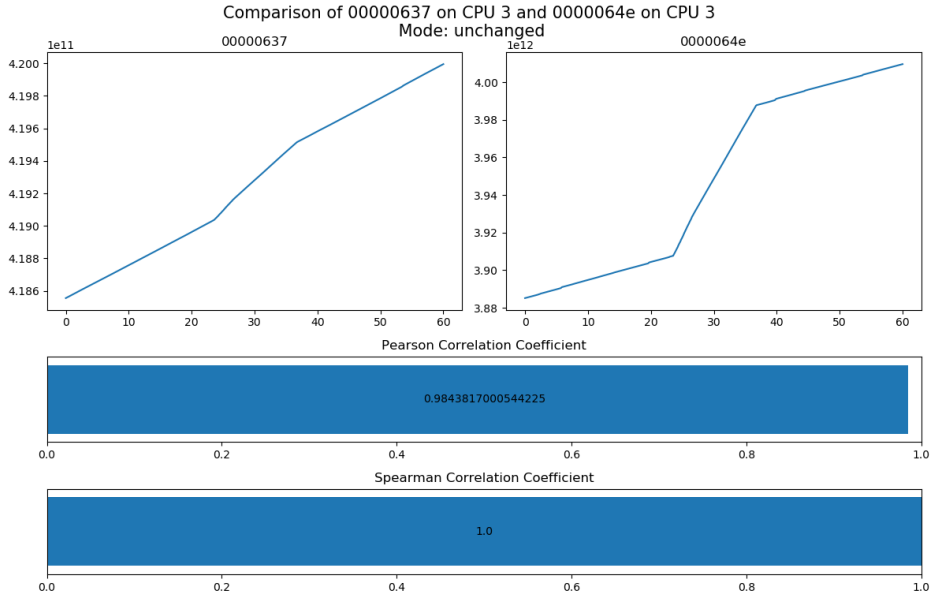


**Figure 10.58:** Correlation of MSR 0x637 and MSR 0x64e on the Intel Core i7-6700K.

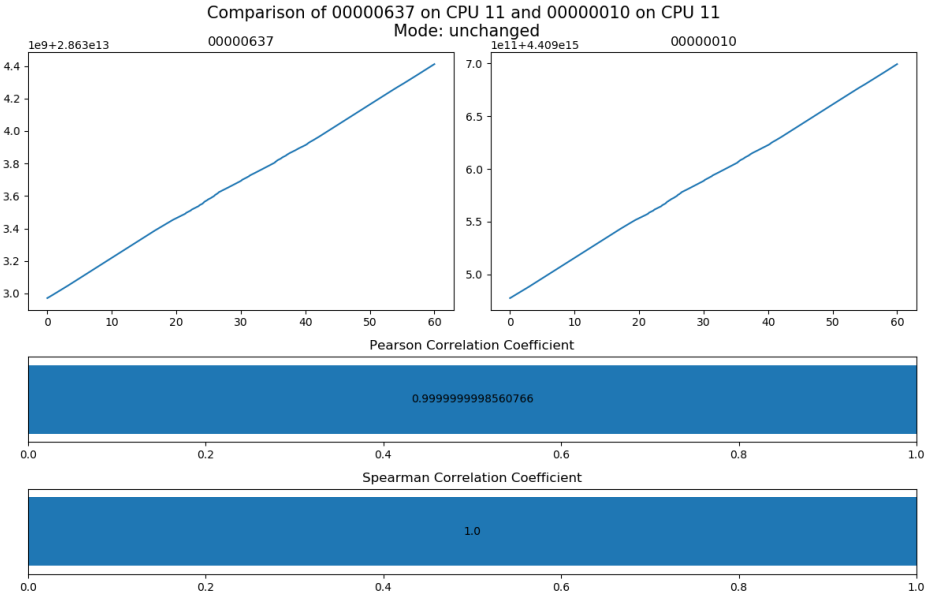


**Figure 10.59:** Correlation of MSR 0x637 and MSR 0x10 on the Intel Core i7-8700K.

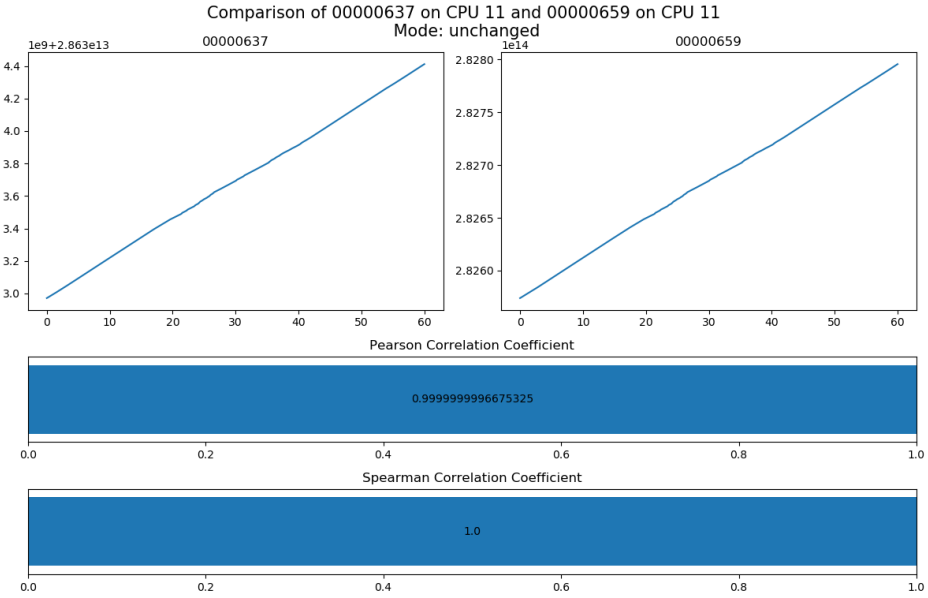


**Figure 10.60:** Correlation of MSR 0x637 and MSR 0x659 on the Intel Core i7-8700K.

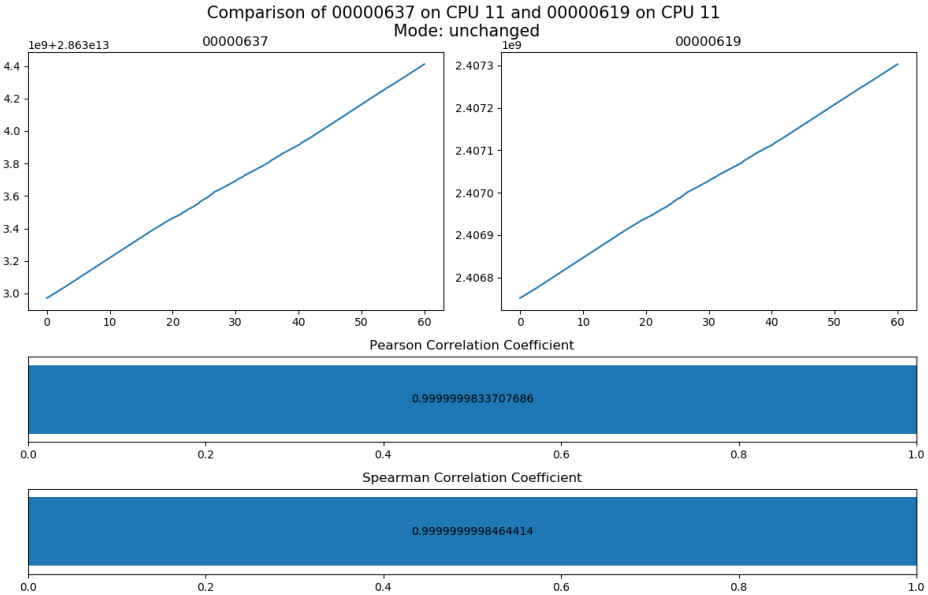


**Figure 10.61:** Correlation of MSR 0x637 and MSR 0x619 on the Intel Core i7-8700K.

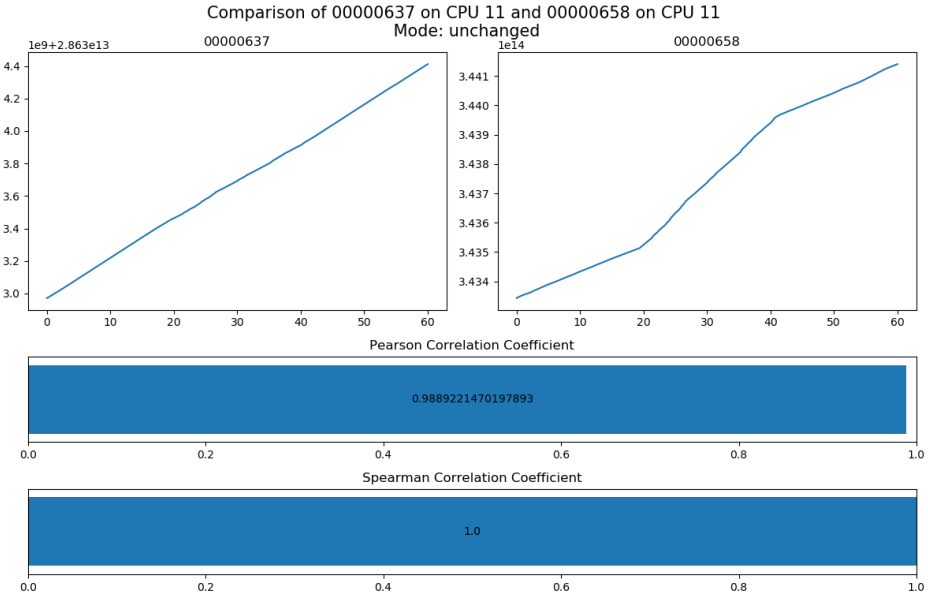


**Figure 10.62:** Correlation of MSR 0x637 and MSR 0x658 on the Intel Core i7-8700K.

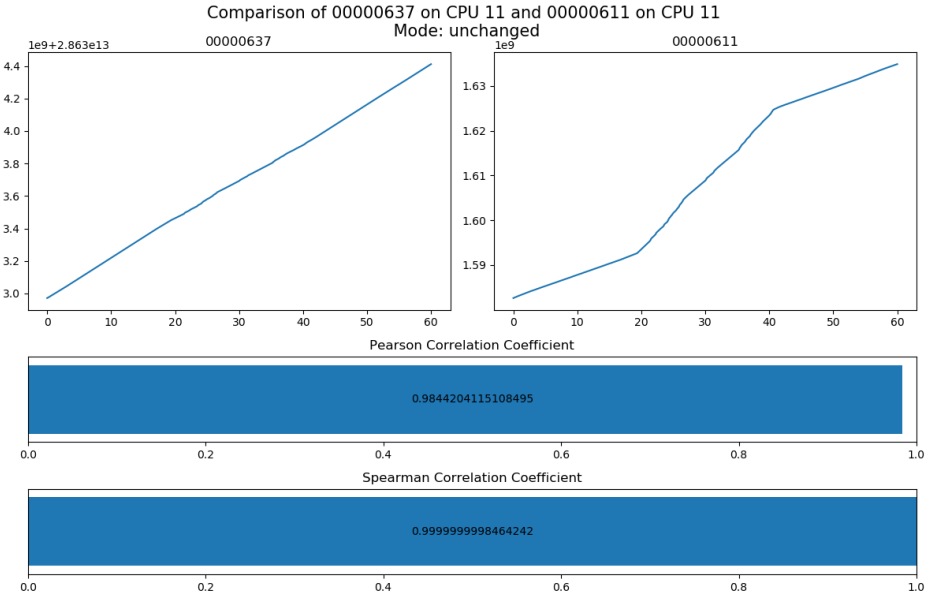


**Figure 10.63:** Correlation of MSR 0x637 and MSR 0x611 on the Intel Core i7-8700K.

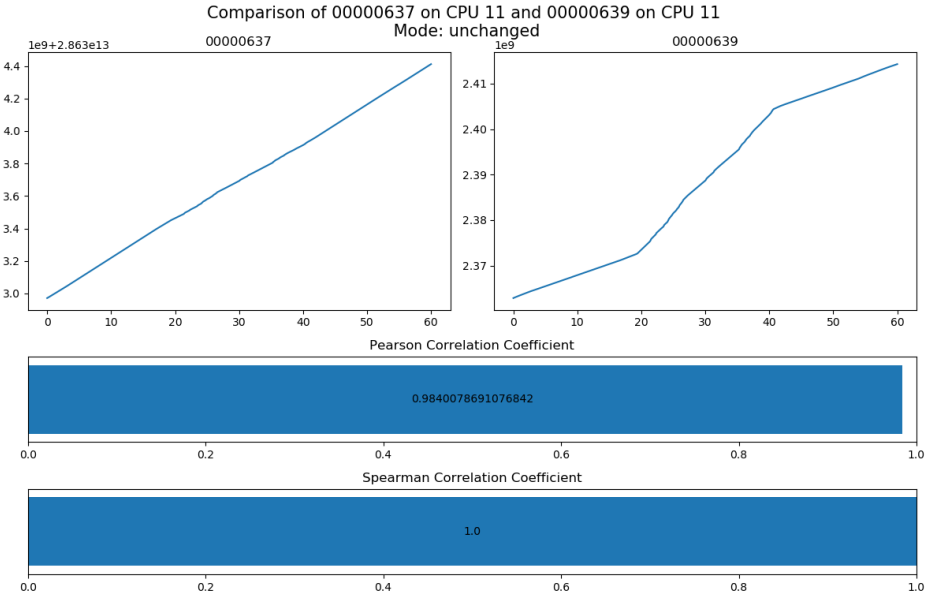


**Figure 10.64:** Correlation of MSR 0x637 and MSR 0x639 on the Intel Core i7-8700K.

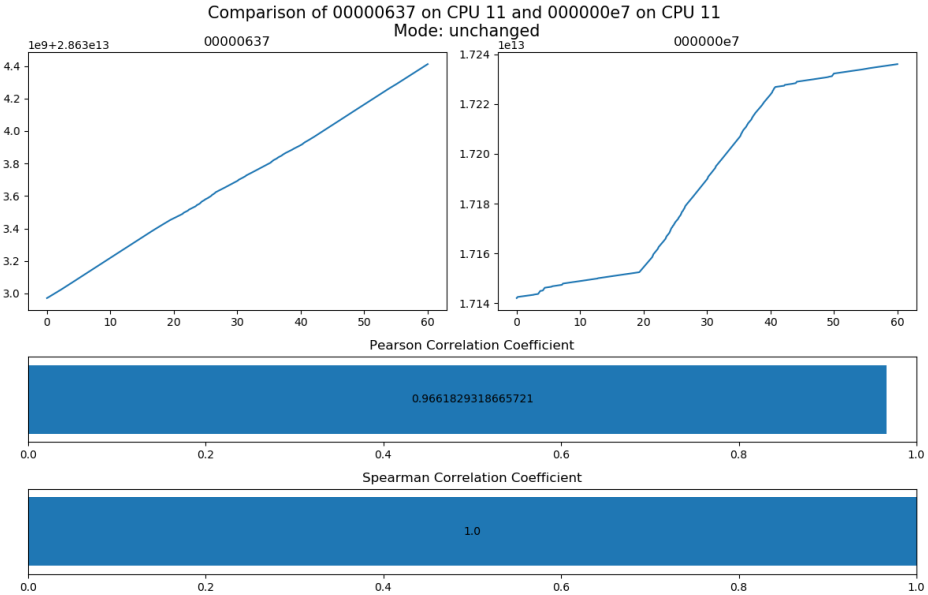


**Figure 10.65:** Correlation of MSR 0x637 and MSR 0xe7 on the Intel Core i7-8700K.

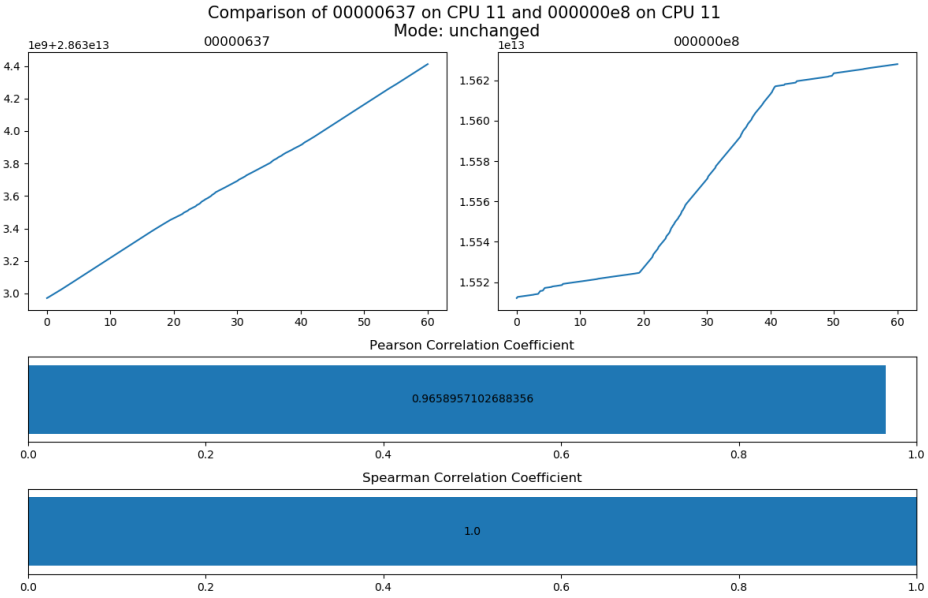


**Figure 10.66:** Correlation of MSR 0x637 and MSR 0xe8 on the Intel Core i7-8700K.

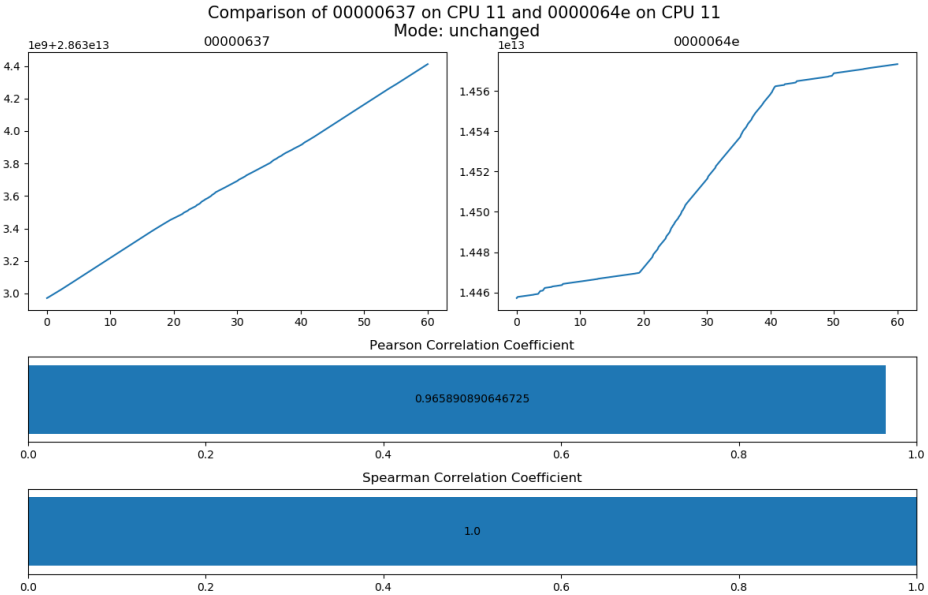


**Figure 10.67:** Correlation of MSR 0x637 and MSR 0x64e on the Intel Core i7-8700K.

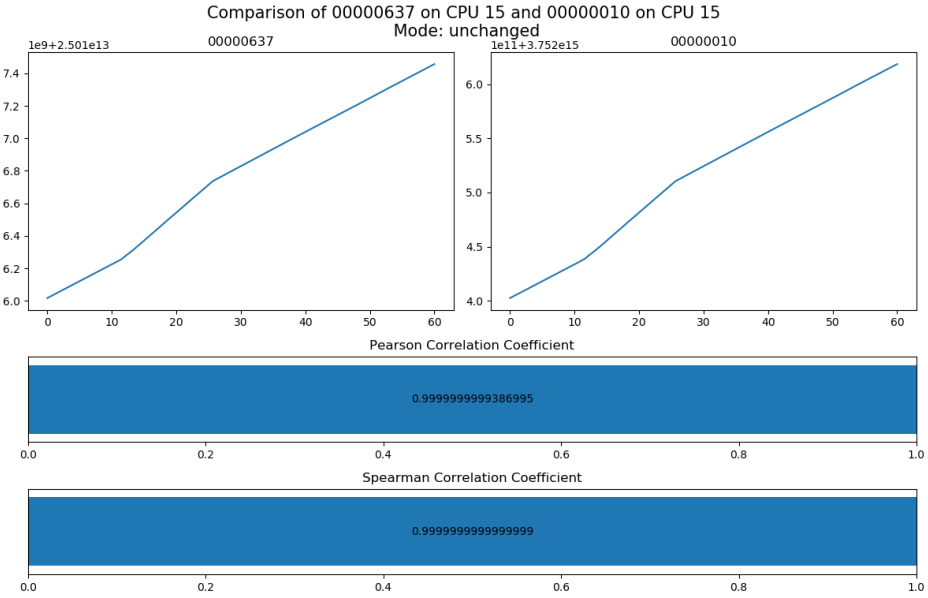


**Figure 10.68:** Correlation of MSR 0x637 and MSR 0x10 on the Intel Core i9-9900K.

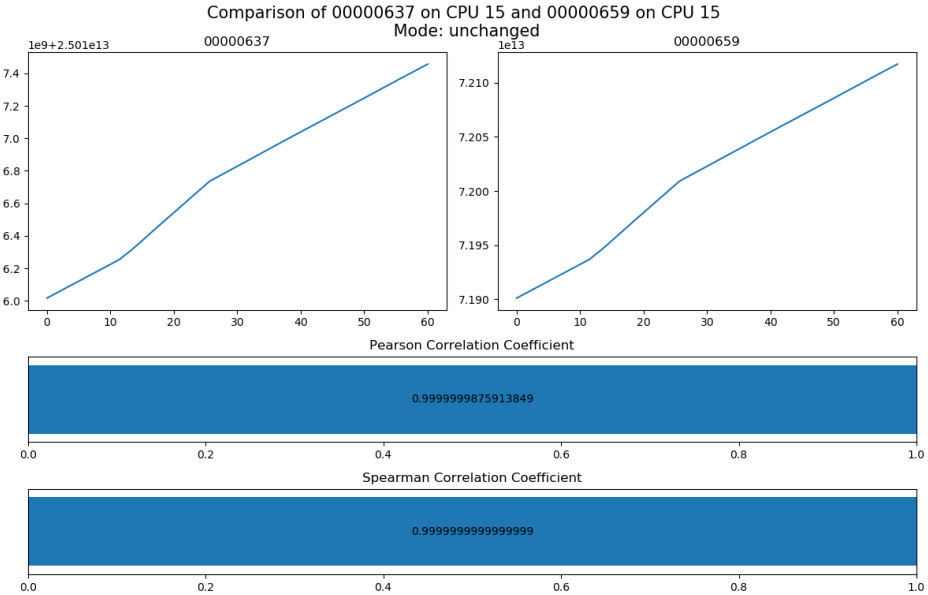


**Figure 10.69:** Correlation of MSR 0x637 and MSR 0x659 on the Intel Core i9-9900K.

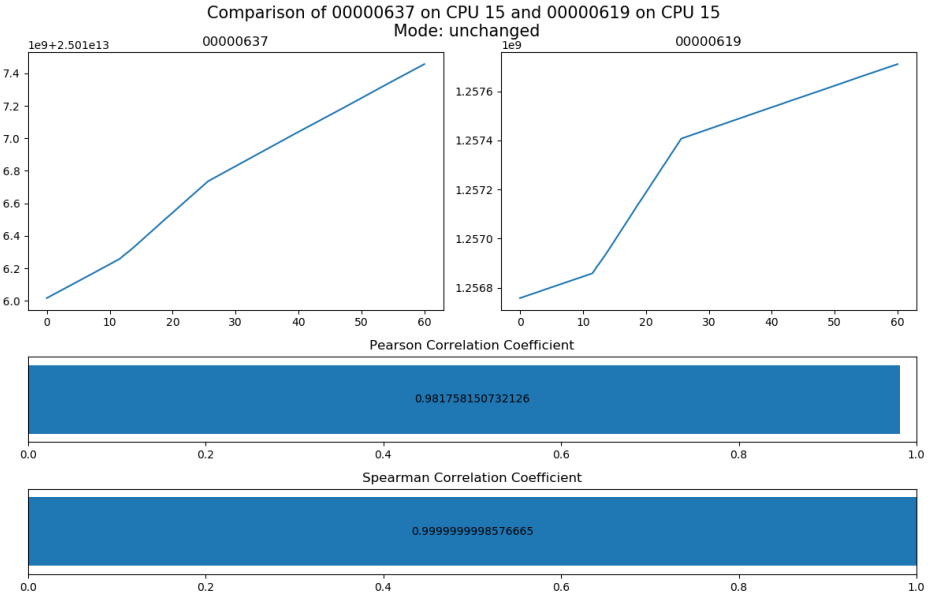


**Figure 10.70:** Correlation of MSR 0x637 and MSR 0x619 on the Intel Core i9-9900K.

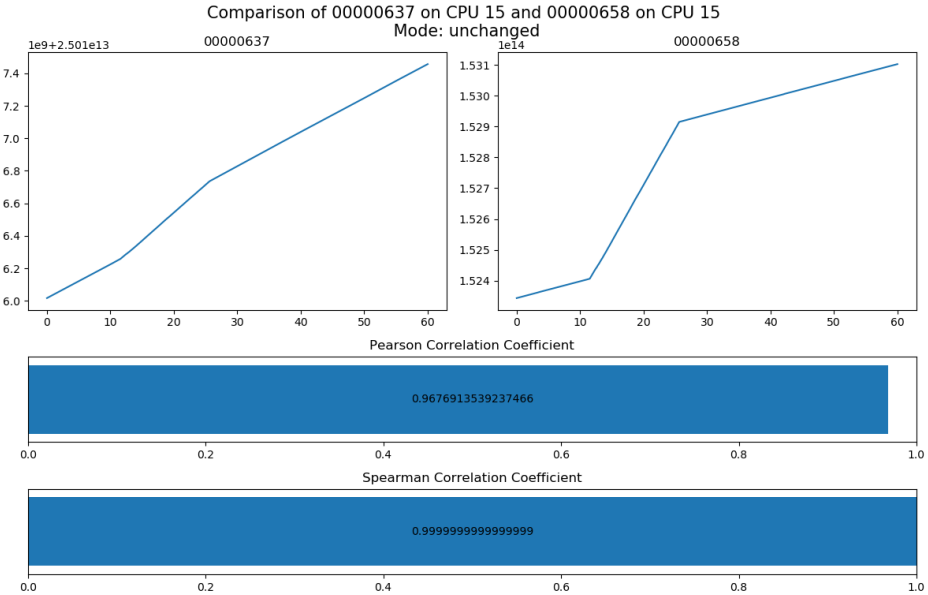


**Figure 10.71:** Correlation of MSR 0x637 and MSR 0x658 on the Intel Core i9-9900K.

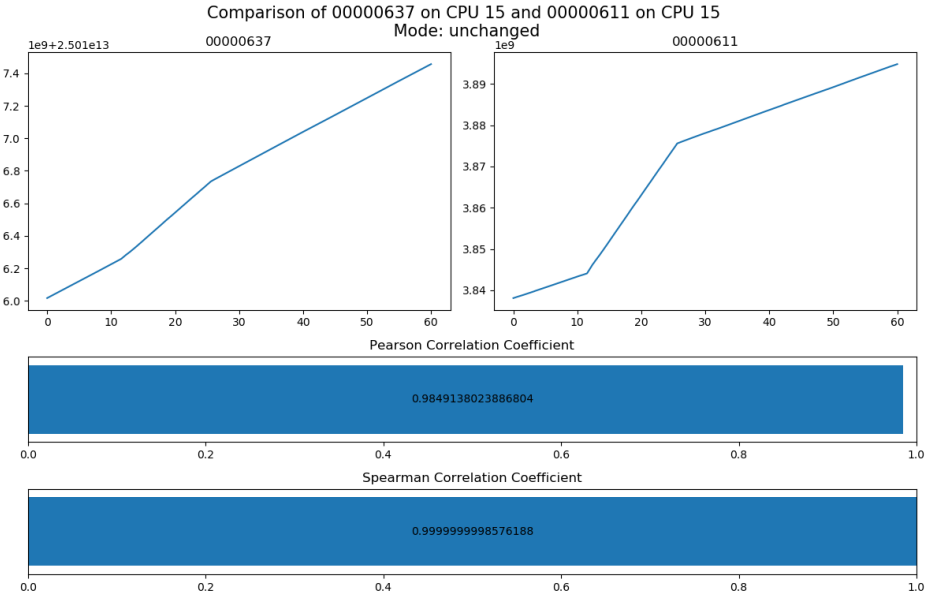


**Figure 10.72:** Correlation of MSR 0x637 and MSR 0x611 on the Intel Core i9-9900K.

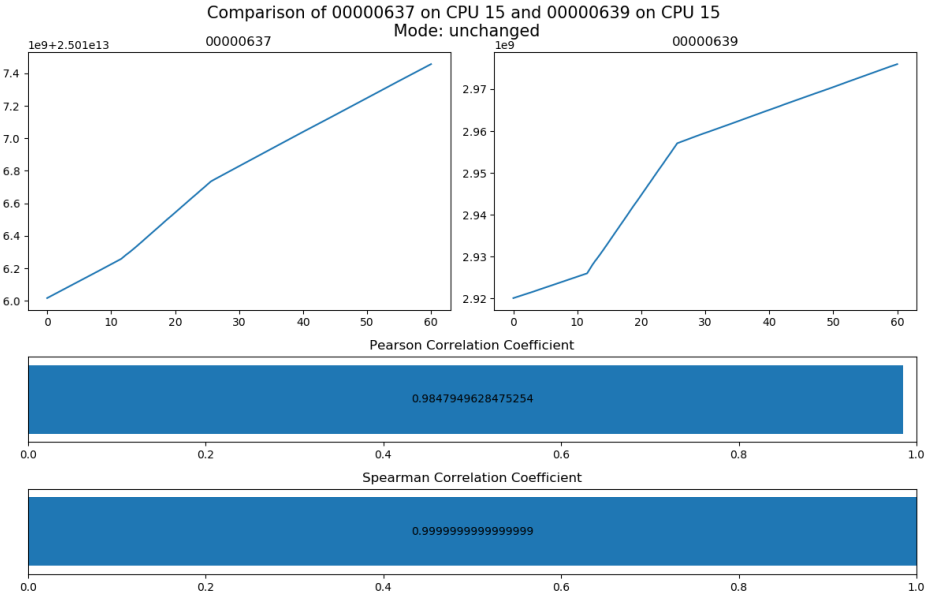


**Figure 10.73:** Correlation of MSR 0x637 and MSR 0x639 on the Intel Core i9-9900K.

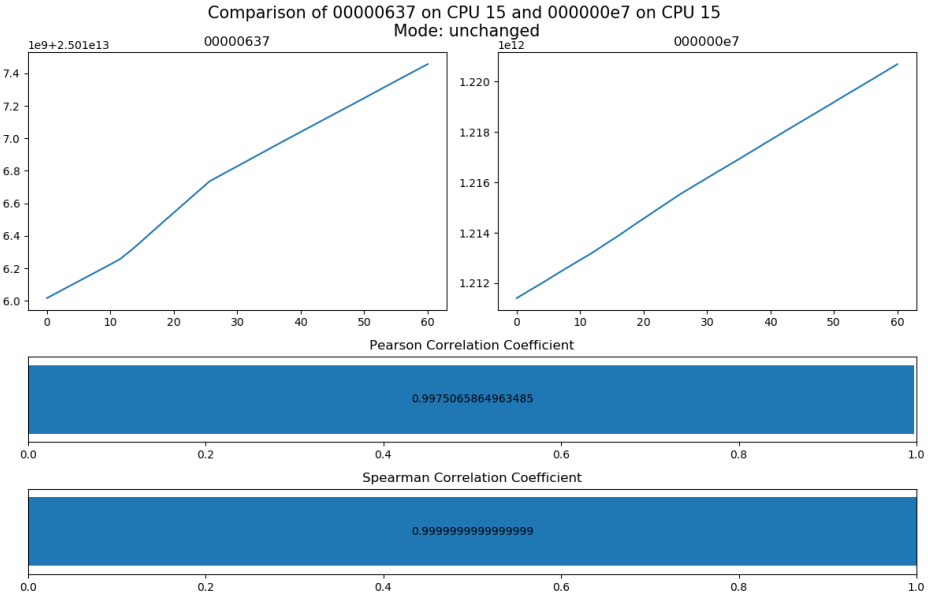


**Figure 10.74:** Correlation of MSR 0x637 and MSR 0xe7 on the Intel Core i9-9900K.

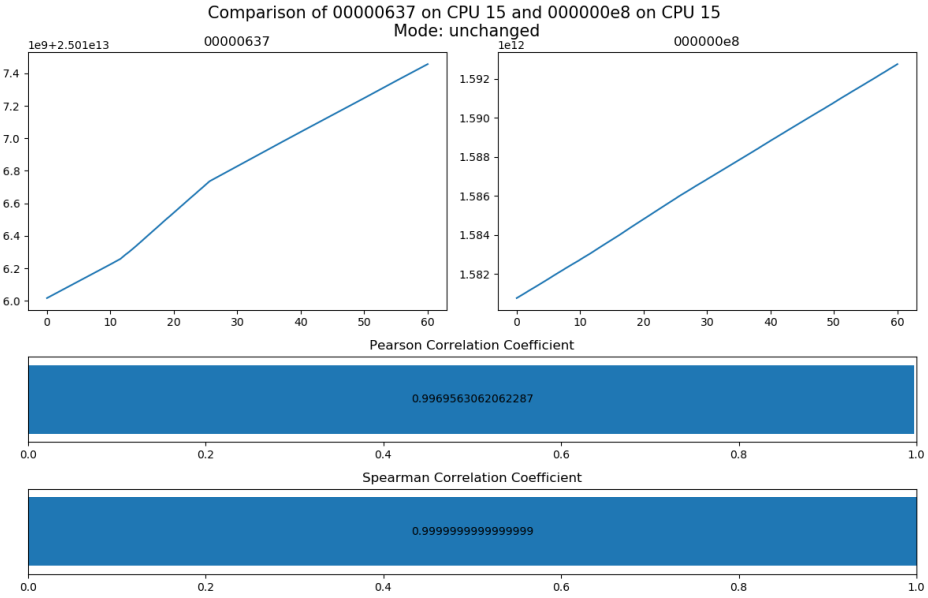


**Figure 10.75:** Correlation of MSR 0x637 and MSR 0xe8 on the Intel Core i9-9900K.

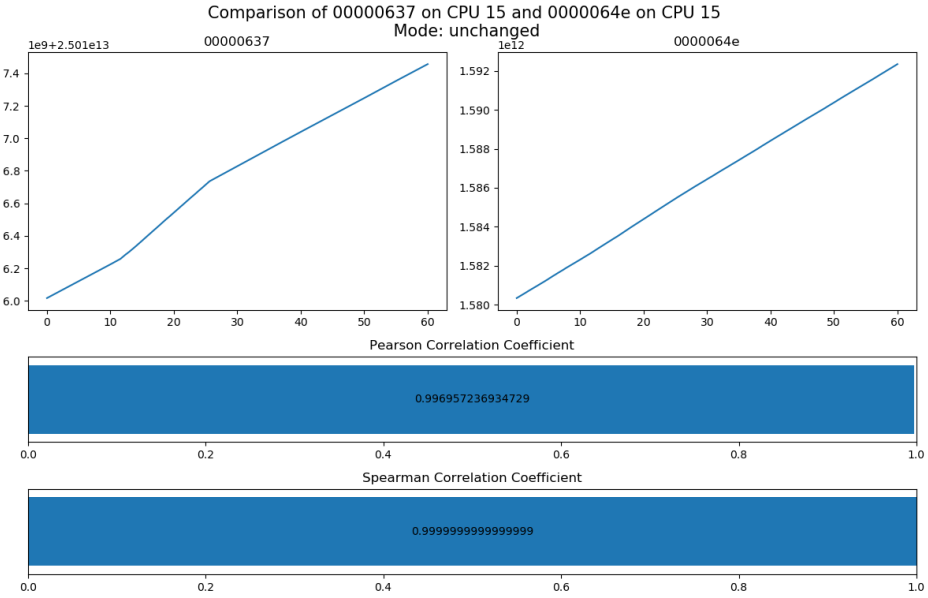


**Figure 10.76:** Correlation of MSR 0x637 and MSR 0x64e on the Intel Core i9-9900K.