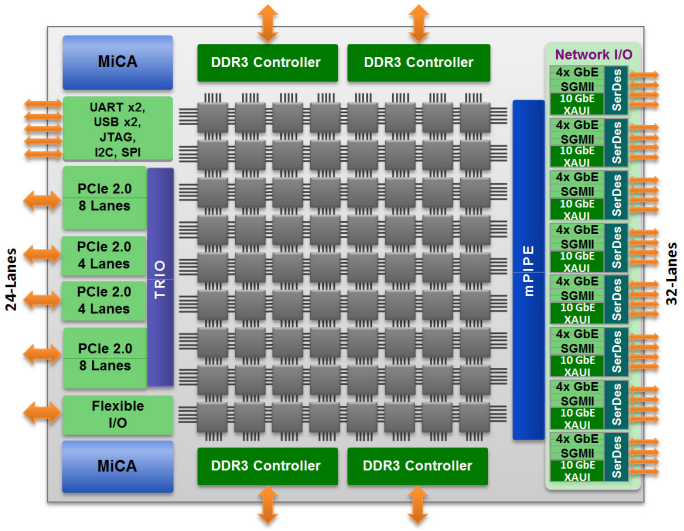
TILE-Gx8072™ Processor

Specification Brief

The TILE-Gx8072™ Processor is optimized for intelligent networking, multimedia and cloud applications and delivers remarkable compute and I/O with complete "system-on-a-chip" features. The device includes 72 identical processor cores (tiles) interconnected with Tilera's iMesh™ on-chip network. Each tile consists of a full-featured processor core as well as L1 and L2 cache and a non-blocking Terabit/sec switch that connects the tiles into the mesh and providing full cache coherence among all the cores.

The TILE-Gx8072™ is ideal for applications such as:

- 80 Gbps of networking dataplane offload
- High-peformance compute offload across PCIe
- H.264/H.265 high-density video transcoding



Powerful Processor Cores

- 72 cores @ 1.0 to 1.2 GHz
- 64-bit architecture (datapath and address)
- 3 execution pipelines
- Robust virtual memory system with TLBs, multiple page size support and Hardwall™ protection
- ISA extensions for multimedia and SIMD processing

Cache

- 23 Mbytes total on-chip cache
- Dynamic Distributed Cache (DDC™) scalable hardware coherence
- 32 KB L1i, 32K L1d per core
- 256 KB L2 per core
- 18 MB coherent L3 cache

iMesh Interconnect

- Five independent low-latency mesh networks
- >100 Tbps aggregate bandwidth
- Non-blocking, cuthrough switching with 1 clock cycle per hop

Integrated Memory Controllers

- Four 72-bit DDR3 controllers with ECC support
- 1 TB total memory capacity
- Up to 1,866 MT/s speeds
- Advanced request reordering

PCI Express

- 96 Gbps of PCIe throughput
- Six integrated Gen2 PCIe controllers (5G SerDes) with 24 lanes
- Each configurable as root complex or endpoint
- High-performance coherent transaction DMA engine
- Multiple configurable transaction modes for efficient data movement
- SR-IOV support

StreamIO Interfaces

- Six high-performance transaction ports for chip-to-chip or FPGA interconnect
- Multiplexed with PCIe SerDes
- 20 Gbps peak performance per 4-lane port

Networking Interfaces

- Eight 10 Gbps XAUI ports, including double-XAUI support
- Up to thirty two 10/100/1000 SGMII ports (multiplexed with XAUI ports)
- Egress QoS queuing and traffic shaping support
- IEEE1588v2 precision timing controller support
- IEEE802.1Qbb priority flow control and datacenter Ethernet (DCE) support
- Precision 1ns granularity packet timestamping

mPIPE™ Wire-speed Packet Engine

- C-programmable classification
- 120 Mpps performance for minimum size packets
- Programmable checksum and CRC offload for packet headers and payload
- Multi-mode load-balancer with direct-to-cache packet delivery
- Flexible buffer manager with 64 configurable memory domains

MiCA Acceleration Engines

- MiCA™ engines deliver low-latency, high-bandwidth offload
- 40 Gbps encryption throughput (-E option)
- Support for IPsec, SSL, TLS, MACsec, SRTP, 3GPP
- Public Key accelerator (RSA, DSA, DH, ECC)
- True random number generator (TRNG)

System Integration Features

- Two USB 2.0 interfaces; one host and one host/endpoint
- Four I²C interfaces
- One SPI (master) interface
- Two high-speed UART interfaces
- 48 GPIO/Interrupt pins
- JTAG port

Package Information

- 45 mm x 45 mm BGA
- 1 mm ball pitch

Ordering Guide

Device	Part Number	Core Frequency	Memory Speed	# of Tiles	Operating Temp	Package
TILE-Gx8072	TLR4-07280DG -10C	1.0 GHz	1,600 MT/s	72	Commercial	1,847 BGA
TILE-Gx8072	TLR4-07280DG -10CE (with crypto)	1.0 GHz	1,600 MT/s	72	Commercial	1,847 BGA

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PRELIMINARY: Specifications subject to change without notice.

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