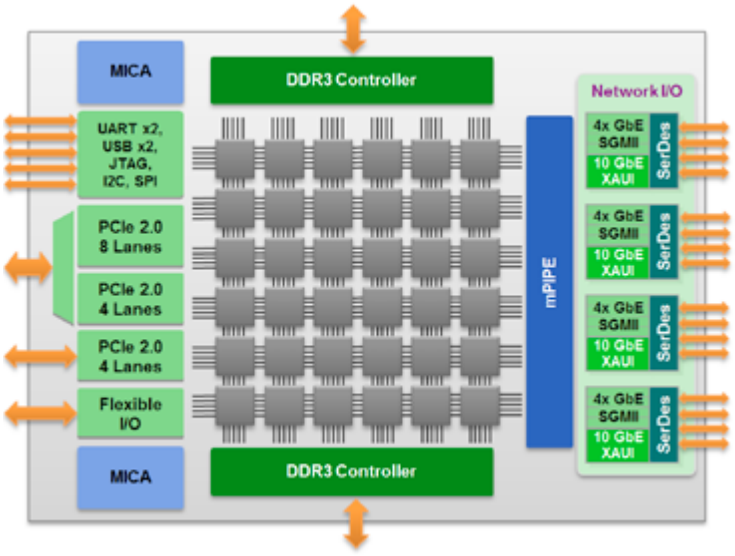
TILE-Gx8036™ Processor

Specification Brief

The TILE-Gx8036™ Processor is optimized for networking and multimedia applications and delivers enormous compute and I/O with complete "system-on-a-chip" features. The device includes 36 identical processor cores (tiles) interconnected with Tilera's iMesh™ on-chip network. Each tile consists of a full-featured processor core as well as L1 and L2 cache and a non-blocking switch that connects the tiles into the mesh. Each tile can independently run a full operating system, or a group of tiles can run a multi-processing OS, like SMP Linux. The TILE-Gx8036 is ideal for sophisticated networking applications requiring 20 to 40 Gbps of performance.



Powerful Processor Cores

- 36 cores @ 1.0 to 1.2 GHz
- 64-bit architecture (datapath and address)
- 3 execution pipelines
- Robust virtual memory system with TLBs and Hardwall™ protection
- ISA extensions for multimedia and SIMD processing

Cache

- 12 Mbytes total on-chip cache
- Dynamic Distributed Cache (DDC™) scalable hardware coherence
- 32 KB L1i, 32K L1d per core
- 256 KB L2 per core
- 9 MB coherent L3 cache

iMesh Interconnect

- Five independent low-latency mesh networks
- 60 Tbps aggregate bandwidth
- Non-blocking, cuthrough switching with 1 clock cycle per hop

Integrated Memory Controllers

- Two 72-bit DDR3 controllers with ECC support
- 512 GB total memory capacity
- Up to 1,866 MTps speeds
- Advanced request reordering

PCI Express

- Three integrated Gen2 PCIe controllers (5G SerDes)
- Each configurable as root complex or endpoint
- High-performance coherent transaction DMA engine
- Multiple configurable transaction modes for efficient data movement
- SR-IOV support

StreamIO Interfaces

- Three high-performance transaction ports for chip-to-chip or FPGA interconnect
- Multiplexed with PCIe SerDes
- 20 Gbps peak performance per 4-lane port

Networking Interfaces

- Four 10 Gbps XAUI ports, including double-XAUI support
- Up to sixteen 10/100/1000 SGMII ports (multiplexed with XAUI ports)
- Egress QoS queuing and traffic shaping support
- IEEE1588v2 precision timing controller support
- IEEE802.1Qbb priority flow control and datacenter Ethernet (DCE) support

mPIPE™ Wire-speed Packet Engine

- C-programmable classification
- 60 Mpps performance for minimum size packets
- Programmable checksum and CRC offload for packet headers and payload
- Multi-mode load-balancer with direct-to-cache packet delivery
- Flexible buffer manager with 32 configurable memory domains

Crypto and Compression Acceleration

- MiCA™ engines deliver low-latency, high-bandwidth offload
- 40 Gbps encryption throughput
- Support for IPsec, SSL, TLS, MACsec, SRTP, 3GPP
- Public Key accelerator (RSA, DSA, DH, ECC)
- True random number generator
- Deflate compress/decompress with Gzip compatibility

System Integration Features

- Two USB 2.0 interfaces; one host and one host/endpoint
- Four I^2C interfaces
- One SPI (master) interface
- Two high-speed UART interfaces
- 64 GPIO/Interrupt pins
- JTAG port

Package Information

- 37.5 mm x 37.5 mm BGA
- 1 mm ball pitch

Ordering Guide

Device	Part Number	Core Frequency	Memory Speed	# of Tiles	TypicalPower*	Operating Temp	Package
TILE-Gx8036	TLR4-03680CG-10C	1.0 GHz	1,600 MTps	36	22 W	Commercial	1,265 BGA
TILE-Gx8036	TLR4-03680CG-12C	1.2 GHz	1,866 MTps	36	28 W	Commercial	1,265 BGA

*Power may vary based on application and I/O configuration

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