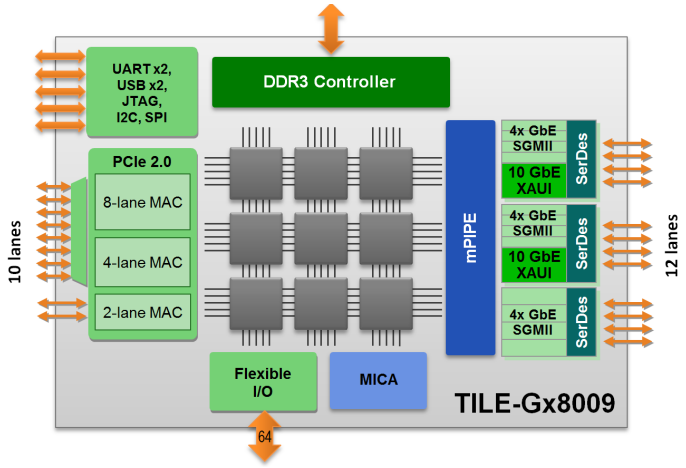
TILE-Gx8009™ Processor

Specification Brief

The TILE-Gx8009™ Processor is optimized for networking and multimedia applications and delivers enormous compute and I/O with complete "System-on-a-Chip" features. The device includes nine identical processor cores (tiles) interconnected with Tilera's iMesh™ on-chip network. Each tile consists of a full-featured processor core as well as L1 and L2 cache and a non-blocking switch that connects the tiles in the mesh. Each tile can independently run a full operating system, or a group of tiles can run a multi-processing OS, like SMP Linux. The TILE-Gx8009 is ideal for sophisticated networking applications requiring 5 to 10 Gbps of performance and it maintains pinout and software compatibility with Tilera's TILE-Gx16™ and TILE-Gx36™ processors.



Powerful Processor Cores

- Nine cores @ 1.0 to 1.2 GHz
- 64-bit architecture (datapath and address)
- Three execution pipelines
- Robust virtual memory system with TLBs and Hardwall™ protection
- ISA extensions for multimedia and SIMD processing

Cache

- 3 Mbytes total on-chip cache
- Dynamic Distributed Cache (DDC™) scalable hardware coherence
- 32KB L1i, 32K L1d per core
- 256KB L2 per core
- 2.3MB coherent L3 cache

iMesh Interconnect

- Five independent low-latency mesh networks
- 10 Tbps aggregate bandwidth
- Non-blocking, cuthrough switching with one clock cycle per hop

Integrated Memory Controllers

- 72-bit DDR3 controller with ECC support
- 64GB total memory capacity
- Up to 1600 MTps speeds
- Advanced request reordering

PCI Express

- Three integrated Gen2 PCIe controllers, 10-lanes
- Each configurable as root complex or endpoint
- High-performance coherent transaction DMA engine
- Multiple configurable transaction modes for efficient data movement
- SR-IOV support

StreamIO Interfaces

- Two high-performance transaction ports for chip-to-chip or FPGA interconnect
- Multiplexed with PCIe SerDes
- 20Gbps peak performance per 4-lane port

Networking Interfaces

- Two 10 Gbps XAUI ports
- Up to twelve 10/100/1000 SGMII ports (eight multiplexed with XAUI ports)
- Egress QoS queuing and traffic shaping support
- IEEE1588v2 precision timing controller support
- IEEE802.1Qbb priority flow control and datacenter Ethernet (DCE) support

mPIPE™ Wire-speed Packet Engine

- C-programmable classification
- 15Mpps performance for minimum size packets
- Programmable checksum and CRC offload for packet headers and payload
- Multi-mode load-balancer with direct-to-cache packet delivery
- Flexible buffer manager with 32 configurable memory domains

Crypto and Compression Acceleration

- Crypto and Compression Acceleration (-E option)
- MiCA™ engines deliver low-latency, high-bandwidth offload
- 10Gbps encryption throughput
- Support for IPsec, SSL, TLS, MACsec, SRTP, 3GPP
- Public Key accelerator (RSA, DSA, DH, ECC)
- True random number generator
- Deflate compress/decompress with Gzip compatibility

System Integration Features

- Two USB 2.0 interfaces; one host and one host/endpoint
- Three I^2C interfaces
- One SPI (master) interface
- Two high-speed UART interfaces
- Sixty-four GPIO/Interrupt pins
- JTAG port

Package Information

- 37.5 mm x 37.5 mm BGA
- 1 mm ball pitch

Ordering Guide

Device	Part Number	Core Frequency	Memory Speed	# Cores	MiCA Accel.	Typical Power*	Operating Temp	Package
TILE-Gx8009	TLR4-00980CG-10C	1.0 GHz	1333 MT/s	9	No	9 W	Commercial	1265-BGA
TILE-Gx8009	TLR4-00980CG-10CE	1.0 GHz	1333 MT/s	9	Yes	10 W	Commercial	1265-BGA
TILE-Gx8009	TLR4-00980CG-12C	1.2 GHz	1600 MT/s	9	No	11 W	Commercial	1265-BGA
TILE-Gx8009	TLR4-00980CG-12CE	1.2 GHz	1600 MT/s	9	Yes	12 W	Commercial	1265-BGA

* Power may vary based on application and I/O configuration.

PB033-03 Oct2012 SG