Velegapudi Ramakrishna Siddhartha Engineering College::Vijayawada
(Autonomous)

VR20

II /IV B Tech Degree Examinations(November 2021)
Third Semester
Department of Information Technology
20IT3304:COMPUTER ORGANIZATION

Time:3Hrs	**MODEL QUESTION PAPER**	Max Marks:70

Part – A is Compulsory
Answer one (01) question from each unit of Part – B
Answers to any single question or its part shall be written at one place only

Cognitive Levels(K): K1-Remember;K2-Understand; K3-Apply; K4-Analyze; K5-Evaluate; K6-Create

Q. No		**Question**	**Marks**	**Course Outcome**	**Cog. Level**
Part - A			**10X1=10M**		
1	a	Define internal hardware organization of a digital computer.	1	CO1	K1
	b	What is the significance of three state buffer gates?	1	CO1	K2
	c	List the phases of an instruction cycle.	1	CO2	K1
	d	Define the terms microoperation, microinstruction and microprogram.	1	CO1	K1
	e	What is the purpose of addressing modes?	1	CO1	K2
	f	Specify the format of microinstruction?	1	CO1	K1
	g	Define hit ratio.	1	CO4	K1
	h	State locality of reference property.	1	CO4	K1
	I	What are the disadvantages of strobe control method?	1	CO4	K2
	j	What is a multiprocessor system?	1	CO1	K1
Part - B			**4X15 =60M**		
		UNIT - I			
2	a	A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. i)How many selection inputs are there in each multiplexer? ii) What sizes of multiplexers are needed? iii) How many multiplexers are there in the bus? Draw a diagram of a bus system for four registers and each register consisting of four bits using multiplexers.	8	CO1	K3
	B	Explain 4-bit arithmetic circuit with neat diagram.	7	CO1	K2
		(OR)			
3	a	Briefly discuss about the control unit of a basic computer with necessary block diagram.	9	CO2	K2
	b	Write the register transfer operations for the given memory reference instructions i) ADD ii) STA iii) BSA iv) ISZ v) BUN vi) LDA	6	CO2	K2
		UNIT - II			
4	a	Describe microprogram sequencer for a control memory with	8	CO2	K2

		neat circuit diagram			
	b	Draw the block diagram of a control memory with necessary hardware for selecting the next microinstruction address**.**	7	CO2	K2
(OR)					
5	a	Write a program to evaluate the arithmetic statement using i) General register computer with three address instruction ii) Accumulator type computer with one address instruction. $x = \frac{A - B + C * (D * E - F)}{G + H * K}$	7	CO1	K5
	b	A two word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction stored at W+1 and is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is i) direct ii) indirect iii) relative iv) indexed	8	CO1	K4
UNIT - III					
6	a	Apply Booths multiplication algorithm to multiply the numbers -14 and +21.	8	CO3	K3
	b	Design hardware used for the addition and subtraction of two decimal numbers in signed-magnitude representation and draw the flowchart.	7	CO3	K2
(OR)					
7	a	Summarize the mapping procedures for the organization of cache memory.	8	CO4	K2
	b	Explain Associative memory with neat block diagram.	7	CO4	K2
UNIT - IV					
8	a	Explain DMA data transfer with neat block diagram	8	CO4	K2
	b	Discuss in brief asynchronous data transfer.	7	CO4	K2
(OR)					
9	a	List and explain any three schemas for establishing an interconnection network.	9	CO1	K2
	b	Compare and contrast Memory-Mapped I/O with Isolated I/O	6	CO4	K4

Designation	**Name in Capitals**	**Signature with Date**
Course Coordinators	Dr.K.SITA KUMARI JANGAM EBENEZER	
Program Coordinator	Dr.G.KALYANI	
Head of the Department	Dr. M.SUNEETHA	

ELAGAPUDI RAMAKRISHNA

SIDDHARTHA ENGINEERING COLLEGE::VIJAYAWADA

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Dt.12-06-2019

GUIDELINES FOR FRAMING MODEL QUESTION PAPER

The model papers for all subjects in a semester are gathered from the departments whenever a course is offered for the first time adopting new regulation. All the Heads of the Departments are requested to direct their faculty to strictly adhere to the following guidelines while framing the model question papers for the subjects of UG and PG courses in the new curriculum.

1. Questions must be covered unit-wise uniformly as per the syllabus without missing the competency.

2. The question paper shall reflect the ***Bloom's Cognitive Levels of Learning***.

   Cognitive Levels (K): K1-Remember; K2-Understand; K3-Apply; K4-Analyze; K5-Evaluate; K6-Create

   - The composition of question paper shall have questions at different complexity levels as listed below:
     - Questions that can be attempted by an average student (K1 & K2) 40%
     - Questions of intermediate complexity (K3 & K4) 40-50%
     - Questions of design and application oriented nature (K5 & K6) 10-20%

3. Question paper is to be set conforming to the OBE pattern clearly mentioning the Course Outcomes and Bloom's Cognitive Levels against each question.

4. The questions are to be set with minimum 2 sub-questions (a) & (b) for each main question to the extent possible covering entire syllabus in the unit.

5. Specify the marks against each question / part of a question in Part B.

6. The figures, if any, may be computer aided or neatly drawn with black pen indicating clearly the values/dimensions.

7. Prepare the one mark questions in only sentence form. Answers to these questions must be unique and having short answers limited to three/four lines.

PRINCIPAL