

**DEPARTMENT OF INFORMATION TECHNOLOGY : : VRSEC**  
**20IT3304 COMPUTER ORGANIZATION**  
**ASSIGNMENT I QUESTION BANK**  
**A.Y 2021-2022**

Question No.		Question	Course Outcome	BTL
1.	a	Design a combinational circuit that performs the addition and subtraction micro operation of two 4 bit binary numbers	CO1	Understand
	b	<p>A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.</p> <p>i) How many selection inputs are there in each multiplexer?</p> <p>ii) What sizes of multiplexers are needed?</p> <p>iii) How many multiplexers are there in the bus?</p> <p>Draw a diagram of a bus system for four registers and each register consisting of four bits using multiplexers.</p>	CO1	Analyze
2	a	Design a circuit diagram for performing the addition of two 4 bit binary numbers	CO1	Understand
	b	<p>Draw the block diagram for the hardware that implements the following statements:</p> $x + yz: AR \leftarrow AR + BR$ <p>Where AR and BR are two n bit registers and x, y and z are control variables. Include the logic gates for the control function (symbol + designates an OR operation in a control or a Boolean function but that it represents an arithmetic plus in a microoperation).</p>	CO1	Apply
3	a	Design a circuit diagram for 4 bit arithmetic circuit.	CO1	Understand
	b	Design an arithmetic circuit with one selection variable S and two n bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry $C_{in}$ . Draw the logic diagram for the first two stages.	CO1	Analyze

		<table><tr><td>S</td><td>C<sub>in</sub> = 0</td><td>C<sub>in</sub> = 1</td></tr><tr><td>0</td><td>D= A + B(add)</td><td>D = A + 1(increment)</td></tr><tr><td>1</td><td>D=A-1 (decrement)</td><td>D = A +B'+1(subtract)</td></tr></table>	S	C <sub>in</sub> = 0	C <sub>in</sub> = 1	0	D= A + B(add)	D = A + 1(increment)	1	D=A-1 (decrement)	D = A +B'+1(subtract)																												
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4	a	Briefly discuss about the control unit of a basic computer with necessary block diagram	CO2	Understand																																			
	b	<p>The following control inputs are active in the bus system (ref fig 6.4). For each case specify the register transfer that will be executed during the next clock transition.</p> <table><tr><td>S.No</td><td>S<sub>2</sub></td><td>S<sub>1</sub></td><td>S<sub>0</sub></td><td>LD of Register</td><td>Memory</td><td>Adder</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>IR</td><td>Read</td><td>-</td></tr><tr><td>2</td><td>1</td><td>1</td><td>0</td><td>PC</td><td>-</td><td>-</td></tr><tr><td>3</td><td>1</td><td>0</td><td>0</td><td>DR</td><td>Write</td><td>-</td></tr><tr><td>4</td><td>0</td><td>0</td><td>0</td><td>AC</td><td>-</td><td>Add</td></tr></table>	S.No	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	LD of Register	Memory	Adder	1	1	1	1	IR	Read	-	2	1	1	0	PC	-	-	3	1	0	0	DR	Write	-	4	0	0	0	AC	-	Add	CO2	Analyze
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3	1	0	0	DR	Write	-																																	
4	0	0	0	AC	-	Add																																	
5	a	Explain Memory reference instructions with Register transfer statements	CO2	Understand																																			
	b	<p>Assume that the first six memory reference instructions in the basic computer are specified in the following table. EA is the effective address that resides in AR during time T<sub>4</sub>. Assume that the adder and logic circuit in the bus system can perform XOR operation. AC ←AC ⊕ DR. Assume further that the adder and logic circuit cannot perform subtraction directly. The subtraction must be done using the 2's complement of subtrahend by complementing and incrementing AC. Give the sequence of register transfer statements needed to execute each of the listed instructions starting from timing T<sub>4</sub>. Note that the value in AC should not change unless the instruction specifies a change in its content. You can use TR to store the content of AC temporary or you can exchange DR and AC</p> <table><tr><td>Symb ol</td><td>Opcod e</td><td>Symbolic Designation</td><td>Description in words</td></tr><tr><td>XOR</td><td>000</td><td>AC←AC ⊕</td><td>Exclusive OR to AC</td></tr></table>	Symb ol	Opcod e	Symbolic Designation	Description in words	XOR	000	AC←AC ⊕	Exclusive OR to AC	CO2	Apply																											
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				M[EA]																																																						
		ADM	001	M[EA] ← M[EA] + AC	Add AC to Memory																																																					
		SUB	010	AC ← AC – M[EA]	Subtract Memory from AC																																																					
		XCH	011	AC ←M[EA], M[EA] ←AC	Exchange AC and Memory																																																					
		SEQ	100	If (M[EA] ==AC) then PC ←PC + 1	Skip on equal																																																					
		BPA	101	If (AC > 0) then (PC←EA)	Branch if AC is positive and non zero																																																					
6.	a	Illustrate the applications of logic microoperations with suitable examples				CO1	Understand																																																			
	b	Derive a combinational circuit that selects and generates any one of the 16 logic functions listed in the table below				CO1	Analyze																																																			
		<table><tr><th>Boolean function</th><th>Microoperation</th><th>Name</th></tr><tr><td><math>F_0 = 0</math></td><td><math>F \leftarrow 0</math></td><td>Clear</td></tr><tr><td><math>F_1 = xy</math></td><td><math>F \leftarrow A \wedge B</math></td><td>AND</td></tr><tr><td><math>F_2 = xy'</math></td><td><math>F \leftarrow A \wedge \overline{B}</math></td><td></td></tr><tr><td><math>F_3 = x</math></td><td><math>F \leftarrow A</math></td><td>Transfer A</td></tr><tr><td><math>F_4 = x'y</math></td><td><math>F \leftarrow \overline{A} \wedge B</math></td><td></td></tr><tr><td><math>F_5 = y</math></td><td><math>F \leftarrow B</math></td><td>Transfer B</td></tr><tr><td><math>F_6 = x \oplus y</math></td><td><math>F \leftarrow A \oplus B</math></td><td>Exclusive-OR</td></tr><tr><td><math>F_7 = x + y</math></td><td><math>F \leftarrow A \vee B</math></td><td>OR</td></tr><tr><td><math>F_8 = (x + y)'</math></td><td><math>F \leftarrow \overline{A \vee B}</math></td><td>NOR</td></tr><tr><td><math>F_9 = (x \oplus y)'</math></td><td><math>F \leftarrow \overline{A \oplus B}</math></td><td>Exclusive-NOR</td></tr><tr><td><math>F_{10} = y'</math></td><td><math>F \leftarrow \overline{B}</math></td><td>Complement B</td></tr><tr><td><math>F_{11} = x + y'</math></td><td><math>F \leftarrow A \vee \overline{B}</math></td><td></td></tr><tr><td><math>F_{12} = x'</math></td><td><math>F \leftarrow \overline{A}</math></td><td>Complement A</td></tr><tr><td><math>F_{13} = x' + y</math></td><td><math>F \leftarrow \overline{A} \vee B</math></td><td></td></tr><tr><td><math>F_{14} = (xy)'</math></td><td><math>F \leftarrow \overline{A \wedge B}</math></td><td>NAND</td></tr><tr><td><math>F_{15} = 1</math></td><td><math>F \leftarrow \text{all 1's}</math></td><td>Set to all 1's</td></tr></table>						Boolean function	Microoperation	Name	$F_0 = 0$	$F \leftarrow 0$	Clear	$F_1 = xy$	$F \leftarrow A \wedge B$	AND	$F_2 = xy'$	$F \leftarrow A \wedge \overline{B}$		$F_3 = x$	$F \leftarrow A$	Transfer A	$F_4 = x'y$	$F \leftarrow \overline{A} \wedge B$		$F_5 = y$	$F \leftarrow B$	Transfer B	$F_6 = x \oplus y$	$F \leftarrow A \oplus B$	Exclusive-OR	$F_7 = x + y$	$F \leftarrow A \vee B$	OR	$F_8 = (x + y)'$	$F \leftarrow \overline{A \vee B}$	NOR	$F_9 = (x \oplus y)'$	$F \leftarrow \overline{A \oplus B}$	Exclusive-NOR	$F_{10} = y'$	$F \leftarrow \overline{B}$	Complement B	$F_{11} = x + y'$	$F \leftarrow A \vee \overline{B}$		$F_{12} = x'$	$F \leftarrow \overline{A}$	Complement A	$F_{13} = x' + y$	$F \leftarrow \overline{A} \vee B$		$F_{14} = (xy)'$	$F \leftarrow \overline{A \wedge B}$	NAND	$F_{15} = 1$	$F \leftarrow \text{all 1's}$	Set to all 1's
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Designation	Name in Capitals	Signature with Date
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