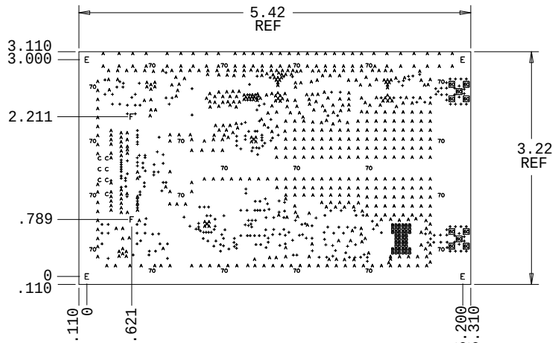
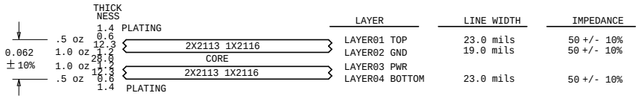
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



HOLE CHART				
ALL UNITS ARE IN INCHES				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	0.010	+.003/-.010	PLATED	330
A	0.012	+.003/-.012	PLATED	633
B	0.018	+/-.002	PLATED	46
C	0.040	+/-.003	PLATED	7
D	0.060	+/-.003	PLATED	10
70	0.070	+/-.003	PLATED	21
E	0.125	+/-.003	PLATED	4
F	0.040	+/-.003	NON-PLATED	2



1. Specifications (unless otherwise specified):
   - 1.0 Unless otherwise defined on this drawing, fabricate board per Current Revision of IPC-6012, Class 2 requirements.
   - 1.1 Producibility study - it is the responsibility of the supplier to conduct a thorough review of the artwork and media for Range Networks anufacturability in the supplier's process compliant to all applicable specifications. Range Networks must be advised in writing (in advance of manufacturing) of any changes, revisions, or corrections made or recomendations to ensure conformance to standards, and of any specifications that cannot be met.
   - 1.2 Use Range Networks PCB artwork RNRAD1-RF-COMBO-R5
   - 1.3 Board must be compliant with UL 94V-0 .
2. Material
   - 2.0 Natural Epoxy/Glass Laminate FR-4. w/Tg min of 170 degrees Celsius, .062thick +/-10 % measured over area free of soldermask.
   - 2.1 See stack up for copper weights
   - 2.2 Color to be opaque.
   - 2.3 Number of Layers: 4
3. Soldermask
   - 3.0 Soldermask both sides with (green color) liquid photo-imageable soldermask, .003 max. thickness.
   - 3.1 Soldermask over - bare copper.
   - 3.2 Via pads are encroached. Bottom side test pad vias are exposed.
4. Drilling
   - 4.0 All hole diameters are finished sizes.
   - 4.1 All holes to be +/-.003 from true position unless otherwise specified.
   - 4.2 All hole diameters to be +/-.003 unless otherwise specified.
   - 4.3 An N.C Drill file has been supplied-see drill table.
   - 4.4 Minimum annular ring is 0.001". No breakout is permitted.
5. Remove all unused inner layers pads.
6. Finish
   - 6.0 Surface finish: Immersion gold, 2-5 micro-inches over 100 micro-inches minimum of electroless nickel
   - 6.1 Plate holes thru with copper .0010 min to .002 max. thickness. Finished hole size dimensions apply after plating.
   - 6.2 Finished boards shall not have nicks, scratches, voids, exposed copper, poor plating or mis-drilled holes.
7. Silkscreen
   - 7.0 Silkscreen using white non-conductive epoxy or equivalent (both sides).
   - 7.1 No silkscreen allowed on exposed lands or in holes.
   - 7.2 Burn out silkscreen with soldermask.
   - 7.3 Minimum clearance between silkscreen legend and vias, pads or holes, to be .005
   - 7.4 Registration to be +/-.005 and must pass peel test.
8. Electrical test
   - 8.0 All boards must be 100% electrically tested for open and shorts at10 Volts.
   - 8.1 Apply test stamp in an area clear of silk and parts on solder side of PCB.
   - 8.2 Continuity: Test threshold not to exceed 10 Ohms, using a test current of 10 milliAmperes or less. Maximum open circuit voltage during continuity test not to exceed 10 Volts. Isolation Resistance: 10M Ohms, measured with a voltage of 200 Volts. The test system shall provide a means of limiting the energy delivery to
9. Cleanliness
   - 9.0 Boards shall be free of fiber glass dust or any other foreign material.
   - 9.1 Finished boards must conform to no more than 10 uG/in(squared) ionic contamination.
10. Packaging
    - 10.0 There shall be a max of 25 units per package, individually wrapped and packaged so as to prevent damage during handling,shipping and storage.
11. Bow and twist
    - 11.0 Maximum board warpage in any direction shall not exceed 0.7% (.007" per linear inch).
12. Impedance controlled construction and certification is required.
13. Inspection
    - 13.0 Automatic optical inspection of all layers required.
14. Markings
    - 14.0 Fab will be permanently marked or etched with Manufacturer's logo, date of Fab manufacture and UL 94V-0 rating.
15. Data Verification
    - 15.0 Vendor will do a netlist to Gerber compare with the supplied IPC-356D file prior to releasing to manufacturing. If discrepancies are found written permission must be obtained prior to proceeding. An e-mail confirmation is required and should be sent to the designer their e-mail address is located in the readme.txt.
16. Add thieving to balance the copper distribution. The thieving consists of 50 mil round pads on 100 mil centers. A 100 mil keepout of all etched features will be maintained.

DWG NO. RNRAD1-RF-COMBO-R5 | SH 1 | REV 5

DO NOT SCALE DRAWING

MATERIAL: SEE NOTES

REMOVE ALL BURRS AND SHARP EDGES

NEXT ASSY P/N | MODEL

DRAWN	Rocket EMS	DATE 03/22/12
CHECKED		
MECH ENG		
PROJ ENG		
MFG ENG		
		DRAWING REV 07

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND INCLUDE PLATING AND OR PAINT.
DECIMAL .XXX ± .005 .XX ± .01 | FRACTION ± | ANGLE ±1°

RANGE NETWORKS

DESCRIPTION: FAB DRAWING RF-COMBO BOARD

CODE IDENT	SIZE	DRAWING NO.	REV
	D	RNRAD1-RF-COMBO-R5	5

SCALE: NONE | SHEET 1OF1