**JRP Quantum Power**

**Quantum traceability for AC power standards**

**D1 Report**

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# Version control

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| **Version** | **Date** | **Comment** |
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# Introduction

This documents explain the design and implementation of a multiplexer to be used on a power measurements system based on the Programable Josephson Voltage Standard. The following figures shows an example, the digitizer measures one signal at the time, the current, the voltage and the Josephson Voltage, this last one can be adjusted to calibrate the digitizer at the same level than the signal to be measured.

The digitizer takes a fixed number of periods of each channel, so a switching time in the order of ms will be required. In addition, the switching must be synchronized with the signals so the multiplexer must include and external trigger.

In the power measurements system, the digitizer can be a Keysight 3458 multimeter or a NI-5922 oscilloscope.

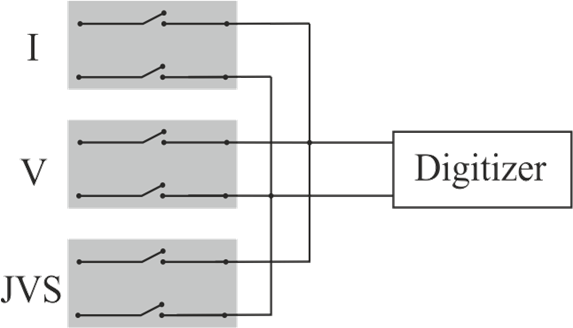
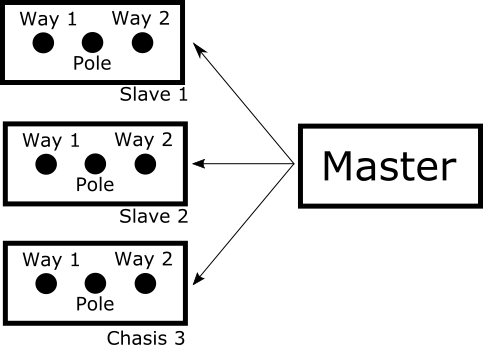


Figure 1: power measurement system. A digitizer measures the current, the voltage and the Josephson voltage in an alternating mode. Some periods of each signal are measured periodically and the JVS standard can be adjusted to calibrate the corresponding range of the multimeter.

This multiplexer is designed to be flexible, the switching sequence and the trigger can be configured by an PC. In addition, it is built in a modular form, with a master board that controls slave boards and includes timing functionalities. The slave boards have a single pole and double throw (SPDT or 2-to-1), or a single pole and four throw (SPFT or 4-to-1). The user can use many of them controlled by the master, as the next figure shows.

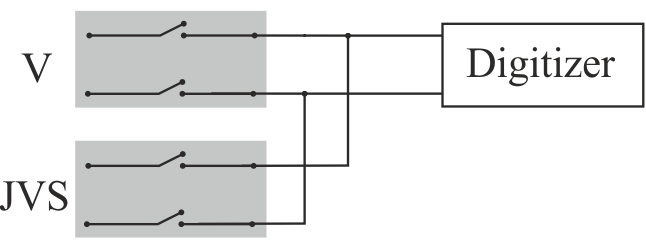


**Figure 1:** three slave boards SPDT controlled by a single master board.

## Specification

The modular design of the multiplexer allows multiple configurations that can be selected by the user connecting the boards between them. The multiplexer uses the strategies break-before-make in order to avoid short circuits between sources and it switches synchronized with an external signal.

The signals are considered differential, so the switch commutes positive and negative terminals of the voltage source. Two slave boards have been designed, one has two throws and one pole, as the next figure shows, and the other has four throws and one pole. The slave board is reversible; the SPDT board can be considered as 2 inputs - 1 output (2-to-1) or 1 input - 2 output (1-to-2).



**Figure 2**: one slave board SPDT ready to measure a voltage source and the JVS.

Channel specification

* Maximum input voltage 60 V peak
* Turn on/off time: <3 ms
* Differential signal
* Coaxial connector for input and output signals
* Bounce-free operation
* Individual Guard connection for each signals (binding post)
* Ground connection for the multiplexer
* Reversible operation

General specification

* Trigger input (BNC connector, opto-isolated)
* USB connection to PC for configuration and control
* 9 V DC External supply

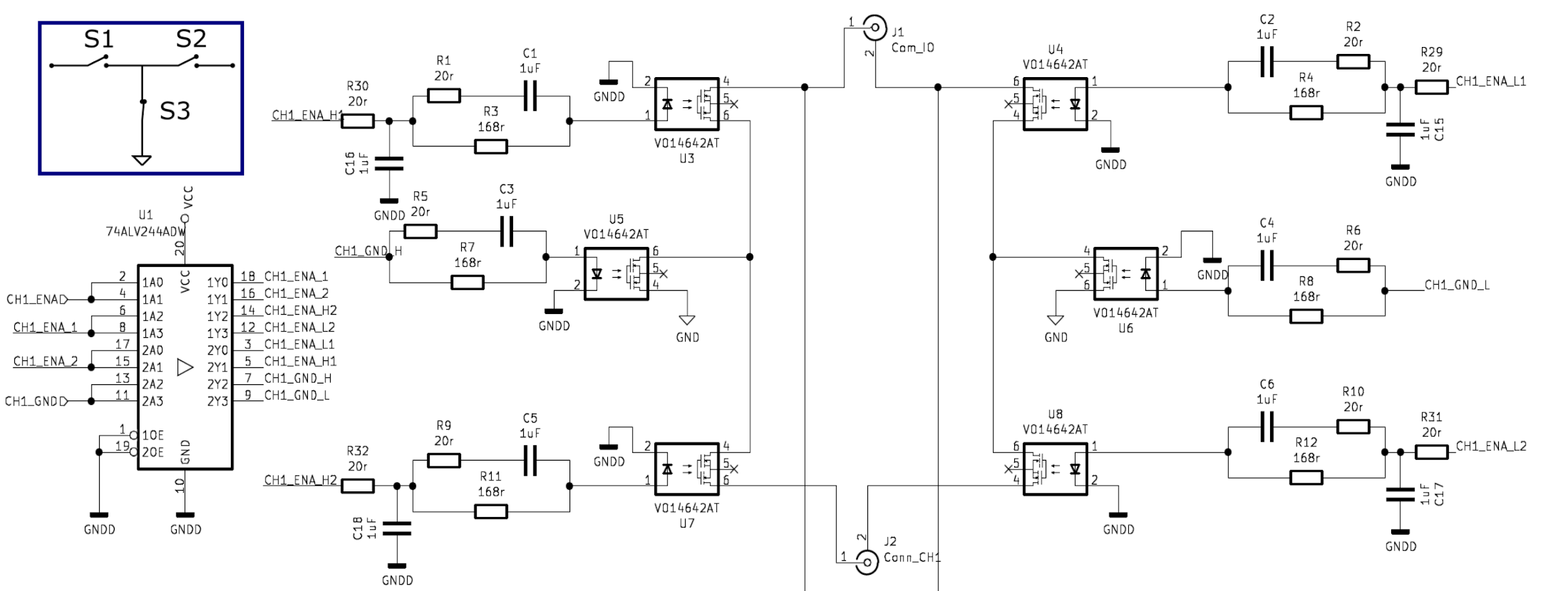
Uncertainty contribution

* 0.5 ohm On-resistance
* Off-isolation at 1 MHz < -90 dB
* Crosstalk at 1 MHz < 100 dB
* Uncertainty contribution < 0.2 ppm at power line frequency
* Maximum uncertainty due to multiplexer: 1 ppm at 1 kHz.

# Theory of operation

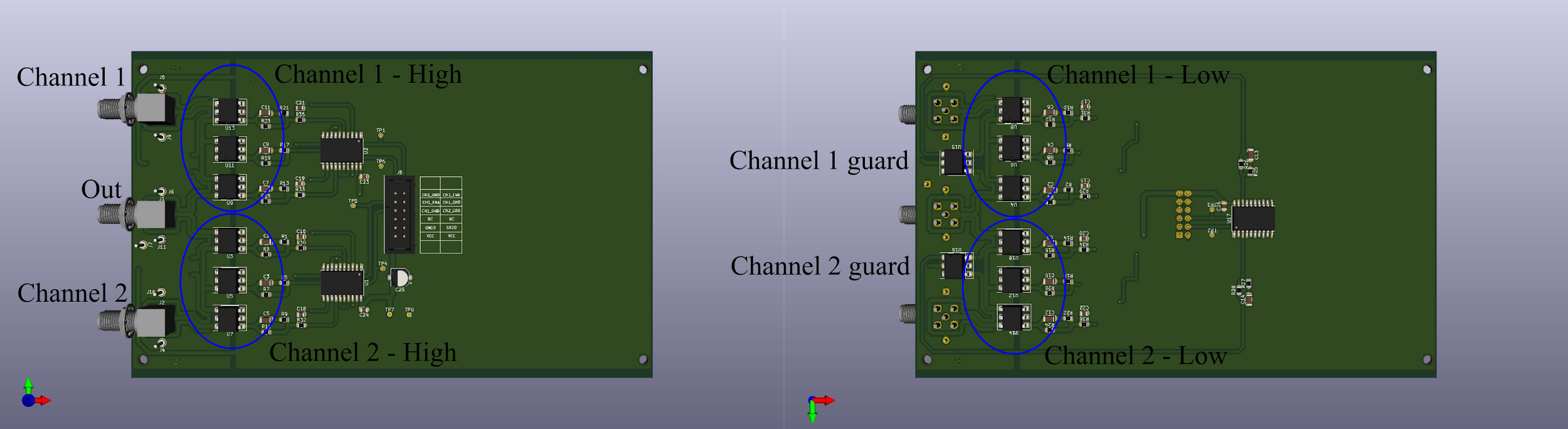
## Slave board

Each switch is built in T-configuration using three solid-state relays to improve the overall off-isolation. The next figure shows a simple scheme in the blue box, S1 is connected to the voltage source and its output is connected with two relays. S3 connects the signal path to ground and S2 connects the signal path to the output. The figure shows the circuit schematic, the relays U3 - U7 are the signal relay for the high terminal and the U4 - U8 for the low terminal. The relays U5 and U6 are used to tie to ground the middle point, the ground is floating and can be connected to the source ground. The capacitances and resistor networks are used to improve transition time and reduced charge injection.



**Figure 3:** Circuit schematics for one differential channel, the switches are connected for each polarity in T configuration as the blue box shows.

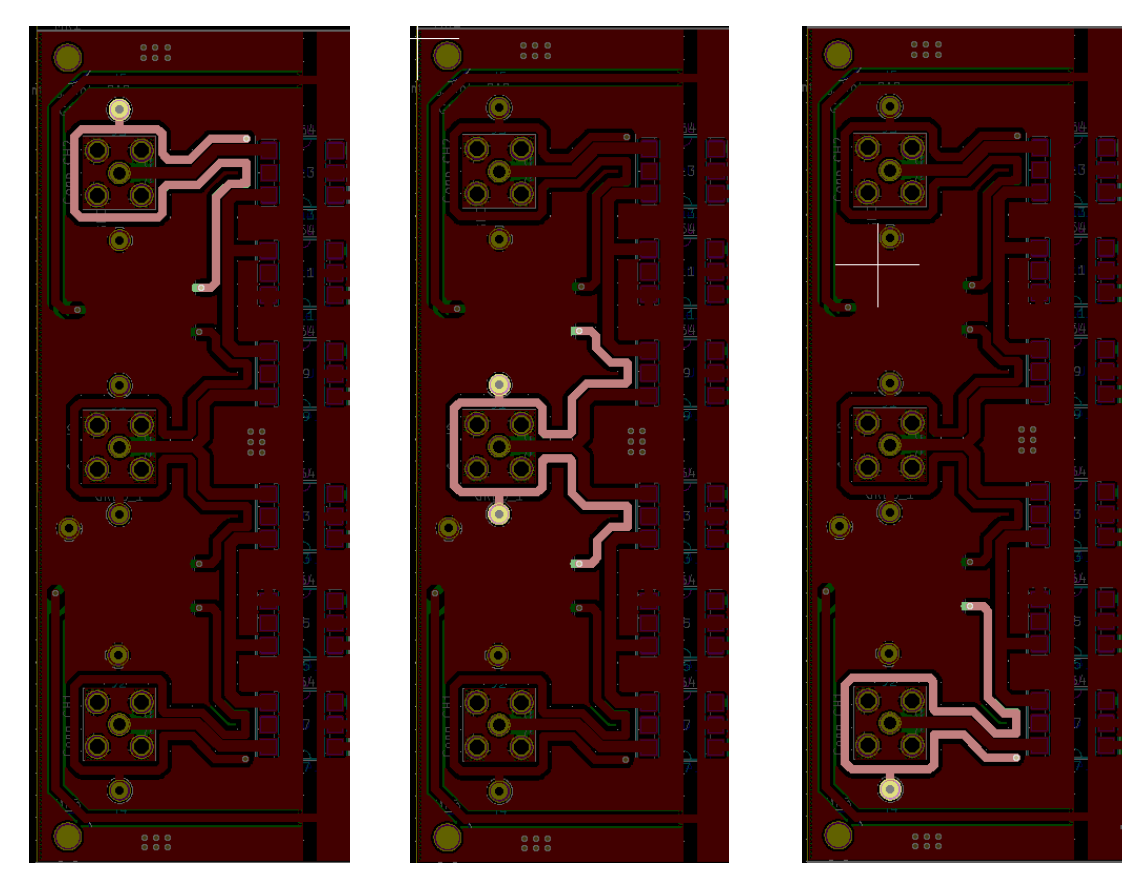
The circuit board has a coaxial design, minimizing inductance path and stray capacitance. The figure 4 shows the top and bottom side of the slave-board, on one side are the high terminal relays and the other side has the low terminal relays. Both sides are organized equally to minimize the area enclosed by the current path. Three guarding rings are used to reduce the stray capacitance between channels and output, they can be connected to the instrument's guards. Several test points were included to measure the digital signal, they are indicated in the top side.



**Figure 4:** (left) top and (right) bottom of the slave 2-to1 board.

During the open or close process, the activation of each relay must be done preventing a short circuit. A break-before-make strategy is implemented: first all switches are opened and then the correct configuration is set. A secure time is included to prevent a short circuit and will be set considering the relay specifications.

**Guard connection:** The slave board has switches to connect the guard of each throw with the guard of the pole, and the connectors are surrounded by a ring at guard potential. The figure 5 shows the example to the slave board SPDT.

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**Figure 5:** (left) schematic circuit of the guard relays of the salve board SPDT. (right) guard rings on each connector.

**PhotoMos relay:** the following table shows the characteristic of the relay used on the first prototype. It was selected comparing by simulations elements from different manufacturer, and we found that this element has a balanced specification and it is available to buy.

**Table 3:** PhotoMos relay VO14642AABTR specification.

|  |  |
| --- | --- |
|  | **VO14642AABTR** |
| **ON-Resistance** | 0.18 Ω (AC) |
| **Max. voltage** | 60 V |
| **On-time** | 370 μs / 800 μs |
| **Off-time** | 50 μs / 800 μs |
| **Stray capacitance** | 200 pF |
| **Control current** | 0.5 mA to 20 mA |
| **Family** | Vishay |

In the case that the application requires another specification on the relay, the market offers a large number of compatible devices with different capabilities. The following table shows some equivalents elements with its mains characteristic obtained from specifications:

|  |  |
| --- | --- |
| **Relay** | **Main characteristics** |
| **PVT2125SPbf** | 150 V input voltage |
| **ASSR-1511-301E** | Low stray capacitance |
| **PVN012APbF** | Low on-resistance |

## Firmware and Flow chart

**Switching sequence matrix**

The switching sequence is transferred to the multiplexer by USB port and internally stored for further uses. The switching sequence can be considered as a matrix where each row represents the state of all the slave boards. The transition between each row will be controlled by a switching event. The user can configure the row value and in practice no more than 32 rows will be necessary. For example, if 3 slave boards are connected in a 4 step process, the matrix is:

**Table 6:** binary switching sequence matrix for SPDT slave boards.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Step | Slave 1  Ch1 | Slave 1 Ch2 | Slave 2  Ch1 | Slave 2 Ch2 | Slave 3  Ch1 | Slave 3 Ch2 | Delay time (number of external trigger) |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 10 |
| 2 | 0 | 1 | 0 | 1 | 0 | 1 | 15 |
| 3 | 0 | 1 | 0 | 1 | 0 | 1 | 15 |
| 4 | 1 | 0 | 1 | 0 | 1 | 0 | 10 |

In the binary matrix one bit indicates the state of one channel, 0 indicates open and 1 indicates close. The matrix can be built with two bytes for channel states, so a total of 16 switches can be controlled, plus an extra byte to the numbers of clocks.

Byte 1:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| S4-CH2 | S4-CH1 | S3-CH2 | S3-CH1 | S2-CH2 | S2-CH1 | S1-CH2 | S1-CH1 |

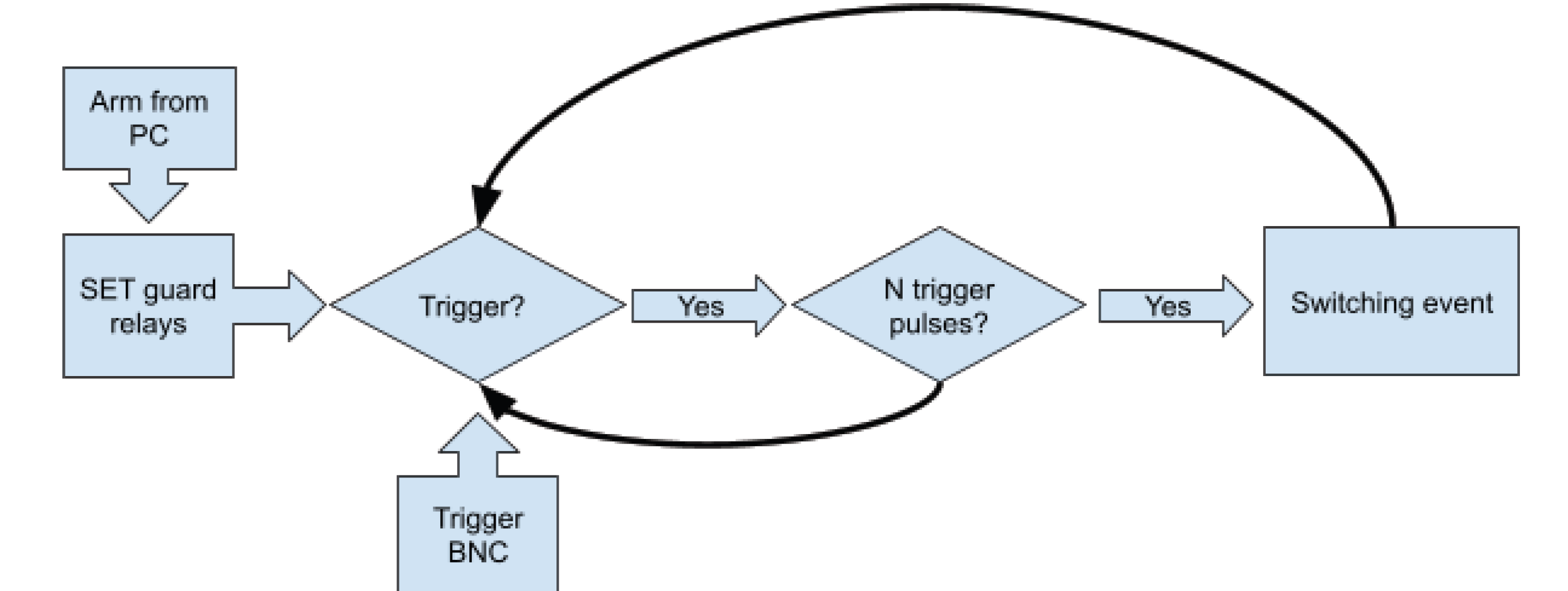
Byte 2:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  | S6-CH2 | S6-CH1 | S5-CH2 | S5-CH1 |

Byte 3: numbers of external trigger from 0 to 255

**Remote operation**

A trigger tree is considered to control the switching sequence, first the master board is armed and then, the state of the multiplexer channels change synchronized with the switching event. The arm and disarm message is provided by the PC. The switching event is defined as a trigger signal at trigger BNC plus a delay time based on integer numbers of trigger pulses. The following figure presents the trigger tree.



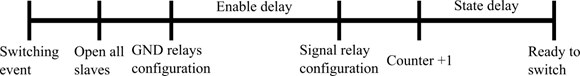
**Figure 8:** trigger tree, the Arm message is provided by PC and “N” is the number of

external trigger pulses configured for each row in the matrix sequence.

**Switching pseudocode**

The following sequence gives information about the switching procedure, for more information goes to Annex 4.

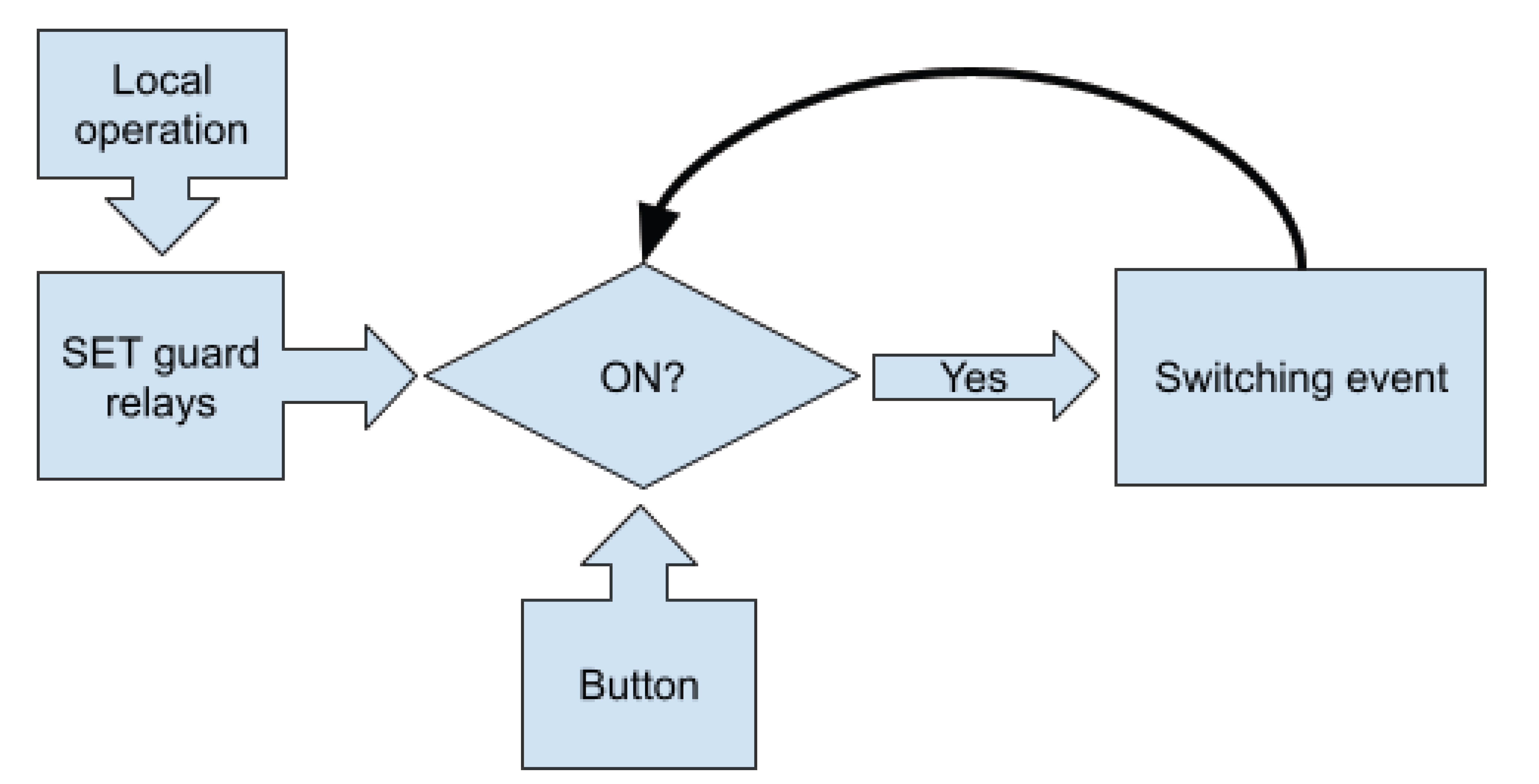
1. The PC configures the multiplexer and loads the switching matrix.
2. The PC arm the multiplexer.
3. The switches that connect the source guard are activated and they are not modified during the sequence.
4. The controller detects a trigger signal, the user can select positive or negative slopes.
5. The controller counts the numbers of pulses. When the configured value is reached the switching event is produced.
6. The controller writes FALSE on the “Ready for Trigger” bit.
7. Switching event (see figure 9):
   1. All the chanells are opened. (Signal relays are opened, GND relay are closed).
   2. b. The GND switches of the ON channels are turned off.
   3. An enable delay time is implemented to prevent a short circuit. The secure time is 2 times the turn-off time of the relay.
   4. The corresponding signal relays are configured based on the corresponding row of the sequence matrix.
   5. The switch remains in the actual state during the delay configured.
   6. A counter to indicate the following matrix row is incremented.
8. The controller returns to point 4 and writes TRUE on the “Ready for Trigger” bit.
9. If a disarm command is received the controller returns to configuration state.



**Figure 9:** time diagram of the operations after switching event, items 7a to 7f. The Enable delay must be larger than the maximum turn-off time of the relay.

**Local operation**

The multiplexer can be configured on local operation. The button “ENA CH” runs the sequence step by step, each time that the user pushes the button the multiplexer changes the state following the sequence matrix, which must be previously loaded or the default sequence will be used.

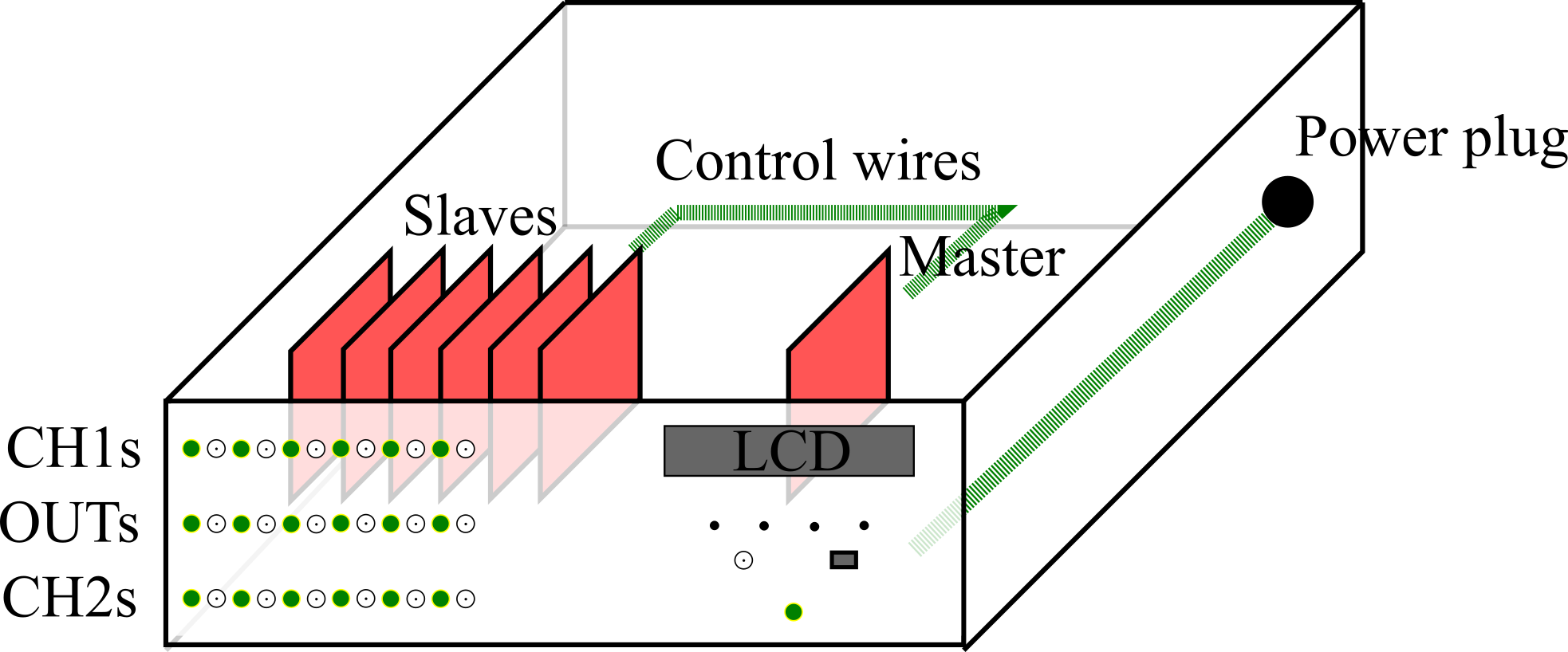


**Figure 10:** in local operation, the multiplexer changes between

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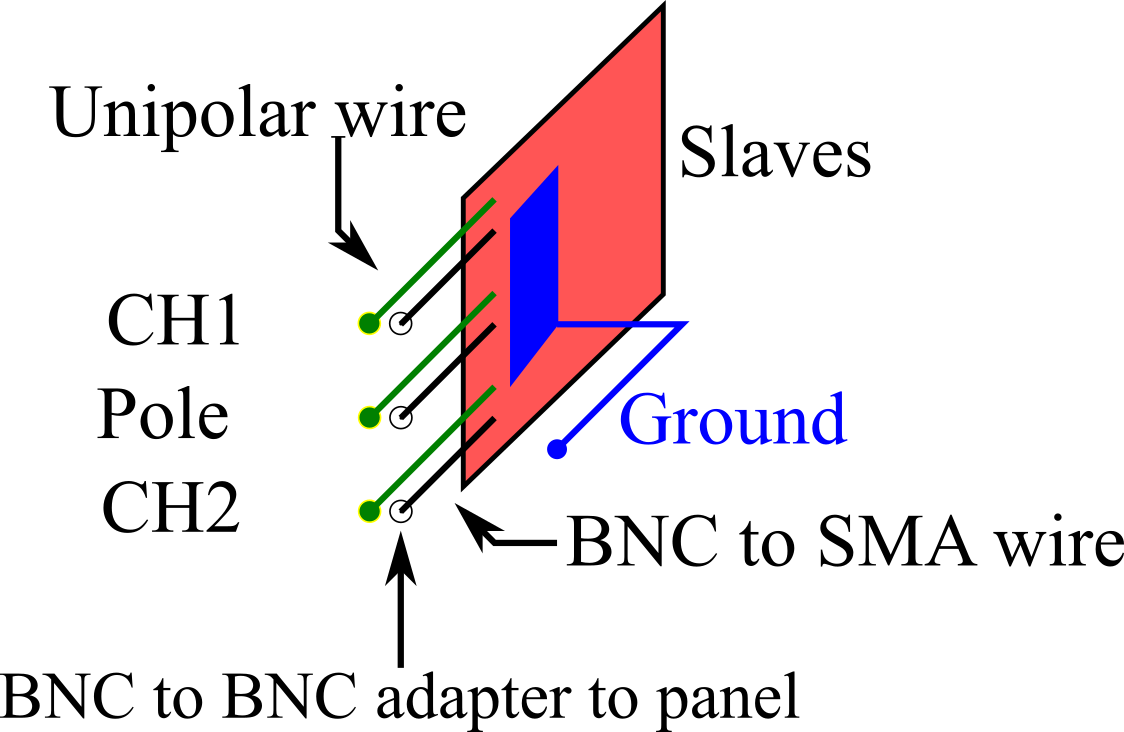
# Installation and connections

All the boards are designed to be fixed in a standard 19” case with a height of 3U (127 mm). The following figure shows one possible configuration with three SPDT slaves boards.



**Figure 11:** recommended configuration of the case for SPDT slave boards.

Each slave can be connected to the front panel by means of coaxial wire for signals and unipolar wire for guard and ground. The guard voltage provides a shield ring around the inputs and the outputs, they help to reduce the stray capacitance between signals. The ground voltage is connected to the middle point of the T-configuration during turn-off state. In order to obtain high off-isolation, the ground terminal must be the source GND and it must be connected by means of a low impedance wire.

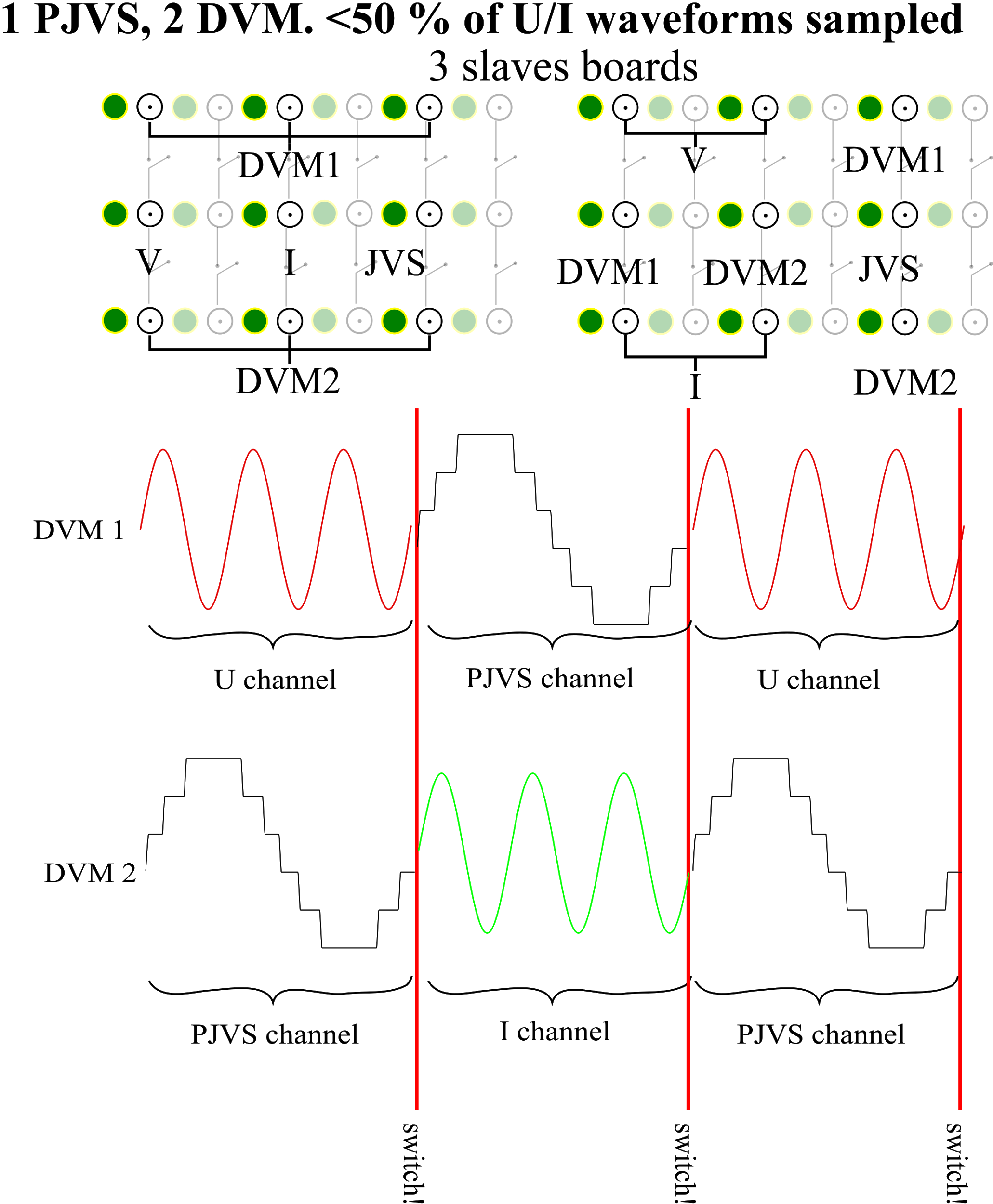
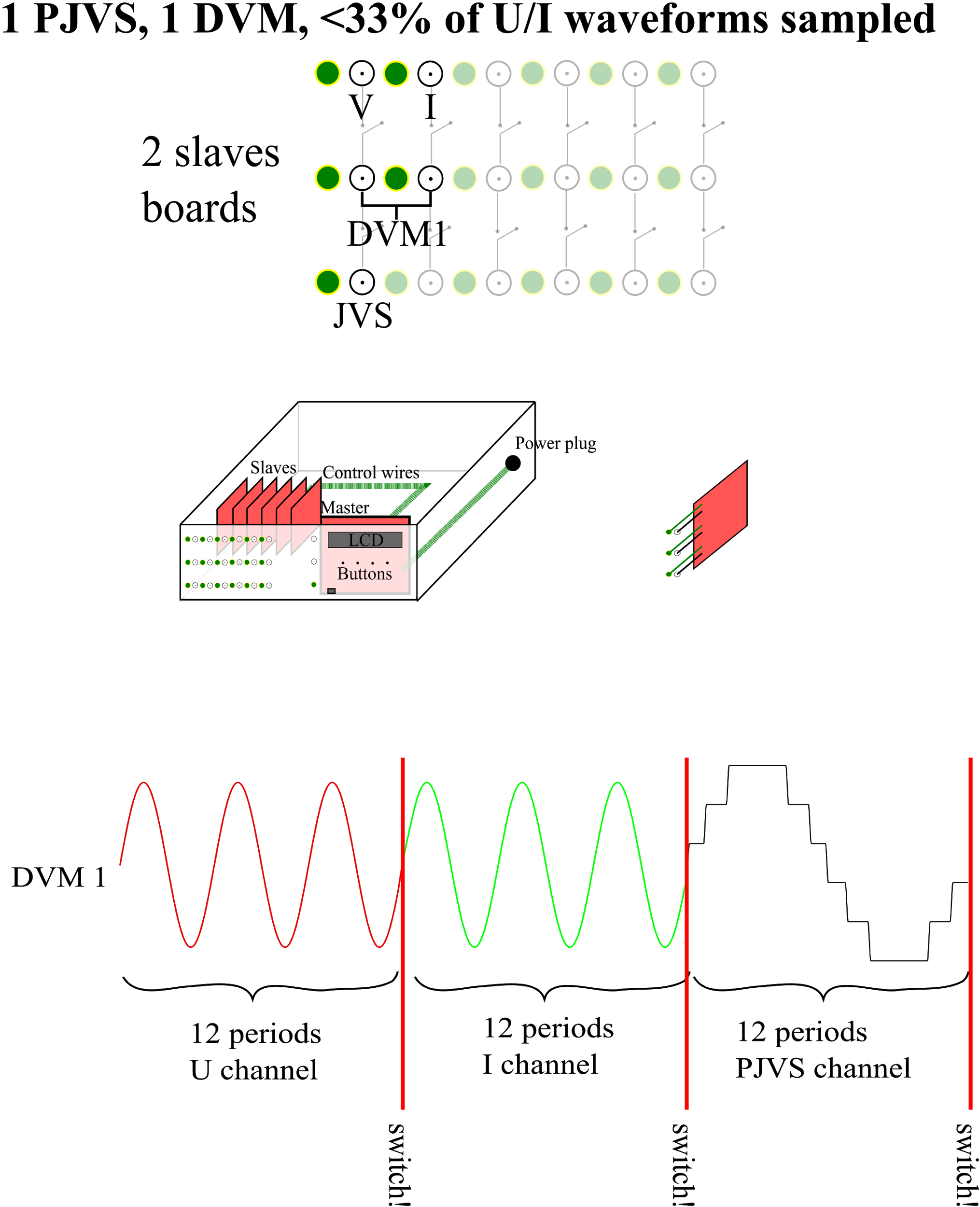


**Figure 12:** connection diagram of the SPDT slave board.

The following figures show possible connections for the 2-to-1 board and the 4-to-1 board, and for different cases: 1, 2 and 3 multimeters.

We also include the connection for the DC voltage measurement by differential method with the JVS.

In all the cases, the diagram shows all the allowed slaves boards and the shadow BNCs are not used in that connection.



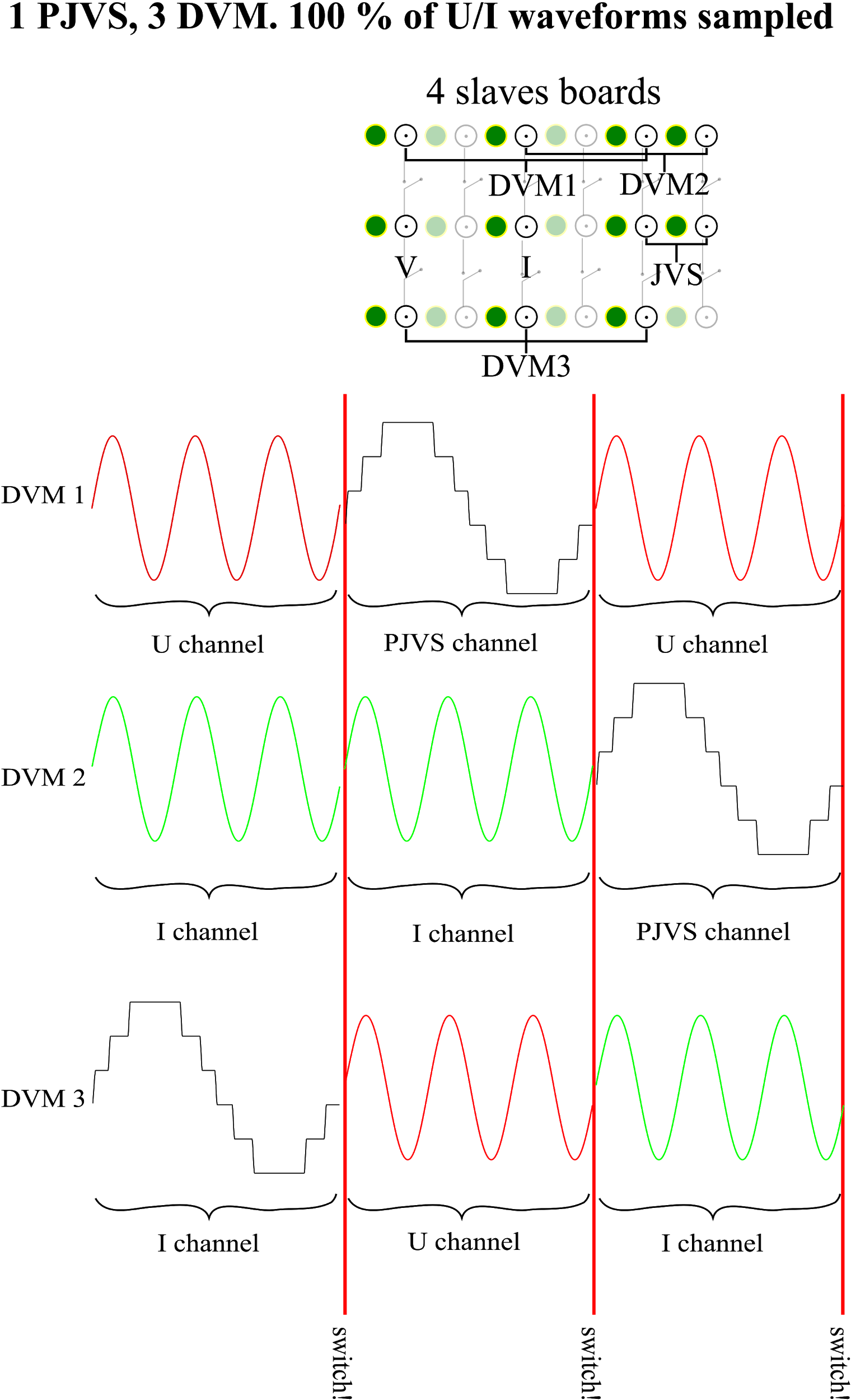
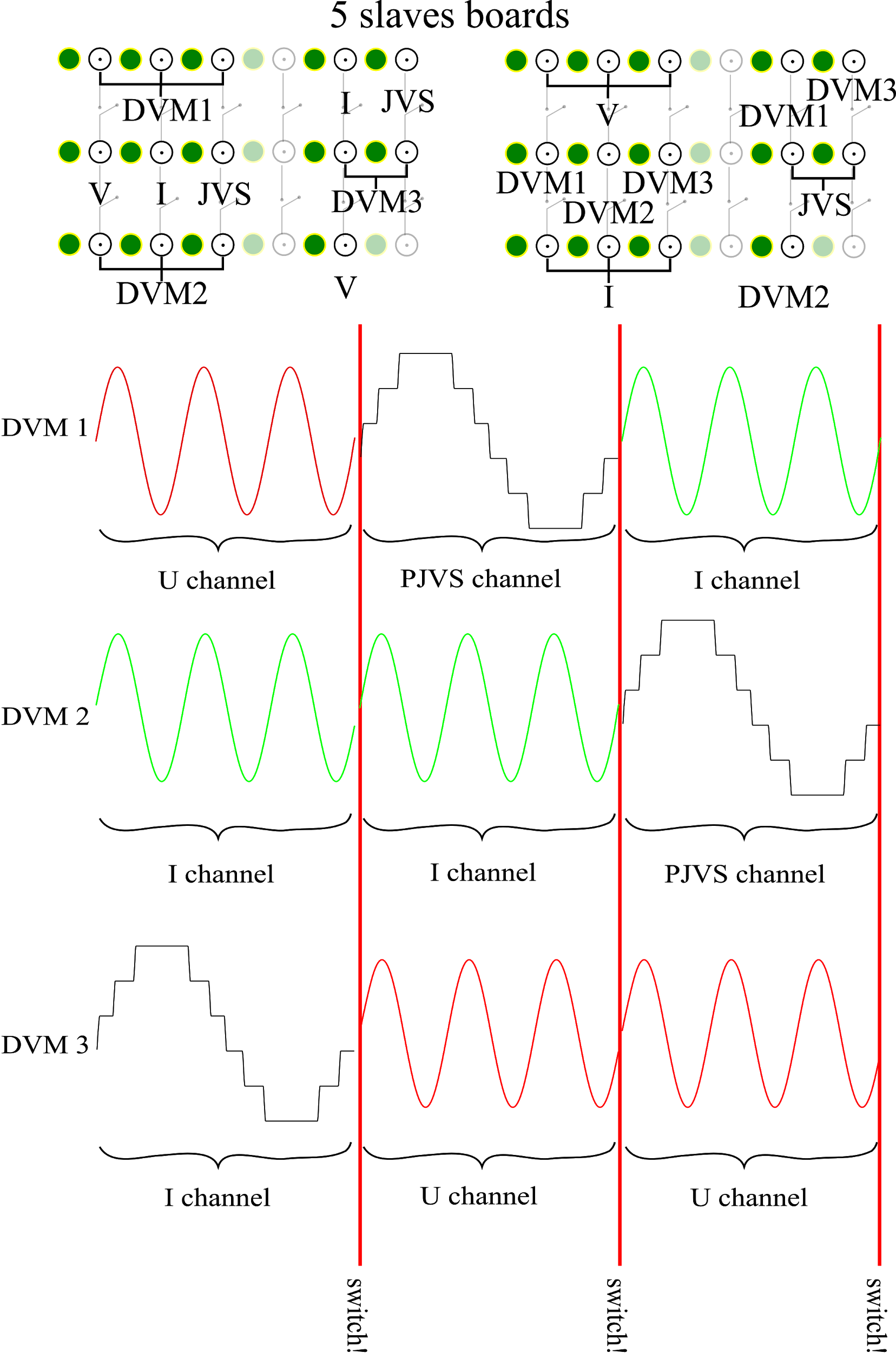
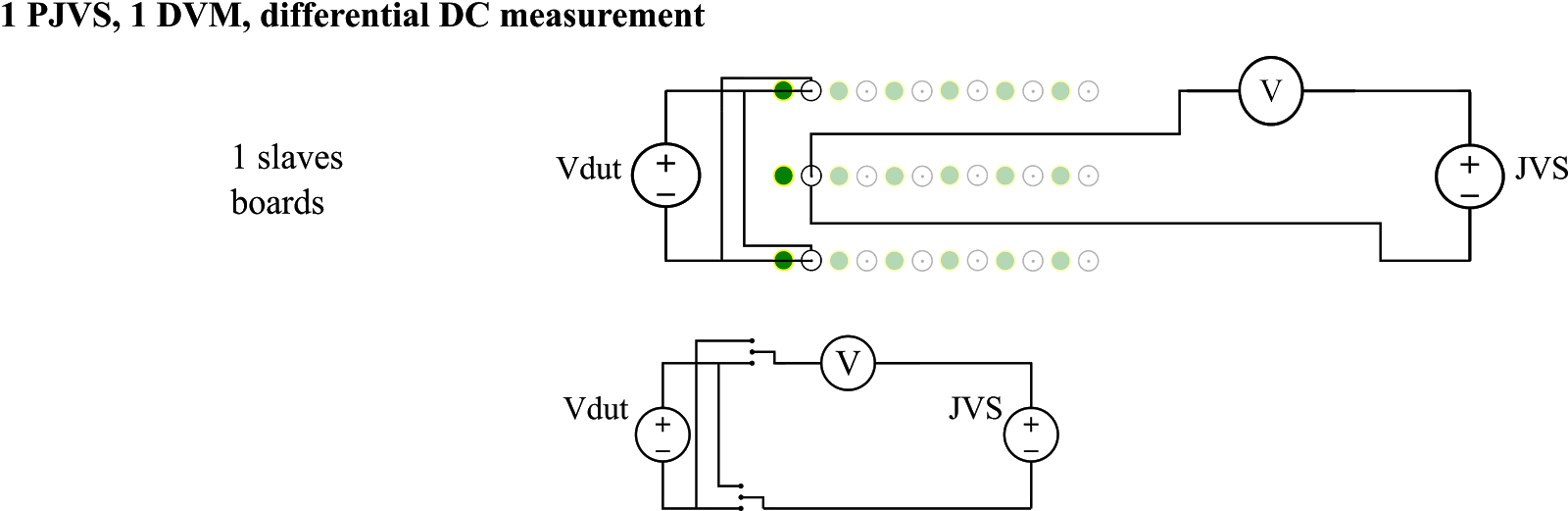
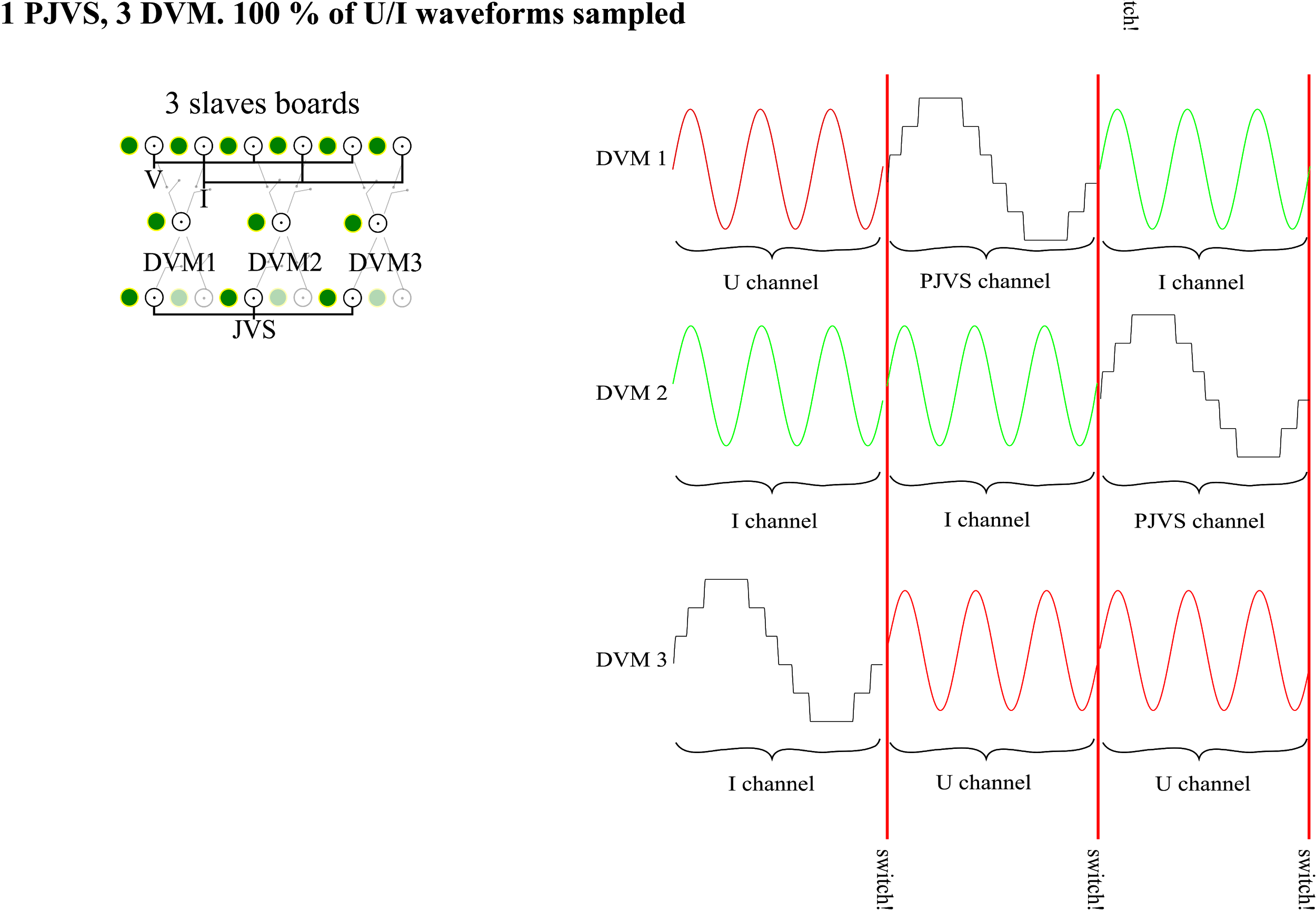
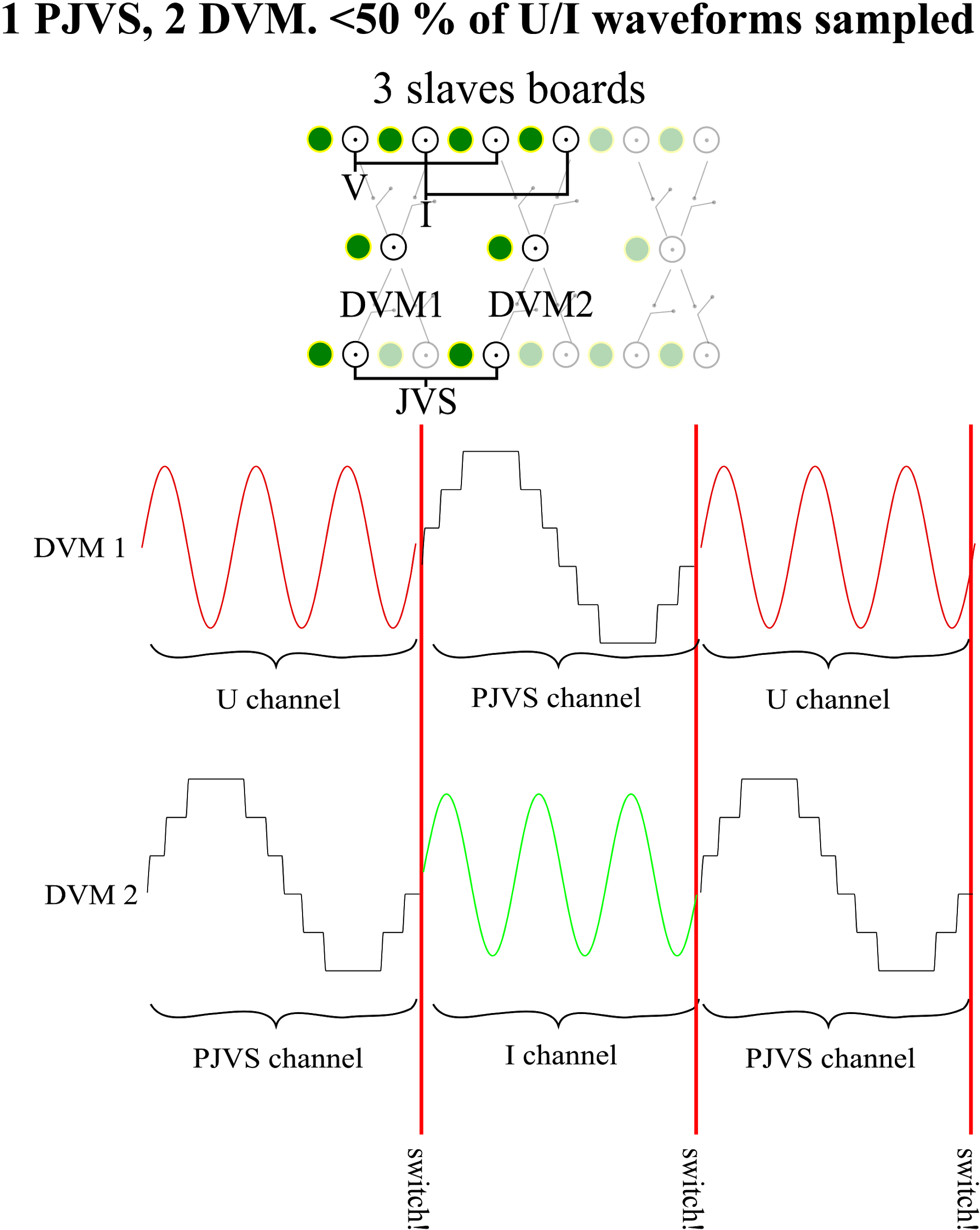
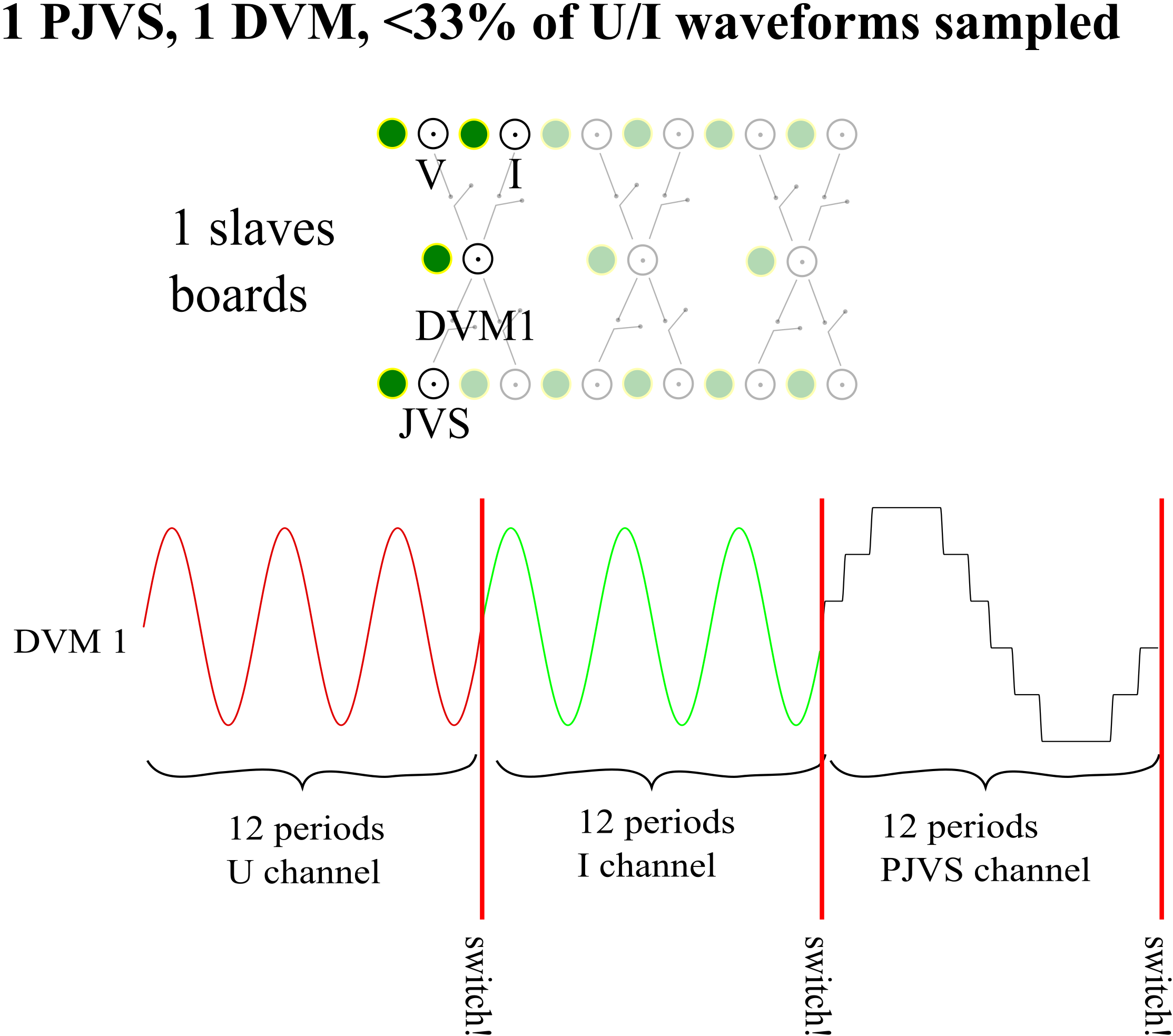
 

Figure 13: connection diagram for 1, 2 and 3 multimeter for SPDT (2-to-1) slaves board.



**Figure 14:** connection diagram for DC measurement with SPDT slave board

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**Figure 15:** connection diagram for 1, 2 and 3 multimeter for SPFT (4-to-1) slaves board.

# LabVIEW driver

**About**

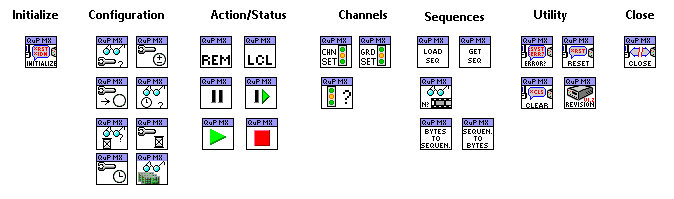
For implementation of the multiplexer into already developed software (TWM), a LabVIEW driver have been made. The driver can be accessed here:

<https://github.com/KaeroDot/QPsw/tree/main/QuPMX/QuPMXLabVIEWdriver>

**Driver structure**

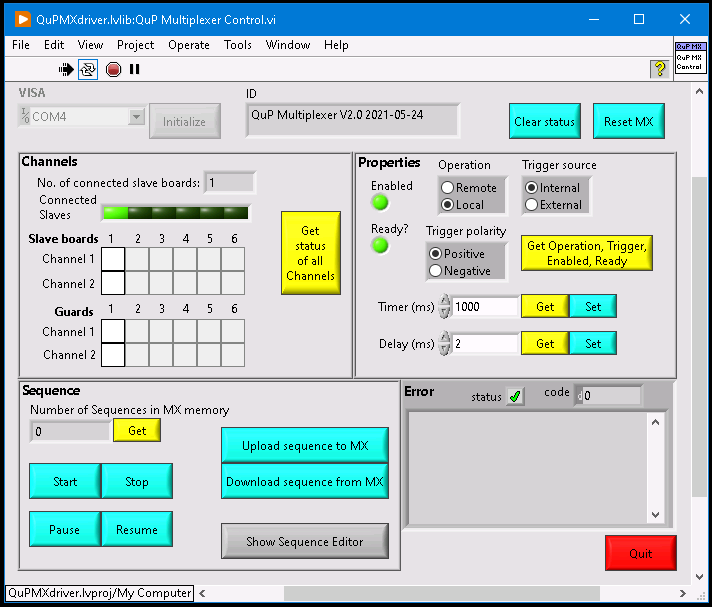
Driver is made in typical Initialize-Use-Close method. VIs for configuration and setup have been created according commands implemented in the firmware of the multiplexer.

The VI Tree is shown in following figure:



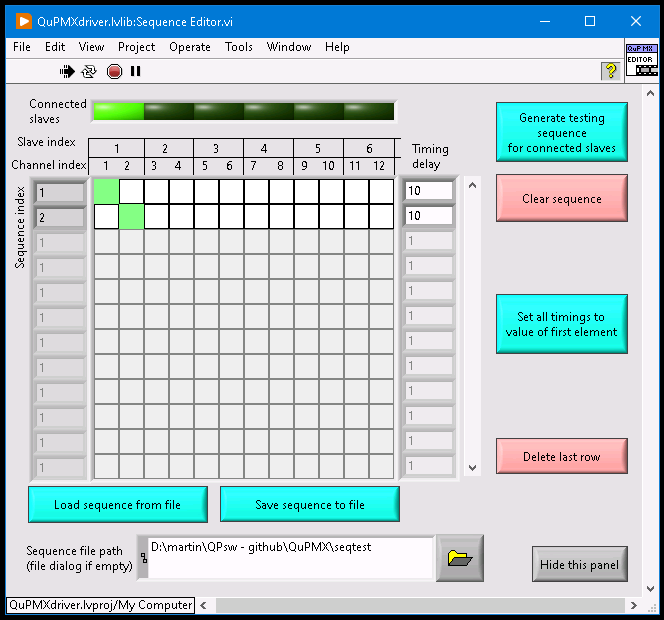
**Multiplexer Control software and Driver Example**

As an example for use of the driver, a multiplexer control software *QuP Multiplexer Control* have been developed. The control software gives ability to manually control the multiplexer and set and read properties:



The connection status of the slave boards can be changed by pressing appropriate buttons (white rectangles on the left side of graphical user interface).

The sequences that are to be loaded into multiplexer can be edited in the Sequence Editor after pressing button *Show Sequence Editor*.



Any sequence can be manually created, loaded or saved from/to a file and uploaded or downloaded from/to multiplexer.

**Compiled binaries**

The latest version of the compiled binaries of the driver library and control software can be accessed here:

<https://github.com/KaeroDot/QPsw/tree/main/QuPMX/QuPMXControl>

To run the control software, a run time libraries for LabVIEW 2020 are required.

List of resources

* User manual
* Schematic circuit in pdf format
* Gerber files
* List of components with RS-AMIDATA code
* Drawings/CAD of a suggested front panel
* Python test script
* Python simulator of the scanner.

File name “multiplexer\_sim.py”

* Arduino firmware
* CH340 driver

# Annex 1: analog circuit description

## Board connectors

**Table 1:** slave board connectors.

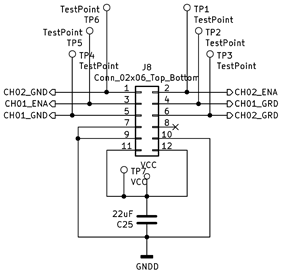
|  |  |
| --- | --- |
| **Identification** | **Connector** |
| Control and supply | Ribbon Cable. PMOD interface. |
| Way 1, Way 2, Pole | SMA on board |
| Guard | Unipolar terminal |
| Ground | Unipolar terminal |

## Board digital pin-out

a 12-pin double-row connector (PMOD type) is used to connect the controller board and the relay board.

**Table 2:** slave board digital lines.

|  |  |  |
| --- | --- | --- |
| **PIN** | **Name** | **Comment** |
| 1 | CH02\_GND | Channel 2 ground connection |
| 2 | CH02\_ENA | Channel 2 enable |
| 3 | CH01\_ENA | Channel 1 enable |
| 4 | CH01\_GRD | Channel 1 guard connection |
| 5 | CH01\_GND | Channel 1 ground connection |
| 6 | CH02\_GRD | Channel 2 guard connection |
| 7 | BD | Digital line tied to GND to indícate that the board is connected. |
| 8 | No connected | No connected |
| 9-10 | GND | Digital ground |
| 11-12 | Vcc | Digital voltage supply |



**Figure 6:** schematic circuit of the digital lines connector.

## Test points list

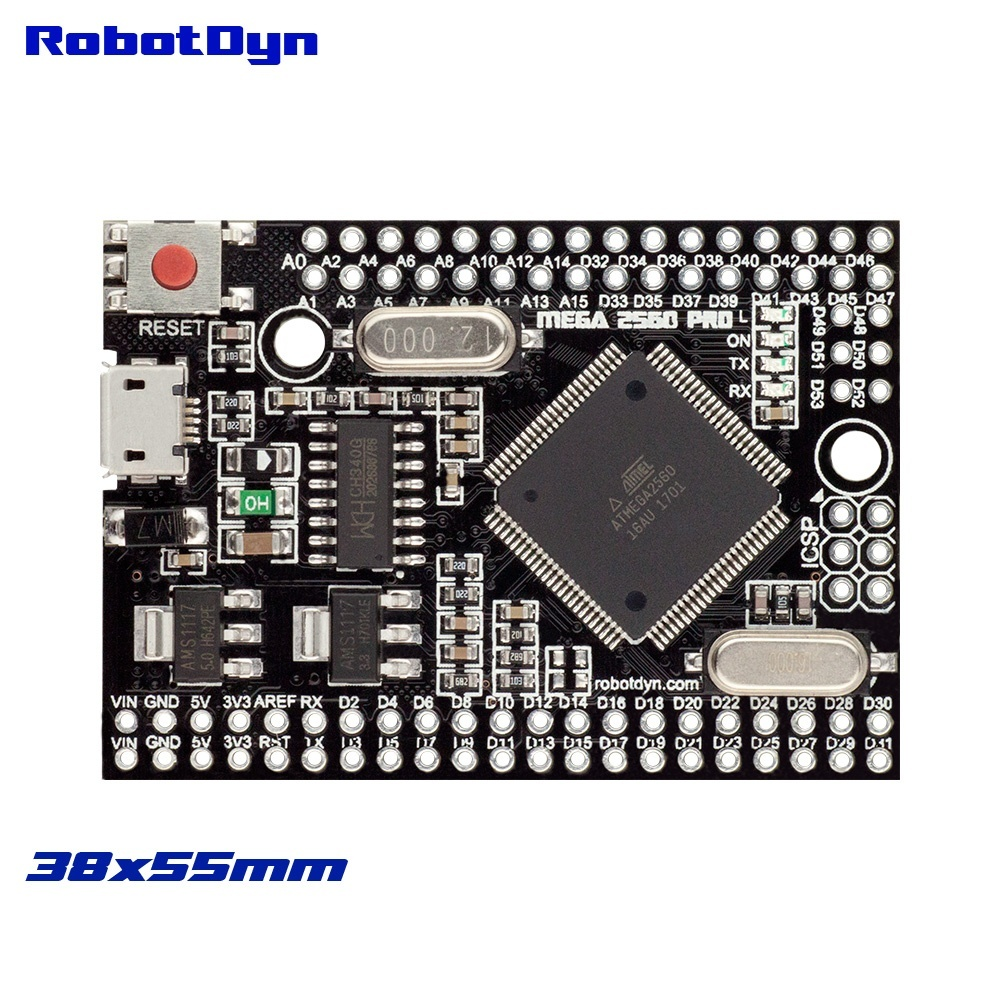
**Table 8:** test points on the SPDT slave board.

|  |  |
| --- | --- |
| **Test points** | **Signal** |
| 0 | GND Digital |
| 1 | CH02\_ENA |
| 2 | CH01\_GRD |
| 3 | CH02\_GRD |
| 4 | CH02\_GND |
| 5 | CH01\_GND |
| 6 | CH01\_ENA |
| 7 | VCC |

# Annex 2: digital circuit description

## Master board

The master is built with an Arduino board and a shield board, this last one includes the connectors for 12 switches, and a voltage regulator to supply the slave boards. This voltage regulator is connected to an external supply of 12 V using a standard power connector Jack and Plug 2.1 mm x 5 mm. The Arduino-based board and the display are supplied by the USB connector. The used display is a 16x4 liquid crystal display (LCD) with I2C Communication.



**Figure 7:** Arduino-based board manufactured by RobotDyn, https://robotdyn.com/mega-2560-pro-embed-ch340g-atmega2560-16au.html.

**Table 4:** master board connectors.

|  |  |
| --- | --- |
| **Identification** | **Connector** |
| Control and supply for slave control | Ribbon Cable. PMOD type. |
| Supply | Screw terminal |
| Clock IN | Opto-isolated BNC |
| Communication to PC | USB |

**Table 5:** master board buttons.

|  |  |
| --- | --- |
| **Identification** | **Button** |
| RST | Reset the multiplexer to power-on state |
| LOC/REM | To select local and remote operation |
| ENA CH | Run the sequence step by step. |
| μC RESET | Master reset. Microcontroller reset (hidden button) |

## Power-on state

1) All channels OPEN

2) All GRD OPEN

3) Local operation

4) Trigger Internal

5) Internal timer 1000 ms

## Serial configuration

Baud rate: 9600

Data Bits: 8 bits

Parity: None

Stop bit: 1 bit

Termination char: LF

Timeout: 10 s

Enable termination: FALSE

Flow control: none

## Driver for CH340 USB-Serial converter

Users of Windows PC must install a driver in order to have connection with the microcontroller by serial com.

The driver is available on the server in the directory: Multiplexer design / QPM design 2020 / Firmware / CH340\_WinDRV.

In addition, the driver can be obtained from the board manufactured webpage <https://robotdyn.com/mega-2560-pro-embed-ch340g-atmega2560-16au.html>.

Or from the chip manufacturer:

<http://www.wch-ic.com/products/CH340.html>

<http://www.wch-ic.com/search?q=CH340&t=downloads>

# Annex 3: Source of errors

On-resistance: limits the measurement uncertainty. Error = RON / (RON + ZV)

# Annex 3:Switching firmware