CALIFORNIA STATE UNIVERSITY, NORTHRIDGE

Department of Electrical and Computer Engineering

ECE 526L

LAB – 3: Delays for Primitives

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Introduction:

In this lab, we learned about delays for primitive, firstly, we applied 0 ns delay then changes the delays as per the instructions from lab manuals.

Methodology/Procedure:

Section 3_1:

1. Open a new folder as **Lab3_526l**, create new file name as **Lab3_1.v**
2. Write the code exactly as in the lab manual and set the initial delay as 0 ns for every delays.
3. Then, create another file name as **Lab3_1_tb.v**
4. Write the code as it was with all the possible combinations of the truth table.
5. After that, gave command **vcs -debug_access+all Lab3_1.v Lab_3_1.tb.v** to check the simulations and fix the errors.
6. Gave Command **simv**.
7. Create the log file as **Lab3_1.Log** using **simv-l Lab3.log** and open **vcdplus.vpd**
8. Select all the signals and open DVE window.
9. Match the result with the truth table.

Section 3_2:

1. Create a new file name as **Lab3_2.v .**
2. Write the code exactly as in the lab manual and set the delay from the lab manual.
3. Then, create another file name as **Lab3_2_tb.v** , write the code as it was with all the possible combinations of the truth table.
4. After that, gave command **vcs -debug_access+all Lab_3_2.v Lab_3_2.tb.v** to check the simulations and fix the error.
5. Gave Command **simv**.
6. Create the log file as **Lab_3_2.Log** using **simv-l Lab3.log** and open **vcdplus.vpd .**
7. Select all the signals and open DVE window.
8. Match the result with the table.

Section 3_3:

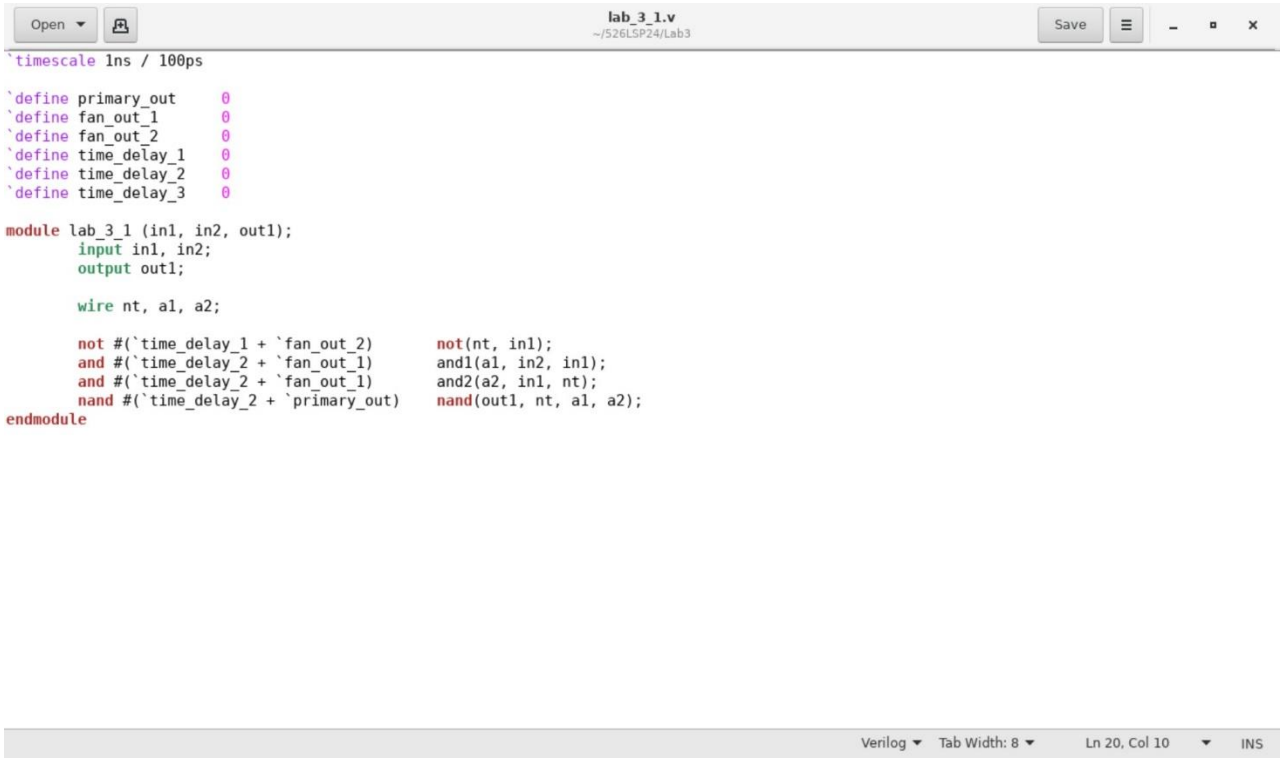
1. Create a new file name as **Lab3_3.v .**
2. Write the code exactly as in the lab manual and set the delay from the lab manual.
3. Then, create another file name as **Lab3_3_tb.v** , write the code as it was with all the possible combinations of the truth table.
4. After that, gave command **vcs -debug_access+all Lab_3_3.v Lab_3_3.tb.v** to check the simulations and fix the error.
5. Gave Command **simv** .
6. Create the log file as **Lab_3_3.Log** using **simv-l Lab3.log** and open **vcdplus.vpd .**
7. Select all the signals and open DVE window.
8. Match the result with the table.

Discussion:

The experiment's findings showed that changing the delay settings significantly affected how the rudimentary circuit behaved. The overall speed and dependability of the circuit were impacted by delays in signal propagation that occurred when delays were raised above specific thresholds. On the other hand, lowering delays below ideal thresholds may lead to irregular behavior and timing infractions.

Section-1

Code 3_1:




```
`timescale 1ns / 100ps

`define primary_out     0
`define fan_out_1       0
`define fan_out_2       0
`define time_delay_1    0
`define time_delay_2    0
`define time_delay_3    0

module lab_3_1 (in1, in2, out1);
        input in1, in2;
        output out1;

        wire nt, a1, a2;

        not #(`time_delay_1 + `fan_out_2)       not(nt, in1);
        and #(`time_delay_2 + `fan_out_1)       and1(a1, in2, in1);
        and #(`time_delay_2 + `fan_out_1)       and2(a2, in1, nt);
        nand #(`time_delay_2 + `primary_out)    nand(out1, nt, a1, a2);
endmodule
```

lab_3_1_tb - Notepad

File Edit Format View Help

```
`timescale 1ns / 1ns

`define monitor_str_1 "%d: in1 = %b, in2 = %b, ! out = %b"

module lab3_1_tb();
        reg in1, in2;
        wire out;
        lab_3_1 UUT(in1,in2,out);

        initial begin
                $monitor(`monitor_str_1, $time, in1, in2, out);
        end

        initial begin
        $vcdpluson;
        #15 in1 = 1'b0;
            in2 = 1'b0;
        #15 in1 = 1'b0;
            in2 = 1'b1;
        #15 in1 = 1'b1;
            in2 = 1'b0;
        #15 in1 = 1'b1;
            in2 = 1'b1;
        #15 $finish;
        end
endmodule
```

Ln 1, Col 1 | 100% | Unix (LF) | UTF-8

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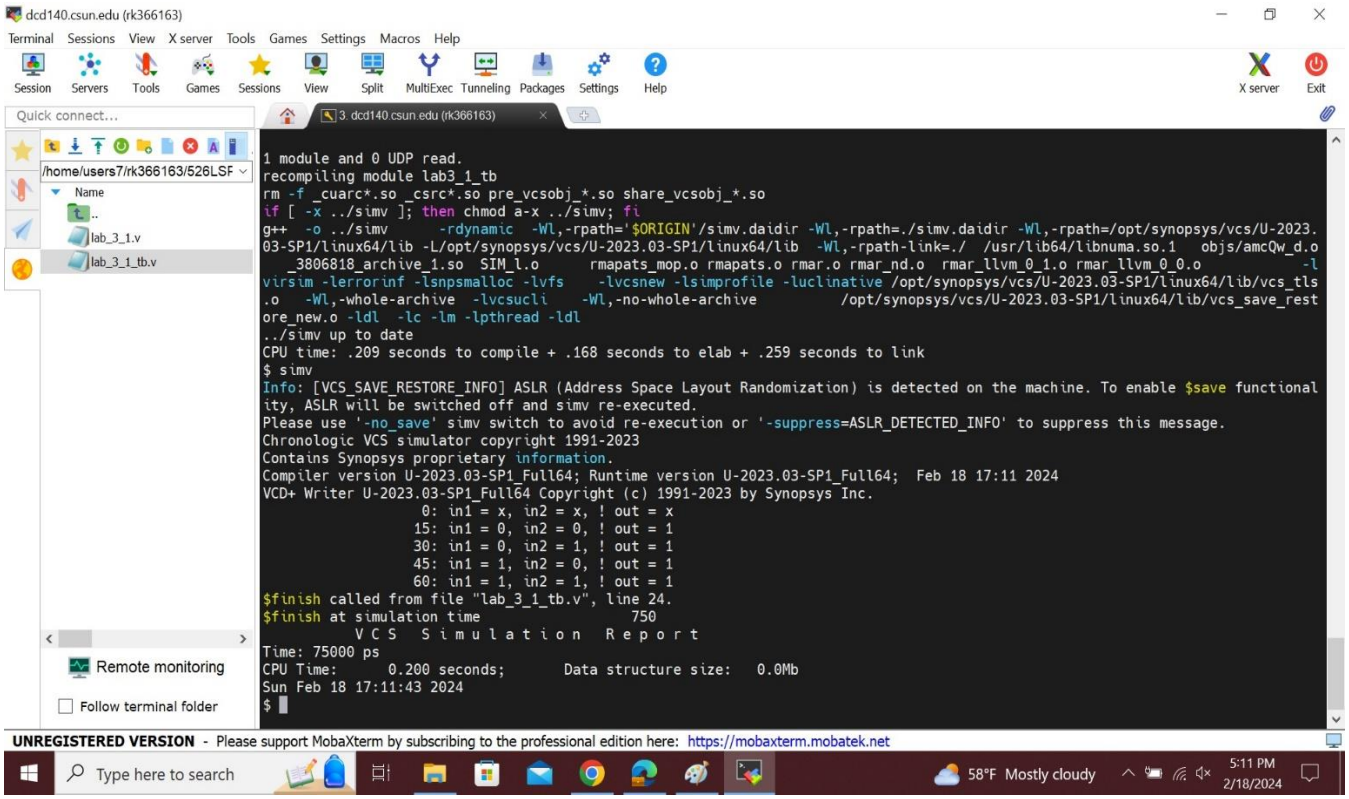
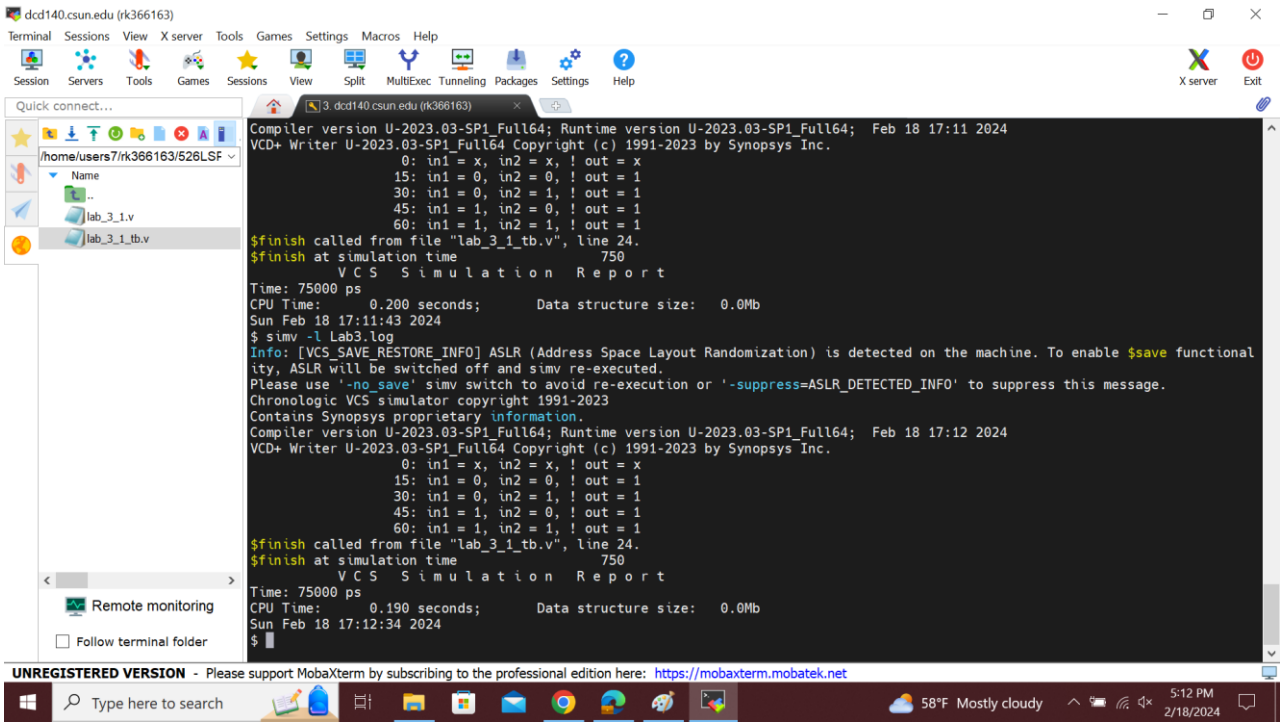
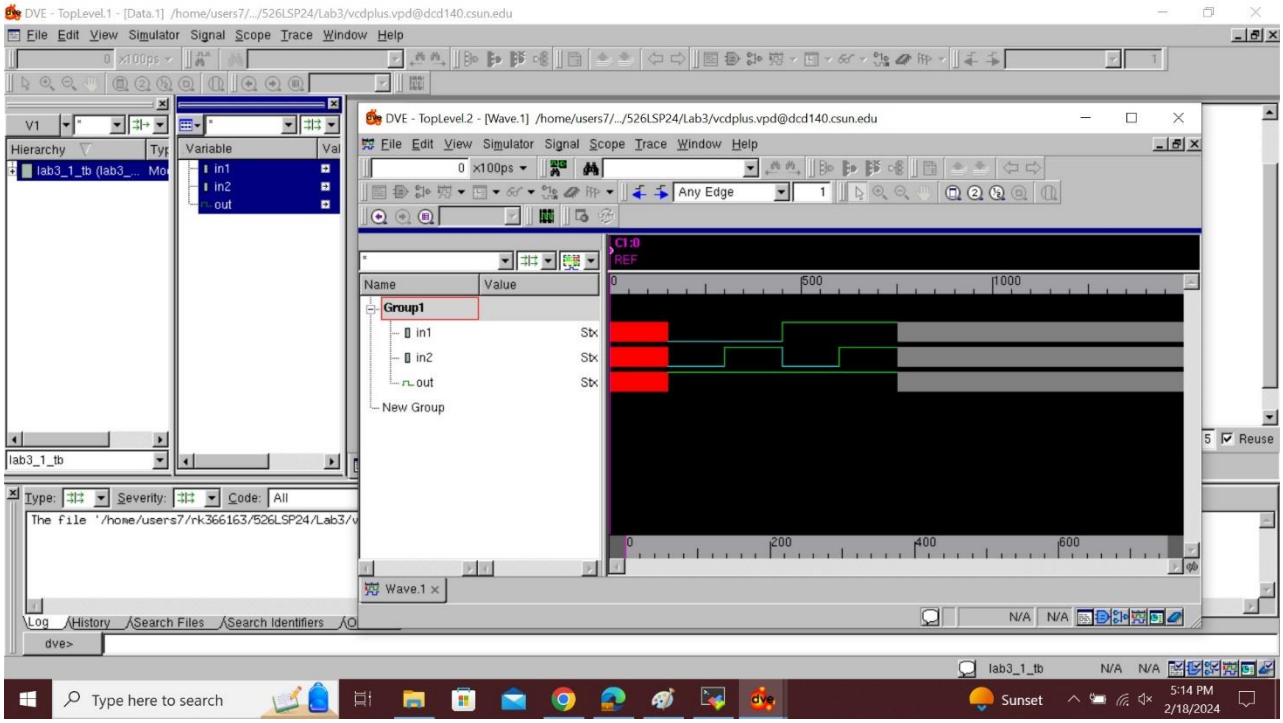
Simv 3_1:



Log file 3_1:



Wave 3_1:



Section-2

Code 3_2:

lab_3_2.v
~/526LSP24/Lab3

```
`timescale 1ns / 100ps

`define primary_out     5
`define fan_out_1       0.5
`define fan_out_2       1
`define fan_out_3       1.5
`define time_delay_1    1
`define time_delay_2    2
`define time_delay_3    4
`define time_delay_4    5

module lab_3_2 (in1, in2, out2);
        input in1, in2;
        output out2;

        wire nt, a1, a2;

        not #(`time_delay_1 + `fan_out_2)       not1(nt, in1);
        and #(`time_delay_2 + `fan_out_1)       and1(a1, in2, in1);
        and #(`time_delay_2 + `fan_out_1)       and2(a2, in1, nt);
        nand #(`time_delay_3 + `primary_out)    nand1(out2, nt, a1, a2);
endmodule
```

Verilog Tab Width: 8 Ln 23, Col 1 INS

Open ▾ | lab_3_2_tb.v ~/526LSP24/Lab3 | Save

lab_3_2.v | lab_3_2_tb.v

```
`timescale 1ns / 1ns

`define monitor_str_1 "%d: in1 = %b, in2 = %b, a1 = %b, a2 = %b, nt = %b ! out = %b"

module lab3_2_tb();
        reg in1, in2;
        wire out2;
        lab_3_2 UUT(in1,in2,out2);

        initial begin
                $monitor(`monitor_str_1, $time, in1, in2, out);
        end

        initial begin
                $monitor(`monitor_str_1, $time, in1, in2, UUT.nt, UUt.a1, UUT.a2, out2);
        end

        initial begin
        $vcdpluson;
        #15 in1 = 1'b0;
            in2 = 1'b0;
        #15 in1 = 1'b0;
            in2 = 1'b1;
        #15 in1 = 1'b1;
            in2 = 1'b0;
        #15 in1 = 1'b1;
            in2 = 1'b1;
        #15 $finish;
        end
endmodule
```

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Simv 3_2:

dcd140.csun.edu (rk366163)

Terminal Sessions View X server Tools Games Settings Macros Help

Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help X server Exit

Quick connect...

3. dcd140.csun.edu (rk366163)

/home/users7/rk366163/526LSF

Name

..
csrc
DVEfiles
simv.daidir
Lab3.log
lab_3_1.v
lab_3_1_tb.v
lab_3_2.v
lab_3_2_tb.v
udi.key
vcdplus.vpd

Remote monitoring

Follow terminal folder

```
g++  -o ../simv      -rdynamic  -Wl,-rpath='$ORIGIN'/simv.daidir -Wl,-rpath=./simv.daidir -Wl,-rpath=/opt/synopsys/vcs/U-2023.03-SP1/linux64/lib -L/opt/synopsys/vcs/U-2023.03-SP1/linux64/lib  -Wl,-rpath-link=./  /usr/lib64/libnuma.so.1   objs/amcQw_d.o   _3836164_archive_1.so  SIM_l.o      rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o           -lvirsim -lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinative /opt/synopsys/vcs/U-2023.03-SP1/linux64/lib/vcs_tls.o   -Wl,-whole-archive  -lvcsucli    -Wl,-no-whole-archive          /opt/synopsys/vcs/U-2023.03-SP1/linux64/lib/vcs_save_restore_new.o -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .233 seconds to compile + .164 seconds to elab + .256 seconds to link
$ simv
Info: [VCS_SAVE_RESTORE_INFO] ASLR (Address Space Layout Randomization) is detected on the machine. To enable $save functionality, ASLR will be switched off and simv re-executed.
Please use '-no_save' simv switch to avoid re-execution or '-suppress=ASLR_DETECTED_INFO' to suppress this message.
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version U-2023.03-SP1_Full64; Runtime version U-2023.03-SP1_Full64;  Feb 18 17:34 2024
VCD+ Writer U-2023.03-SP1_Full64 Copyright (c) 1991-2023 by Synopsys Inc.
                   0: in1 = x, in2 = x, a1 = x, a2 = x, nt = x ! out = x
                  15: in1 = 0, in2 = 0, a1 = x, a2 = x, nt = x ! out = x
                  17: in1 = 0, in2 = 0, a1 = 1, a2 = x, nt = x ! out = x
                  18: in1 = 0, in2 = 0, a1 = 1, a2 = 0, nt = 0 ! out = x
                  27: in1 = 0, in2 = 0, a1 = 1, a2 = 0, nt = 0 ! out = 1
                  30: in1 = 0, in2 = 1, a1 = 1, a2 = 0, nt = 0 ! out = 1
                  45: in1 = 1, in2 = 0, a1 = 1, a2 = 0, nt = 0 ! out = 1
                  47: in1 = 1, in2 = 0, a1 = 0, a2 = 0, nt = 0 ! out = 1
                  60: in1 = 1, in2 = 1, a1 = 0, a2 = 0, nt = 0 ! out = 1
                  63: in1 = 1, in2 = 1, a1 = 0, a2 = 1, nt = 0 ! out = 1
$finish called from file "lab_3_2_tb.v", line 24.
$finish at simulation time                  750
           V C S   S i m u l a t i o n   R e p o r t
Time: 75000 ps
CPU Time:      0.210 seconds;       Data structure size:   0.0Mb
Sun Feb 18 17:34:35 2024
$
```

UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net

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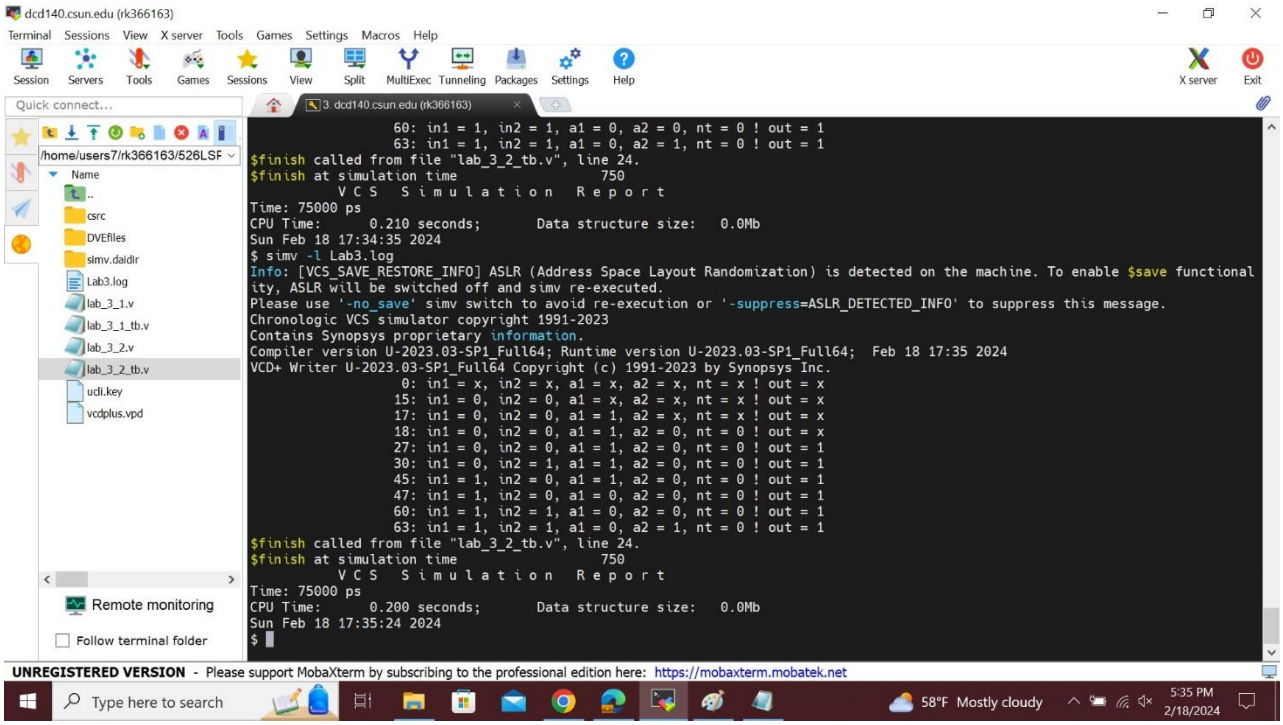
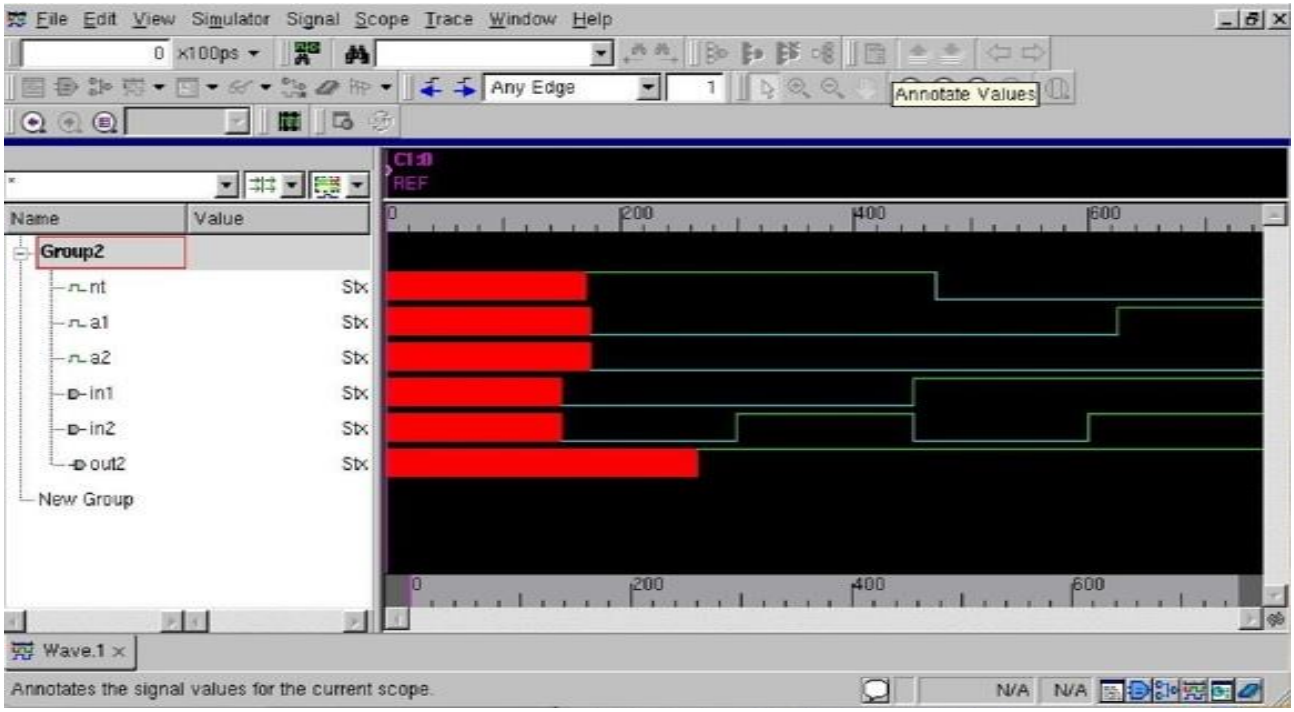
Log File 3_2:



Wave 3_2:



Section-3

Code 3_3:

Lab3_3 - Notepad

File Edit Format View Help

```
`timescale 1 ns / 100 ps

`define primary_out   5
`define fan_out_1     0.5
`define fan_out_2     1
`define fan_out_3     1.5
`define time_delay_1  1
`define time_delay_2  2
`define time_delay_3  4
`define time_delay_4  5


module Lab3_3  (in1, in2, out3);
                input in1, in2;
                output out3;

                wire nt,a1,a2,o;

                not  #(`time_delay_1 + `fan_out_3)  not1(nt, in1);
                and  #(`time_delay_2 + `fan_out_1)  and1(a1,in2,in1);
                and  #(`time_delay_2 + `fan_out_2)  and2(a2,in1,nt);
                or       #(`time_delay_2 + `fan_out_1)  or1(o,nt,a2);
                nand #(`time_delay_4 + `primary_out) nand1(out3,a2,o,nt,a1);

endmodule
```

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Lab3_3_tb - Notepad

File Edit Format View Help

```
`timescale 1 ns /100 ps

`define monitor_str_1 "%d: in1 = %b, in2 = %b, a1 = %b, a2 = %b, nt =%b, o = %b, | out = %b"

module Lab3_3_tb();
        reg in1, in2;
        wire out;
        wire a1, a2, nt, o;
        Lab3_3 UUT(in1,in2,out);
        initial begin
        $monitor(`monitor_str_1, $time, in1,in2, UUT.a1, UUT.a2, UUT.nt, o , out);
        end
        initial begin
        $vcdpluson;
        #15     in1  = 1'b0;
                in2  = 1'b0;

        #15     in1  = 1'b0;
                in2  = 1'b1;

        #15     in1  = 1'b1;
                in2  = 1'b0;

        #15     in1  = 1'b1;
                in2  = 1'b1;
        #15 $finish;
        end
endmodule
```

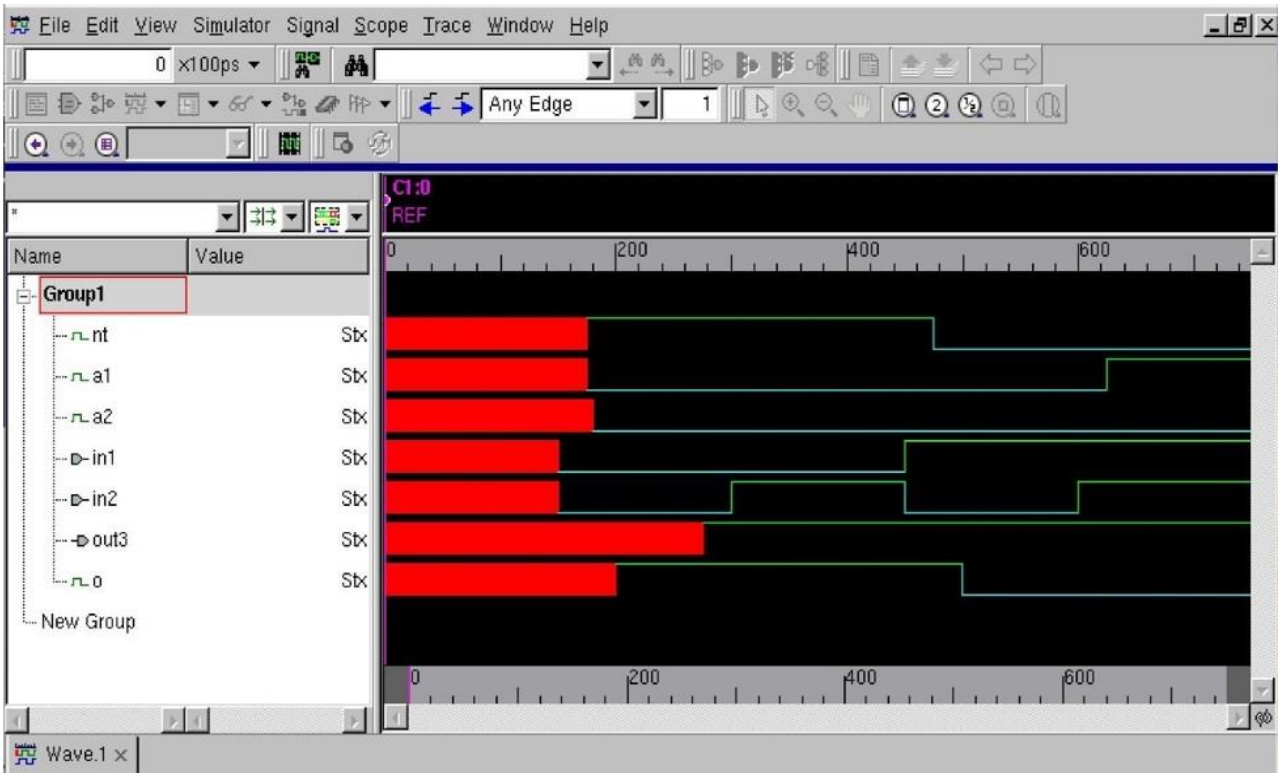
Ln 1, Col 1 | 100% | Windows (CRLF) | UTF-8

Type here to search | 55°F Mostly cloudy | 10:35 PM 2/20/2024

Simv 3_2:

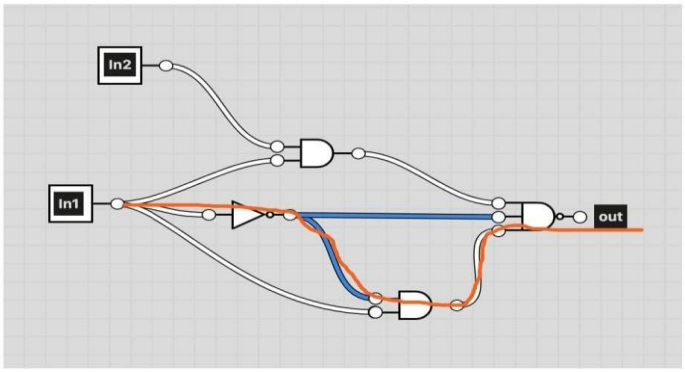
```
 simv re-executed.
Please use '-no_save' simv switch to avoid re-execution or '-suppress=ASLR_DETEC
TED_INFO' to suppress this message.
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version U-2023.03-SP1_Full64; Runtime version U-2023.03-SP1_Full64;  Fe
b 14 20:33 2024
VCD+ Writer U-2023.03-SP1_Full64 Copyright (c) 1991-2023 by Synopsys Inc.
                  0: in1 = x, in2 = x, a1 = x, a2 = x, nt =x, o = z, | out = x
                 15: in1 = 0, in2 = 0, a1 = x, a2 = x, nt =x, o = z, | out = x
                 18: in1 = 0, in2 = 0, a1 = 0, a2 = x, nt =1, o = z, | out = x
                 18: in1 = 0, in2 = 0, a1 = 0, a2 = 0, nt =1, o = z, | out = x
                 28: in1 = 0, in2 = 0, a1 = 0, a2 = 0, nt =1, o = z, | out = 1
                 30: in1 = 0, in2 = 1, a1 = 0, a2 = 0, nt =1, o = z, | out = 1
                 45: in1 = 1, in2 = 0, a1 = 0, a2 = 0, nt =1, o = z, | out = 1
                 48: in1 = 1, in2 = 0, a1 = 0, a2 = 0, nt =0, o = z, | out = 1
                 60: in1 = 1, in2 = 1, a1 = 0, a2 = 0, nt =0, o = z, | out = 1
                 63: in1 = 1, in2 = 1, a1 = 1, a2 = 0, nt =0, o = z, | out = 1
$finish called from file "Lab3_3_tb.v", line 26.
$finish at simulation time                  750
           V C S   S i m u l a t i o n   R e p o r t
Time: 75000 ps
CPU Time:      0.180 seconds;       Data structure size:   0.0Mb
Wed Feb 14 20:33:13 2024
$
```

Wave 3_3:



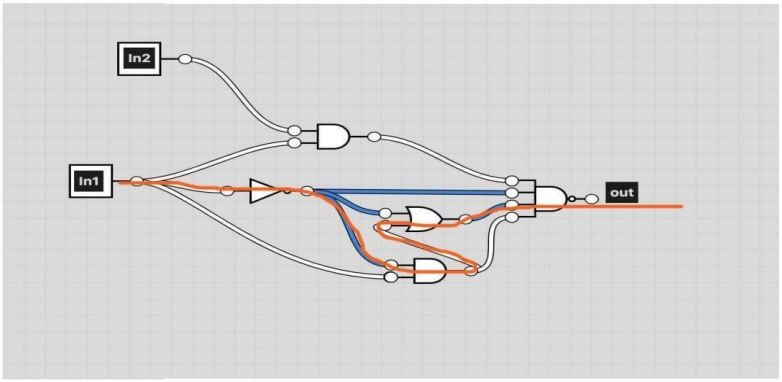
Lab report questions:

1. **What is the longest path of the 1st circuit?**



In the above figure, I have drawn the longest path of the circuit that is input which travels from the NOT gate first and then travels to the AND gates, which reaches the final output through the NAND gate. comparing two remaining two paths this is the longest path because other path has only two gates to reach the output where as in this path it has to travel in 3 gates which makes delay in time.

2. **What is the longest path of the 2nd circuit?**



The longest path of the circuit is drawn above is because the input starts from the NOT gate and it travels to the AND gate, then it goes to the OR gate and finally the output comes out through the NAND gate.

On comparing to all other paths, this is the longest part because it has to travel through 4 gates.

Analysis of result:

Primitive delays are the shortest time delays that can happen when a signal goes through a gate or group of gates in a digital circuit. A basic delay element in digital circuits is produced by this gate combination. The exact delay period will vary based on the circuit's gate characteristics and gate propagation delays. In this lab 1st initial the delays are zero and in second part when we change the values of primitives then the delay will be changed. Finally, the output will be say that the propagation delay will be there for the different delays for their individual values what we given in the code.

Conclusion:

In this lab, we completed the gate delays for the given primitives and the numeric values by using some commands and some tools by the linux synopsis VCS.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, neither have I allowed nor I will let anyone to copy my work.

Name(printed) Raj Kumar

Name(signed) Raj Kumar Date 02/18/2024