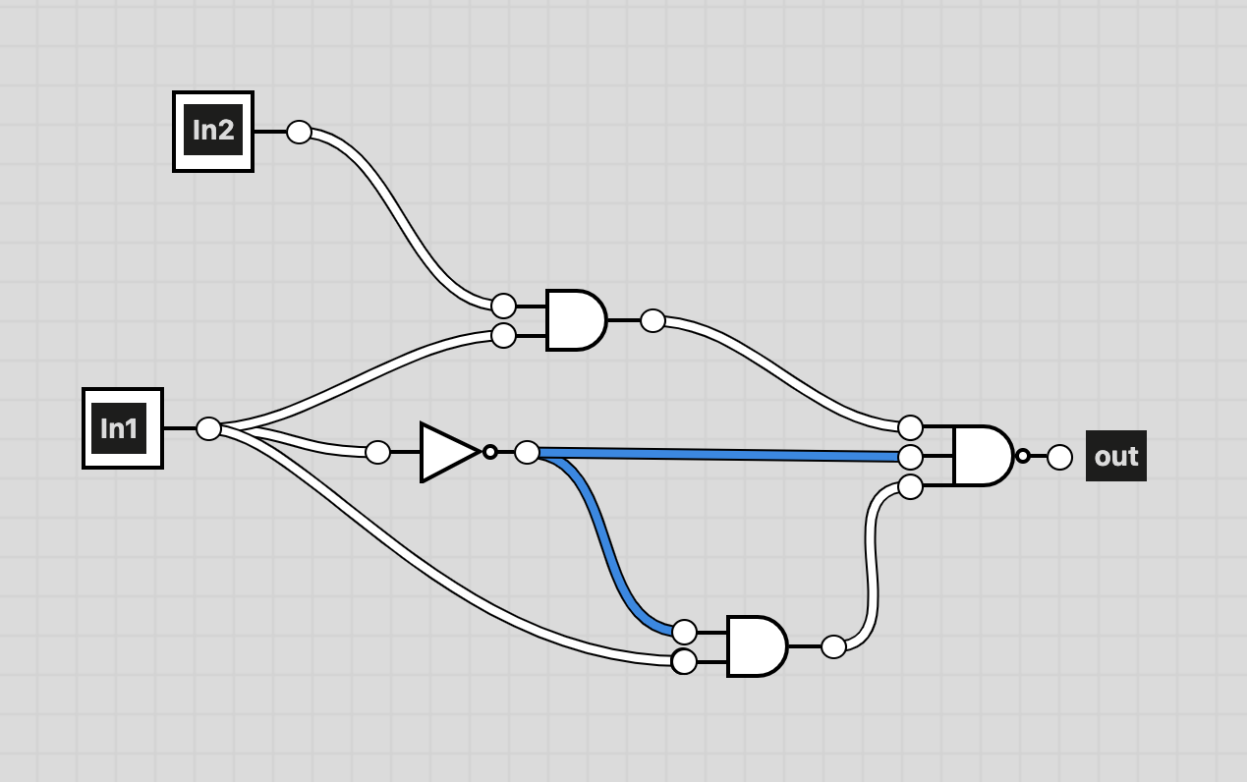
ECE 526L Lab3

In this portion of the Lab, you are presented with below code that uses delays for primitives. Initially all delays are 0ns.



Lab2.v | Lab2_tb.v | Lab2_complete.v

```
`timescale 1 ns / 100 ps

`define PRIMARY_OUT     0       // ns (primary outputs)
`define FAN_OUT_1       0       // ns (one output fanout)
`define FAN_OUT_2       0       // ns (two output fanout)
`define TIME_DELAY_1    0       // ns (one input gates)
`define TIME_DELAY_2    0       // ns (two input gates)
`define TIME_DELAY_3    0       // ns (three input gates)


module Lab2_1 (in1,in2,out1);
        input in1,in2;
        output out1;

        wire NT,A1,A2;

        not  #(`TIME_DELAY_1 + `FAN_OUT_2)   NOT1(NT,in1);
        and  #(`TIME_DELAY_2 + `FAN_OUT_1)   AND1(A1,in2,in1);
        and  #(`TIME_DELAY_2 + `FAN_OUT_1)   AND2(A2,in1,NT);
        nand  #(`TIME_DELAY_3 + `PRIMARY_OUT)   NAND1(out1,NT,A1,A2);

endmodule
```

//////////////////////////////////////TB

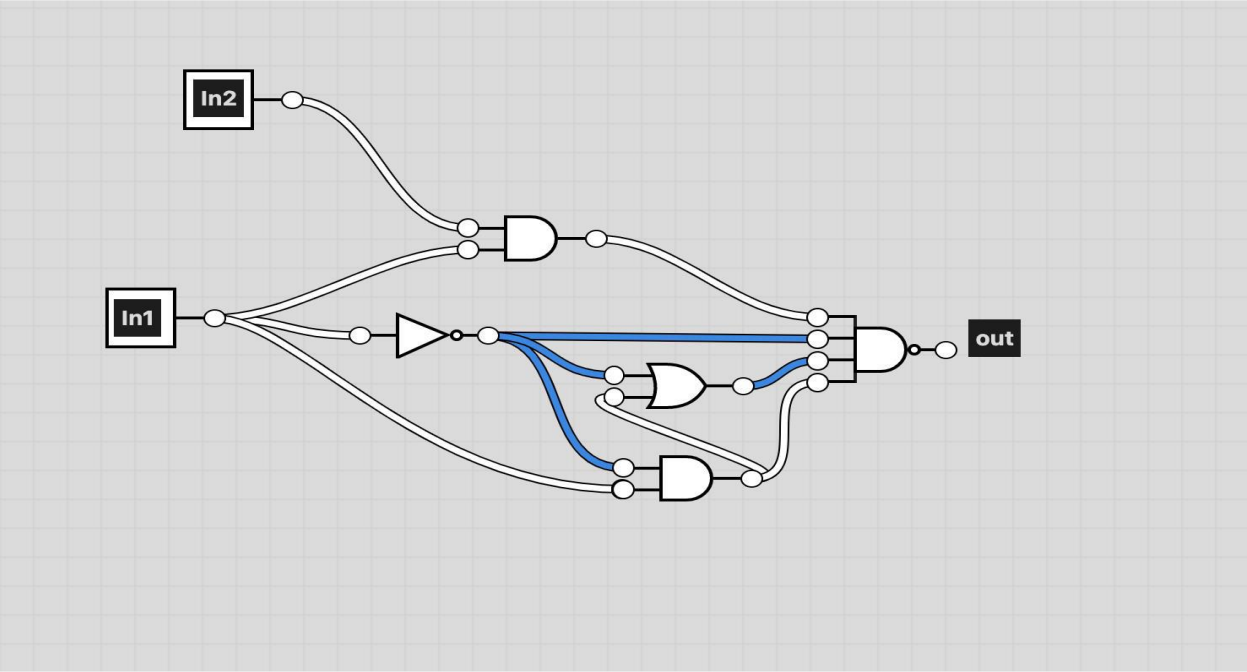
```
`timescale 1 ns / 1 ns

`define MONITOR_STR_1 "%d: in1 = %b, in2 = %b, | out = %b"


module Lab2_1_tb();
        reg in1, in2;
        wire out;
        Lab2_1 UUT(in1,in2,out);

        initial begin
                $monitor(`MONITOR_STR_1, $time, in1, in2, out);
        end

        initial begin
        $vcdpluson; // For graphical viewer (waveforms)
        #15 in1 = 1'b0;
            in2 = 1'b0;
        #15 in1 = 1'b0;
            in2 = 1'b1;

        #15 $finish;
        end
endmodule
```

Simulate the code and add the remaining cases to test all possible combinations of in1 and in2 (don't need to include x and z).
Also add internal wire signals A1, A2, NT to monitor using "." operator.
Then change the delays to values of table below and simulate again, show how these delays change the waveforms in your lab report with images.

Primary_out	5ns
Fan_out_1	0.5ns
Fan_out_2	1ns
Fan_out_3	1.5ns
Time_delay_1	1ns
Time_delay_2	2ns
Time_delay_3	4ns
Time_delay_4 (4 input gate)	5ns

Lab report question: What's the critical path (longest delay) of this design?

Change the circuit to below circuit and simulate again with delays.



Lab report question: What's the critical path (longest delay) of this new design?