ECE 526L Lab5

This lab is continuation of Lab4, in this lab you should reuse the DFF you developed in Lab4 and create a Verilog model of the 8-bit register with the organization shown in Figure 3.

The register has the logic symbol shown in Figure 4. From its symbol, the functions of the register's reset (RST) and enable (ENA) can be inferred. Use the following module header:

module register(CLK, RST, ENA, DATA, R);

input CLK, ENA, RST;

input [7:0] DATA; output [7:0] R;

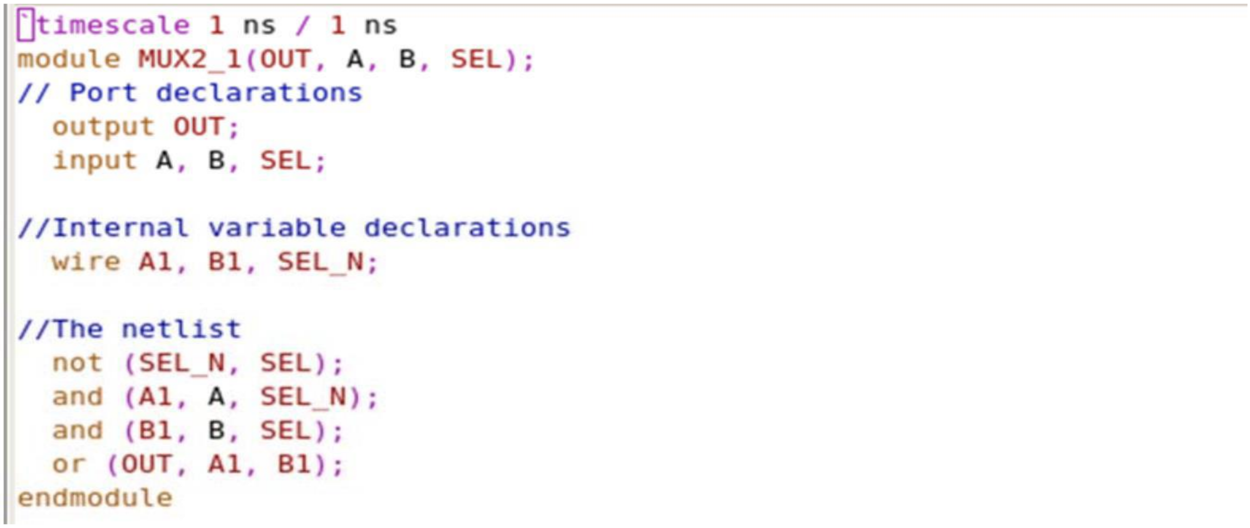
.

.

.

endmodule

Use the multiplexor model provided below or the behavioral one, where needed. Add the same gate delays for the multiplexor cells as used elsewhere from lab4.



```
`timescale 1 ns / 1 ns
module MUX2_1(OUT, A, B, SEL);
// Port declarations
  output OUT;
  input A, B, SEL;

//Internal variable declarations
  wire A1, B1, SEL_N;

//The netlist
  not (SEL_N, SEL);
  and (A1, A, SEL_N);
  and (B1, B, SEL);
  or (OUT, A1, B1);
endmodule
```

Write a testbench module, reg_test.v to verify the functionality of your design. Include stimuli to test the following:

- The register resets when RST is zero.
- The contents of the data bus are clocked into the register when ENA is asserted.
- The contents of the register are preserved and the contents of the data bus are ignored when the register is clocked with ENA deasserted.

You can incorporate a clock generator with a suitable period for your design in your test bench instead of changing the clock signal value every step.

To reduce typographical errors, put your invocation of the compiler into a force file. This is a text file that contains all the commands and arguments you would otherwise have to type in on the command line with each invocation of the compiler.

For example, if you have design files FileA.sv and FileB.sv and test fixture file tb_TOP.sv, your force file would consist of

```
vcs -debug_access+all –sverilog FileA.sv FileB.sv tb_TOP.sv
```

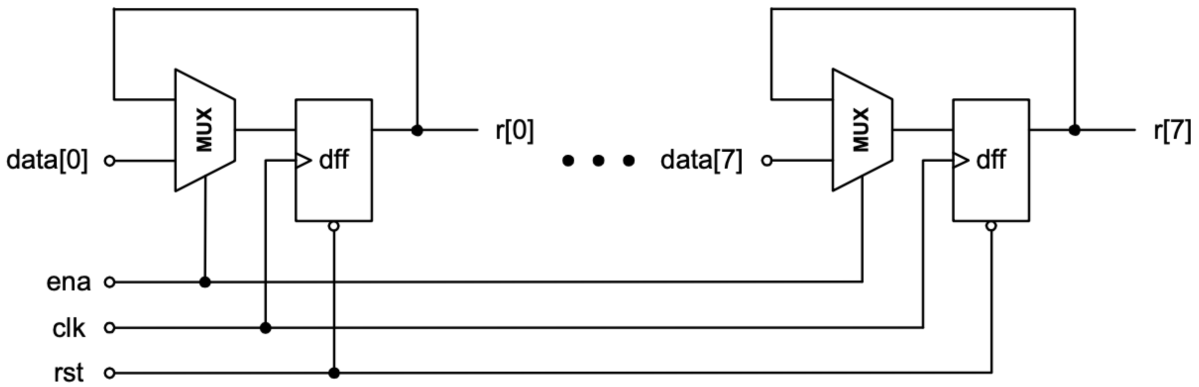
Save the force file in a suitable file time with a .f extension.

By default, Linux files are not executable. Make your force file executable by typing from the command line

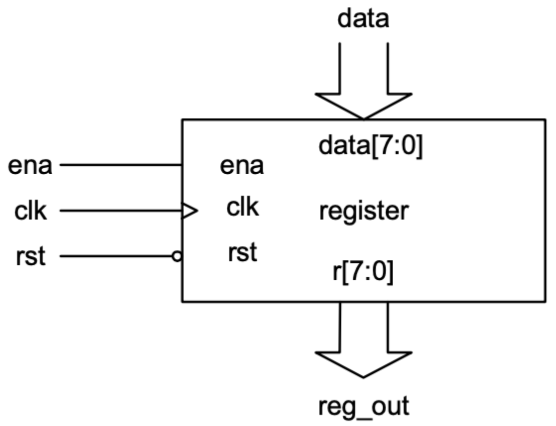
```
chmod +x <filename>.f
```

Calculate the maximum operating frequency of the entire design. In order to do this, you should calculate the longest path’s delay.

Demonstrate in your simulation and analyze in your report what happens when you exceed that frequency. Correlate your calculated and observed maximum frequencies.



Schematic for 8-bit Register with Clear
Figure 3



Circuit Symbol for Register
Figure 4