Astable ICM7555 PCB

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Description

This mini project is meant to be an introduction to PCB design. It follows the tutorial provided by Contextual Electronics, which briefly covers how to convert a schematic into a PCB, specifically with surface mount components. This project is not meant to be complex, but rather gives an insight into the procedure of design → schematic → modelling → assembly. This includes IPC standards, although non-trivial for this prototype, how to effectively use component data sheets, the physical structure of a PCB, and the design practices that are used most often.

Implementation

During the design process, the following modifications were made:

- The addition of a switch to cut-off the battery.
- Larger SMD components (1206) to give some additional error room when soldering.
- Custom libraries for the battery holder and switch.

Theory

The CMOS 7555 timer was chosen due to its improved voltage range over the standard bipolar NE/SE555 timer, which allows a coin cell battery to be used. In fact, it is the exact equivalent to the NE/SE555 for most applications, especially as an astable multivibrator. The internal functional diagram shown in Figure 1 includes two comparators, an SR latch, and an NMOS discharge transistor. The astable configuration shown in Figure 2 can be described using the functional diagram shown in Figure 2, where pins 2 ($\overline{\text{TRIGGER}}$) and 6 (THRESHOLD) control the state of the comparators.

Regardless of the values of resistors R_A and R_B, the initial state at pin 3 is logic high (H), as the capacitor is held discharged by the internal NMOS discharge transistor. When the voltage across the capacitor voltage begins to increase, it reaches a value that is $2/3V_{DD}+$, which sets comparator A to output H. As a result, the SR latch is reset and the output is logic low (L). At this point, the NMOS transistor gate terminal is H, which allows the current to discharge from the capacitor through R_B to ground. During this phase, the voltage on the capacitor drops below $1/3V_{DD}$, which sets the SR latch to output H, and turns the discharge transistor off. The capacitor begins to charge again and follows the same self triggering multivibrator effect. The waveform of the capacitor and output voltage can be seen in Figure 3.

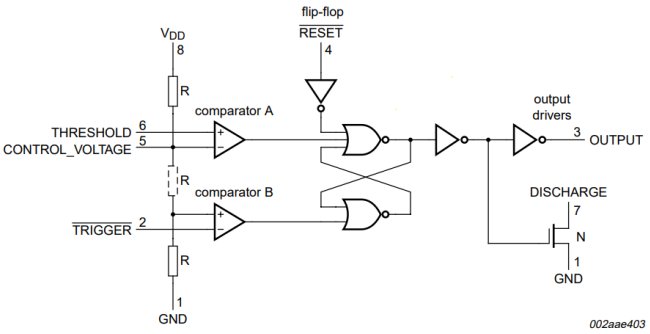


Figure 1: The functional diagram, where pin 5 (CONTROL_VOLTAGE) and the positive terminal of comparator B represent $2/3V_{DD}$ and $1/3V_{DD}$, respectively.

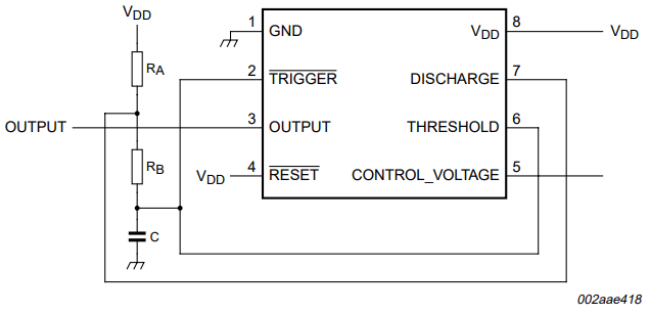


Figure 2: The astable configuration, where the voltage on capacitor C acts as a set and reset for the SR latch through both comparators.

The data sheet provides the frequency f and duty cycle δ of the square wave output, given the values of R_A, R_B, and C:

$$f = \frac{1.44}{(R_A + 2R_B) \times C}$$

$$\delta = \frac{R_A + R_B}{R_A + 2R_B}$$

For the frequency, the resistors and capacitor are inversely proportional to the frequency as the time constant is increased. The duty cycle is solely dependent on the ratio of

both resistors. Theoretically, according to the given resistor values in Figure 6, f $\simeq$ 1.53Hz and $\delta \simeq 50\%$.

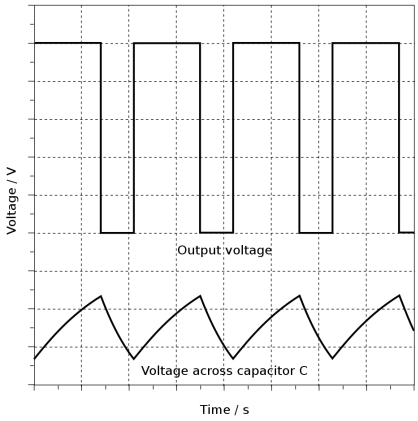


Figure 3: The waveform of the astable configuration.

Schematic

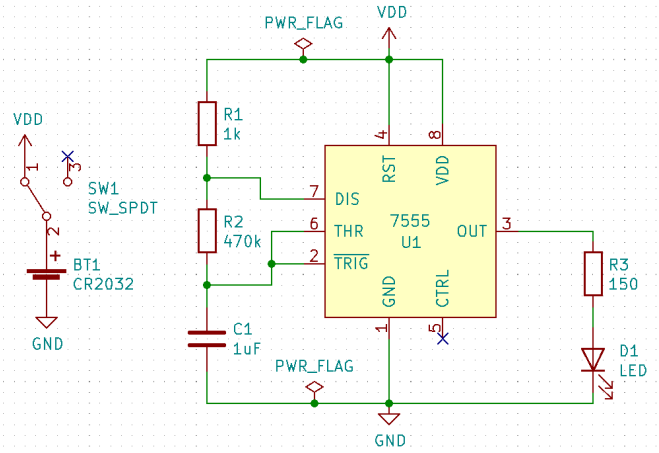
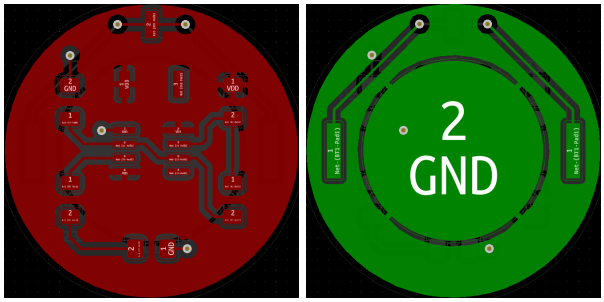


Figure 4: The schematic of the circuit in KiCad.

Design



(a) The front copper layer (b) The back copper layer

Figure 5: The PCB design

For the PCB design, the 7555 timer was placed exactly in the middle of the circular cut-out. A circular shape was chosen to fit the contour of the 2032 cell battery, and both the top and bottom layers were plated with a power and ground plane, respectively.

Summary

Results

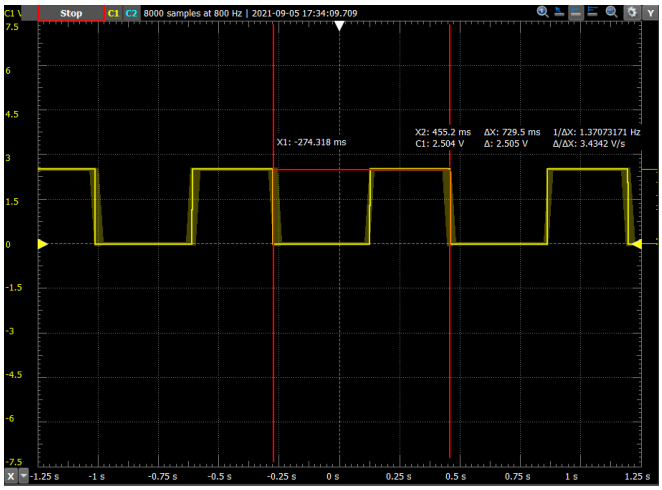


Figure 6: The output frequency using the AD2.

An AD2 was used to measure the waveform after the parts were soldered. The output frequency measured around 1.36 HZ, a little lower than the calculated frequency.

What was Learned

- Basic PCB structure.
- Creating custom footprints via a data sheet.
- Creating custom symbols for chips.
- PCB layout and design in KiCad.
- Trace width and other sizing constraints.

Sources

- https://en.wikipedia.org/wiki/555_timer_IC
- https://www.renesas.com/us/en/document/dst/icm7555-icm7556-datasheet
- https://www.youtube.com/c/contextualelectronics