Asynchronous FIFO report

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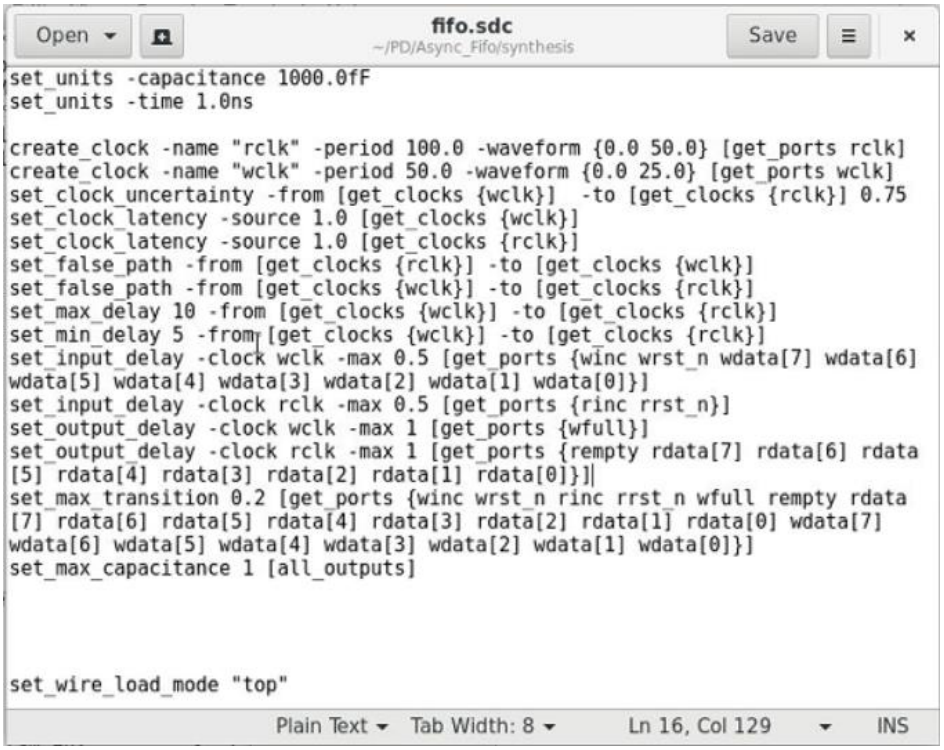
Task not applicable in genus for FIFO

- Generated clock definition
- Virtual clock
- Half cycle path
- Multicycle path
- Disable timing arcs
- Case analysis

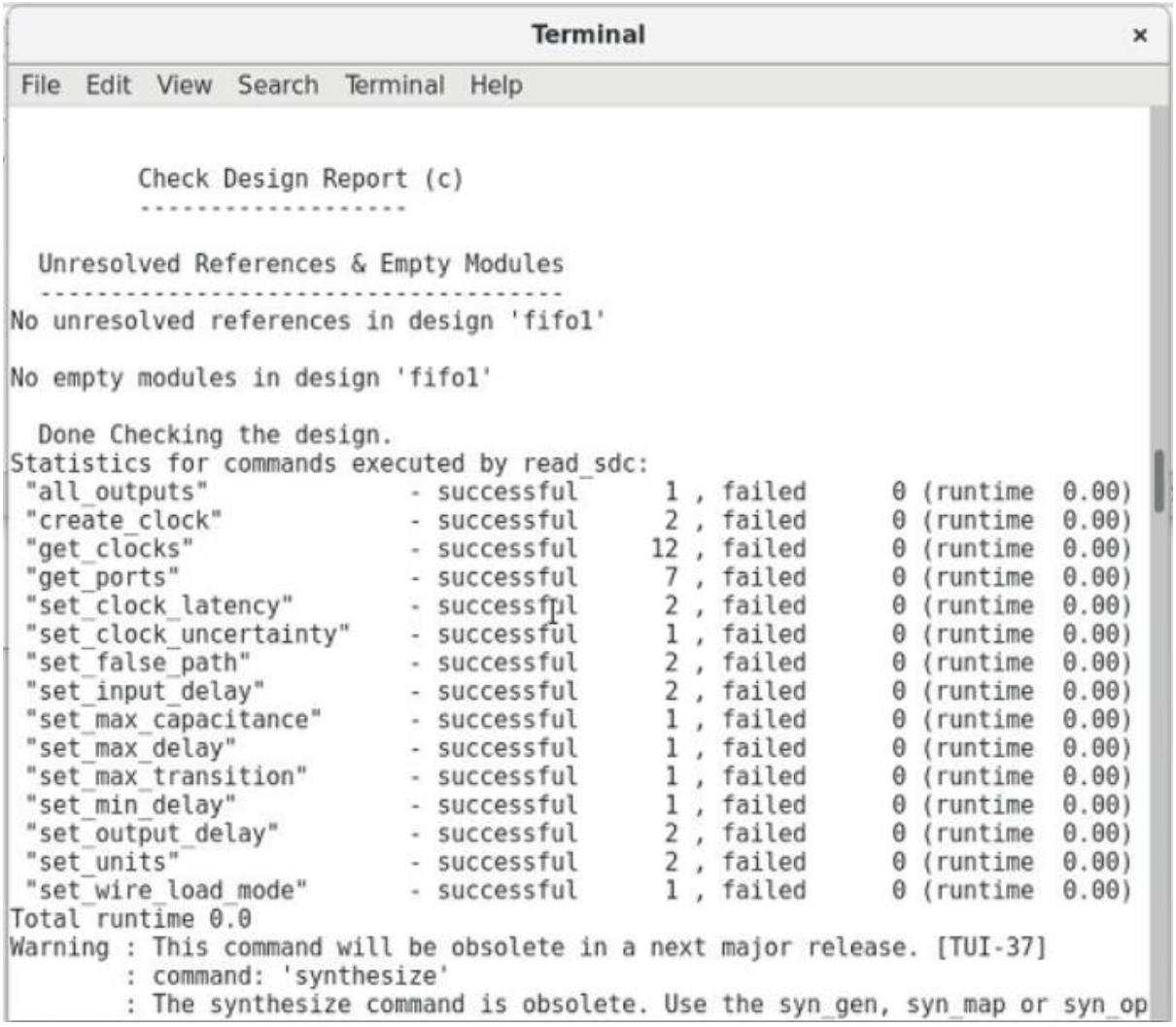
Task done

- Create clock definition
- Input delay
- Output delay
- Max delay
- Min delay
- Max transition
- Max capacitance
- Clock latency
- Clock uncertainty
- False path

SDC file



TCL file


Terminal
File Edit View Search Terminal Help
Check Design Report (c)
Unresolved References & Empty Modules
No unresolved references in design 'fifo1'
No empty modules in design 'fifo1'
Done Checking the design.
Statistics for commands executed by read_sdc:
"all_outputs" - successful 1 , failed 0 (runtime 0.00)
"create_clock" - successful 2 , failed 0 (runtime 0.00)
"get_clocks" - successful 12 , failed 0 (runtime 0.00)
"get_ports" - successful 7 , failed 0 (runtime 0.00)
"set_clock_latency" - successful 2 , failed 0 (runtime 0.00)
"set_clock_uncertainty" - successful 1 , failed 0 (runtime 0.00)
"set_false_path" - successful 2 , failed 0 (runtime 0.00)
"set_input_delay" - successful 2 , failed 0 (runtime 0.00)
"set_max_capacitance" - successful 1 , failed 0 (runtime 0.00)
"set_max_delay" - successful 1 , failed 0 (runtime 0.00)
"set_max_transition" - successful 1 , failed 0 (runtime 0.00)
"set_min_delay" - successful 1 , failed 0 (runtime 0.00)
"set_output_delay" - successful 2 , failed 0 (runtime 0.00)
"set_units" - successful 2 , failed 0 (runtime 0.00)
"set_wire_load_mode" - successful 1 , failed 0 (runtime 0.00)
Total runtime 0.0
Warning : This command will be obsolete in a next major release. [TUI-37]
: command: 'synthesize'
: The synthesize command is obsolete. Use the syn_gen, syn_map or syn_op

Sanity check

check_design

```
No LEF file read in.

        Check Design Report (c)
        -----------------------
Summary
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             Name                                Total
-------------------------------------------------------
Unresolved References                                0
Empty Modules                                        0
Unloaded Port(s)                                     0
Unloaded Sequential Pin(s)                           0
Unloaded Combinational Pin(s)                        0
Assigns                                              0
Undriven Port(s)                                     0
Undriven Leaf Pin(s)                                 0
Undriven hierarchical pin(s)                         0
Multidriven Port(s)                                  0
Multidriven Leaf Pin(s)                              0
Multidriven hierarchical Pin(s)                      0
Multidriven unloaded net(s)                          0
Constant Port(s)                                     0
Constant Leaf Pin(s)                                 0
Constant hierarchical Pin(s)                         0
Preserved leaf instance(s)                           0
Preserved hierarchical instance(s)                   0
Feedthrough Modules(s)                               0
Libcells with no LEF cell                            0
Physical (LEF) cells with no libcell                 0
Subdesigns with long module name                     0
Physical only instance(s)                            0
Logical only instance(s)                           339
```

report timing

```
legacy_genus:/> report timing
Warning : Timing problems have been detected in this design. [TIM-11]
        : The design is 'fifo1'.
        : Use 'check_timing_intent' or 'report timing -lint' to report more information.
============================================================
  Generated by:           Genus(TM) Synthesis Solution 19.12-s121_1
  Generated on:           Feb 01 2022  08:20:45 pm
  Module:                 fifo1
  Technology library:     uk65lscllmvbbr_100c25_tc
  Operating conditions:   uk65lscllmvbbr_100c25_tc (balanced_tree)
  Wireload mode:          top
  Area mode:              timing library
============================================================

       Pin                Type      Fanout Load Slew Delay Arrival
                                          (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------------
(clock wclk)            launch                              0 R
                        latency                  +1000    1000 R
(fifo.sdc_line_13)      ext delay                 +500    1500 R
winc                    in port          5  6.1    0    +0    1500 R
wptr_full/winc
  g154/B                                                +0    1500
  g154/Z                ND2B1M2R         3  2.8   54   +36    1536 F
  g153/NA                                               +0    1536
  g153/Z                ND2B1M2R         3  2.8   57   +97    1632 F
  g151/NA                                               +0    1632
  g151/Z                ND2B1M2R         3  2.8   57   +98    1730 F
  g149/NA                                               +0    1730
  g149/Z                ND2B1M2R         3  2.8   57   +98    1828 F
  g145/NA                                               +0    1828
  g145/Z                ND2B1M2R         2  2.0   49   +92    1920 F
  g140/B1                                               +0    1920
  g140/Z                MOAI22M2RA       3  4.8   89  +137    2057 F
  g138/A                                                +0    2057
  g138/Z                XOR2M2RA         3  3.8   48  +106    2164 F
  g175/A                                                +0    2164
  g175/Z                CKND2M2R         1  1.2   30   +37    2201 R
  g165/B                                                +0    2201
  g165/Z                OAI211M2R        1  1.2   56   +47    2248 F
  g164/D                                                +0    2248
  g164/Z                NR4M1R           1  1.3  119   +84    2332 R
  wfull_reg/D      <<<  DFQRM2RA                       +0    2332
  wfull_reg/CK          setup                  0      +58    2391 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock wclk)            capture                            50000 R
                        latency                  +1000    51000 R
-------------------------------------------------------------------
Cost Group   : 'wclk' (path_group 'wclk')
Timing slack :   48609ps
Start-point  : winc
End-point    : wptr_full/wfull_reg/D
```

report design_rules

```
legacy_genus:/> report design_rules
================================================================
  Generated by:           Genus(TM) Synthesis Solution 19.12-s121_1
  Generated on:           Feb 01 2022  08:22:21 pm
  Module:                 fifo1
  Technology library:     uk65lscllmvbbr_100c25_tc
  Operating conditions:   uk65lscllmvbbr_100c25_tc (balanced_tree)
  Wireload mode:          top
  Area mode:              timing library
================================================================

Max_transition design rule: no violations.


Max_capacitance design rule: no violations.


Max_fanout design rule: no constraints.
```

Note: Generated files from genus are provided in the below github link

https://github.com/rjoshi30/Assign1_EEN212022.git