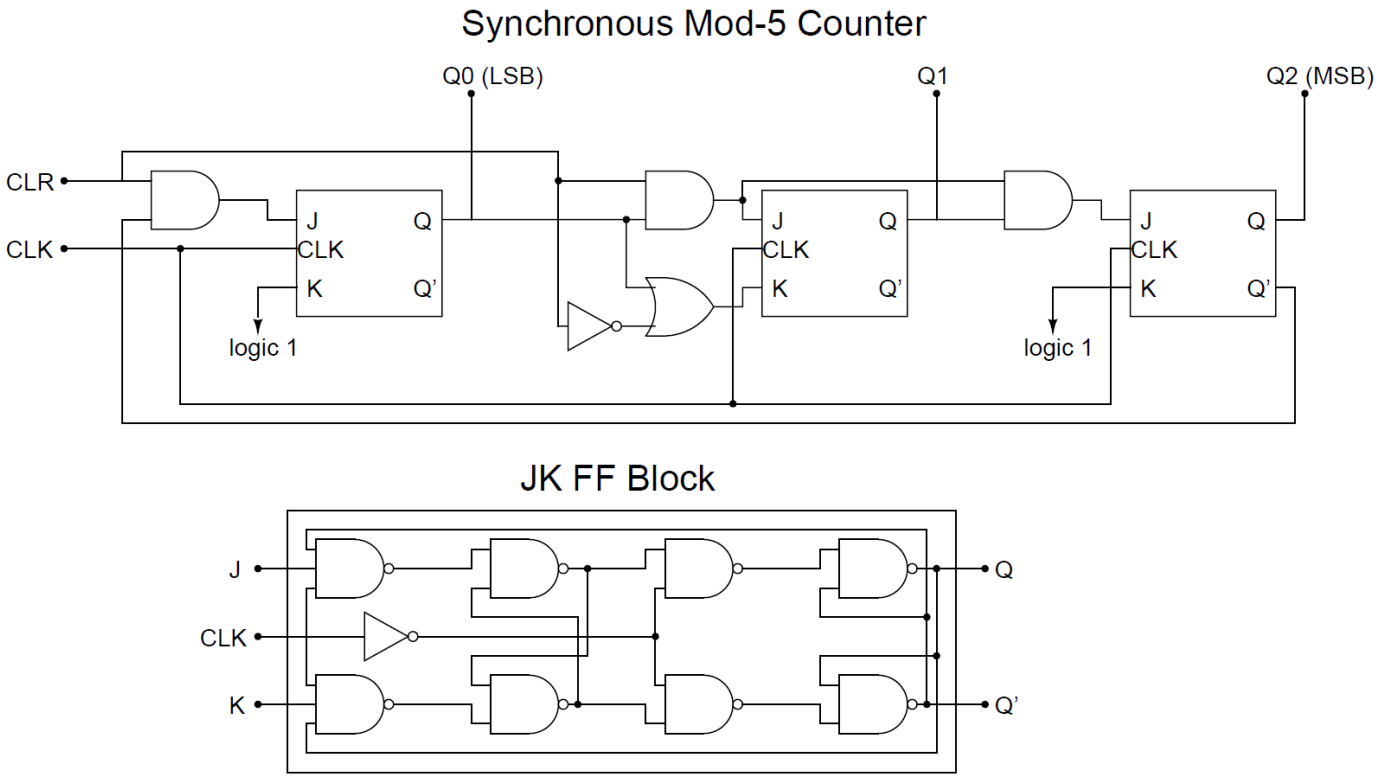
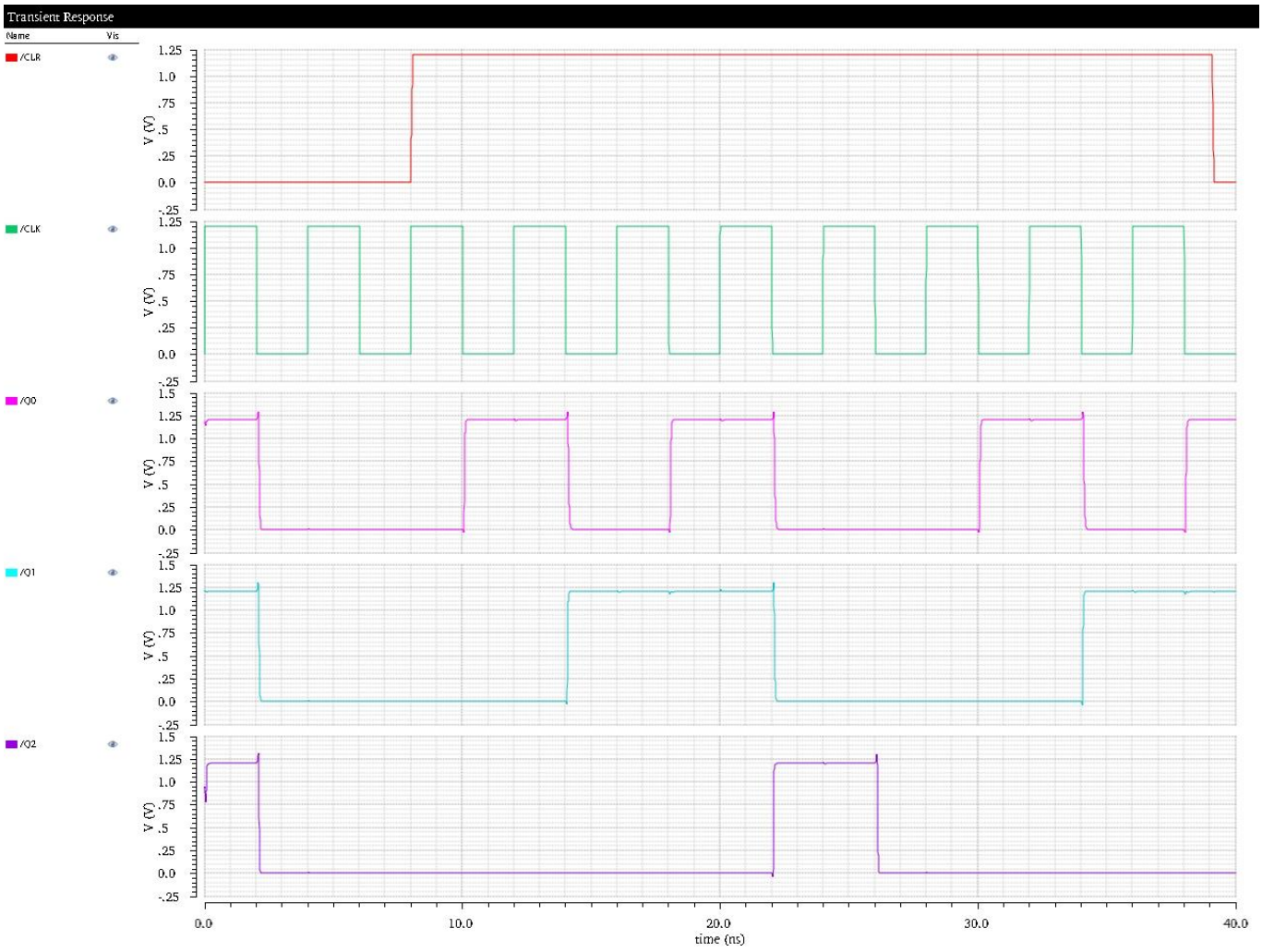
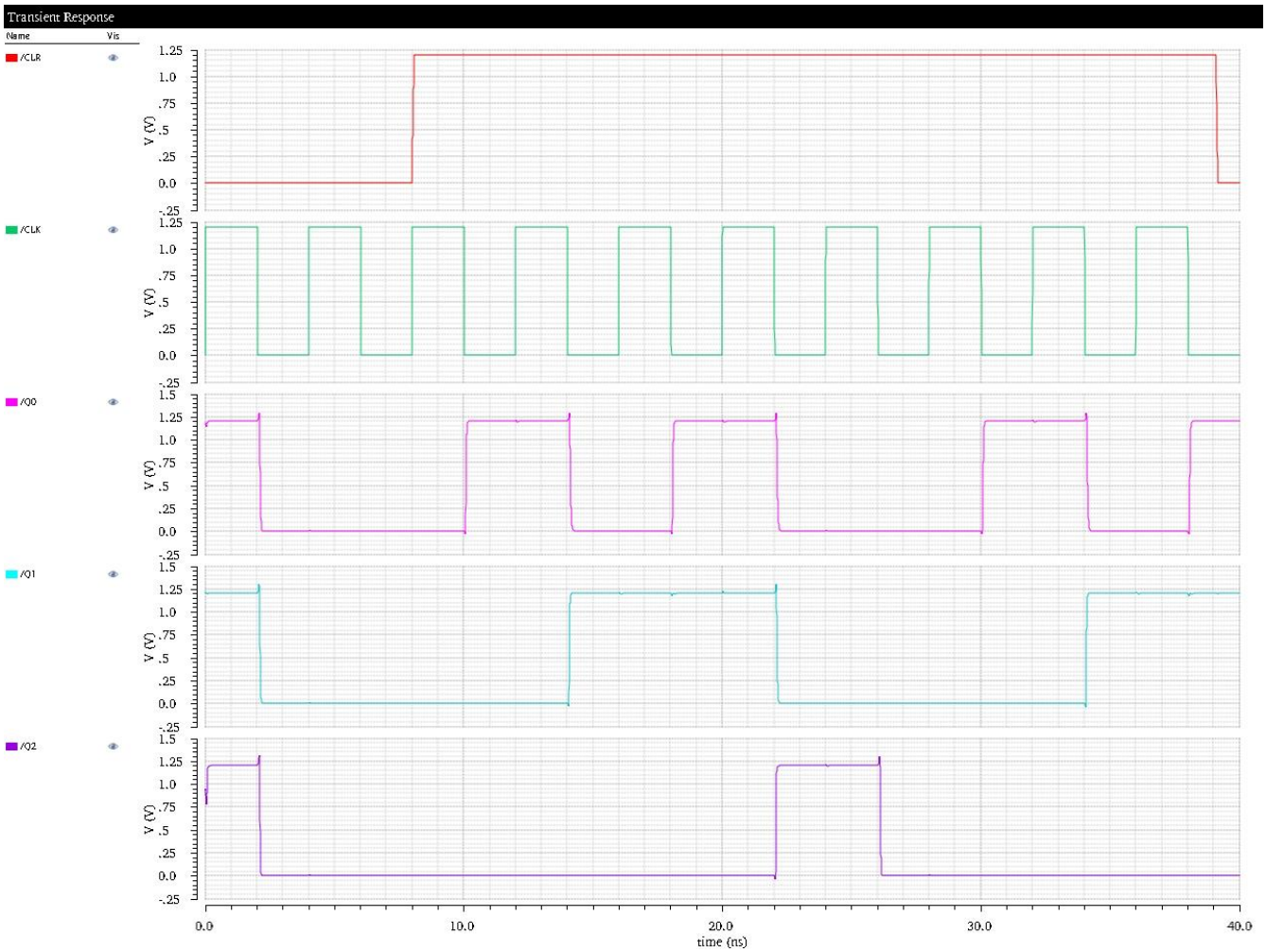
Counter Schematic



Counter schematic simulation



Counter post layout simulation



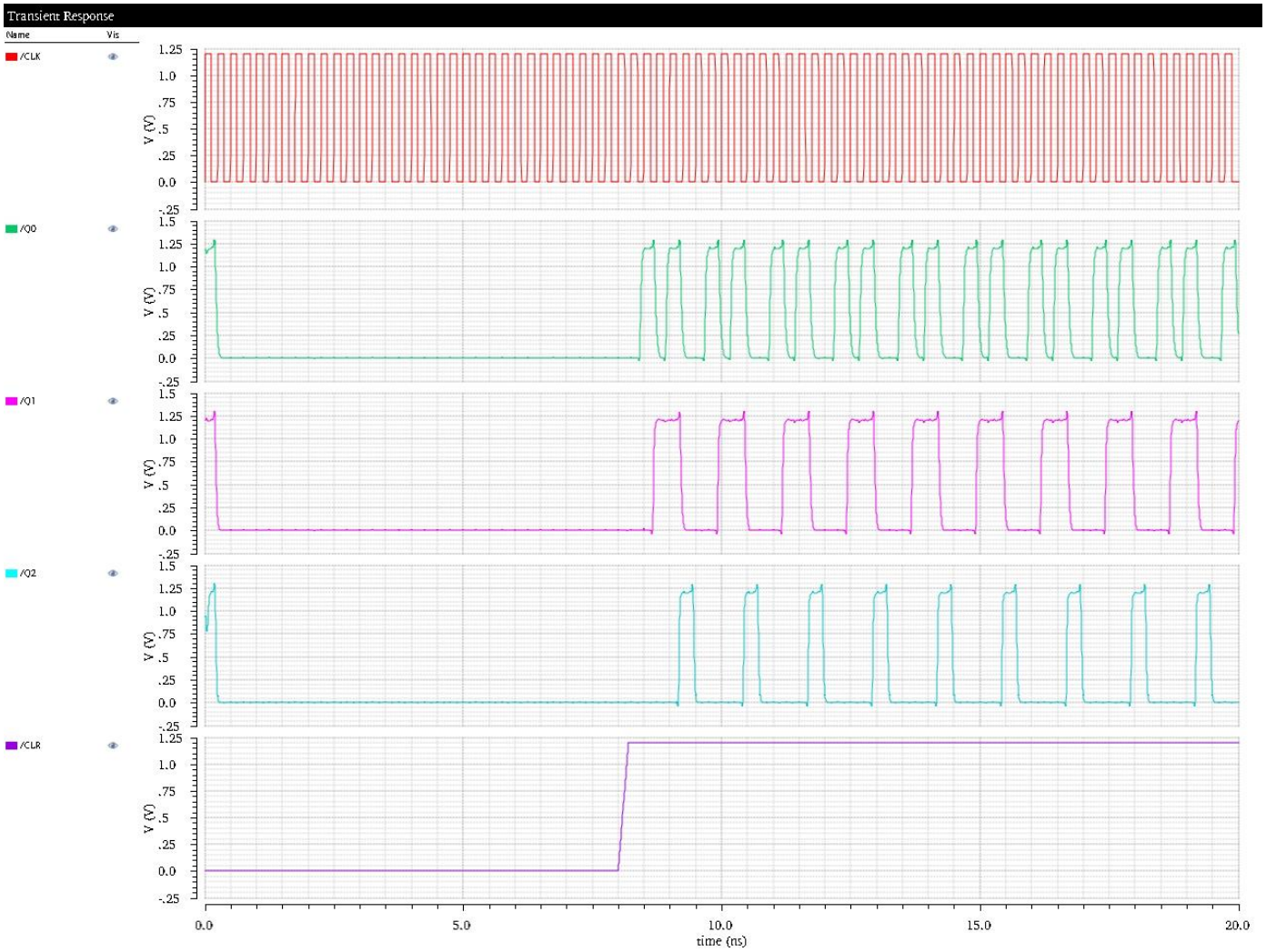
Timing analysis:

Rise time = 46.94ps

Fall time = 68.46ps

Maximum frequency of operation is around 4 GHz

Counter simulation @ clock frequency of 4 GHz



Achieved targets:

- Final height and width of cell are 1.4um and 42.2 um respectively.
- Counter is working properly for the clock frequency of 250 MHz
- DRC (except 2) and LVS errors are cleared.

Unachieved targets:

- Two of the DRC errors (one due to low poly density and other due to low Al density) are not cleared as the design requirements of poly and Al was less than the specified value.