

## Synchronous Mod 5 Counter

### Verilog code

```
'timescale 1ns / 1ps
// Company:
// Engineer:
//
// Create Date: 13.10.2021 10:29:45
// Design Name:
// Module Name: Mod5Counter
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////

module Mod5Counter(out,clk,clr);
    output [2:0] out;
    input clk,clr;
    reg [2:0] out;

    always @(posedge clk or negedge clr)
    begin
        if(!clr)
            out<=3'b000;
        else if(out<4)
            out<=out+1;
        else
            out<=3'b000;
    end
endmodule
```

## Sdc file

```
1 set sdc_version 1.7
2
3
4
5 set_units -capacitance 1000fF
6 set_units -time 1000ps
7
8
9
10 # Set the current design
11 current_design counter
12
13
14
15 create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
16 set_clock_transition -rise 0.1 [get_clocks "clk"]
17 set_clock_transition -fall 0.1 [get_clocks "clk"]
18 set_clock_uncertainty 0.1 [get_ports "clk"]
19 #set_clock_uncertainty -setup 1 [get_ports "clk"]
20 #set_clock_uncertainty -hold 1 [get_ports "clk"]
21 #set_clock_gating_check -setup 0.0
22
23
24
25 set_input_delay -max 1.0 [get_ports "clr"] -clock [get_clocks "clk"]
26 set_output_delay -max 1.0 [get_ports "out"] -clock [get_clocks "clk"]
27
28
29
30 set_wire_load_mode "top"
```

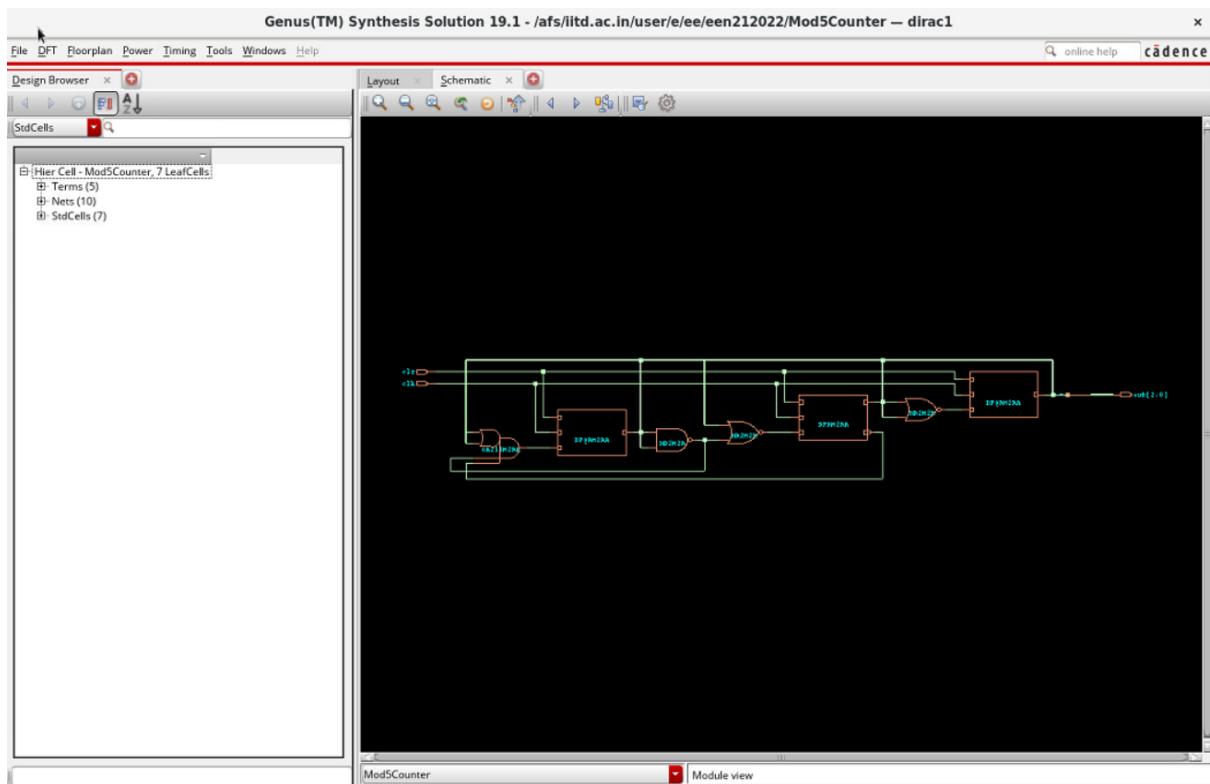
## TCL file

```
1 set search_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs"
2 set_attribute lib_search_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs/"
3 set_attribute hdl_search_path "./rtl/Mod5Counter.v"
4 set_attribute library "uk651sc1lmvbbr_100c25_tc_cos.lib"
5 set mylist [get_attribute init_hdl_search_path]
6 read_hdl -v2001 $mylist
7 elaborate
8 check_design -unresolved
9 read_sdc ./synthesis/counter.sdc
10 synthesize -to_mapped -effort high
11 write_hdl > counter_netlist.v
12 write_sdc > counter_sdc.sdc
```

## Synthesis

Terminal						
File	Edit	View	Search	Terminal		
drc_bufs	0	(	0 /	0 ) 0.00		
drc_fopt	0	(	0 /	0 ) 0.00		
drc_bufb	0	(	0 /	0 ) 0.00		
simple_buf	0	(	0 /	0 ) 0.00		
dup	0	(	0 /	0 ) 0.00		
crit_dnsz	0	(	0 /	0 ) 0.00		
crit_upsz	0	(	0 /	0 ) 0.00		
crit_slew	0	(	0 /	0 ) 0.00		
Trick	Calls	Accepts	Attempts	Time(secs)		
plc_st	0	(	0 /	0 ) 0.00		
plc_star	0	(	0 /	0 ) 0.00		
drc_bufs	0	(	0 /	0 ) 0.00		
drc_fopt	0	(	0 /	0 ) 0.00		
drc_bufb	0	(	0 /	0 ) 0.00		
simple_buf	0	(	0 /	0 ) 0.00		
dup	0	(	0 /	0 ) 0.00		
crit_dnsz	0	(	0 /	0 ) 0.00		
crit_upsz	0	(	0 /	0 ) 0.00		
Trick	Calls	Accepts	Attempts	Time(secs)		
plc_st	0	(	0 /	0 ) 0.00		
plc_star	0	(	0 /	0 ) 0.00		
drc_bufs	0	(	0 /	0 ) 0.00		
drc_fopt	0	(	0 /	0 ) 0.00		
drc_bufb	0	(	0 /	0 ) 0.00		
dup	0	(	0 /	0 ) 0.00		
crit_dnsz	0	(	0 /	0 ) 0.00		
crit_upsz	0	(	0 /	0 ) 0.00		
=====						
Stage : incr_opt						
=====						
Message Summary						
=====						
Id	Sev	Count	Message Text			
PA-7	Info	2	Resetting power analysis results. All computed switching activities are removed.			
SYNTH-5	Info	1	Done mapping.			
SYNTH-7	Info	1	Incrementally optimizing.			
Info : Done incrementally optimizing. [SYNTH-8]						
: Done incrementally optimizing 'Mod5Counter'.						
Finished SDC export (command execution time mm:ss (real) = 00:00).						

## Gate Level netlist



## Timing analysis

```
legacy_genus:/> report timing
Warning : Timing problems have been detected in this design. [TIM-11]
  : The design is 'Mod5Counter'.
  : Use 'check_timing_intent' or 'report timing -lint' to report more information.
=====
Generated by:          Genus(TM) Synthesis Solution 19.12-s121_1
Generated on:          Oct 17 2021 03:50:43 pm
Module:                Mod5Counter
Technology library:   uk65lscllmvbbr_100c25_tc
Operating conditions: uk65lscllmvbbr_100c25_tc (balanced_tree)
Wireload mode:         top
Area mode:             timing library
=====

      Pin          Type      Fanout Load Slew Delay Arrival
                           (fF)  (ps)  (ps)  (ps)
-----+-----+-----+-----+-----+-----+-----+-----+
(clock clk)          launch          0      0      0      R
out_reg[2]/CK        DFRM2RA      3    2.9    33    +212    212  F
out_reg[2]/0          <<<  interconnect    33      +0      212  F
out[2]                out port          +0      212  F
(counter.sdc_line_6) ext delay        +1000   1212  F
-----+-----+-----+-----+-----+-----+-----+-----+
(clock clk)          capture        10000  R
uncertainty          uncertainty    -100    9900  R
-----+-----+-----+-----+-----+-----+-----+-----+
Cost Group : 'clk' (path_group 'clk')
Timing slack : 8688ps
Start-point : out_reg[2]/CK
End-point   : out[2]
```

## Power analysis

```
Terminal
File Edit View Search Terminal Help
Timing slack : 8788ps
Start-point : out_reg[2]/CK
End-point : out[2]

legacy_genus:/> report power
Info  : Joules engine is used. [RPT-16]
      : Joules engine is being used for the command report_power.
Info  : ACTP-0001 [ACTPInfo] Activity propagation started for stim#0 netlist
      : Mod5Counter
Info  : ACTP-0009 [ACTPInfo] Activity Propagation Progress Report : 100%
Info  : ACTP-0001 Activity propagation ended for stim#0
Info  : PWRA-0001 [PwrInfo] compute_power effective options
      : -mode : vectorless
      : -skip_propagation : 1
      : -frequency_scaling_factor : 1.0
      : -use_clock_freq : stim
      : -compat : voltus
      : -stim :/stim#0
      : -fromGenus : 1
Info  : ACTP-0001 Timing initialization started
Info  : ACTP-0001 Timing initialization ended
Info  : PWRA-0002 [PwrInfo] Skipping activity propagation due to -skip_ap
      : option....
Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for vectorless
      : flow. Ignoring frequency scaling.
Info  : PWRA-0002 Voltus compat mode is set for power analysis.
Warning: PWRA-0304 [PwrWarn] -stim option is not applicable with vectorless mode
      : of power analysis, ignored this option.
Info  : PWRA-0002 Started 'vectorless' power computation.
Info  : PWRA-0002 Finished power computation.
Info  : PWRA-0007 [PwrInfo] Completed successfully.
      : Info=9, Warn=2, Error=0, Fatal=0
Instance: /Mod5Counter
Power Unit: W
PDB Frames: /stim#0/frame#0

-----  

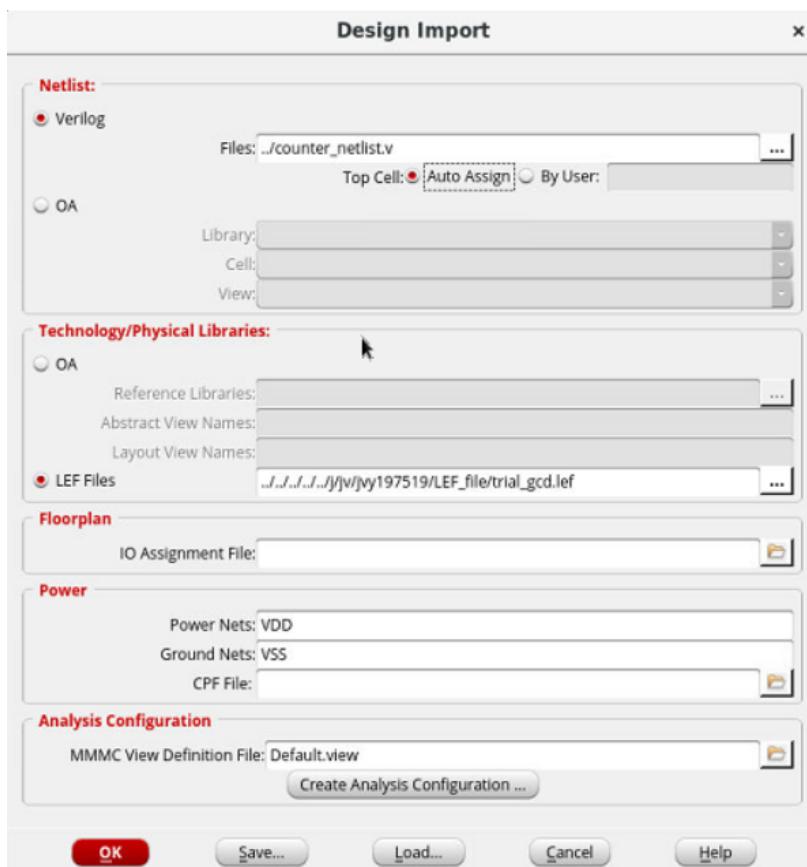
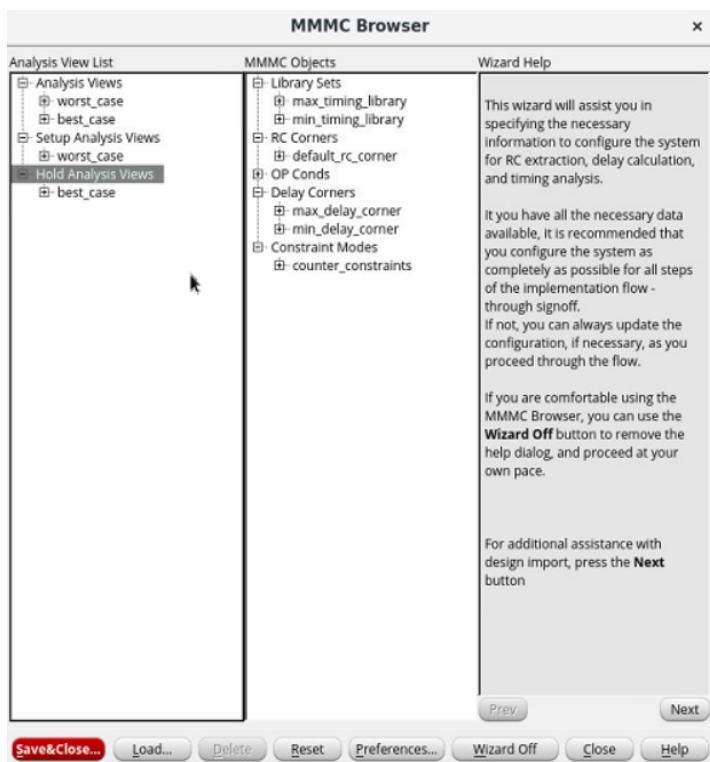
Category      Leakage      Internal I      Switching      Total      Row%
-----  

  memory      0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
  register    1.05184e-09  1.92333e-06  6.45773e-08  1.98896e-06  83.93%
  latch       0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
  logic       2.83578e-10  9.29104e-08  5.76737e-08  1.50868e-07  6.37%
  bbox        0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
  clock       0.00000e+00  0.00000e+00  2.30000e-07  2.30000e-07  9.71%
  pad         0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
  pm          0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
-----  

  Subtotal    1.33542e-09  2.01624e-06  3.52251e-07  2.36983e-06  100.01%
  Percentage  0.06%      85.08%      14.86%      100.00%  100.00%
-----  

legacy_genus:/>
```

## Physical design



Terminal

```

File Edit View Search Terminal Help
Completed (cpu: 0:00:07.8 real: 0:00:08.0)
Set Shrink Factor to 1.00000
Summary of Active RC-Corners :

Analysis View: worst_case
RC-Corner Name      : default_rc_corner
RC-Corner Index     : 0
RC-Corner Temperature : 25 Celsius
RC-Corner Cap Table  : ''
RC-Corner PreRoute Res Factor   : 1
RC-Corner PreRoute Cap Factor   : 1
RC-Corner PostRoute Res Factor  : 1 {1 1 1}
RC-Corner PostRoute Cap Factor  : 1 {1 1 1}
RC-Corner PostRoute XCap Factor : 1 {1 1 1}
RC-Corner PreRoute Clock Res Factor : 1 [Derived from postRoute_res (effortLevel low)]
RC-Corner PreRoute Clock Cap Factor : 1 [Derived from postRoute_cap (effortLevel low)]
RC-Corner PostRoute Clock Cap Factor : 1 {1 1 1} [Derived from postRoute_cap (effortLevel low)]
RC-Corner PostRoute Clock Res Factor : 1 {1 1 1} [Derived from postRoute_res (effortLevel low)]
RC-Corner Technology file: '../../../../../service/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC000000A_B11/RuleDecks/QRC/RCmin/qrcTechFile'

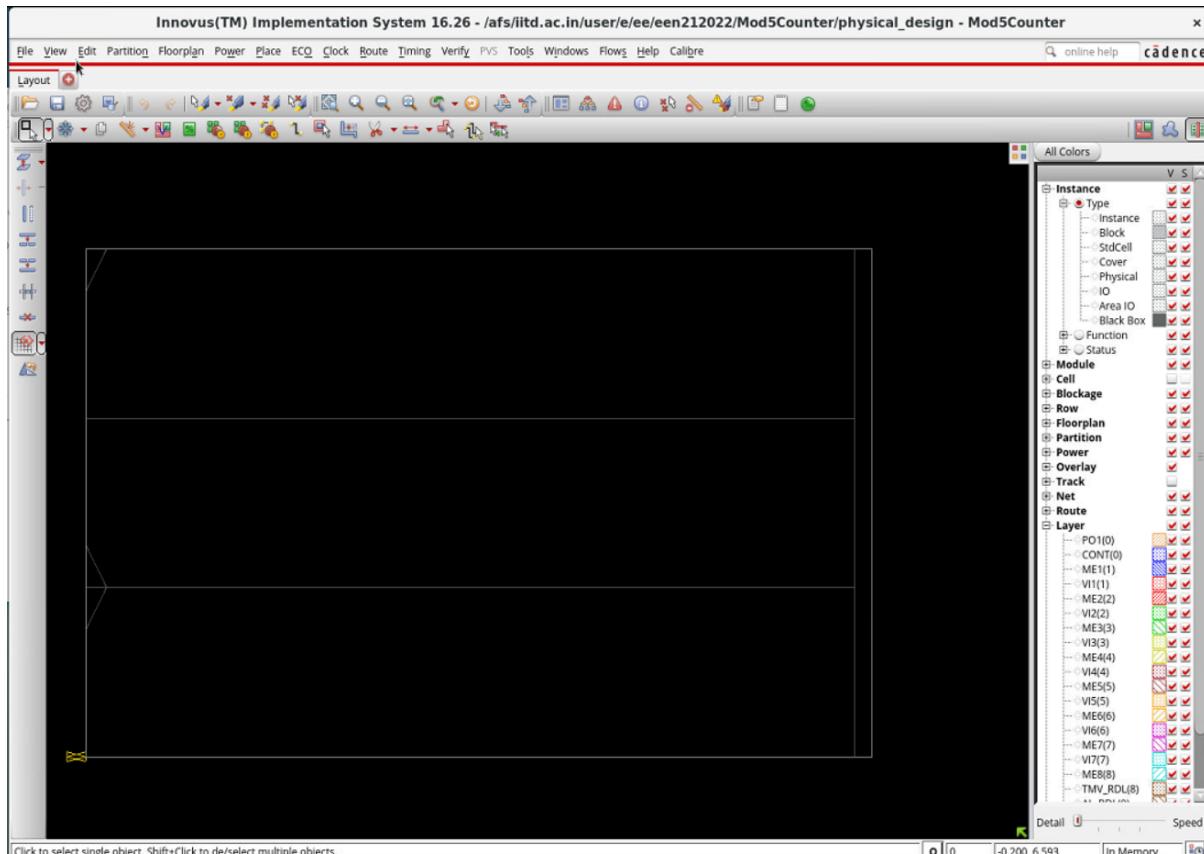
Analysis View: best_case
RC-Corner Name      : default_rc_corner
RC-Corner Index     : 0
RC-Corner Temperature : 25 Celsius
RC-Corner Cap Table  : ''
RC-Corner PreRoute Res Factor   : 1
RC-Corner PreRoute Cap Factor   : 1
RC-Corner PostRoute Res Factor  : 1 {1 1 1}
RC-Corner PostRoute Cap Factor  : 1 {1 1 1}
RC-Corner PostRoute XCap Factor : 1 {1 1 1}
RC-Corner PreRoute Clock Res Factor : 1 [Derived from postRoute_res (effortLevel low)]
RC-Corner PreRoute Clock Cap Factor : 1 [Derived from postRoute_cap (effortLevel low)]
RC-Corner PostRoute Clock Cap Factor : 1 {1 1 1} [Derived from postRoute_cap (effortLevel low)]
RC-Corner PostRoute Clock Res Factor : 1 {1 1 1} [Derived from postRoute_res (effortLevel low)]
RC-Corner Technology file: '../../../../../service/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC000000A_B11/RuleDecks/QRC/RCmin/qrcTechFile'

Default value for postRoute extraction mode's effortLevel (-effortLevel option of setExtractRCMode) changed to 'medium'.

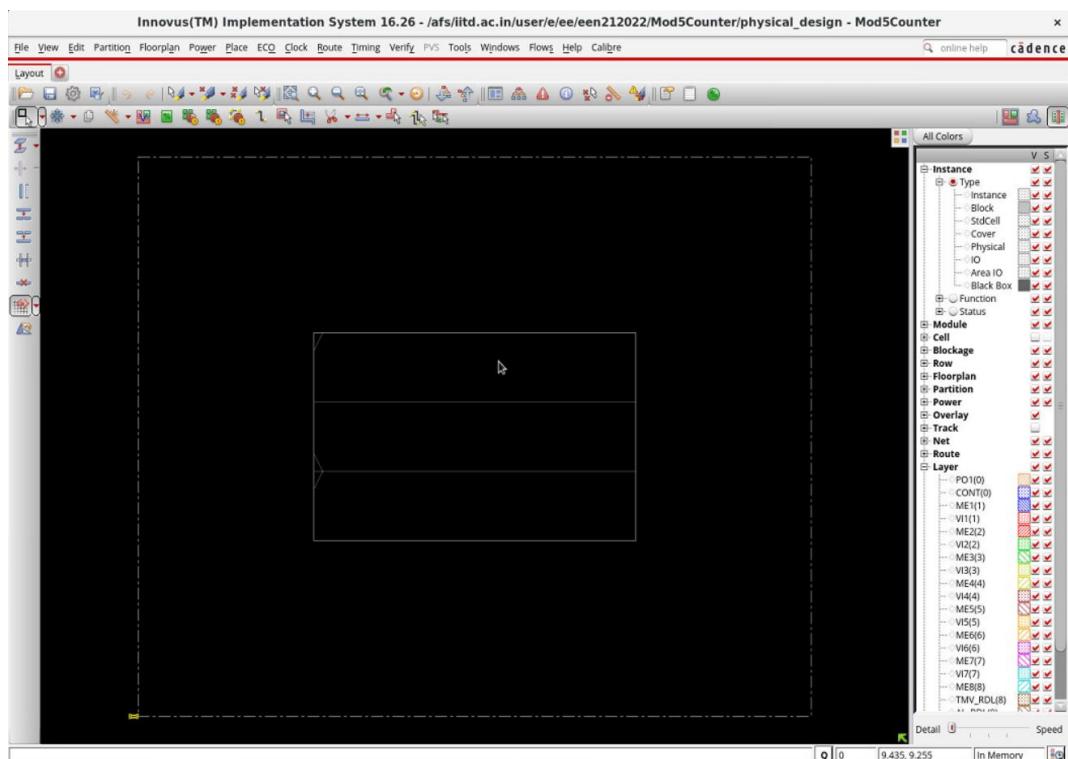
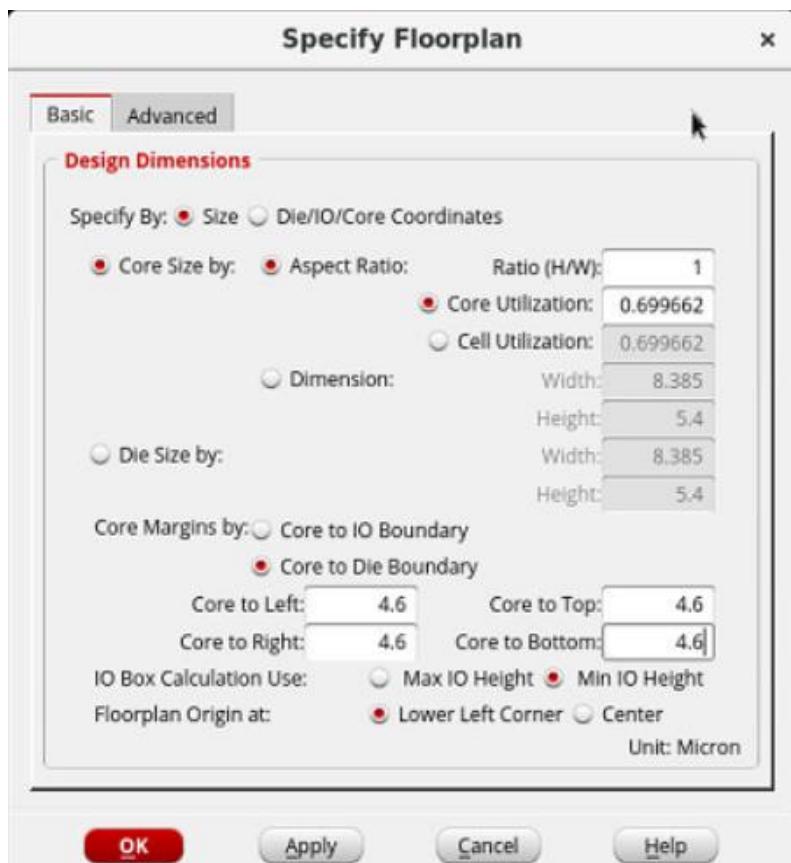
*** Summary of all messages that are not suppressed in this session:
Severity ID      Count Summary
WARNING IMPLF-200 1 Pin '%s' in macro '%s' has no ANTENNAGAT...
WARNING IMPLF-108 1 There is no overlap layer defined in any...
WARNING IMPVL-159 2154 Pin '%s' of cell '%s' is defined in LEF ...
WARNING TCLCMD-1025 2 Option value '%s' for command %s is obso...
WARNING TECHLIB-302 20 No function defined for cell '%s'. The c...
WARNING TECHLIB-436 20 Attribute '%s' on '%s' pin '%s' of cell ...
WARNING TECHLIB-1365 20 The %s vector group for %s has a duplica...
*** Message Summary: 2218 warning(s), 0 error(s)

innovus 1> 

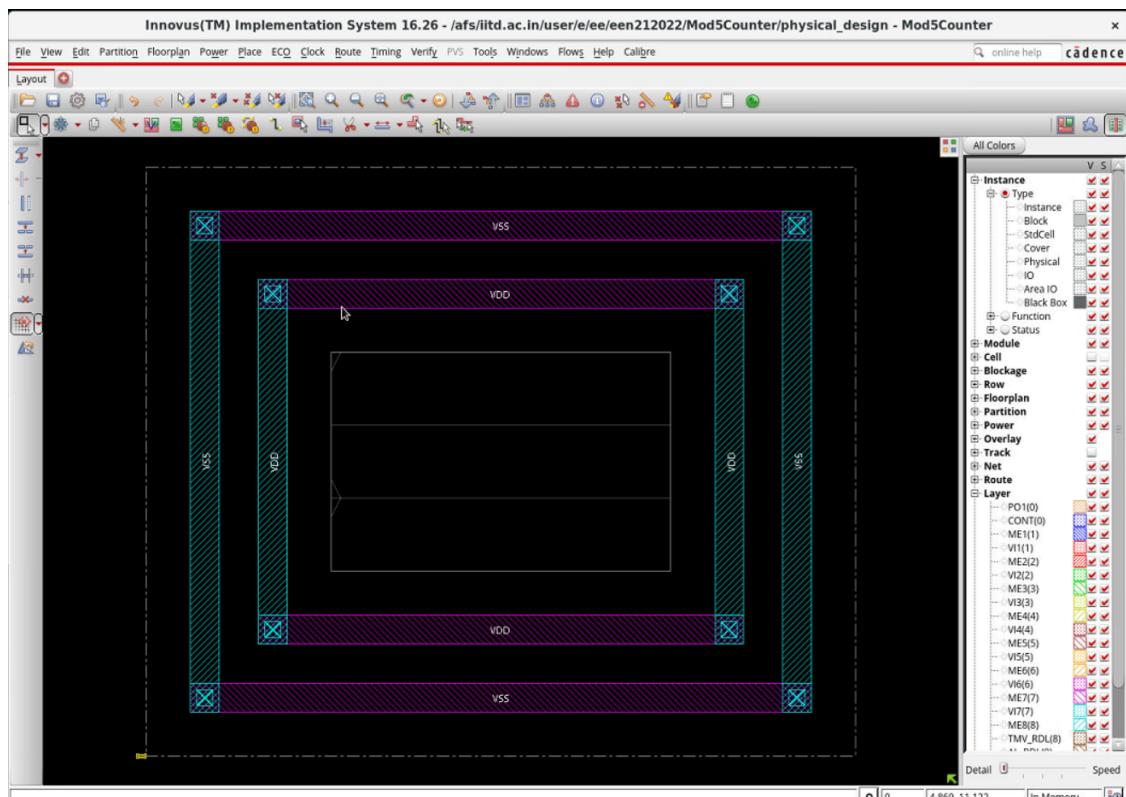
```



## Floor Planning



## Power Planning



Terminal

File Edit View Search Terminal Help

```

RC-Corner PostRoute Clock Res Factor : 1 {1 1 1} [Derived from postRoute_res (effortLevel low)]
RC-Corner Technology file: '../../../../../service/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC000000A_B11/RuleDecks/QRC/RCmin/qrcTechFile'

Analysis View: best_case
RC-Corner Name      : default_rc_corner
RC-Corner Index     : 0
RC-Corner Temperature : 25 Celsius
RC-Corner Cap Table : ''
RC-Corner PreRoute Res Factor      : 1
RC-Corner PreRoute Cap Factor     : 1
RC-Corner PostRoute Res Factor    : 1 {1 1 1}
RC-Corner PostRoute Cap Factor   : 1 {1 1 1}
RC-Corner PostRoute XCap Factor  : 1 {1 1 1}
RC-Corner PreRoute Clock Res Factor : 1 [Derived from postRoute_res (effortLevel low)]
RC-Corner PreRoute Clock Cap Factor : 1 [Derived from postRoute_cap (effortLevel low)]
RC-Corner PostRoute Clock Cap Factor : 1 {1 1 1} [Derived from postRoute_cap (effortLevel low)]
RC-Corner PostRoute Clock Res Factor : 1 {1 1 1} [Derived from postRoute_res (effortLevel low)]
RC-Corner Technology file: '../../../../../service/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC000000A_B11/RuleDecks/QRC/RCmin/qrcTechFile'
Default value for postRoute extraction mode's effortLevel (-effortLevel option of setExtractRCMode) changed to 'medium'.

*** Summary of all messages that are not suppressed in this session:  I
Severity ID      Count  Summary
WARNING  IMPLF-200      1  Pin '%s' in macro '%s' has no ANTENNAGAT...
WARNING  IMPLF-108      1  There is no overlap layer defined in any...
WARNING  IMPVL-159     2154  Pin '%s' of cell '%s' is defined in LEF ...
WARNING  TCLCMD-1925     2  Option value '%s' for command %s is obso...
WARNING  TECHLIB-302     20  No function defined for cell '%s'. The c...
WARNING  TECHLIB-436     20  Attribute '%s' on '%s' pin '%s' of cell ...
WARNING  TECHLIB-1365    20  The %s vector group for %s has a duplica...
*** Message Summary: 2218 warning(s), 0 error(s)

innovus 1> Adjusting core size to PlacementGrid : width :8.4 height : 5.4
innovus 1> The ring targets are set to core/block ring wires.
addRing command will consider rows while creating rings.
addRing command will disallow rings to go over rows.
addRing command will ignore shorts while creating rings.

Ring generation is complete.
vias are now being generated.
addRing created 8 wires.
ViaGen created 8 vias, deleted 0 via to avoid violation.
+-----+-----+-----+
|  Layer |  Created |  Deleted |
+-----+-----+-----+
|    ME7 |      4 |     NA |
|    VI7 |      8 |      0 |
|    ME8 |      4 |     NA |
+-----+-----+-----+
innovus 1> 
```

## Add Stripes

Basic Advanced Via Generation Mode Preview

### Set Configuration

Net(s): VDD VSS



Layer: ME6(6) Directions:  Vertical  Horizontal

Width: 0.3

Spacing: 0.4

Update

### Set Pattern

Set-to-set distance: 2.5  Number of sets: 1  Bumps  Over:

Over P/G pins Pin layer:   Pin Width:

Master name:   Selected blocks  All blocks

Over Physical Pins Pin layer:   Pin Width:

### Stripe Boundary

Core ring  Pad ring:   All domains

Design boundary  Create pins  Each selected block/domain/fence

Specify rectangular area

X1:  Y1:  X2:  Y2:

Specify rectilinear area

### First/Last Stripe

Start from:  Left  Right  Top  Bottom

Relative from core or selected area Start:  Stop:

Absolute Start:   Stop:

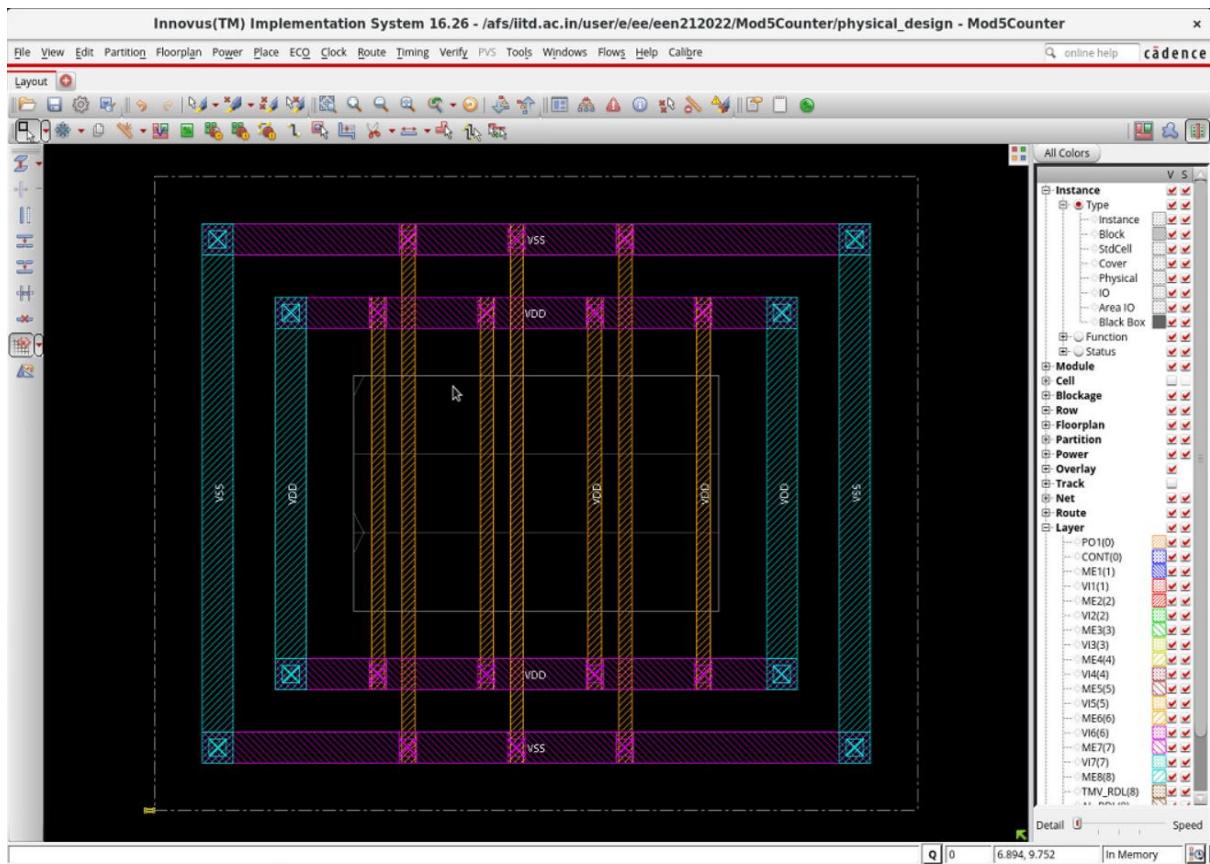
OK

Apply

Defaults

Cancel

Help



```

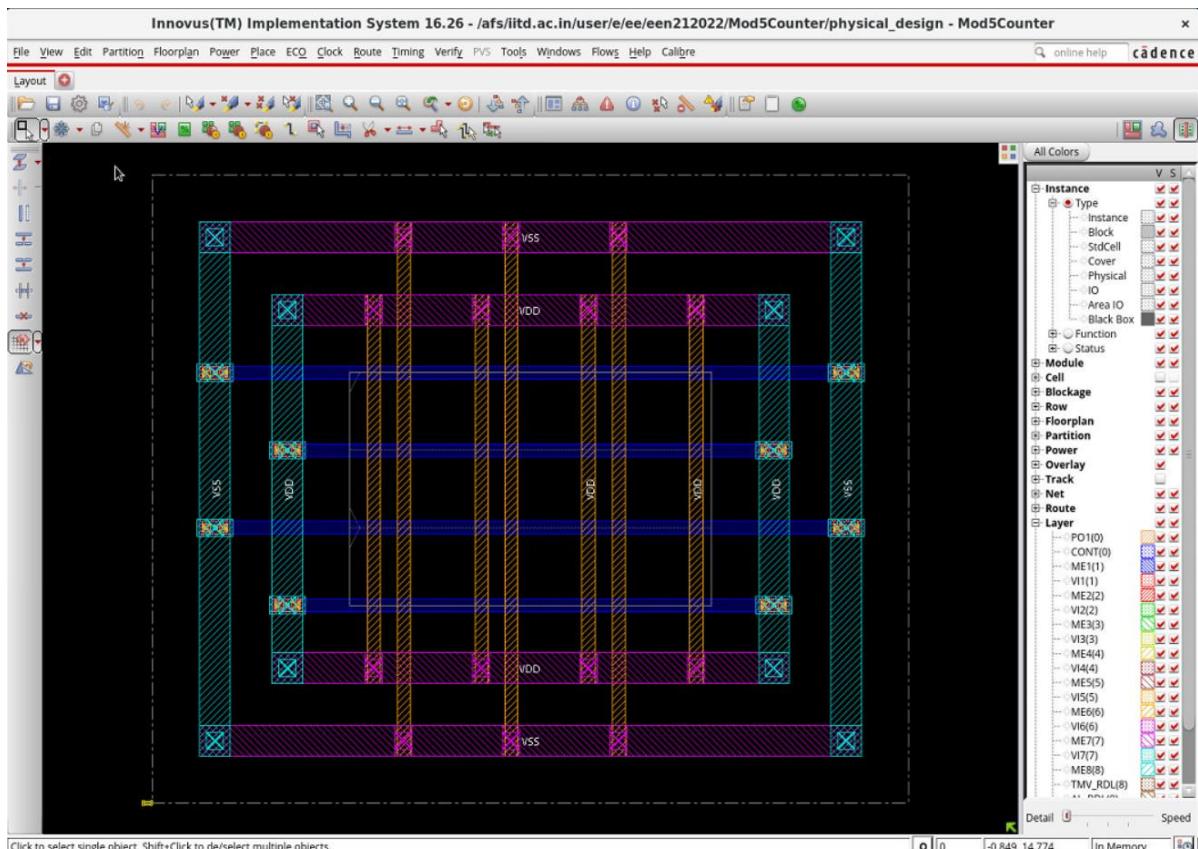
Terminal
File Edit View Search Terminal Help
WARNING TCLCMD-1025      2 Option value '%s' for command %s is obso...
WARNING TECHLIB-302        20 No function defined for cell '%s'. The c...
WARNING TECHLIB-436        20 Attribute '%s' on '%s' pin '%s' of cell ...
WARNING TECHLIB-1365       20 The %s vector group for %s has a duplica...
*** Message Summary: 2218 warning(s), 0 error(s)

innovus l> Adjusting core size to PlacementGrid : width :8.4 height : 5.4
innovus l> The ring targets are set to core/block ring wires.
addRing command will consider rows while creating rings.
addRing command will disallow rings to go over rows.
addRing command will ignore shorts while creating rings.

Ring generation is complete.
vias are now being generated.
addRing created 8 wires.
ViaGen created 8 vias, deleted 0 via to avoid violation.
+---+---+---+
| Layer | Created | Deleted |
+---+---+---+
| ME7 | 4 | NA |
| V17 | 8 | 0 |
| ME8 | 4 | NA |
+---+---+---+
innovus l> addStripe will allow jog to connect padcore ring and block ring.
Stripes will stop at the boundary of the specified area.
When breaking rings, the power planner will consider the existence of blocks.
Stripes will not extend to closest target.
The power planner will set stripe antenna targets to none (no trimming allowed).
Stripes will not be created over regions without power planning wires.
The entire stripe set will break at the domain if one of the nets is not in the domain.
addStripe will break automatically at non-default domains when generating global stripes over the core area or default domain.
AddStripe segment minimum length set to 1
Offset for stripe breaking is set to 0.

**WARN: (IMPPP-193): The currently specified spacing 0.4000 in -spacing option might create min enclosed area violation. The required min enclosed area for layer ME6 is 0.3100. If violation happens, increase the spacing to around 0.6068. The recommended spacing is the square root of min enclosure area.
Starting stripe generation ...
Non-Default Mode Option Settings :
NONE
Stripe generation is complete.
vias are now being generated.
addStripe created 7 wires.
ViaGen created 14 vias, deleted 0 via to avoid violation.
+---+---+---+
| Layer | Created | Deleted |
+---+---+---+
| ME6 | 7 | NA |
| VI6 | 14 | 0 |
+---+---+---+
innovus l>

```



Terminal

File Edit View Search Terminal Help

Begin power routing ...

\*\*WARN: (IMPSR-554): The specified top target layer is beyond top routing layer. Set top target layer to 8.

\*\*WARN: (IMPSR-1253): Cannot find any standard cell pin connected to net VDD.

Run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as 'USE POWER' or 'USE GROUND'.

\*\*WARN: (IMPSR-1253): Cannot find any standard cell pin connected to net VSS.

Run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as 'USE POWER' or 'USE GROUND'.

\*\*WARN: (IMPSR-468): Cannot find any standard cell pin connected to net VDD.

Use setRouteMode -corePinReferenceMacro <standard cell> to specify a reference macro for followpin connection, or run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as "USE POWER" or "USE GROUND".

\*\*WARN: (IMPSR-468): Cannot find any standard cell pin connected to net VSS.

Use setRouteMode -corePinReferenceMacro <standard cell> to specify a reference macro for followpin connection, or run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as "USE POWER" or "USE GROUND".

CPU time for FollowPin 0 seconds

\*\*WARN: (IMPSR-468): Cannot find any standard cell pin connected to net VSS.

Use setRouteMode -corePinReferenceMacro <standard cell> to specify a reference macro for followpin connection, or run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as "USE POWER" or "USE GROUND".

\*\*WARN: (IMPSR-468): Cannot find any standard cell pin connected to net VSS.

Use setRouteMode -corePinReferenceMacro <standard cell> to specify a reference macro for followpin connection, or run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as "USE POWER" or "USE GROUND".

CPU time for FollowPin 0 seconds

Number of Core ports routed: 8

Number of Followpin connections: 4

End power routing: cpu: 0:00:00, real: 0:00:00, peak: 2033.00 megs.

Begin updating DB with routing results ...

Updating DB with 0 via definition ...Extracting standard cell pins and blockage .....

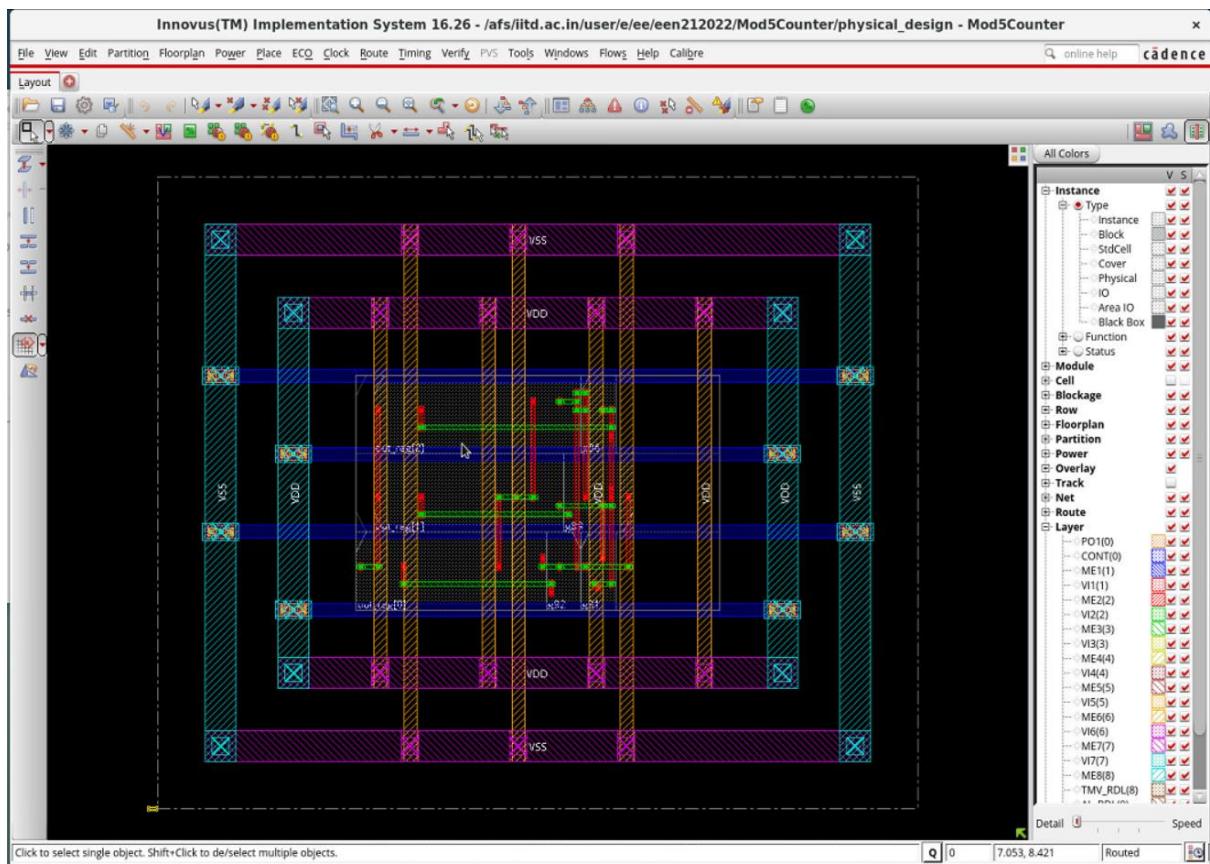
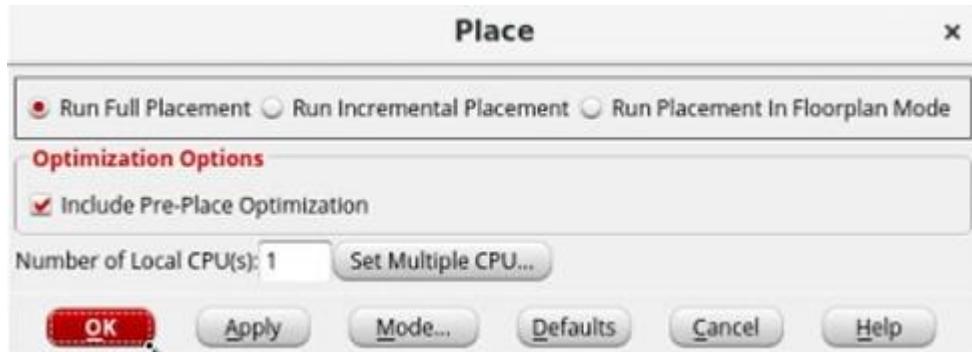
Pin and blockage extraction finished

sroute created 12 wires.

ViaGen created 56 vias, deleted 0 via to avoid violation.

Layer	Created	Deleted
ME1	12	NA
VI1	8	0
VI2	8	0
VI3	8	0
VI4	8	0
VI5	8	0
VI6	8	0
VI7	8	0

## Placement



Terminal

```

File Edit View Search Terminal Help
[NR-eGR] numTracksPerClockWire : 0
[NR-eGR] Layer1 has no routable track
[NR-eGR] Layer2 has single uniform track structure
[NR-eGR] Layer3 has single uniform track structure
[NR-eGR] Layer4 has single uniform track structure
[NR-eGR] Layer5 has single uniform track structure
[NR-eGR] Layer6 has single uniform track structure
[NR-eGR] Layer7 has single uniform track structure
[NR-eGR] Layer8 has single uniform track structure
[NR-eGR] Layer9 has single uniform track structure
[NR-eGR] numRoutingBlks=0 numInstBlks=0 numPGBlocks=163 numBumpBlks=0 numBoundaryFakeBlks=0
[NR-eGR] numPreroutedNet = 0 numPreroutedWires = 0
[NR-eGR] Read numTotalNets=10 numIgnoredNets=0
[NR-eGR] There are 1 clock nets ( 0 with NDR ).
[NR-eGR] ===== Routing rule table =====
[NR-eGR] Rule id 0. Nets 10
[NR-eGR] id=0 ndrTrackId=0 ndrViaId=-1 extraSpace=0 numShields=0 maxHorDemand=1 maxVerDemand=1
[NR-eGR] Pitch: L1=360 L2=400 L3=400 L4=400 L5=800 L6=800 L7=1600 L8=1600 L9=12000
[NR-eGR] =====
[NR-eGR] Layer group 1: route 10 net(s) in layer range [2, 9]
[NR-eGR] earlyGlobalRoute overflow of layer group 1: 0.00% H + 0.00% V. EstWL: 3.780000e+01um
[NR-eGR]
[NR-eGR] Overflow after earlyGlobalRoute (GR compatible) 0.00% H + 0.00% V
[NR-eGR] Overflow after earlyGlobalRoute 0.00% H + 0.00% V
Local HotSpot Analysis: normalized max congestion hotspot area = 0.00, normalized total congestion hotspot area = 0.00 (area is in unit of 4 s
td-cell row bins)
Skipped repairing congestion.
[NR-eGR] Layer1(ME1)(F) length: 0.000000e+00um, number of vias: 27
[NR-eGR] Layer2(ME2)(V) length: 2.258000e+01um, number of vias: 28
[NR-eGR] Layer3(ME3)(H) length: 1.700000e+01um, number of vias: 0
[NR-eGR] Layer4(ME4)(V) length: 0.000000e+00um, number of vias: 0
[NR-eGR] Layer5(ME5)(H) length: 0.000000e+00um, number of vias: 0
[NR-eGR] Layer6(ME6)(V) length: 0.000000e+00um, number of vias: 0
[NR-eGR] Layer7(ME7)(H) length: 0.000000e+00um, number of vias: 0
[NR-eGR] Layer8(ME8)(V) length: 0.000000e+00um, number of vias: 0
[NR-eGR] Layer9(AL_RDL)(H) length: 0.000000e+00um, number of vias: 0
[NR-eGR] Total length: 3.958000e+01um, number of vias: 55
End of congRepair (cpu=0:00:00.1, real=0:00:00.0)
*** Finishing placeDesign default flow ***
**** Total cpu 0:0:13
**** Total real time 0:0:14
**placeDesign ... cpu = 0: 0:13, real = 0: 0:14, mem = 2014.8M **

*** Summary of all messages that are not suppressed in this session:
Severity ID          Count Summary
WARNING IMPDC-1629      1 The default delay limit was set to %d. T...
WARNING IMPSP-9025      1 No scan chain specified/traced.
*** Message Summary: 2 warning(s), 0 error(s)

innovus 1>

```

## Pre-CTS Timing



```
Terminal
File Edit View Search Terminal Help
PreRoute RC Extraction DONE (CPU Time: 0:00:00.0 Real Time: 0:00:00.0 MEM: 2014.805M)
#####
# Design Stage: PreRoute
# Design Name: Mod5Counter
# Design Mode: 90nm
# Analysis Mode: MMMC Non-OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
AAE INFO: 1 threads acquired from CTE.
Calculate delays in BcWc mode...
Total number of fetched objects 10
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2116.25 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.5 real=0:00:00.0 totSessionCpu=0:07:38 mem=2116.2M)

-----
timeDesign Summary I

Setup views included:
worst_case

+---+ +---+ +---+ +---+
| Setup mode | all | req2reg | default |
+---+ +---+ +---+ +---+
| WNS (ns):| 8.619 | 9.250 | 8.619 |
| TNS (ns):| 0.000 | 0.000 | 0.000 |
| Violating Paths:| 0 | 0 | 0 |
| All Paths:| 9 | 3 | 6 |
+---+ +---+ +---+ +---+

+---+ +---+ +---+ +---+
| DRVs | Real | Total |
+---+ +---+ +---+ +---+
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+---+ +---+ +---+ +---+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+---+ +---+ +---+ +---+

Density: 69.841%
Routing Overflow: 0.00% H and 0.00% V
-----
Reported timing to dir timingReports
Total CPU time: 0.72 sec
Total Real time: 1.0 sec
Total Memory Usage: 2061.015625 Mbytes
innovus 1> █
```



```

Terminal
File Edit View Search Terminal Help
RC Corner Indexes          0
Capacitance Scaling Factor : 1.00000
Resistance Scaling Factor : 1.00000
Clock Cap. Scaling Factor : 1.00000
Clock Res. Scaling Factor : 1.00000
Shrink Factor              : 1.00000
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Using Quantus QRC technology file ...
Updating RC grid for preRoute extraction ...
Initializing multi-corner resistance tables ...
PreRoute RC Extraction DONE (CPU Time: 0:00:00.0  Real Time: 0:00:00.0  MEM: 2038.086M)
#####
# Design Stage: PreRoute
# Design Name: Mod5Counter
# Design Mode: 90nm
# Analysis Mode: MMC Non-OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
AAE_INFO: 1 threads acquired from CTE.
Calculate delays in BcWc mode...
*** Calculating scaling factor for min_timing_library libraries using the default operating condition of each library.
Total number of fetched objects 10
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2116.74 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.2 real=0:00:00.0 totSessionCpu=0:07:48 mem=2116.7M)

-----
timeDesign Summary
-----

Hold views included:
best_case

+-----+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns):| 0.093 | 0.093 | 0.000 |
| TNS (ns):| 0.000 | 0.000 | 0.000 |
| Violating Paths:| 0 | 0 | 0 |
| All Paths:| 3 | 3 | 0 |
+-----+-----+-----+-----+

Density: 69.841%
Routing Overflow: 0.00% H and 0.00% V
-----
Reported timing to dir timingReports
Total CPU time: 0.42 sec
Total Real time: 0.0 sec
Total Memory Usage: 2039.34375 Mbytes
innovus 1>

```

## Clock Tree Synthesis

```
File Edit View Search Terminal Help
**optDesign ... cpu = 0:00:07, real = 0:00:08, mem = 2158.9M, totSessionCpu=0:09:32 **

-----
optDesign Final Summary

I

Setup views included:
worst_case

+-----+
| Setup mode | all | reg2reg | default |
+-----+
| WNS (ns): | 8.662 | 9.260 | 8.662 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 9 | 3 | 6 |
+-----+



+-----+
|           Real           |           Total           |
| DRVs       | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+
| max_cap   | 0 (0)          | 0.000    | 0 (0)          |
| max_tran  | 0 (0)          | 0.000    | 0 (0)          |
| max_fanout| 0 (0)          | 0         | 0 (0)          |
| max_length| 0 (0)          | 0         | 0 (0)          |
+-----+



Density: 69.841%
Routing Overflow: 0.00% H and 0.00% V

**optDesign ... cpu = 0:00:07, real = 0:00:08, mem = 2156.9M, totSessionCpu=0:09:32 **
** Finished optDesign **

External::finishedDesign done. (took cpu=0:00:12.4 real=0:00:12.7)
Runtime done. (took cpu=0:00:21.0 real=0:00:21.1)
Coverage % = 99.5

Runtime Summary:
=====

wall % time children called name
+-----+
21.07 100.00 21.07 0
21.07 100.00 20.96 1 Runtime
1.72 8.17 1.72 1 CCOpt::Phase::Initialization
1.72 8.17 1.72 1 Check Prerequisites
0.03 0.13 0.00 1 Leaving CCOpt scope - CheckPlace
1.69 8.04 0.00 1 Validating CTS configuration
0.03 0.13 0.00 1 Leaving CCOpt scope - optDesignGlobalRouteStep
```

Terminal

File Edit View Search Terminal Help

```
0.03 0.15 0.03 1 Stage:::Insertion Delay Reduction
0.00 0.01 0.00 1 Removing unnecessary root buffering
0.00 0.01 0.00 1 Removing unconstrained drivers
0.02 0.11 0.00 1 Reducing insertion delay 1
0.00 0.01 0.00 1 Removing longest path buffering
0.00 0.01 0.00 1 Reducing insertion delay 2
2.37 11.24 2.31 1 CCOpt::Phase::Implementation
0.01 0.03 0.00 1 Stage:::Reducing Power
0.00 0.01 0.00 1 Reducing clock tree power 1
0.00 0.01 0.00 1 Reducing clock tree power 2
0.03 0.14 0.03 1 Stage:::Balancing
0.03 0.13 0.00 1 Approximately balancing fragments step
0.00 0.01 0.00 1 Approximately balancing fragments bottom up
0.00 0.01 0.00 1 Improving fragments clock skew
0.01 0.06 0.00 1 Approximately balancing step
0.00 0.01 0.00 1 Fixing clock tree overload
0.00 0.01 0.00 1 Approximately balancing paths 1
0.01 0.07 0.00 1 Leaving CCOpt scope
0.01 0.04 0.01 1 Stage:::Polishing
0.00 0.01 0.00 1 Improving clock skew
0.00 0.02 0.00 1 Reducing clock tree power 3
0.00 0.01 0.00 1 Improving insertion delay
1.95 9.25 1.91 1 Stage:::Routing
0.13 0.62 0.00 1 Leaving CCOpt scope - ClockRefiner
1.78 8.45 0.00 1 Leaving CCOpt scope - NanoRouter
0.00 0.02 0.00 1 Leaving CCOpt scope
0.29 1.36 0.13 1 Stage:::PostConditioning
0.12 0.59 0.00 3 Leaving CCOpt scope
0.00 0.02 0.00 1 Fixing DRVs
0.00 0.01 0.00 1 Buffering to fix DRVs
0.23 1.10 0.00 1 Tidy Up And Update Timing
12.66 60.07 0.00 1 External::optDesign
```

---

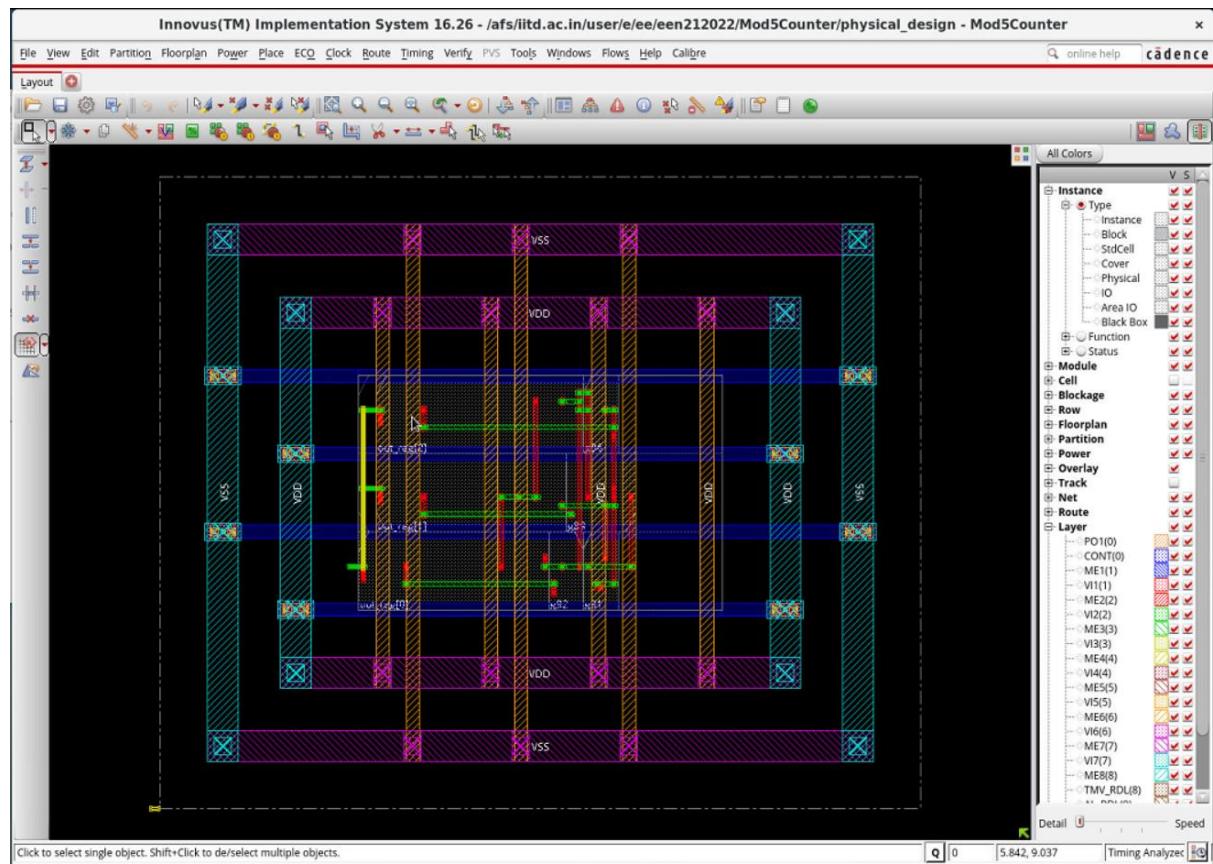
\*\*\* Summary of all messages that are not suppressed in this session:

Severity	ID	Count	Summary
WARNING	IMPEXT-3530	6	The process node is not set. Use the com...
WARNING	IMPSP-9025	1	No scan chain specified/traced.
WARNING	IMPOPT-576	1	4d nets have unplaced terms.
WARNING	IMPOPT-665	5	5 %s : Net has unplaced terms or is connec...
WARNING	IMPCOPT-1076	3	3 %s slew time target of %s is too low. It...
WARNING	IMPCOPT-1361	6	6 Routing configuration for %s nets in clo...
WARNING	IMPCOPT-2197	4	4 Unable to find a suitable hinst for a %s...
ERROR	IMPCOPT-1209	1	1 Non-leaf slew time target of %s is too...
ERROR	IMPCOPT-5054	1	1 Net %s is not completely connected after...
WARNING	IMPCOPT-2269	5	5 Failed to find a legal location near (%f...

\*\*\* Message Summary: 31 warning(s), 2 error(s)

\*\*ccopt design ... cpu = 0:00:21, real = 0:00:21, mem = 2089.8M, totSessionCpu=0:09:34 \*\*

innovus 5> innovus 5> [ ]



## Post-CTS Timing



```

Terminal
File Edit View Search Terminal Help
WARNING IMPSP-9025      1 No scan chain specified/traced.
WARNING IMPOPT-576        1 %d nets have unplaced terms.
WARNING IMPOPT-665        5 %s : Net has unplaced terms or is connec...
WARNING IMPCCOPT-1076      3 %s slew time target of %s is too low. It...
WARNING IMPCCOPT-1361      6 Routing configuration for %s nets in clo...
WARNING IMPCCOPT-2197      4 Unable to find a suitable hinst for a %s...
ERROR  IMPCCOPT-1209      1 Non-leaf slew time target of %s is too...
ERROR  IMPCCOPT-5054      1 Net %s is not completely connected after...
WARNING IMPCCOPT-2269      5 Failed to find a legal location near (%f...
*** Message Summary: 31 warning(s), 2 error(s)

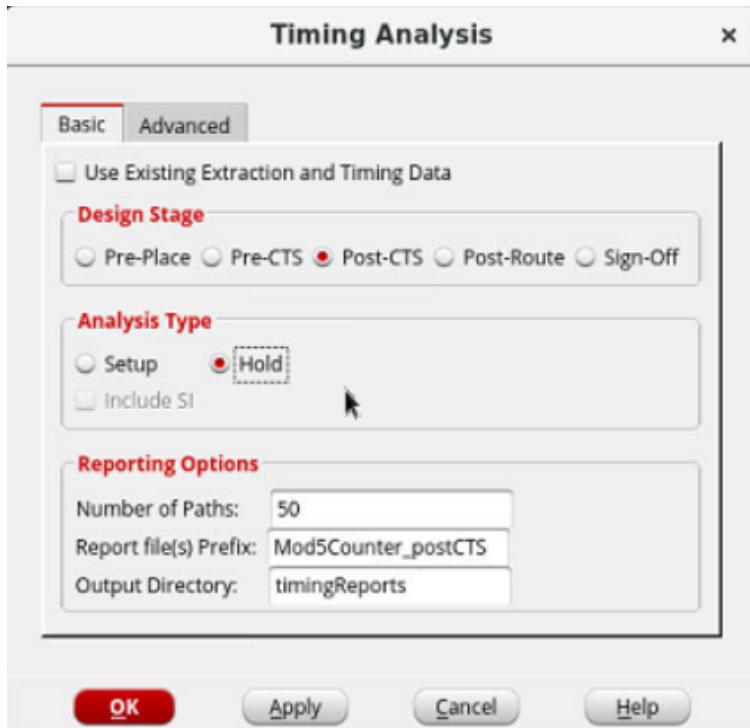
**ccopt design ... cpu = 0:00:21, real = 0:00:21, mem = 2089.8M, totSessionCpu=0:09:34 **
innovus 5> innovus 5> Start to check current routing status for nets...
All nets are already routed correctly.
End to check current routing status for nets (mem=2089.8M)

----- timeDesign Summary -----
I

Setup views included:
worst_case

+-----+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns):| 8.662 | 9.260 | 8.662 |
| TNS (ns):| 0.000 | 0.000 | 0.000 |
| Violating Paths:| 0 | 0 | 0 |
| All Paths:| 9 | 3 | 6 |
+-----+-----+-----+-----+
+-----+-----+-----+
|          Real          |          Total          |
| DRVs      | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap   | 0 (0)        | 0.000    | 0 (0)        |
| max_tran  | 0 (0)        | 0.000    | 0 (0)        |
| max_fanout| 0 (0)        | 0        | 0 (0)        |
| max_length| 0 (0)        | 0        | 0 (0)        |
+-----+-----+-----+-----+
Density: 69.841%
Routing Overflow: 0.00% H and 0.00% V
-----+
Reported timing to dir timingReports
Total CPU time: 0.11 sec
Total Real time: 1.0 sec
Total Memory Usage: 2087.765625 Mbytes
innovus 5> 

```



**Terminal**

```

File Edit View Search Terminal Help
RCMode: PreRoute
  RC Corner Indexes      0
  Capacitance Scaling Factor : 1.00000
  Resistance Scaling Factor : 1.00000
  Clock Cap. Scaling Factor : 1.00000
  Clock Res. Scaling Factor : 1.00000
  Shrink Factor          : 1.00000
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Using Quantus QRC technology file ...
Initializing multi-corner resistance tables ...
PreRoute RC Extraction DONE (CPU Time: 0:00:00.0  Real Time: 0:00:00.0  MEM: 2069.617M)
#####
# Design Stage: PreRoute
# Design Name: Mod5Counter
# Design Mode: 90nm
# Analysis Mode: MMMC Non-OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
AAE INFO: 1 threads acquired from CTE.
Calculate delays in BcWe mode...
*** Calculating scaling factor for min_timing_library libraries using the default operating condition of each library.
Total number of fetched objects 10
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2146.76 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.2 real=0:00:01.0 totSessionCpu=0:10:29 mem=2146.8M)

-----
timeDesign Summary
-----

Hold views included:
best_case

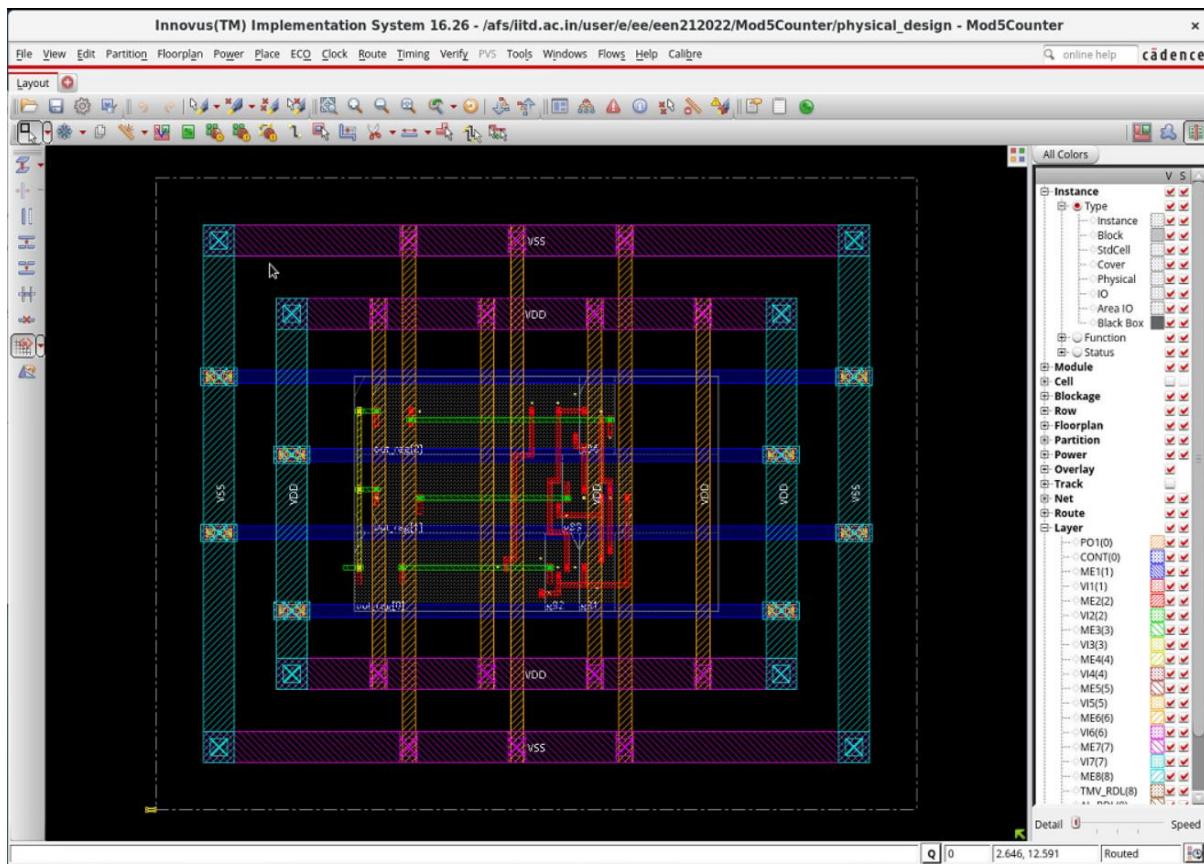
+-----+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns): | 0.090 | 0.090 | 0.000 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 3 | 3 | 0 |
+-----+-----+-----+-----+

Density: 69.841%
Routing Overflow: 0.00% H and 0.00% V
-----
Reported timing to dir timingReports
Total CPU time: 0.44 sec
Total Real time: 1.0 sec
Total Memory Usage: 2069.375 Mbytes
innovus 5> 

```

## Routing the design





```

Terminal
File Edit View Search Terminal Help
#Total number of nets with non-default rule or having extra spacing = 1
#Total wire length = 37 um.
#Total half perimeter of net bounding box = 48 um.
#Total wire length on LAYER ME1 = 0 um.
#Total wire length on LAYER ME2 = 21 um.
#Total wire length on LAYER ME3 = 12 um.
#Total wire length on LAYER ME4 = 4 um.
#Total wire length on LAYER ME5 = 0 um.
#Total wire length on LAYER ME6 = 0 um.
#Total wire length on LAYER ME7 = 0 um.
#Total wire length on LAYER ME8 = 0 um.
#Total wire length on LAYER AL_RDL = 0 um.
#Total number of vias = 39
#Up-Via Summary (total 39):
#
#-----
# Metal 1      27
# Metal 2      9
# Metal 3      3
#-----
#                  39
#
#detailRoute Statistics:
#Cpu time = 00:00:02
#Elapsed time = 00:00:02
#Increased memory = 2.42 (MB)
#Total memory = 1230.54 (MB)
#Peak memory = 1579.28 (MB)
#
#globaDetailRoute statistics:
#Cpu time = 00:00:07
#Elapsed time = 00:00:07
#Increased memory = 7.53 (MB)
#Total memory = 1230.05 (MB)
#Peak memory = 1579.28 (MB)
#Number of warnings = 7
#Total number of warnings = 55
#Number of fails = 0
#Total number of fails = 0
#Complete globaDetailRoute on Sun Oct 17 19:20:27 2021
#
#routeDesign: cpu time = 00:00:07, elapsed time = 00:00:07, memory = 1230.05 (MB), peak = 1579.28 (MB)
*** Summary of all messages that are not suppressed in this session:
Severity ID          Count Summary
WARNING IMPEXT-3493   1  The design extraction status has been re...
WARNING IMPEXT-3530   1  The process node is not set. Use the com...
WARNING TCLCMD-1403   1  '%s'
*** Message Summary: 3 warning(s), 0 error(s)
innovus 5>

```

## Verify Geometry



```
Terminal
File Edit View Search Terminal Help
#Cpu time = 00:00:07
#Elapsed time = 00:00:07
#Increased memory = 7.53 (MB)
#Total memory = 1230.05 (MB)
#Peak memory = 1579.28 (MB)
#Number of warnings = 7
#Total number of warnings = 55
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Sun Oct 17 19:20:27 2021
#
#routeDesign: cpu time = 00:00:07, elapsed time = 00:00:07, memory = 1230.05 (MB), peak = 1579.28 (MB)

*** Summary of all messages that are not suppressed in this session:
Severity ID          Count Summary
WARNING IMPEXT-3493  1  The design extraction status has been re...
WARNING IMPEXT-3530  1  The process node is not set. Use the com...
WARNING TCLCMD-1403  1  'ss'

*** Message Summary: 3 warning(s), 0 error(s)

innovus 5> *** Starting Verify Geometry (MEM: 2039.4) ***

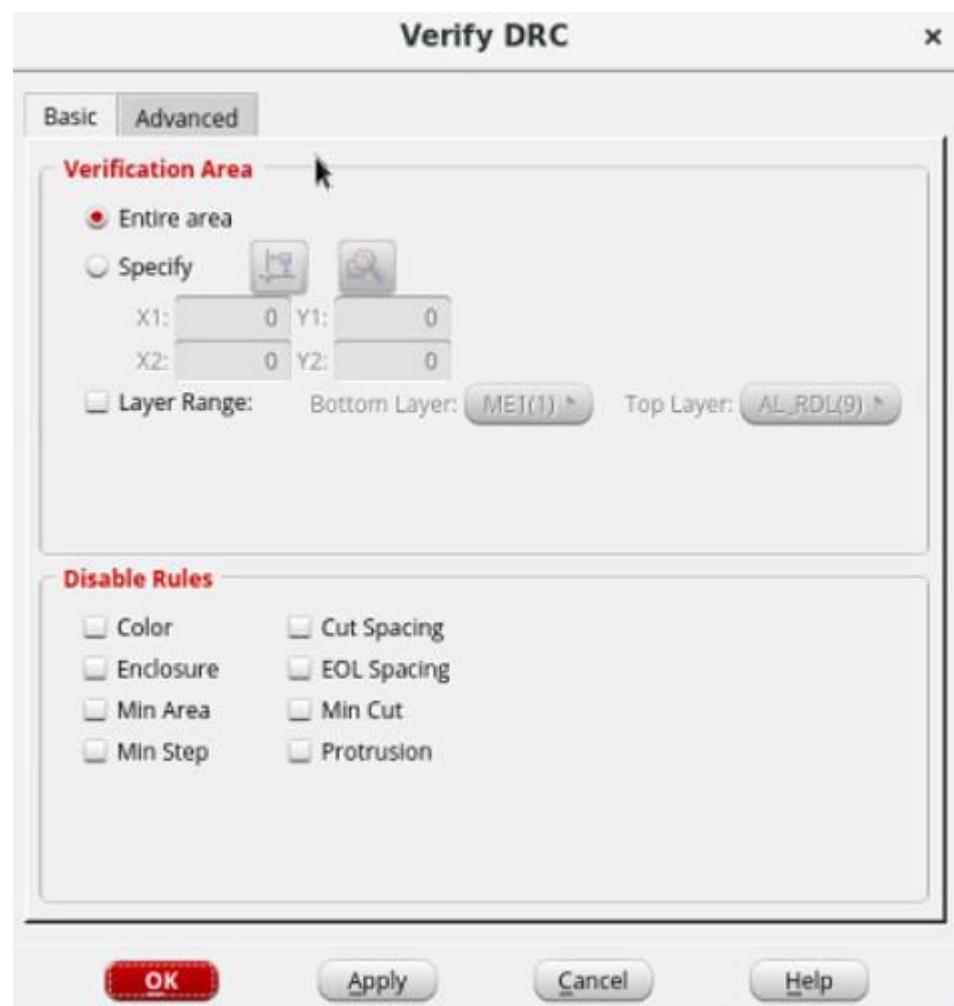
**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this release but will be removed in future
release. Please update your script to use the new command.
VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
..... bin size: 2880
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 1.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary

Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.2 MEM: 105.0M)

innovus 5>
```

## Verify DRC



```
Terminal
File Edit View Search Terminal Help
WARNING IMPEXT-3493      1 The design extraction status has been re...
WARNING IMPEXT-3530      1 The process node is not set. Use the com...
WARNING TCLCMD-1403      1 '%s'
*** Message Summary: 3 warning(s), 0 error(s)

innovus > *** Starting Verify Geometry (MEM: 2039.4) ***

**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this release but will be removed in future release. Please update your script to use the new command.
VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
..... bin size: 2880
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 1.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary
Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.2 MEM: 105.0M)

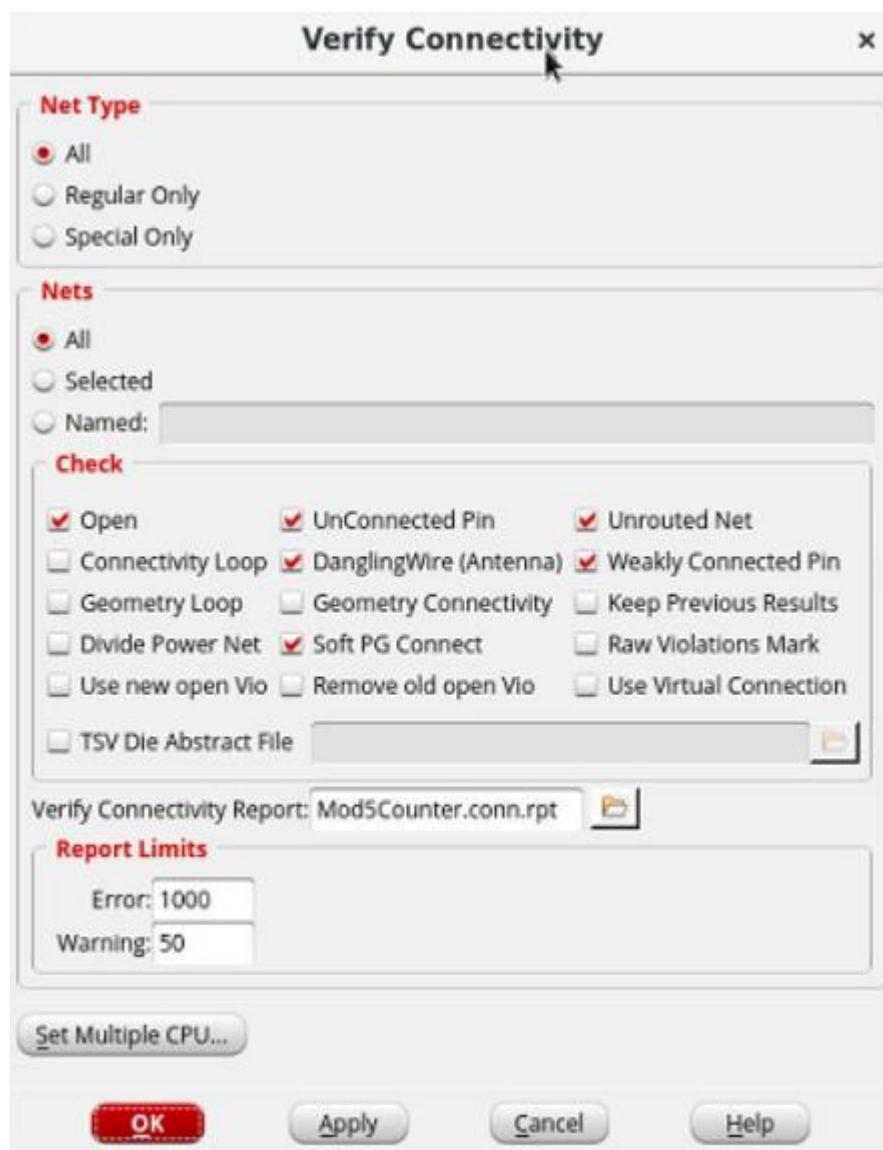
innovus 5> #-report Mod5Counter.drc.rpt      # string, default="", user setting
*** Starting Verify DRC (MEM: 2144.4) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 17.600 14.600} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.0 ELAPSED TIME: 0.00 MEM: 0.0M) ***
```

## Verify Connectivity



```
Terminal
File Edit View Search Terminal Help
Cells      : 0
SameNet    : 0
Wiring     : 0
Antenna    : 0
Short      : 0
Overlap    : 0
End Summary

Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:00.2 MEM: 105.0M)

innovus 5> #-report Mod5Counter.drc.rpt      # string, default="", user setting
*** Starting Verify DRC (MEM: 2144.4) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 17.600 14.600} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.0 ELAPSED TIME: 0.00 MEM: 0.0M) ***

VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Sun Oct 17 19:23:44 2021

Design Name: Mod5Counter
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (17.6000, 14.6000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Sun Oct 17 19:23:44 2021
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0 MEM: 0.000M)

innovus 5>
```