**Example Configuration:**

L1 Size 1KB

L2 Size 2KB

Block Size 64B

Set Associativity 4

Write Policy write back

Allocation Policy write allocate

Max number of outstanding misses 6

L1 hit latency: 1

L2 hit latency: 5

**access-under-misses version:**

Input stream: L1 set L2 set h/m issue time serve time return time pending miss

R 00000000111111 set0 set0 miss 1 1 107 0

R 00000001010101 set1 set1 miss 10 10 116 1

R 00001101101010 set1 set5 miss 20 20 126 2

R 00010001110011 set1 set1 miss 30 30 136 3

W 00011101100011 set1 set5 miss 40 40 146 4

R 00000000111111 set0 set0 L1 hit 50 50 156

R 00100101101101 set1 set5 miss 60 60 166 5

R 00000001010101 set1 set1 L2 hit 70 70 76

R 00000011010101 set3 set3 miss 107 108 214 5

R 00000111101011 set3 set7 miss 110 117 223 6

**sequential version:**

Input stream: L1 set L2 set h/m issue time serve time return time

R 00000000111111 set0 set0 miss 1 1 107

R 00000001010101 set1 set1 miss 10 108 214

R 00001101101010 set1 set5 miss 20 215 321

R 00010001110011 set1 set1 miss 30 322 428

W 00011101100011 set1 set5 miss 40 429 535

R 00000000111111 set0 set0 L1 hit 50 536 537

R 00100101101101 set1 set5 miss 60 538 644

R 00000001010101 set1 set1 L2 hit 70 645 651

R 00000011010101 set3 set3 miss 107 652 758

R 00000111101011 set3 set7 miss 110 759 865