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## **Electrical Properties of Printed Wiring Boards**

Charles W. Jennings

Prepared by Sandia Laboratories, Albuquerque, New Mexico 87115  
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## ELECTRICAL PROPERTIES OF PRINTED WIRING BOARDS

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### ABSTRACT

This report describes results of a series of tests to establish electrical parameters for Sandia/Bendix Standard Process printed wiring boards. Test results are displayed graphically and tabulated for use by sub-system designers. The results include voltage holdoff, current carrying capacity and insulation resistance for double sided bare, coated and encapsulated boards. The boards were fabricated by a panel plating process and contain variable conductor widths and separations. Breakdown voltage in room environment did not occur below 1 kV for any spacing on a board. Average breakdown voltage in kV followed the relationship,  $V = 3.1 S^{0.51}$ , where separation S ranged from 0.25 to 1.5 mm. Parylene or urethane coated, urethane foamed, and glass microballoon filled epoxy encapsulated boards had higher breakdown voltages than bare boards. At low pressure, 660 Pa (5 Torr), breakdowns which ranged from 0.4 to 25 kV were not a function of conductor separation. Low pressure breakdown voltage was generally higher for coated or encapsulated boards although the difference wasn't nearly as great as for room conditions. Current carrying capability of conductors was evaluated from the temperature rise generated with step increases in current. Variations in temperature rise between conductors with the same nominal or design width were correlated with measured differences in conductor cross sectional areas. Resistances calculated from conductor lengths and cross sectional areas were within 10 percent of the measured values. At normal operating temperatures, coated and encapsulated boards were similar in current carrying capacity to bare boards. At currents which caused conductors on bare boards to rapidly burn through, encapsulated conductors increased slowly in temperature until the encapsulation degraded and ruptured. Insulation resistance for all boards ranged from 1 to 230 terohms at 10 to 30% RH. At 92 to 100% RH resistance was 1 to 4 decades lower.

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## TABLE OF CONTENTS

	<u>Page</u>
ABSTRACT	1
INTRODUCTION	6
VOLTAGE HOLDOFF	9
Tests on Bare Boards	10
Coated and Encapsulated Boards	17
CURRENT CARRYING CAPABILITY OF PWB CONDUCTORS	27
Bare Boards	30
Coated and Encapsulated Boards	45
INSULATION RESISTANCE	51
SUMMARY	57
REFERENCES	60

TABLES

	<u>Page</u>
Table 1. Essential Steps in Printed Wiring Board (PWB) Fabrication	7
Table 2. Breakdown Voltage Between Conductors on Bare PWB's at Ambient Conditions	11
Table 3. Effect of Repeated Breakdown on Voltage Holdoff of Bare PWB	16
Table 4. Breakdown Voltage of Encapsulated PWB's at 24°C and 660 Pa	23
Table 5. Breakdown Voltage of Encapsulated PWB's at 24°C and 84 kPa	24
Table 6. Recommended Coplanar Conductor Spacing from IPC-ML-910A	25
Table 7. Temperature Rise Calculations	29
Table 8. Calculation of $\Delta T$ from Resistance Change with Current for 0.25 mm (0.010)* Conductor	31
Table 9. Calculation of $\Delta T$ from Resistance Change with Current for 0.51 mm (0.020) Conductor	32
Table 10. Calculation of $\Delta T$ from Resistance Change with Current for two 0.38 mm (0.15) Parallel Conductors	33
Table 11. Calculation of $\Delta T$ from Resistance Change with Current for 1.27 mm (0.50) Conductor	34
Table 12. Calculation of $\Delta T$ from Resistance Change with Current for two 1.01 mm (0.040) Parallel Conductors	35
Table 13. Currents for 50°C and 100°C Temperature Rise with Different Nominal and Minimum Cross Sectional Areas	39
Table 14. Insulation Resistance of Bare and Encapsulated Boards in Teraohms	52
Table 15. Insulation Resistance of Parylene Coated Boards in Teraohms	54
Table 16. Insulation Resistance of Urethane Coated Boards in Teraohms	55
Table 17. Effect of Time on Insulation Resistance at Different Humidity Environments.	56

\*Values in parenthesis are in inch units.

## FIGURES

	<u>Page</u>
Fig. 1. Board Circuit Patterns	8
Fig. 2. Breakdown Voltage between Conductors as a Function of Separation	12
Fig. 3. Breakdown Path from Lead Edge to Terminal Area	13
Fig. 4. Typical Conductor Cross Section	14
Fig. 5. Voltage Breakdown Path from Conductor with Projection	15
Fig. 6. Effect of Temperature on Breakdown Voltage for Different Conductor Separations at 83 kPa	16
Fig. 7. Voltage Breakdown of Urethane Coated Boards at 24°C and 83.5 kPa	19
Fig. 8. Voltage Breakdown of Parylene Coated Boards at 24°C and 83.5 kPa	20
Fig. 9. Effect of Repeated Voltage Breakdowns of Bare and Coated Boards at 83 kPa and 24°C.	21
Fig. 10. Rated Voltage Between Conductors (From IEC Publication 326)	26
Fig. 11. Resistance Measurement Method	28
Fig. 12. Temperature Rise for Different Currents and Cross Sectional Areas of Uncoated Conductors	36
Fig. 13. Temperature Rise for Different Currents and Conductor Widths and 0.069 mm (0.0027) Thick Copper	37
Fig. 14. Percent Change in Resistance as a Function of Initial Resistance and Current Steps	40
Fig. 15. Plated-through Hole with Thin Copper and Breaks in the Plating	42
Fig. 16. Comparison of Published Temperature Rise-Current Curves with Those of This Study for 1.27 mm (0.050) wide, 0.069 mm (0.0027) Thick Conductor	44
Fig. 17. Comparison of Mean Temperature Rise with Current for a 1.27 mm (0.050) Wide, 0.069 mm (0.0027) Thick Conductor on Bare, Coated and Encapsulated Boards	46
Fig. 18. Comparison of Rate of Temperature Rise of a 0.51 mm (0.020) Wide Conductor on a Parylene Coated and a GMB Encapsulated Board	47

Page

Fig. 19. Explosive Blowout Around Conductor on GMB Encapsulated Board	48
Fig. 20. Blowout Around Conductor on Epoxy Foam Board	49
Fig. 21. Beginning of Thermal Degradation on Bare Board	50

## INTRODUCTION

In an earlier study (1) a special circuit pattern with variable feature sizes was used to evaluate printed wiring board (PWB) processing capabilities. Double sided boards were fabricated in the Bendix, Kansas City and SIA production facilities using a panel plate and solder dip or plate and liquid level process. The essential steps in this process are shown in Table 1. The conductive pattern for each side is shown in Figure 1. This report covers electrical measurements made on these boards as well as a few measurements made on boards fabricated by a pattern plating process with thin clad laminate. Electrical measurements consist of current carrying capability of conductors, voltage to flashover or electrical breakdown between conductors, and insulation resistance between conductors.

Tables and charts in design guides and military standards giving these electrical properties often contain factors of safety and it is difficult to determine the actual capabilities of the boards. This study was set up to measure these capabilities. Testing was frequently extended until functional failure occurred to obtain a better understanding of the failure mode.

The copper clad epoxy glass laminate used was type GH from three different suppliers. Boards tested were from different fabrication lots and from Sandia Laboratories and Bendix Kansas City Division. Coated and encapsulated, as well as bare boards, were tested under different environmental conditions so their electrical properties could be compared. The coatings used were urethane (U) (Laminar X-500) and Parylene (P) (Poly-p-xylylene). The urethane was applied by brushing to a thickness of 0.025 (0.001) to 0.075 (0.003)\* mm. One group

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\*Values in parentheses are in inch units.

TABLE 1  
ESSENTIAL STEPS IN PRINTED WIRING BOARD FABRICATION

Drill Plated-Through-Holes  
 Abrasive and Chemical Cleaning  
 Copper Electroless Plate  
 Copper Electroplate (Pyrophosphate Bath)  
 Surface Abrasion and Cleaning  
 Apply Dry Film Resist

<u>Solder Dip and Level</u>	<u>Solder Plate and Level</u>
Negative Image	Positive Image
Expose and Develop Resist	Expose and Develop Resist
Etch (Chromic-Sulfuric)	Electroplate Solder
Remove Resist	Remove Resist
Drill Non-Plated Holes	Etch (Chromic-Sulfuric)
Solder Dip	Drill None-Plated Holes
Solder Liquid Level	Solder Liquid Level

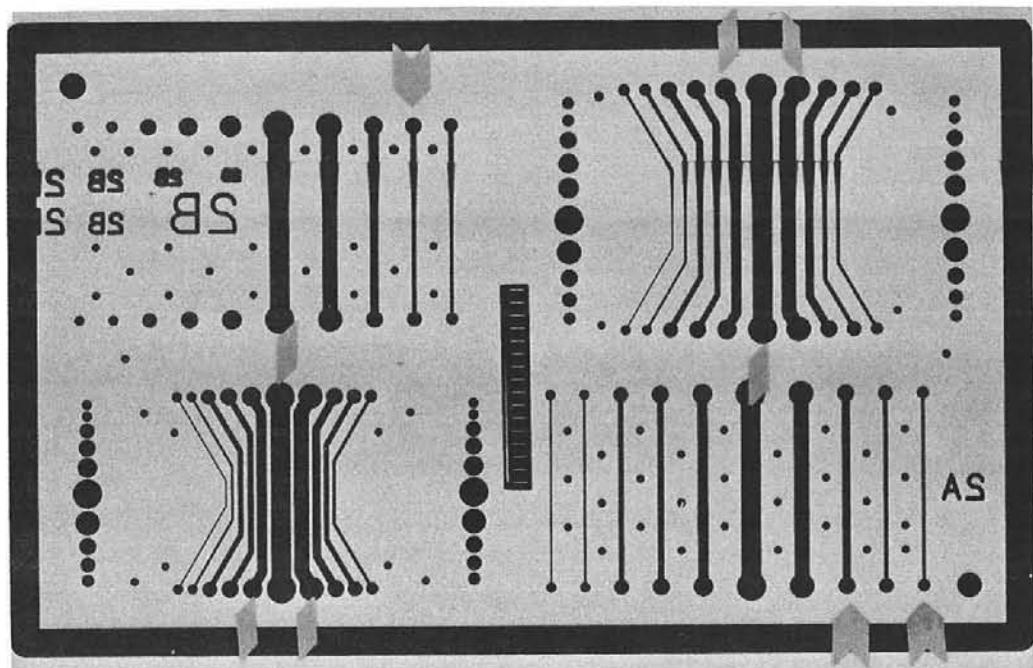
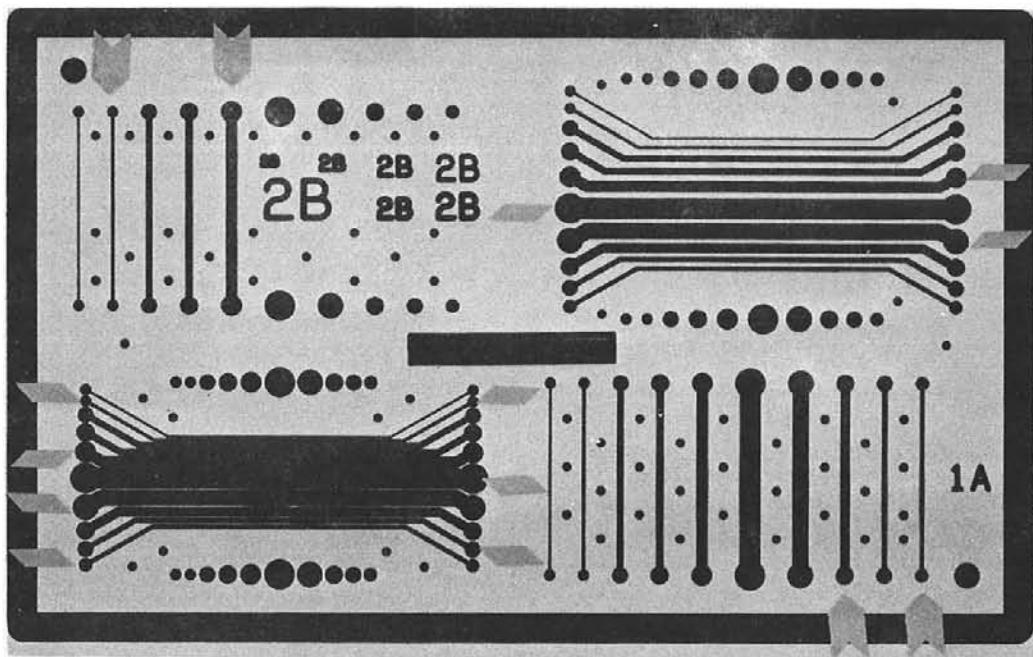


Figure 1. Board Circuit Patterns  
(Arrows show conductors used in current measurements; half arrows show lead connectors for voltage holdoff and surface resistance measurements.)

of boards was Parylene N coated at Lawrence Livermore Laboratory by P. Fleming to a thickness of 0.025 mm. Another group was coated at Bendix Kansas City by S. Degisi to a thickness of 0.012 mm. An epoxy foam (EF), a urethane foam (UF), and a glass microballoon (GMB) filled epoxy were used for encapsulation. Thickness of material on each side of the board ranged from 10 to 15 mm (0.4 to 0.6). The epoxy foam, Ablefoam #5, which was designed to be  $0.35 \text{ g/cm}^3$ , actually foamed out to be  $0.10 \text{ g/cm}^3$  ( $6.2 \text{ lb/ft}^3$ ). The urethane foam was  $0.11$  to  $0.18 \text{ g/cm}^3$  ( $7$  to  $11 \text{ lb/ft}^3$ ). The GMB epoxy encapsulant consisted of 750 parts by weight Epon 828, 90 diethanolamine, and 250 parts GMB filler. The filler was incorporated to provide a low coefficient of expansion to the encapsulant.

#### VOLTAGE HOLDOFF

Voltage flashover or breakdown was measured between conductors with nominal separations of 0.25 (0.010), 0.38 (0.015), 0.51 (0.020), 0.64 (0.025), 0.76 (0.030), 1.02 (0.040), 1.27 (0.050), and 1.52 mm (0.060). For the 0.25 and 0.38 mm separations two pairs of conductors were tested, one at the edge of the conductor group, the other in the middle of the group, as shown in Figure 1. Conductor lengths were 25 (1.0) and 50 mm (2.0). Leads were soldered in holes at the opposite ends of adjacent conductors. For most of the measurements a Hipotronics Model 380-20 ML, 0-30 kV Power Supply was used. Voltage was increased at 250 volt/sec. Flashover was observed both visually and by current pulse sensing circuitry in the Hipotronics unit. A few measurements were made with a Harrison Model 7525A, 0-4 kV Power Supply using visual detection of flashover. Ambient environment was  $24 \pm 2^\circ\text{C}$ , 82 to 84.5 kPa (615 to 635 Torr), and 10 to 40 percent relative humidity. The boards were either suspended from the leads or were set on a Teflon plate in the voltage test chamber.

### Tests on Bare Boards

Figure 2 and Table 2 show breakdown voltages for the different conductor separations on uncoated or bare boards at ambient condition. The curve for breakdown voltage  $V$  as a function of separation  $S$  in millimeters is given by the relationship,  $V = 3.1 S^{0.51}$ .

Breakdown voltages in this investigation compare favorably with those obtained by Chevalier and Broyer (2), and to those of Rainal, Landry and Lahti (3) for small separations. In the region of 1 mm separation the values of Rainal, Landry and Lahti are 20 to 25 percent lower than for this investigation. No breakdowns occurred below 1000 volts at ambient conditions. Failure path was frequently from the sharp edge of a lead which protruded from a hole to an adjacent terminal area. The sharp edge resulted from clipping the excess lead length after soldering. Figure 3 shows such an edge and breakdown path. Note that this is a longer path than that between the terminal areas or conductors. Breakdown path between conductors was usually from the top edge of one conductor to the top edge of another rather than at the laminate interface level where the spacing was smaller. Figure 4 shows a typical conductor edge profile.

Breakdown does not necessarily occur at a surface projection as shown by the failure path in Figure 5. Breakdown occurred at 3 kV from the terminal area to the conductor instead of from the projection to the conductor at a similar distance.

For a few boards, breakdown tests were repeated between the same conductors in the same environment of  $25^{\circ}\text{C}$  and  $20 \pm 10\%$  RH. Table 3 presents typical results for such breakdowns. For some of the separations there is an indication of degradation after the third breakdown.

TABLE 2

Breakdown Voltage Between Conductors  
on Bare PWB's at Ambient Conditions

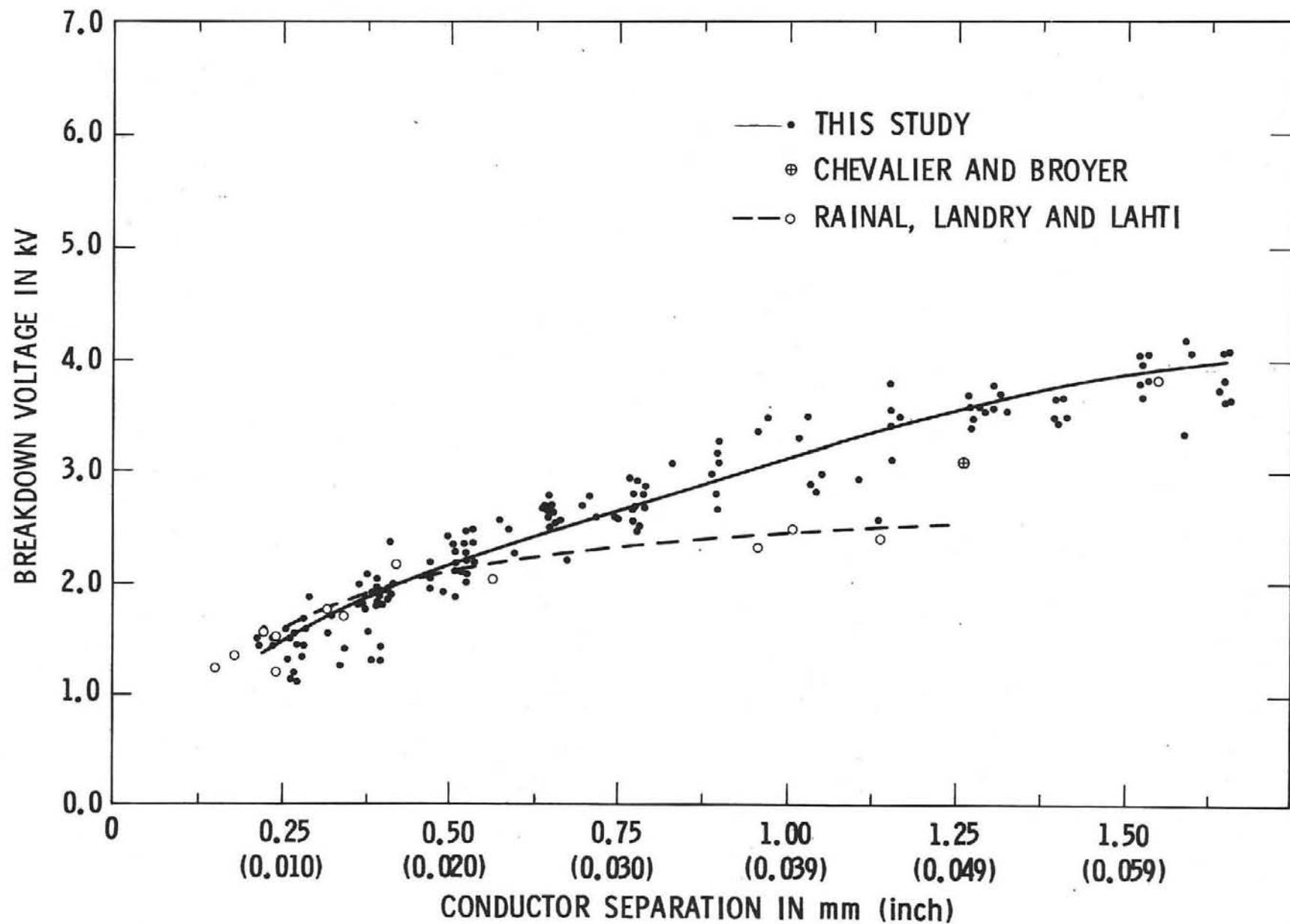
<u>Separation</u> <u>(mm)</u>	<u>Separation</u> <u>(inch)</u>	<u>Mean</u> <u>Breakdown</u> <u>Voltage</u> <u>(kV)</u>	<u>Standard</u> <u>Deviation</u> <u>(kV)</u>	<u>Range</u> <u>(kV)</u>
0.254	(0.010)	1.54# 1.60*	0.32# 0.28*	1.1 - 2.1 1.0 - 2.2
0.381	(0.015)	1.89# 1.92*	0.43# 0.62*	1.3 - 2.5 1.3 - 2.4
0.518	(0.020)	2.19	0.24	2.0 - 2.7
0.635	(0.025)	2.46	0.17	2.2 - 2.9
0.762	(0.030)	2.70	0.25	2.4 - 3.3
1.016	(0.040)	3.13	0.39	2.6 - 3.8
1.27	(0.050)	3.50	0.19	3.2 - 3.9
1.524	(0.060)	3.85	0.24	3.3 - 4.2

#Conductor pair in middle of pattern

\*Conductor pair at outer part of pattern

Figure 2

## Breakdown Voltage between Conductors as a Function of Separation



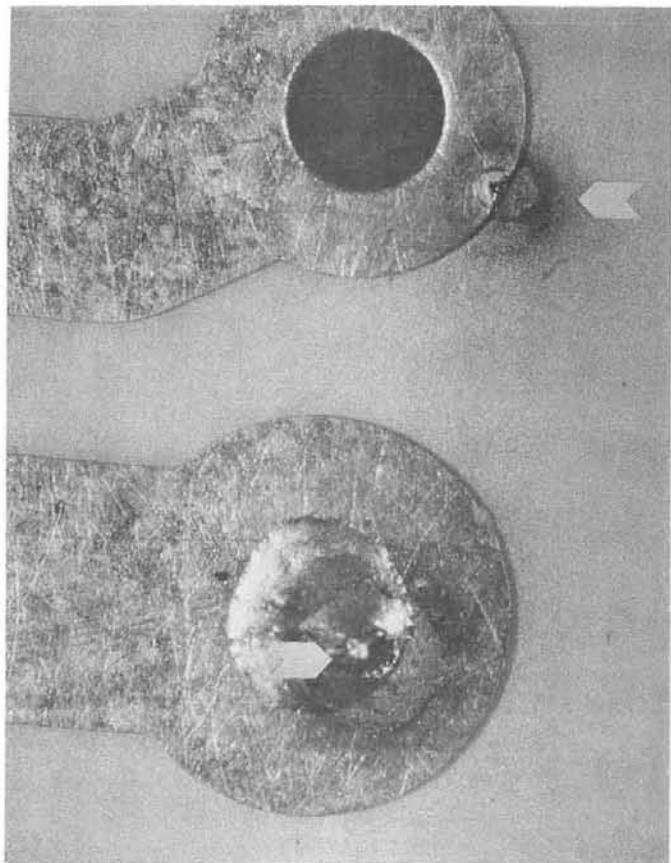


Figure 3  
Breakdown Path from Lead Edge to Terminal Area

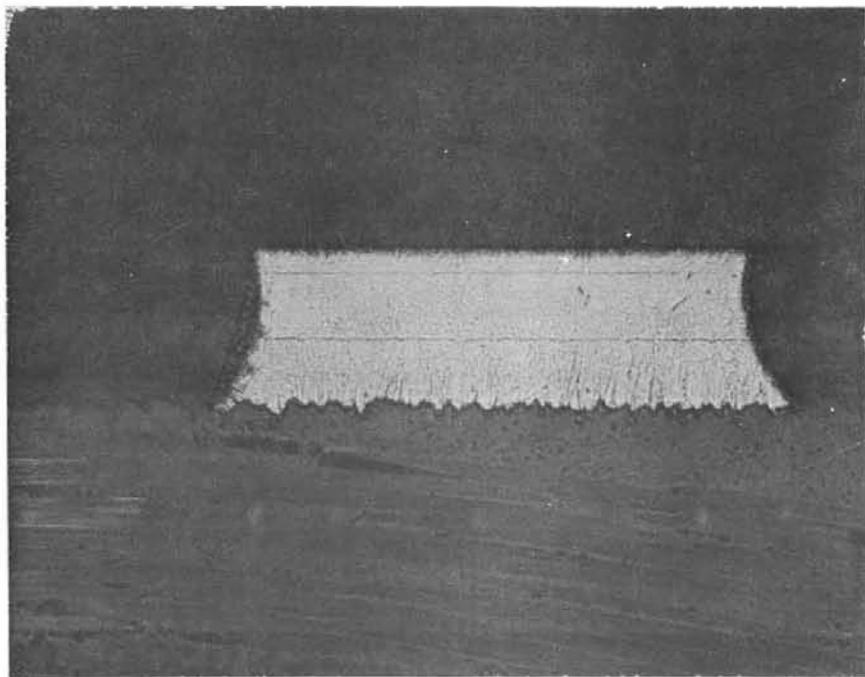


Figure 4  
Typical Conductor Cross Section

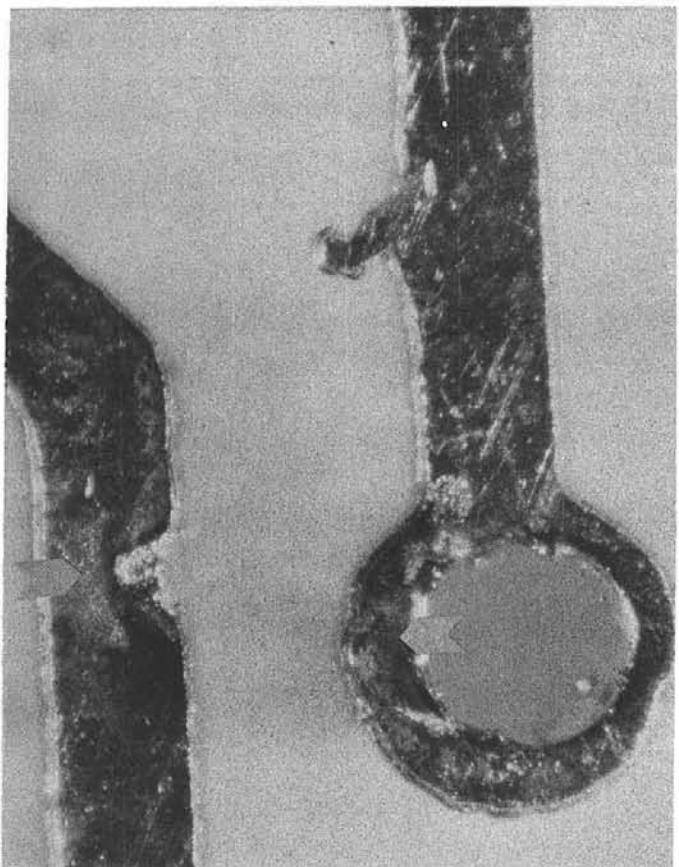


Figure 5  
Voltage Breakdown Path from Conductor with Projection

TABLE 3

Effect of Repeated  
Breakdowns on Voltage Holdoff  
of Bare PWB

Measured Separation <u>(mm)</u>	<u>inch</u>	Breakdown Voltage for Test Number (kV)						<u><math>\bar{X}</math></u> (kV)	<u>S</u> (kV)
		<u>1</u>	<u>2</u>	<u>3</u>	<u>4</u>	<u>5</u>	<u>6</u>		
0.22	(0.009)	1.5	1.5	1.5	0.6	0.9	1.0	1.17	0.39
0.24	(0.009)	1.6	1.6	1.6	1.7	1.6	1.7	1.64	0.05
0.35	(0.014)	2.0	2.0	1.9	1.7	1.8	1.1	1.75	0.34
0.36	(0.014)	1.8	1.5	1.8	1.7	1.7	1.5	1.67	0.14
0.47	(0.019)	2.4	2.4	2.4	2.4	2.4	2.5	2.42	0.04
0.64	(0.025)	2.8	2.6	2.5	2.6	2.5	2.5	2.58	0.12
0.72	(0.028)	2.6	2.9	3.0	2.9	2.9	3.0	2.88	0.15
1.00	(0.039)	3.3	3.2	3.3	3.5	3.4	3.4	3.30	0.09
1.24	(0.049)	3.2	3.6	3.3	3.5	3.4	3.4	3.40	0.14
1.56	(0.061)	4.0	4.2	4.35	3.5	4.1	3.4	3.93	0.39

Breakdown was greater at -58°C and lower at 74°C than at 25°C. The change was most noticeable at the larger conductor separations as shown in Figure 6.

A few measurements were made with a 1 microsecond width pulse. Breakdown voltage was higher and in some instances twice the static breakdown voltage.

At a pressure of 660 Pa (5 Torr) which corresponds to an altitude of approximately 35 km, voltage breakdowns occurred between 400 and 1000 volts. Breakdown voltage did not correlate to separation and the breakdown path was frequently between the leads. As the product of pressure times separation distance corresponded to the region near the minimum of the Paschen curve, this is not surprising.

#### Coated and Encapsulated Boards

Although there was considerable scatter in the ambient breakdown voltages for coated boards, as shown in Figures 7 and 8, most of the values were higher than for bare boards. Thick Parylene coated boards had considerably higher values. Breakdown voltage of coated boards tended to decrease when breakdowns were repeated between the same conductors, as shown in Figure 9. The scatter in voltage for repeated breakdowns is much greater for the coated than the uncoated boards. It is likely that breakdowns initiate at randomly located weak points in the coating giving rise to variations in breakdown path length and voltage.

At low pressure, 660 Pa (5 Torr), breakdowns for the coated boards were only slightly higher than for bare boards. Breakdowns ranged from 600 to 1600 volts. Boards with a thick Parylene coating had higher values than those with thin Parylene or urethane coating. Voltage did not correlate with separation and breakdowns frequently occurred between leads despite attempts to provide adequate lead insulation. A large number of breakdowns occurred in the region where the lead was joined to the board. By coating the portion of the lead protruding from the

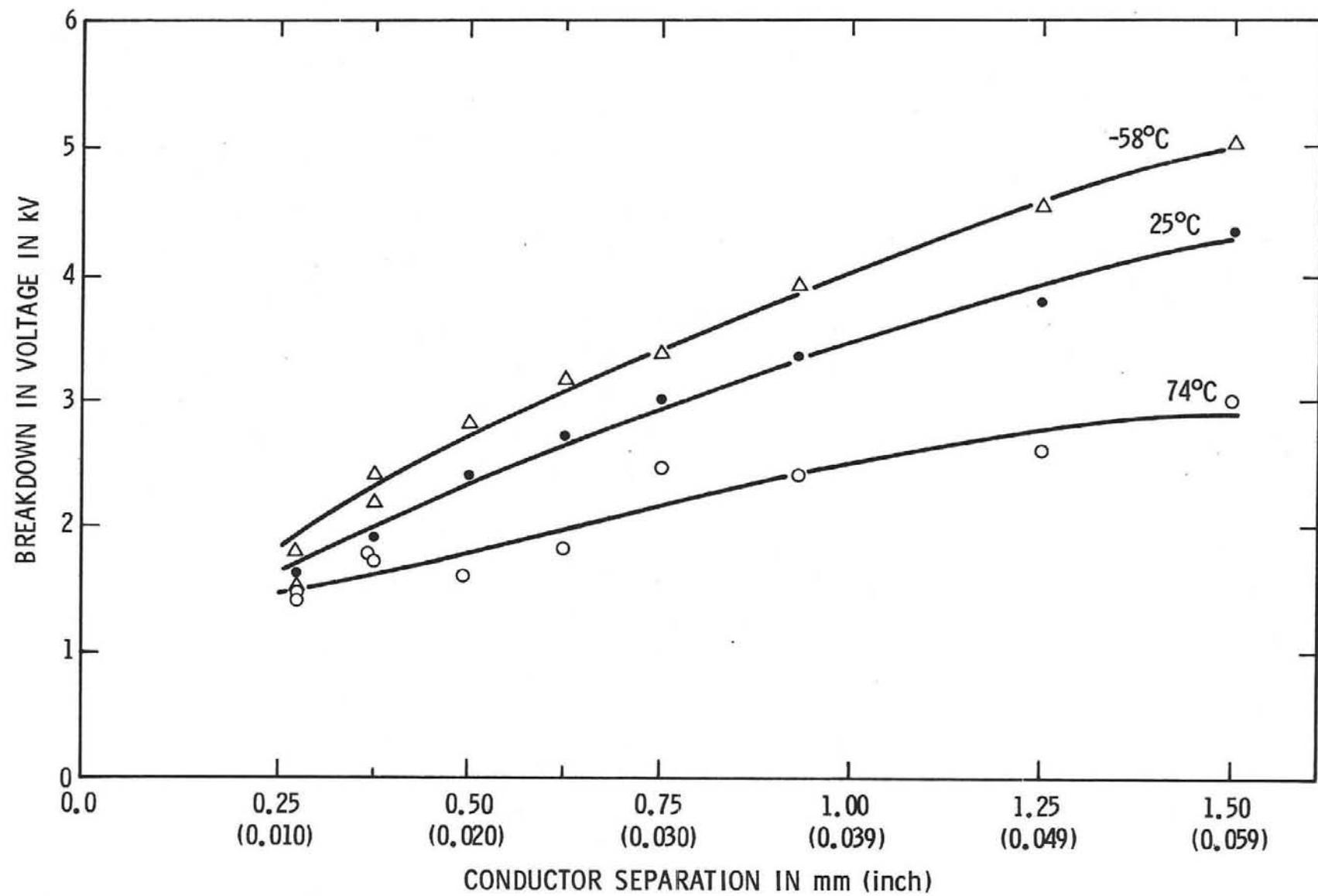


Figure 6

Effect of Temperature on Breakdown Voltage for Different Conductor Separations at 83 kPa

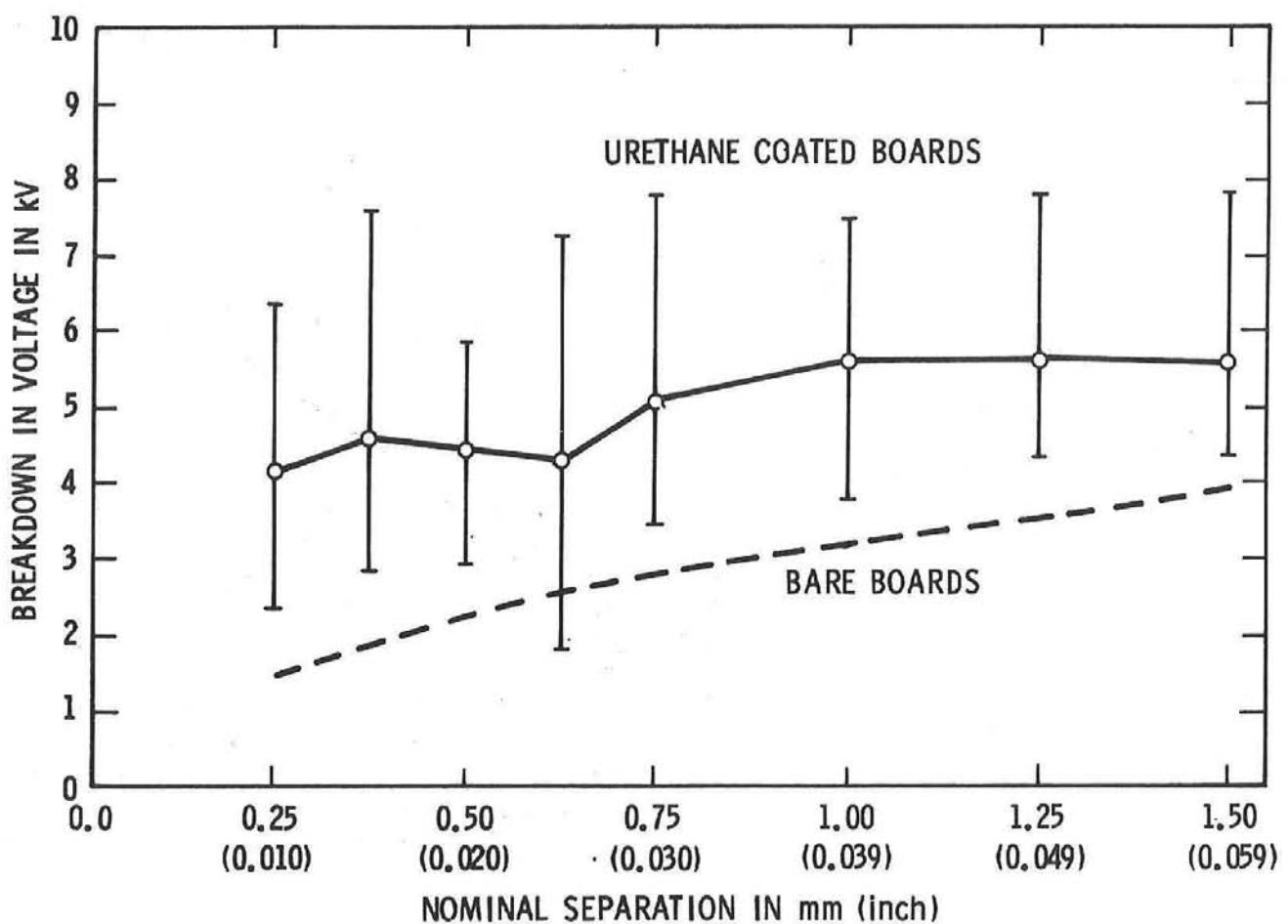


Figure 7

Voltage Breakdown of Urethane Coated Boards at 24°C and  
83.5 kPa

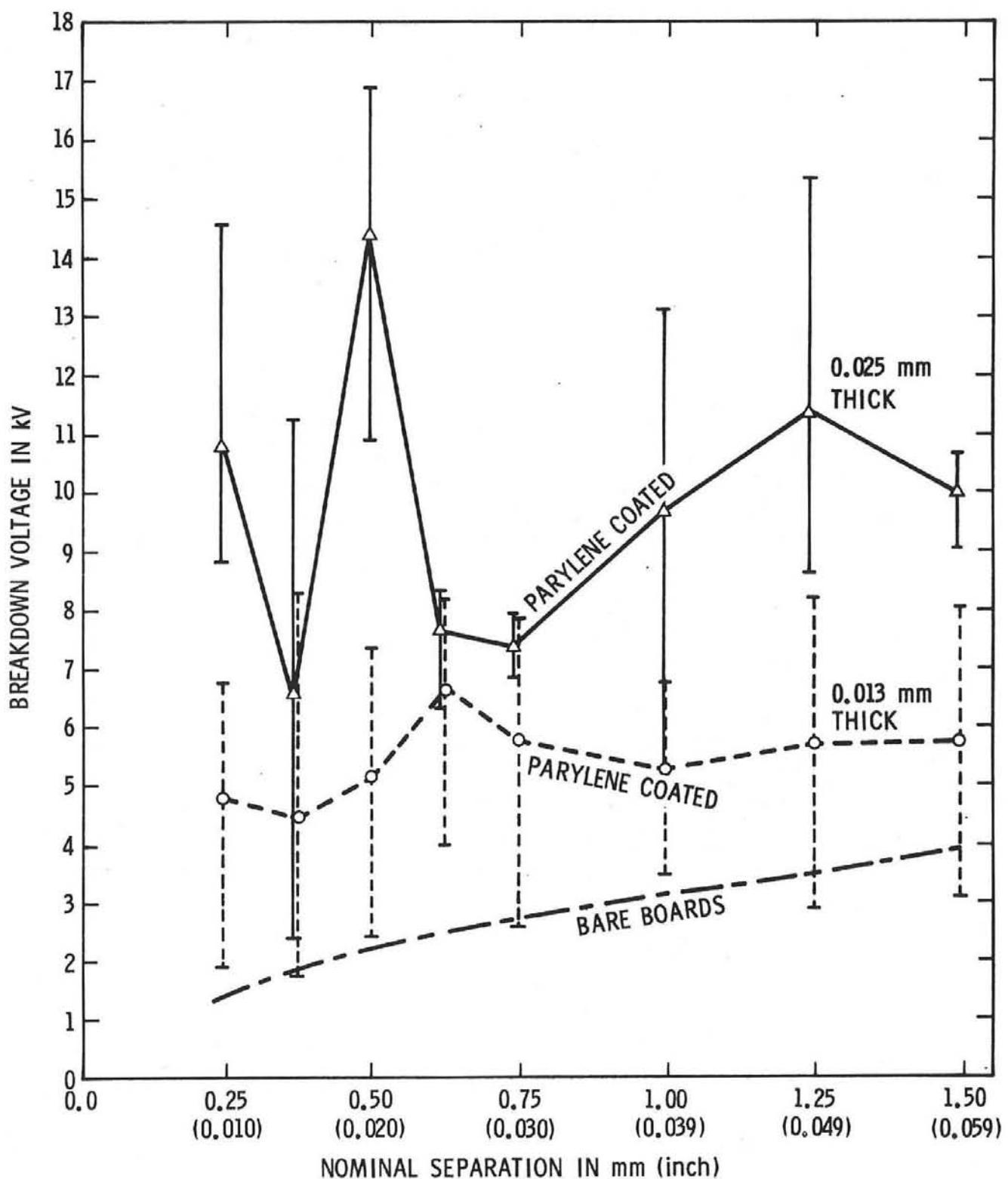


Figure 8

Voltage Breakdown of Parylene Coated Boards at  $24^{\circ}\text{C}$  and  
83.5 kPa

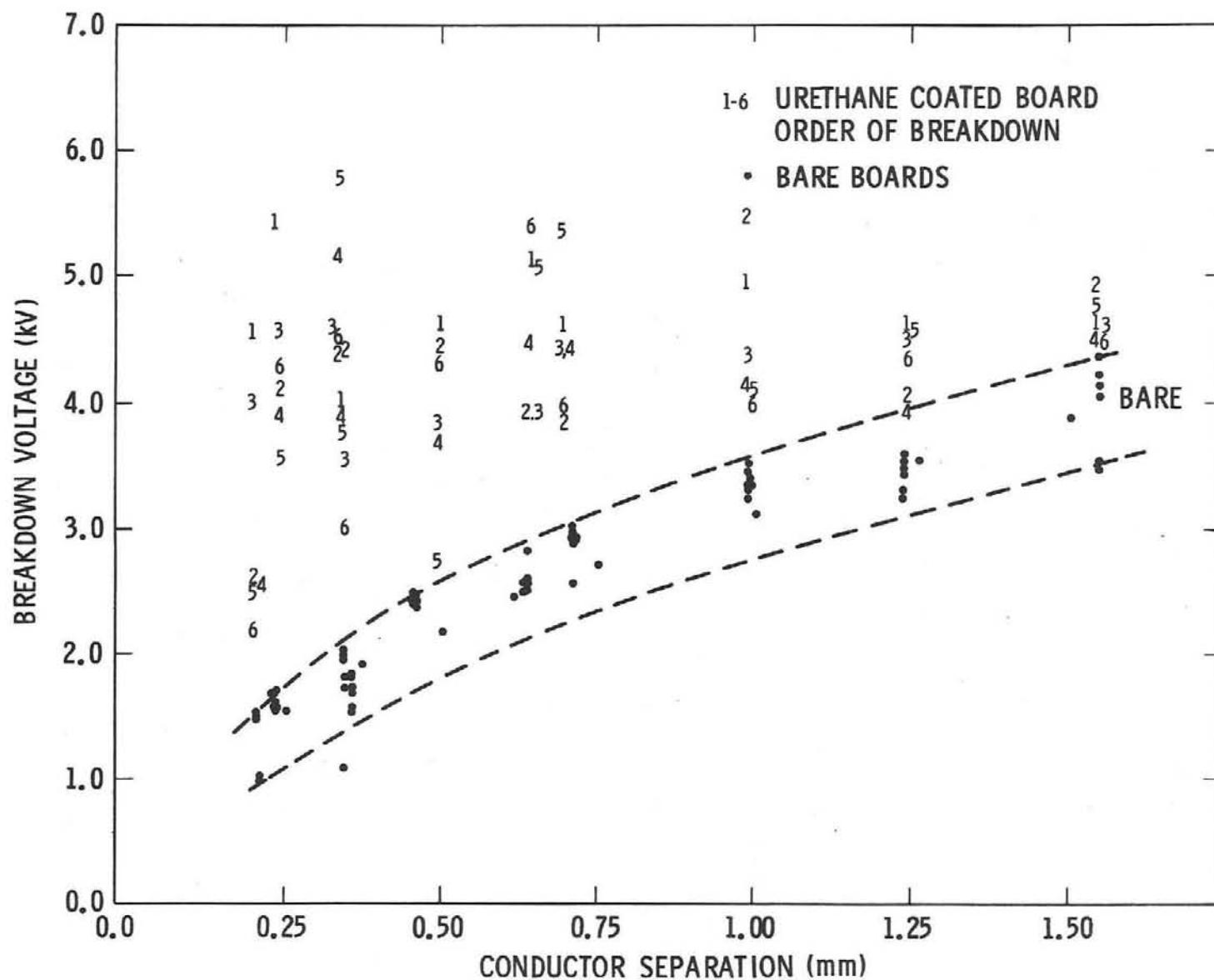


Figure 9

Effect of Repeated Voltage Breakdowns of Bare and Coated Boards at 83 kPa and 24°C

joint with cellulose acetate it was possible to increase the voltage of subsequent breakdowns by several hundred volts.

Breakdown voltages for encapsulated boards at low pressure are given in Table 4. Breakdown still occurred between the leads on foamed boards at low pressure, so the values in Table 4 may be lower than the true voltage holdoff between conductors. Again there was no correlation indicated between breakdown voltage and conductor separation. Coating a board with Parylene prior to epoxy foaming was beneficial both for low and ambient pressure breakdowns.

Breakdown voltages for encapsulated boards at ambient pressure were in general higher, some considerably higher than for bare boards as shown in Table 5. The values in Table 5 for ambient pressure represent a second breakdown, the first occurred at low pressure. However, many of the low pressure breakdowns were between the leads so the values may not necessarily represent true breakdown voltage between conductors. One should regard the values as minimums. There is a very noticeable difference between the breakdown voltages of the GMB encapsulated boards at low and ambient pressure. This was unexpected and the several low voltage breakdowns can probably be attributed to a lack of adhesion between the encapsulant and the laminate. Poor adhesion permitted a thin gap to form at the laminate-encapsulant interface between a few sets of conductors when the pressure was lowered.

The results of this study and published data indicated that the conductor spacing recommendations in MIL-STD-275 and IPC-ML-910A and IEC326, reproduced here as Table 6, and Figure 10 are very conservative, and can be reduced for applications in which circuit pattern space is limited.

TABLE 4  
Breakdown Voltage in Kilovolts of Encapsulated PWB's at 24°C and 660 Pa

Encapsulation	Board #	Nominal Separation in mm (inch)									
		0.25E (0.010)	0.25M (0.010)	0.38M (0.015)	0.38E (0.015)	0.50 (0.020)	0.63 (0.025)	0.75 (0.030)	1.00 (0.040)	1.25 (0.049)	1.50 (0.059)
Epoxy Foam	19	---	0.85	1.5	0.7	1.0	0.8	0.7	2.4	0.6	2.2
	202	1.1	1.4	1.3	1.4	1.5	1.75	1.1	1.25	1.6	1.55
Urethane Foam	108	3.9	1.7	---	6.0	4.9	7.7	8.9	8.2	11.7	4.7
Parylene Coating Epoxy Foam	201	6.7	6.2	4.3	---	3.7	3.7	2.7	9.2	3.9	3.4
Parylene Coating Urethane Foam	113	---	1.9	1.9	4.2	13.5	4.8	2.1	6.9	2.9	2.6
Urethane Coating Urethane Foam	110	2.9	0.6	2.8	2.1	---	3.2	2.0	2.5	1.8	1.3
Epon 828/DEA/GMB	43	12.4	20.2	17.6	16.1	21.3	18.8	> 25	> 25	21	17
	117	3.6	0.8	0.65	1.5	4.2	3.2	0.6		5.9	3.8

E = Edge Conductors

M = Mid Pattern Conductors

TABLE 5

Breakdown Voltages in Kilovolts of Encapsulated PWB's at 24°C and 84 kPa

<u>Encapsulation</u>	<u>Board #</u>	<u>Nominal Separation in mm (inch)</u>									
		<u>0.25E</u> <u>(0.010)</u>	<u>0.25M</u> <u>(0.010)</u>	<u>0.38M</u> <u>(0.015)</u>	<u>0.38E</u> <u>(0.015)</u>	<u>0.50</u> <u>(0.020)</u>	<u>0.63</u> <u>(0.025)</u>	<u>0.75</u> <u>(0.030)</u>	<u>1.00</u> <u>(0.040)</u>	<u>1.25</u> <u>(0.049)</u>	<u>1.50</u> <u>(0.059)</u>
Epoxy Foam	19	---	1.4	1.2	1.8	2.3	2.4	2.7	3.1	3.8	3.7
	202	0.6	0.4	0.9	0.9	1.3	2.0	1.8	3.5	11.3	9.6
Urethane Foam	108	2.3	5.0	---	3.9	9.8	5.1	4.2	5.9	4.4	5.2
Urethane Coating + Urethane Foam	110	---	3.5	1.8	3.1	---	6.9	2.4	9.4	8.5	10.1
Parylene Coating + Epoxy Foam	201	17.8	8.3	10.2	---	14.2	15.8	14.2	10.0	14.8	13.8
Parylene Coating + Urethane Foam	113	---	10.8	5.3	9.1	12.1	5.0	13.6	12.7	12.5	16.3
Epon 828/DEA/GMB	43	16.1	---	24	10	> 25	> 25	> 25	> 25	> 25	> 25
	117	11.1	12.6	13.3	20.6	22	22.4	9.2	9.2	16.5	23

E = Edge Conductors

M = Mid Pattern Conductors

TABLE 6

## Recommended Coplanar Conductor Spacing from IPC-ML-910A

The following shall be used to establish the required minimum spacing for the specific condition of the board application.

A. Conductor Spacing on Uncoated External Layers  
sea level to 10,000 feet inclusive

<u>DC or AC Peak Voltage Between Conductors</u>	<u>Minimum Spacing</u>
0 - 50 Volts	0.38 mm (0.015)
51 - 150	0.64 (0.025)
151 - 300	1.3 (0.05)
301 - 500	2.5 (0.10)
Greater than 500	0.005 mm (0.0002) per volt

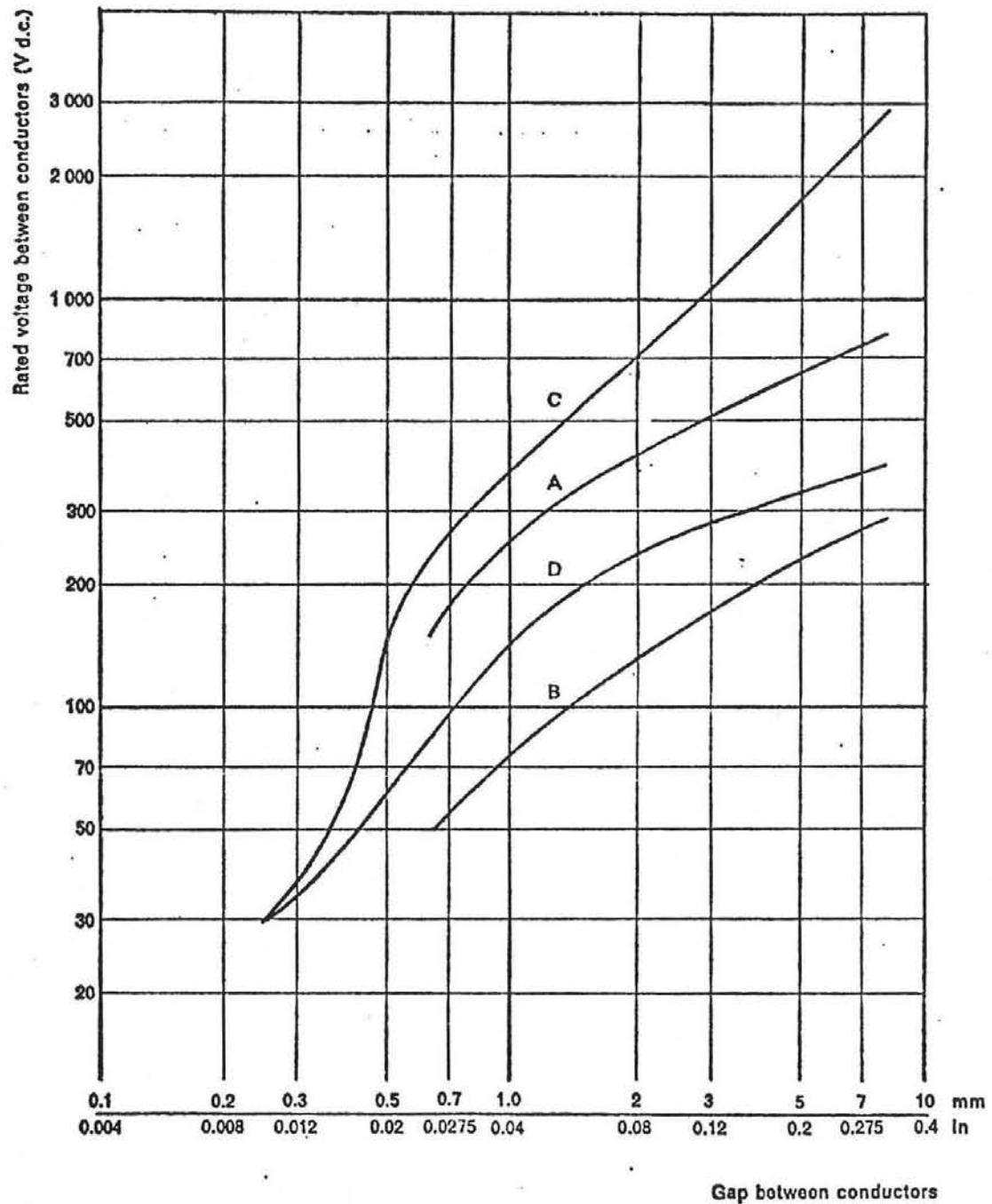
B. Conductor Spacing on Uncoated External Layers  
over 10,000 feet

<u>DC or AC Peak Voltage Between Conductors</u>	<u>Minimum Spacing</u>
0 - 50 Volts	0.64 mm (0.025)
51 - 100	1.5 (0.060)
101 - 170	3.2 (0.125)
171 - 250	12.7 (0.50)
Greater than 500	0.03 mm (0.001) per volt

C. Conductor Spacing on Internal and Coated External Layers  
any altitude\*

<u>DC or AC Peak Voltage Between Conductors</u>	<u>Minimum Spacing</u>
0 - 15 Volts	0.13 mm (0.005)
16 - 30	0.25 (0.010)
31 - 50	0.38 (0.015)
51 - 100	0.50 (0.020)
101 - 300	9.76 (0.030)
301 - 500	1.5 (0.060)
Greater than 500	0.003 mm (0.00012) per volt

\*Coating shall be in accordance with MIL-I-46058 when Section C is used for external layer conductor spacing.



- A** = uncoated up to and including 3 000 m (10 000 ft) altitude
- B** = uncoated over 3 000 m (10 000 ft) up to and including 15 000 m (50 000 ft) altitude
- C** = coated up to and including 3 000 m (10 000 ft) altitude
- D** = coated over 3 000 m (10 000 ft) altitude

Figure 10

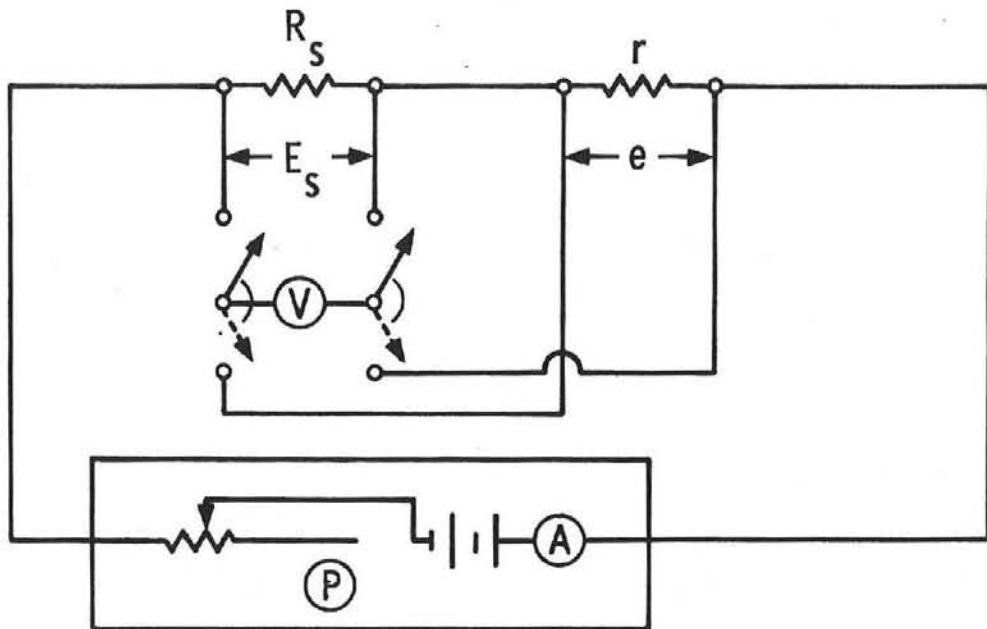
Rated Voltage Between Conductors (From IEC Publication 326)

## CURRENT CARRYING CAPABILITY OF PWB CONDUCTORS

The temperature rise associated with a fixed current in a PWB conductor is a function of conductor geometry and the thermochemical and heat transfer properties of the laminate and conductor. Temperature rise for a given current was measured from the change in electrical resistance of the conductor. Temperature rise could be calculated from an energy balance, however there were uncertainties in the thermal properties of the materials and several assumptions would have to be made to keep the calculations from becoming too complex. Resistance measurements are useful for circuit calculations and they also provide meaningful information on conductor geometry.

Conductor resistance was determined by a potential drop method. The potential across the conductor length as well as across a standard resistor was determined after the current had been established for 30 seconds. The circuit and instrumentation used are shown in Figure 11. The procedure for calculating the average conductor temperature rise from 25°C is given in Table 7. Current was increased in steps until a limiting current was reached for each conductor. Current steps were 0.1, 0.5, 1, 2, 4, 6, 8, 10, and 12 amps dc. Current was limited by conductor burn up, gross degradation of the laminate or encapsulation, and by the power supply. For a few boards a different dc power supply (Harrison 6264A) was used to provide additional current steps of 15, 18, and 20 amps. For the lower current steps a constant resistance was obtained after 30 seconds. At the limiting current step or whenever the resistance changed rapidly, resistance was measured after 600 as well as 30 seconds.

Five conductor widths each 25 mm (1.0) long were measured on each board. The widths consisted of two single conductors 0.25 and 1.25 mm wide on side 1A, a single conductor 0.51 mm(0.020) on side 2A, and two parallel conductors with



$(P)$  = HARRISON 6282A DC POWER SUPPLY  
HEWLETT-PACKARD 0-10V, 0-10A

$(V)$  = DANA MULTIMETER, MODEL 5900

$R_s$  = 0.010 ohm 15 amp STANDARD RESISTANCE

$r$  = CONDUCTOR ON PWB

$(A)$  = AMMETER FOR APPROXIMATING CURRENT

Figure 11  
Resistance Measurement Method

TABLE 7  
Temperature Rise Calculations

$E$  = Voltage across standard resistance,  $R_S$   
 $e$  = Voltage across conductor resistance,  $r$

$$I_1 = \frac{E_1}{R_{S_1}} = \frac{e_1}{r_1} = \text{Low current at Temperature } T_1$$

$$I_2 = \frac{E_2}{R_{S_2}} = \frac{e_2}{r_2} = \text{Current for Temperature } T_2$$

$$r_1 = \frac{e_1 R_S}{E_1} \text{ and } r_2 = \frac{e_2 R_S}{E_2}, R_S = \text{constant at } T_1 \text{ and } T_2$$

$$\frac{r_2}{r_1} = \frac{e_2/E_2}{e_1/E_1} = e_2/e_1 \cdot E_1/E_2 = \frac{r_{T_2}}{r_{T_1}}$$

$$r_{T_2} = r_{T_1} [1 + \alpha(T_2 - T_1)] = r_{T_1} [1 + \alpha\Delta T]$$

$$\Delta T = \frac{1}{\alpha} \left( \frac{r_{T_2}}{r_{T_1}} - 1 \right) = \frac{1}{\alpha} \left( \frac{r_2}{r_1} - 1 \right)$$

at 25°C

$$\alpha = 0.003854$$

$$\Delta T = 259.5 \left( \frac{\frac{e_2}{E_2}}{\frac{e_1}{E_1}} - 1 \right)$$

Example, if  $r_2 = 1.10 r_1$  or a 10% increase in resistance with current  $I_2$ , then  
 $\Delta T = 260 \left( \frac{1.10}{1} - 1 \right) = 26^\circ\text{C}$  temperature rise or average conductor temperature of  
 $51^\circ\text{C}$ , assuming no localized heat concentration.

0.38 (0.015) and 1.02 mm (0.040) segments on both sides. For a few boards measurements were made on a 2.5 mm (0.10) wide 25 mm (1.0) long single conductor on side 2A, and on 50 mm (2.0) long single conductors with widths ranging from 0.25 (0.010) to 2.5 mm (0.100). Current leads consisted of the largest size of copper wire which could be soldered into the hole. Separation between conductors was 4.4 mm (0.17).

Effective conductor widths were measured on a Nikon Measurescope at 30X. For the panel plated boards with conductor edge profiles similar to that shown in Figure 4., the effective conductor width is the distance from the mid point of one conductor edge to the mid point of the other edge. Average copper thickness was estimated from the average of beta backscatter measurements made on 2.5 mm (0.100) conductors on the same side of the board. Measurement error for widths is estimated to be 0.006 mm (0.0002) and for thicknesses, 0.005 mm (0.0002).

Resistances were calculated from cross sections and effective conductor lengths using copper resistivity at 25°C of 1.75 ohm-cm. The effective conductor length is the hole to hole length corrected for the terminal area contributions.

#### Bare Boards

Temperature rises corresponding to the different nominal conductor widths and currents are given in Tables 8 through 12. On Figure 12 temperature rise for the different current steps is plotted against measured conductor cross sectional area. Figure 13 shows the variation in temperature rise with current for different conductor widths and copper thickness corresponding to 2 oz copper (0.069 mm or 0.0027 inch thick).

The average slope of the log-log plots of temperature rise against current is  $2.25 \pm .1$  that is,  $\log \Delta T_2 / \Delta T_1 = 2.25 \log I_2 / I_1$ . For calculations of voltage

TABLE 8

Calculation of  $\Delta T$  from Resistance Change with Current for 0.25 mm (0.010) Conductor  
 i.e.  $\Delta T = [(R_{T_2} \div R_{25^\circ C}) - 1] \cdot 259.5$  from  $T_1 = 25^\circ C$

Board No.	Meas. w (mm)	wxt (mm) <sup>2</sup>	Calc. $R_{25^\circ C}$	Meas. $R_{25^\circ C}$	Current (Amps)						
					.5	1	2	$4^*_{30}$	$4^{**}_{600}$	$6^*_{30}$	$6^{**}_{600}$
5	0.216	0.0143	30.3	34.9	0.4	2.5	12.6	60		179	267
29	0.234	0.0148	29.1	33.7	0.6	2.9	13.8	79			
53	0.264	0.0196	22.0	25.9		4.3	11.7	46			
	0.203	0.0148	29.1	34.1	0.7	3.1	11.4	62			
101	0.112	0.0071	60.9	76.1	4	12	43	303	B		
125	0.150	0.0095	45.3	43.8	0.6	4.2	20	109			
149	0.140	0.0094	46.1	51.9	0.6	5.6	25	167	206		
172	0.102	0.0065	66.9	81.9	2.5	11.4	47	B			
193	0.224	0.0151	28.6	34.6		4.3	15.6	76		254	B
197	0.257	0.0157	27.6	27.8	0.5	3.7	12.0	57	64		
229	0.208	0.0154	28.1	27.7	0.4	2.7	10.8	50	62		
G	0.203	0.0179	24.2	24.3	0.2	2.1	8.6	44	54		
S-6	0.213	0.0154	28.0	32.3		1.7	9.7	53	66		
S-21	0.178	0.0155	27.7	32.5		1.9	10.5	51	63	153	
S-35	0.229	0.0215	20.1	20.2	0.8	5.8	30				
SLL-X	0.305	0.0166	25.9	25.6		9.5	37		90		

B ≡ Burn through, w ≡ width, t ≡ thickness       $w \times t$  ≡ cross sectional area

\*  $4_{30}$  and  $6_{30}$  = currents 4 and 6 amps for 30 seconds

\*\*  $4_{600}$  and  $6_{600}$  = currents of 4 and 6 amps for 600 seconds

TABLE 9

Calculation of  $\Delta T$  from Resistance Change with Current for 0.51 mm (0.020) Conductor  
 i.e.  $\Delta T = [(R_{T_2} \div R_{25^\circ C}) - 1] \cdot 259.5$  from  $T_1 = 25^\circ C$

Board No.	Meas. w (mm)	wxt (mm) <sup>2</sup>	Calc. R <sub>25°C</sub>	Meas. R <sub>25°C</sub>	Current (Amps)						
					1	2	4	6	8	10 <sub>30</sub>	10 <sub>600</sub>
Temperature Change (°C)											
5	0.478	0.0357	11.9	13.1	0.9	3.5	14.7	36	71	135	174
29	0.467	0.0324	13.2	14.9	0.3	3.1	17.4		92	194	
53	0.500	0.0317	13.4	15.7	0.7	4.3	19.8		104	206	B
77	0.432	0.0310	13.7	14.0		3.8	18.4	48	94	183	
101	0.348	0.0281	15.1	15.8	1.9	5.8	22	54	115	242	B
125	0.396	0.0243	17.6	18.7	1.4	6.7	31	84	170		
149	0.371	0.0203	21.0	24.3		5.8	35		B		
172	0.361	0.0234	18.2	19.3	0.9	4.5	27		165		
193	0.465	0.0334	12.7	14.1	0.7	4.4	20	56	102	201	
197	0.452	0.0299	14.3	16.0	1.0	3.9	21		115	251	
229	0.465	0.0282	15.1	16.1		2.7	19		113	230	B
G	0.478	0.0412	10.3	10.2		2.1	10.5	25	49	86	
S-6	0.427	0.0298	14.3	16.7	1.2	4.2	20		102	204	
S-21	0.460	0.0385	11.1	12.6		2.3	13		67	124	
S-35	0.478	0.0419	10.2	10.9		3.4	12.8	32	61	109	
SLL-X	0.478	0.0275	15.5	14.2	16	1.0	15.5	38	79	213	

TABLE 10

Calculation of  $\Delta T$  from Resistance Change with Current for Two 0.38 mm (0.015) Conductors in Parallel  
 i.e.  $\Delta T = [(R_{T_2} \div R_{25^\circ C}) - 1] \cdot 259.5$  from  $T_1 = 25^\circ C$

Board No.	Meas. w (mm)	wxt (mm) <sup>2</sup>	Calc. R <sub>25°C</sub>	Meas. R <sub>25°C</sub>	Current (Amps)						
					2	4	6	8	10	12 <sub>30</sub>	12 <sub>600</sub>
					Temperature Change (°C)						
5	0.676	0.0477	8.93	9.58	2.3	9.4		41	77	139	153
29	0.709	0.0470	9.20	9.67	1.9	8.3	21	40	69	103	147
53	0.765	0.0527	8.20	8.88	1.5	8.9		38	73	118	138
77	0.660	0.0480	9.00	9.26	1.9	8.2	23	47	78	126	165
101	0.483	0.0348	12.4	13.8	5.1	19		84	167	316	B
125	0.572	0.0356	12.1	11.9	1.7	12.6	29	58	109	194	
149	0.518	0.0316	13.7	14.0	2.6	15.1		82	159		
172	0.488	0.0399	12.8	14.2	4.8	20		96	181	B	
193	0.696	0.0485	8.91	9.90	2.4	10.3	24	46	80	152	190
197	0.686	0.0436	9.91	10.5	1.6	9.6		53	118	166	215
229	----	-----	-----	-----	---	-----	--	--	---	---	---
G	0.655	0.0564	7.66	7.43	1.3	7.2		34	60	97	114
S-G	0.681	0.0484	8.93	8.91	2.0	9.4		41	74	117	137
S-21	0.663	0.0590	7.33	7.35	.9	5.3	14	27	44	68	
S-35	0.732	0.0659	6.55	6.46	1.2	6.4	15	27	51	80	
SLL-X	0.805	0.0525	8.23	8.06	1.8	7.9	20	36	64	103	156

TABLE 11

Calculation of  $\Delta T$  from Resistance Change with Current for 1.27 mm (0.050) Conductor  
 i.e.  $\Delta T = [(R_{T_2} \div R_{25^\circ C}) - 1] \cdot 259.5$  from  $T_1 = 25^\circ C$

Board No.	Meas. w (mm)	wxt (mm) <sup>2</sup>	Calc. R <sub>25°C</sub>	Meas. R <sub>25°C</sub>	Current (Amps)						
					2	4	6	8	10	12 <sub>30</sub>	12 <sub>600</sub>
5	1.214	0.0802	5.26	5.90	0.6	3.8	19	32	51	65	
29	1.232	0.0783	5.39	5.78	0.4	3.0	8.9	18	30	48	65
53	1.262	0.0939	4.49	4.95	0.6	3.3	8.0	15	25	38	51
77	1.227	0.0897	4.70	4.85	0.6	3.3	7.2	14.3	24	38	49
101	1.113	0.0706	5.97	6.69	0.8	4.9	11.5	23	39	63	82
125	1.120	0.0712	5.92	6.27		4.8	12	24	40	63	75
149	1.135	0.0761	5.54	5.97	0.9	1.8	10.2	19	32	50	
172	1.102	0.0700	6.02	6.12	0.9	4.5	10.9	21	46	54	
193	1.234	0.0834	5.05	5.58	0.9	4.1	10.3	19	32	49	62
197	1.268	0.0776	5.43	5.35	0.4	3.8	10.0	21	34	53	60
229	1.242	0.0916	4.60	4.25	0.7	3.5	8	15	27	42	50
G	1.214	0.1042	4.04	3.95	0.4	3.1		15.3	27	37	55
S-6	1.219	0.0883	4.78	4.73	0.6	3.9		18	33	49	
S-21	1.212	0.1061	3.97	4.35	0.4	2.5	6.4	12	21	31	
S-35	1.245	0.1170	3.60	3.74	0.6	2.8	6.5	12	21	29	47
SLL-X	1.328	0.0729	5.78	5.91	0.8	3.9	9.8	19	31	48	

TABLE 12

Calculation of  $\Delta T$  From Resistance Change with Current for Two 1.01 mm (0.040) Conductors in Parallel

$$\text{i.e. } \Delta T = [(R_{T_2} \div R_{25^\circ\text{C}}) - 1] \cdot 259.5 \text{ from } T_1 = 25^\circ\text{C}$$

Board No.	Meas. w (mm)	wxt (mm) <sup>2</sup>	Calc $R_{25^\circ\text{C}}$	Meas. $R_{25^\circ\text{C}}$	Current (Amps)						
					2	4	6	8	10	12 <sub>30</sub>	12 <sub>600</sub>
5	1.961	0.1381	3.08	3.35	0.7	2.6		10.6	18.8	29	38
29	1.956	0.1299	3.28	3.36	0.3	1.7	4.6	8.9	14	21	30
53	2.002	0.1387	3.07	3.27	0.4	1.8	4.3	8.4	14	21	29
77	1.941	0.1406	3.03	3.16		2.0	4.6	9.9	17	27	36
101	1.730	0.1248	3.41	3.68	0.4	2.4	5.0	12	20	31	46
125	1.814	0.1131	3.77	3.58	0.5	2.7	5.6	11.9	20	30	43
149	1.768	0.1103	3.86	4.08	0.6	4.2		16.1	27	42	51
172	1.750	0.1144	3.72	3.87	0.4	2.4	5.5	12.6	21	33	40
193	1.969	0.1337	3.19	3.35		1.2	4.0	7.9	13	21	
197	1.953	0.1243	3.43	3.77	0.5	2.6	5.3	11.6	20	30	
299	-----	-----	-----	-----	--	---	---	---	---	--	--
G	1.933	0.1677	2.54	2.54	0.3	1.5	3.6	8.8	15	21	32
S-6	1.938	0.1378	3.09	3.39		2.4		11.7	21	30	35
S-21	1.938	0.1697	2.51	2.50	0.4	1.6	3.5	6.4	10	16	
S-35	1.958	0.1761	2.42	2.34		1.5	4.0	8.5	15	23	30
SLL-X	2.063	(0.1561)	(2.73)	3.63	0.4	2.1		9.7	17	27	40

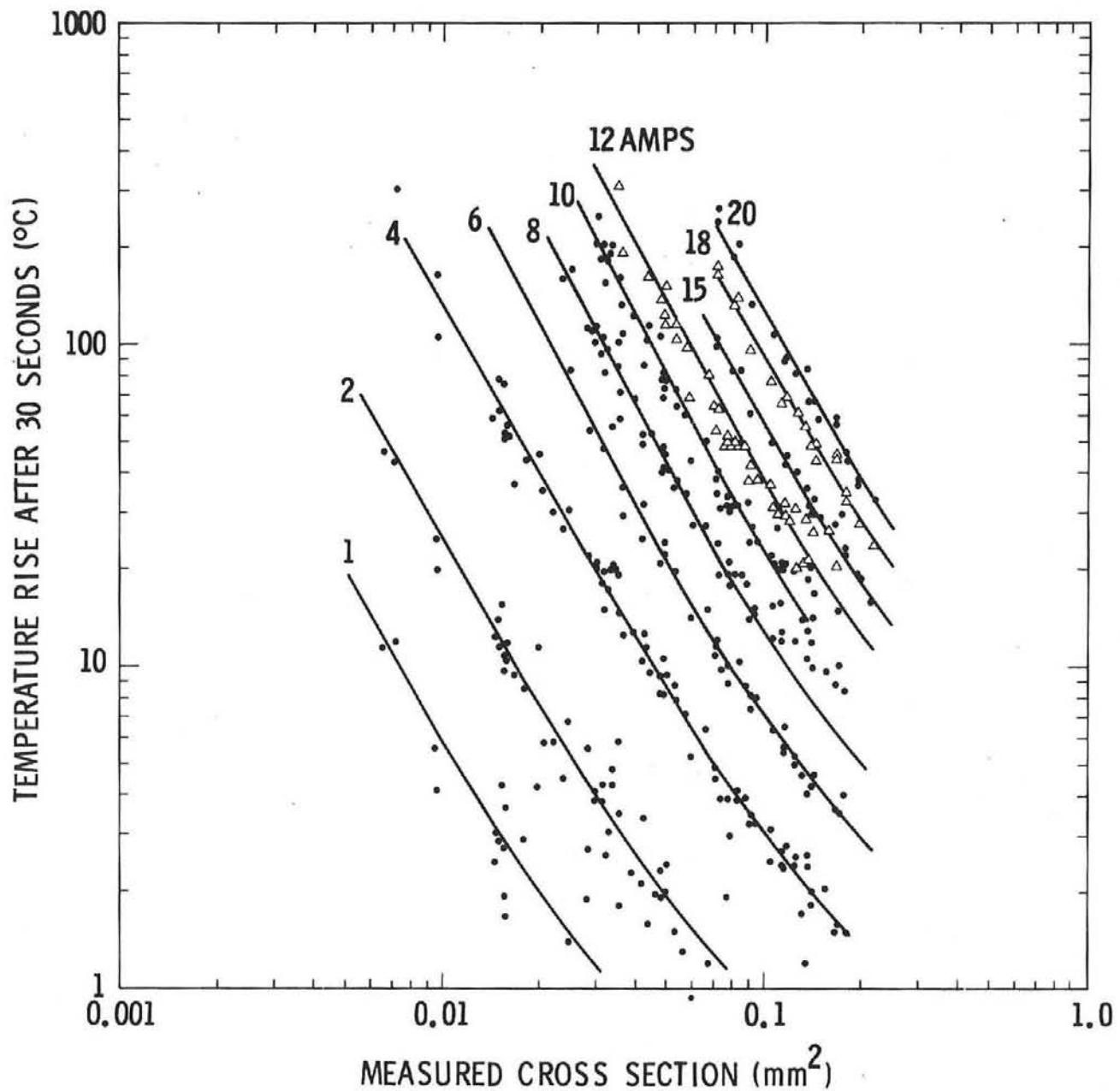


Figure 12

Temperature Rise for Different Currents and Cross Sectional Areas of Uncoated Conductors

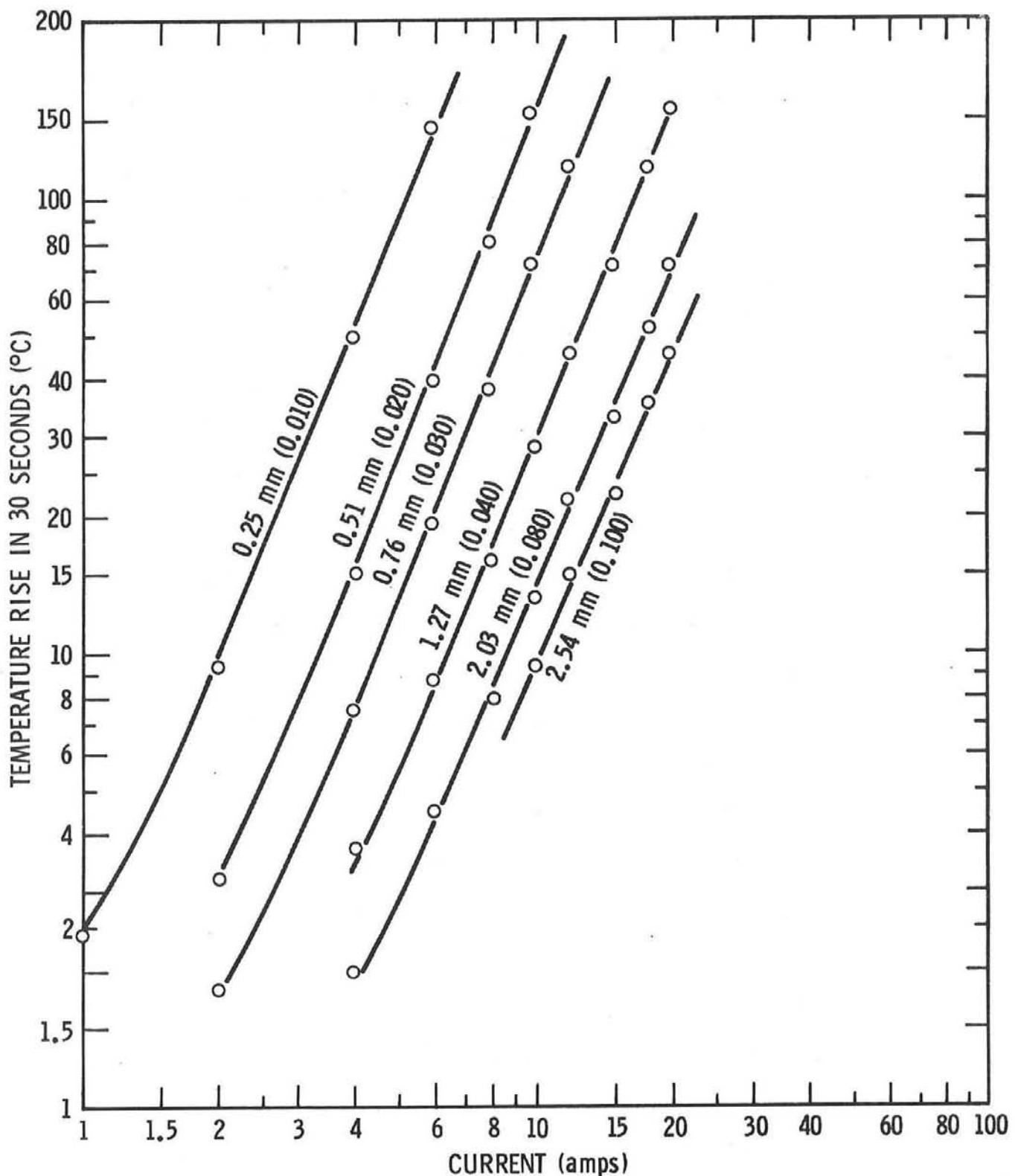


Figure 13

Temperature Rise for Different Currents and Conductor Widths and 0.069 mm (0.0027) Thick Copper

drop in a conductor it may be more convenient to use the percent change in resistance with current. This can be obtained by multiplying the temperature rise by 100  $\alpha$  where  $\alpha$  is the temperature coefficient of resistance of copper (0.00385 at 25°C). Figure 14 shows the percent change in resistance for the different current steps as a function of measured initial resistance expressed as milliohms per 25 mm (1.0) conductor length.

Tables 8 through 12 also tabulate calculated and measured resistances. The measured values average 4 to 10 percent higher than the calculated ones. There are two possible sources for the lower calculated resistance values; the positions at which the voltage leads were attached could have provided longer effective lengths than those used in the calculations and the average effective thickness may have been less than that provided by beta backscatter. The copper roughness at the laminate interface which is averaged into the copper thickness measurement by beta backscatter may not have made an equivalent contribution to the conductivity in the conductor. However, the differences are not large and with proper location of voltage leads resistance measurements should provide a very good and simple means for estimating conductor cross sections. The values should be more meaningful than optical measurements for circuit calculations.

Table 13 lists currents for different minimum allowable cross sectional areas which are estimated to generate temperature rises of 50 and 100°C in 30 seconds. Minimum cross sectional areas correspond to minimum clad and plating thickness [0.031 mm (0.0012) + 0.025 mm (0.0010)] and nominal widths less the etch factor [nominal width - 0.10 mm (0.004)].

The large variations in temperature rise for the same nominal width and current correspond to the large variations in the actual cross sectional area

TABLE 13

Current for 50° and 100°C Temperature  
Rise for Conductors with Nominal and  
Minimum Cross Sectional Areas

Nominal Width (mm)	Nominal* Cross Section (mm) <sup>2</sup>	Minimum** Cross Section (mm) <sup>2</sup>	Current (amps) for Temperature Rise of			
			50°C		100°C	
			Nominal	Minimum Cross Section	Nominal	Minimum Cross Section
0.25 (0.010)	0.017 <sup>4</sup>	0.0085	4	2.5	5.3	3
0.50 (0.020)	0.035	0.020	6.5	4.5	8.5	5.7
1.02 (0.040)	0.070	0.051	10.5	8.8	14	11
1.27 (0.050)	0.087	0.065	12.5	10	17	13
2.03 (0.080)	0.139	0.108	17.5	15	> 20	19
2.54 (0.100)	0.17 <sup>4</sup>	0.13 <sup>4</sup>	21	17	> 20	> 20

\*2 oz copper, 0.069 mm (0.0027) thick

\*\*(nominal width - etch factor) x (minimum clad + min plate thickness)  
= (nominal width - 0.10) x (0.031 + 0.025) mm<sup>2</sup>

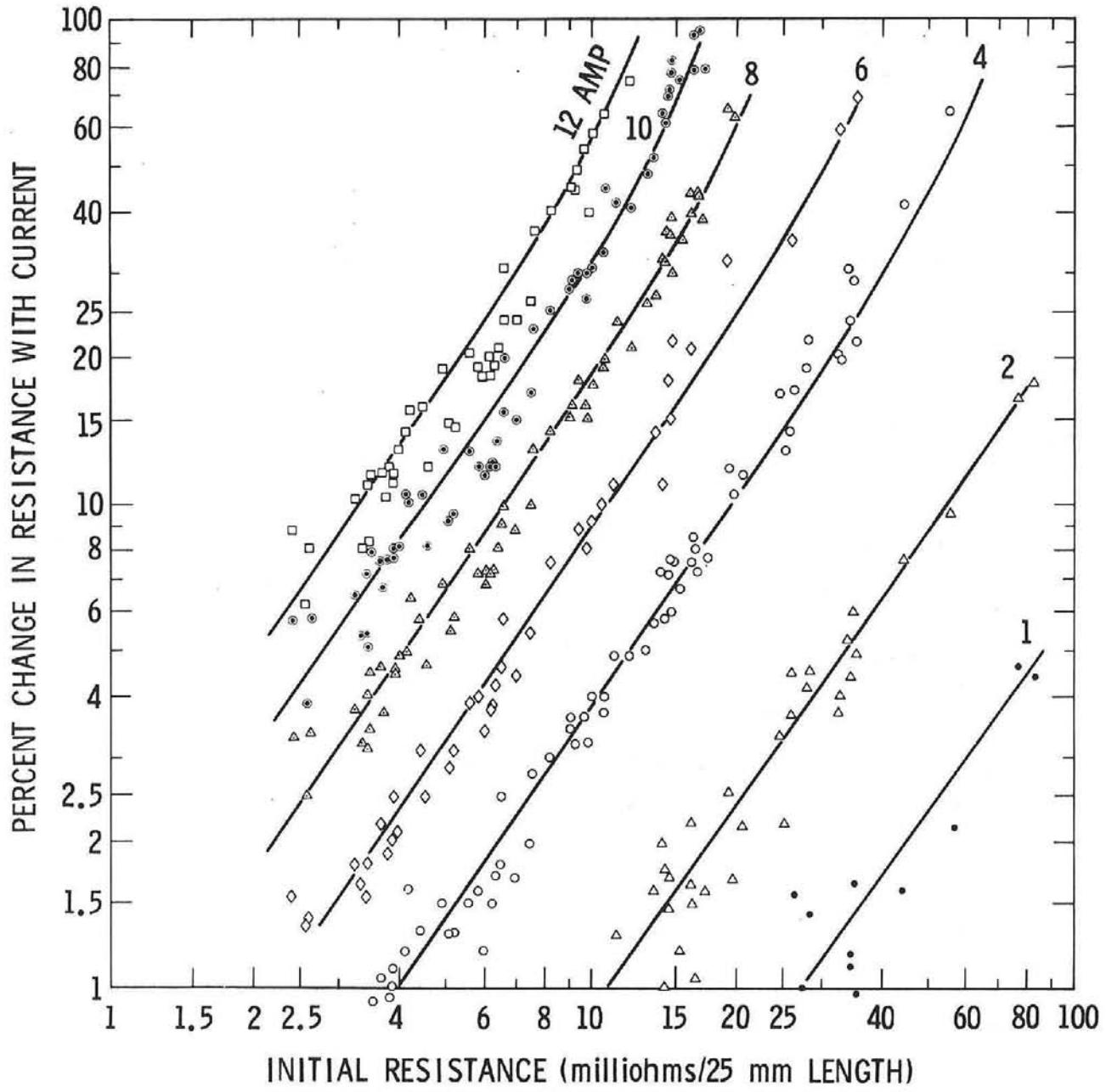


Figure 14

Percent Change in Resistance as a Function of Initial Resistance and Current Steps

of the conductors. These variations indicate the importance of good cross sectional area control during processing. For the narrow conductors width control is the important factor while for the wide conductors copper thickness is more important. For example, a nominal 0.25 mm (0.010) width which is reduced to 0.15 mm (0.006) by the etch factor has a 40 percent change in area, while a thickness change from a typical thickness of 0.69 mm (0.027) to the minimum thickness of 0.56 mm (0.022) causes a 19 percent change. For a 2.54 mm (0.100) nominal width the etch factor reduction to 2.44 mm (0.096) causes a 4 percent change, while the same thickness change as for the narrow conductor causes a 19 percent change in area.

Unless the copper plating in a hole is very thin, its resistance contribution is small compared to that of the conductors attached to it. For a minimum hole wall thickness of 0.025 mm (0.0010) and a minimum conductor thickness of 0.061 mm (0.0024) the conductor width must be 30 percent greater than the hole diameter for its conductivity to be comparable to that of the hole. Typical conductor widths are much less. Also, because the laminate thickness or through hole length is normally a small fraction of the total circuit path, the hole resistance contribution to the total circuit resistance is normally very small. Further, temperature rise is much less in a hole because of the heat dissipation of the terminal areas attached to it. This lower temperature rise in a hole was demonstrated by cutting one end of a parallel conductor and placing the hole in series with the two conductor segments attached to it. When the current was increased to the limiting value, the conductor segments showed degradation while the hole region was unaffected.

If however, the plating in a hole has very thin regions or contains breaks such as shown in Figure 15, but still shows electrical continuity, then local

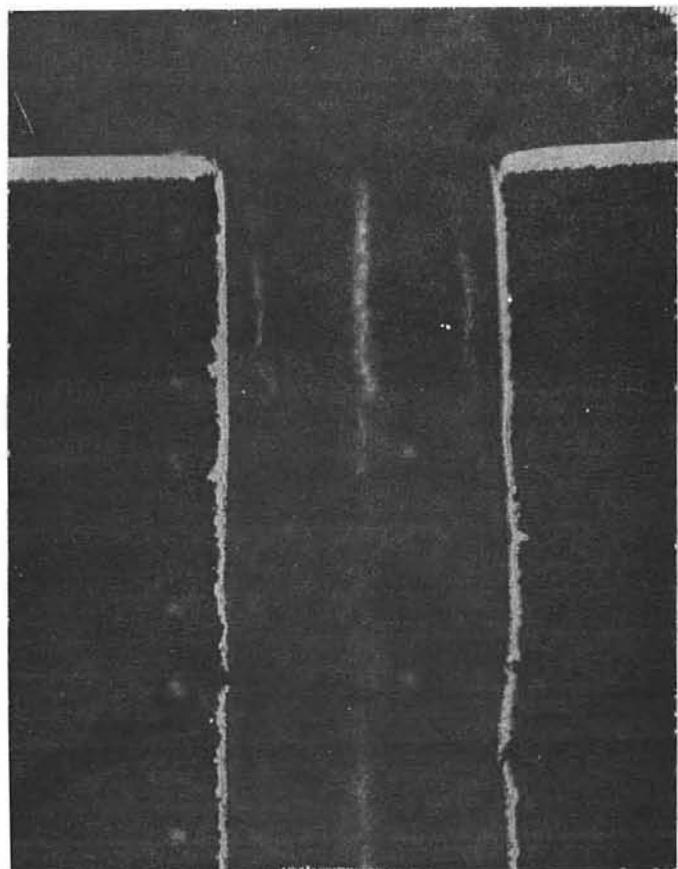


Figure 15

Plated-through Hole with Thin Copper and Breaks in the Plating

hot spots may develop which could result in circuit degradation or failure. On and off current applications to circuitry with such faults could provide a thermal cycling effect which may cause the copper to fatigue and ultimately rupture.

Temperature rises obtained in this study for the different currents and nominal widths are lower than those obtained from MIL-STD-275C and those reported by Noble (4), and Weick (5) for glass epoxy substrates. Figure 16 illustrates these differences for a 1.27 mm (0.050) conductor. The MIL-STD-275C curves include a 10 percent derating (on a current basis) to allow for normal variations in etching techniques, copper thickness, conductor width estimates, and cross sectional area. Curves in IEC 326 are similar to those in MIL-STD-275C. Noble used a 102 mm (4.0) conductor length and the smallest cross sectional area which was observed in five different specimens of the same width line and weight of copper. Weick's values are based on a 305 mm (12) length of conductor on G-10 laminate. No mention was made of how the conductor cross sections were measured. The time of measurement was not specified for the above results so it is assumed that steady state conditions were achieved which would indicate times of more than 30 seconds and correspondingly, higher temperatures. Figure 16 also shows measurements made on 50 mm (2.0) conductor lengths after 30 seconds and after thermal equilibration or when the resistance no longer changed with time. As seen from these results, the longer the conductor the smaller the effect of the heat drain from the leads and terminal areas.

As a check on the temperature calculations, temperature was measured at the mid point of a 25 mm (1.0) long conductor with 0.025 mm (0.001) diameter thermocouple wire. Temperature was within 1 to 2 percent of that obtained from the resistance change with current. The reproducibility of the latter is estimated to be 0.5 to 1 percent.

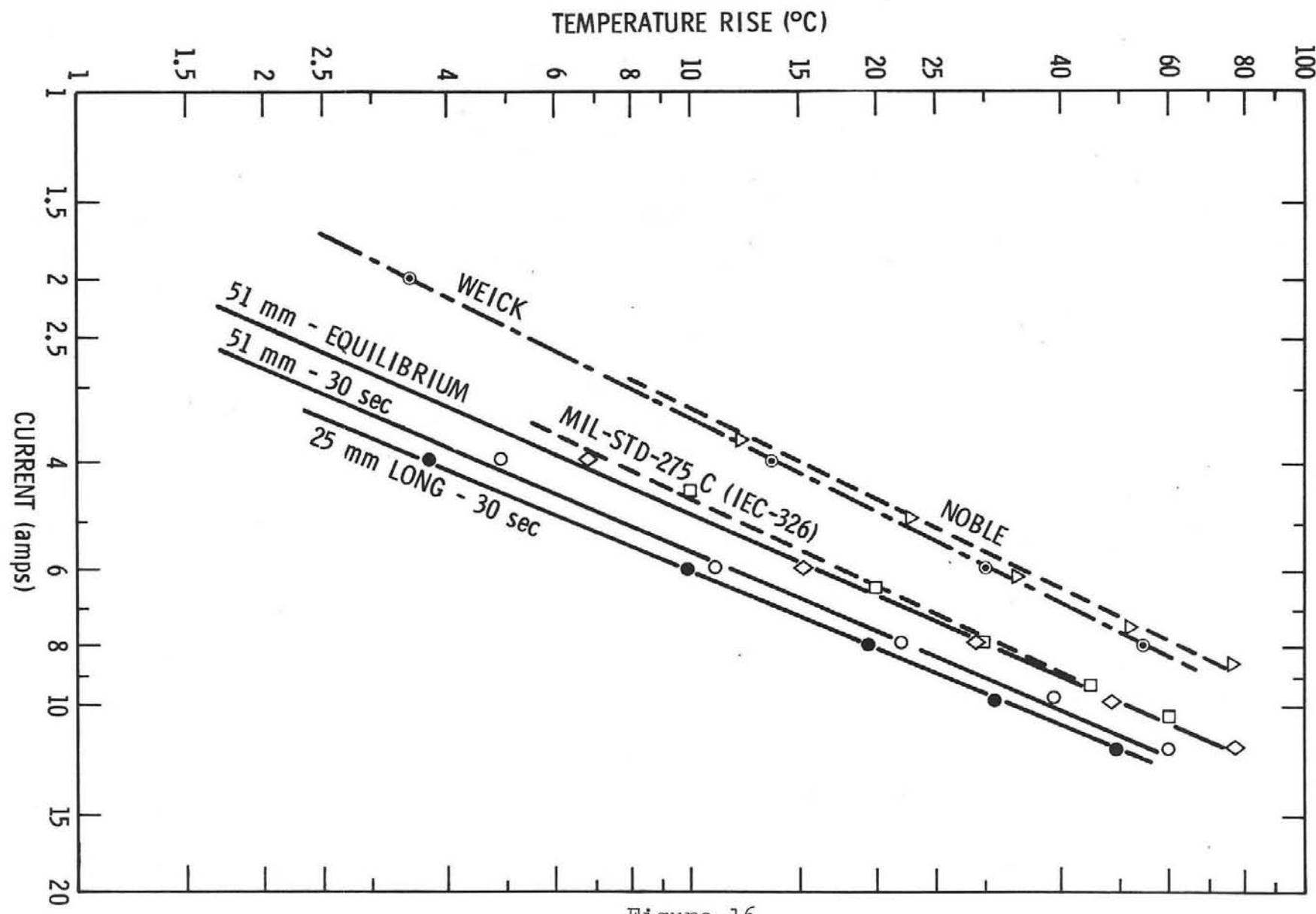


Figure 16

Comparison of Published Temperature Rise-Current Curves with Those of This Study for 1.27 mm (0.050) wide, 0.069 mm (0.0027) Thick Conductor

### Coated and Encapsulated Boards

Temperature rise curves for coated and encapsulated boards are essentially the same as those shown in Figure 12 for bare boards. Figure 17 compares the temperature rise values with current for a 1.27 mm (0.050) wide, 0.069 mm (0.0027) thick conductor on bare, coated, and encapsulated boards. At or above the limiting current the bare and coated conductors rapidly increase in temperature until they glow and burn through. Encapsulated conductors on the other hand increase more steadily in temperature until the encapsulation breaks down. Figure 18 compares the rate of temperature rise for parylene coated and GMB encapsulated conductors. The encapsulation provides an oxygen barrier which prevents the rapid oxidation of the conductors at high currents. As the conductor temperature increases, the polymer surrounding it degrades and pyrolyzes until the gaseous products generate sufficient pressure to explode or rupture the encapsulation. Figure 19 shows an explosive blowout around a 0.51 mm (0.020) conductor on a GMB encapsulated board after 120 minutes. Figure 20 shows an epoxy foam blowout around the same width conductor after 130 minutes. Figure 21 shows the beginning of degradation on a bare board.

If the current is cut off just as the conductor takes on a cherry red coloration or when the estimated conductor temperature is around 500°C, the resistance after cooling to room temperature is not over 10 percent greater than the initial room temperature resistance. This implies that if one cannot visually observe evidence of degradation around a conductor, it may be difficult to determine if an excessive current has been applied for a limited interval. The behavior of bare and encapsulated PWBs subjected to high currents for short intervals has been investigated by Hanchey (6). Conductor widths for currents to 80 amps have been investigated by Friar and McClurg (7).

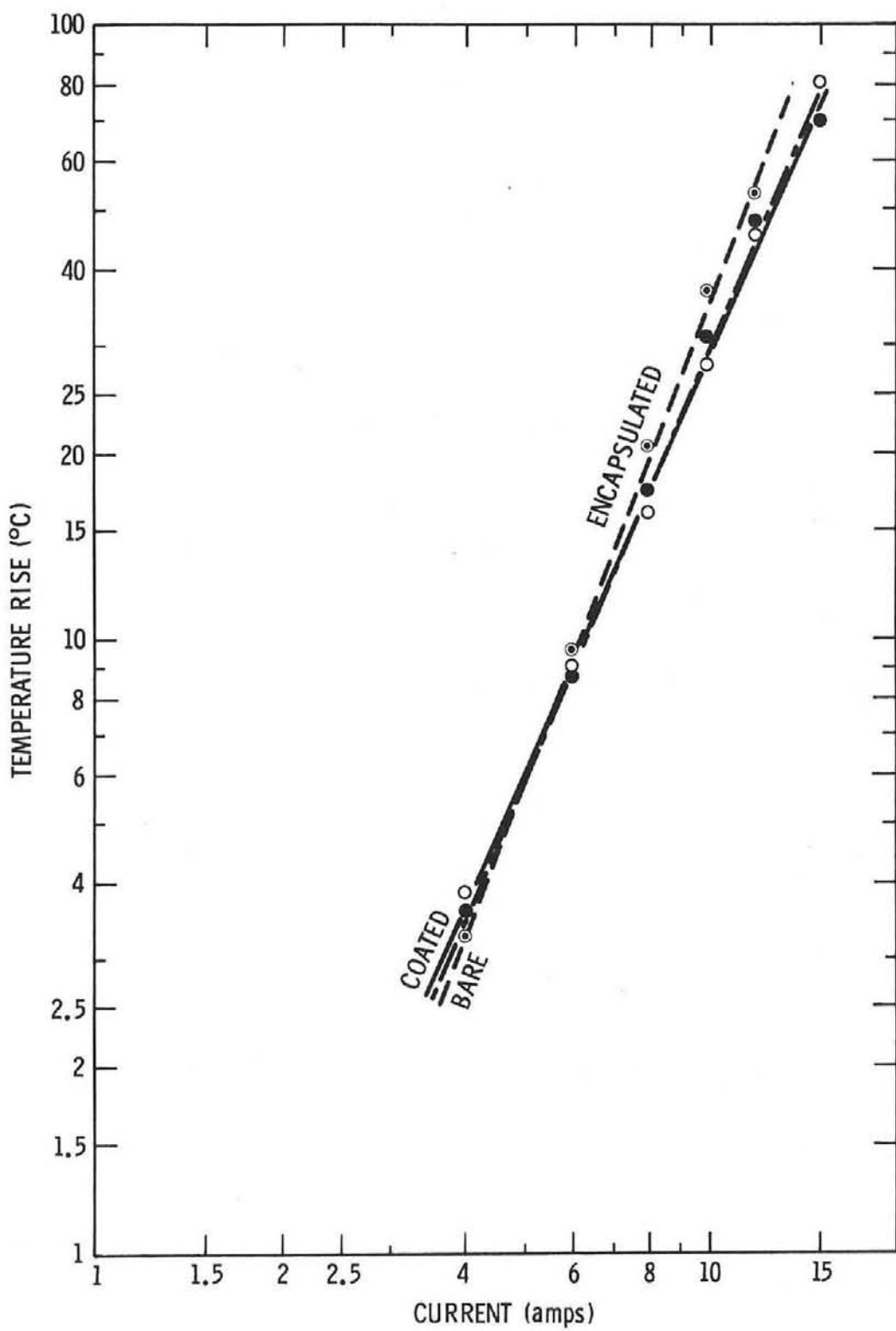


Figure 17

Comparison of Mean Temperature Rise with Current for a 1.27 mm (0.050) Wide, 0.069 mm (0.0027) Thick Conductor on Bare, Coated and Encapsulated Boards

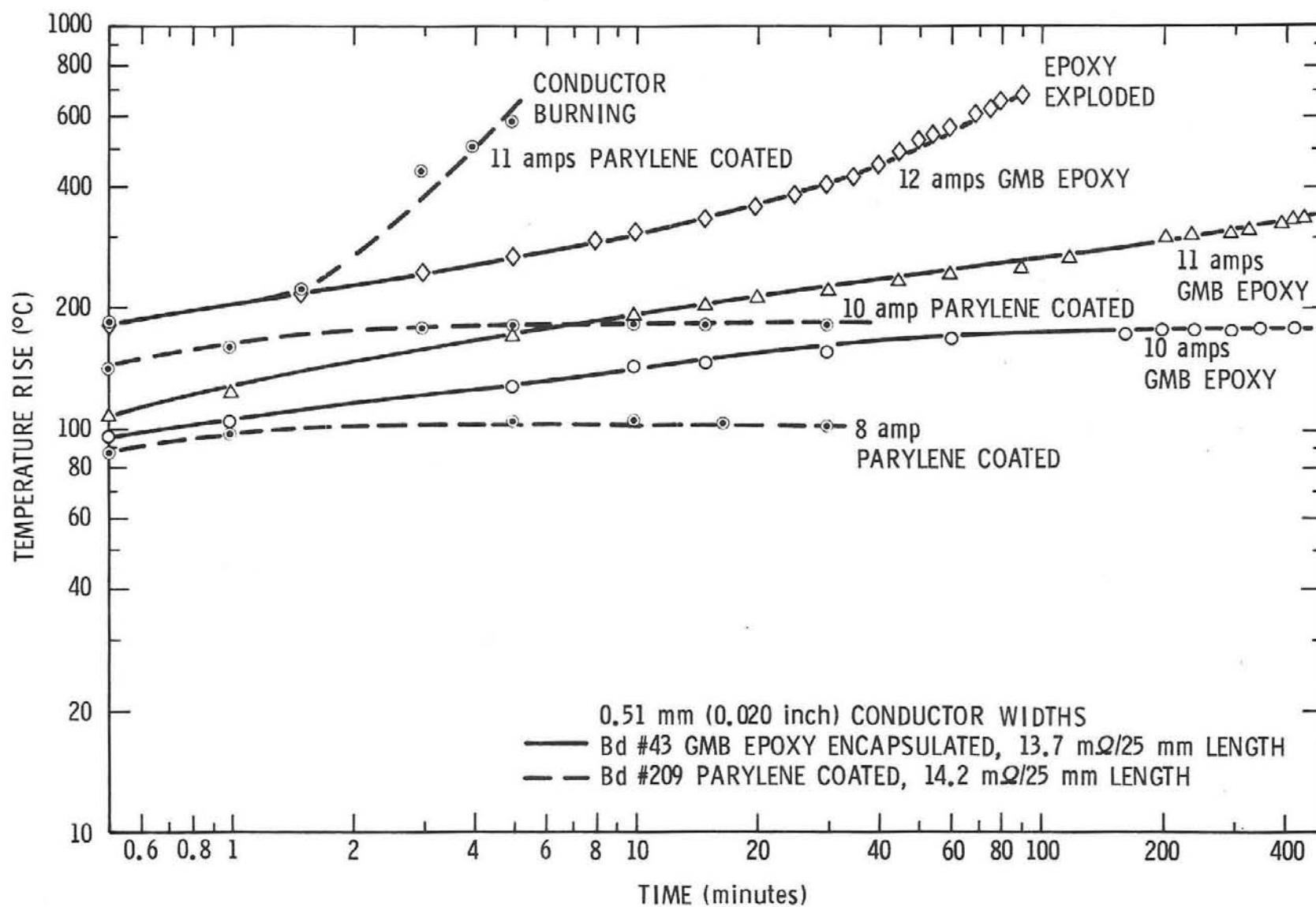


Figure 18

Comparison of Rate of Temperature Rise of a 0.51 mm (0.020) Wide Conductor on a Parylene Coated and a GMB Encapsulated Board

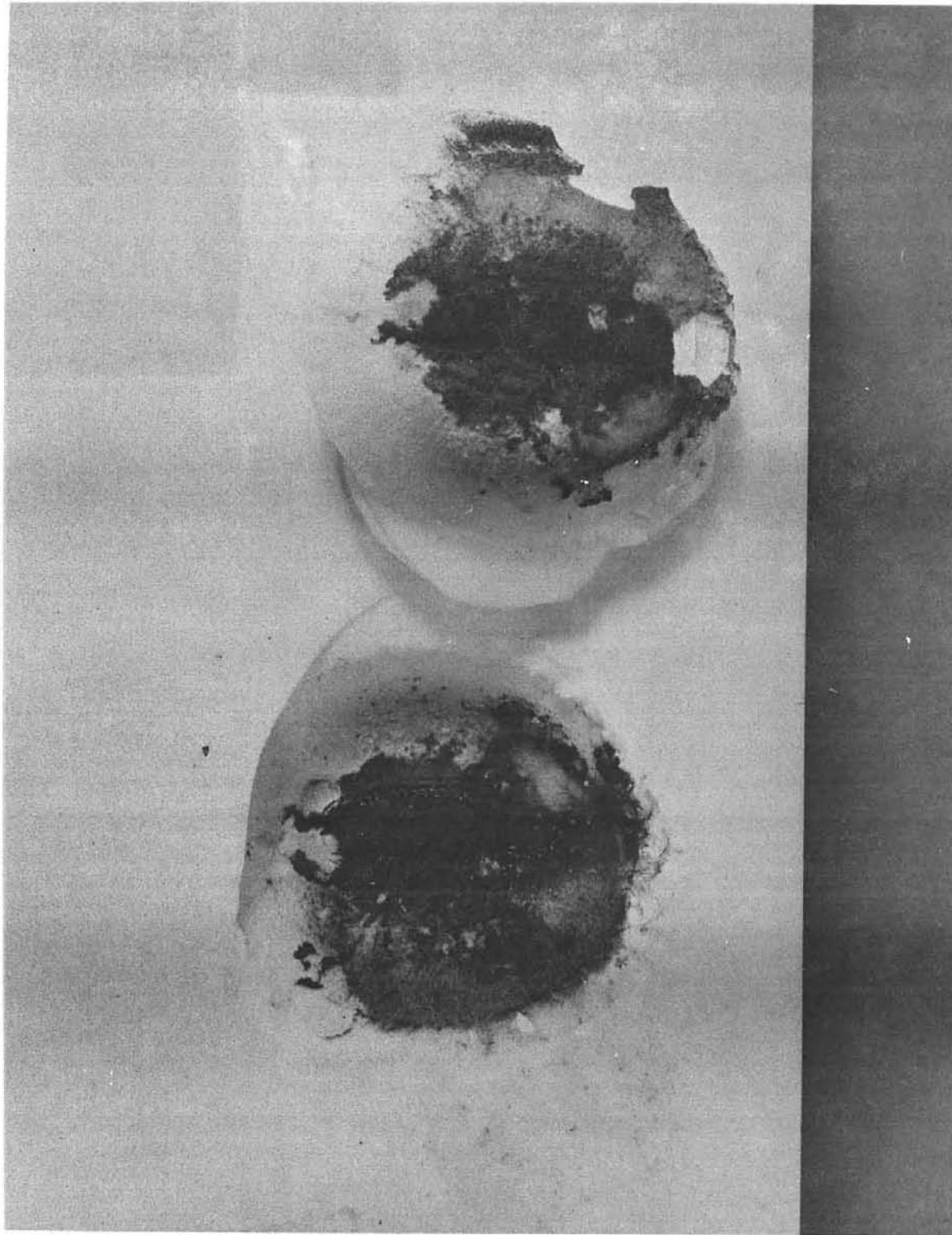


Figure 19  
Explosive Blowout Around Conductor on GMB Encapsulated Board

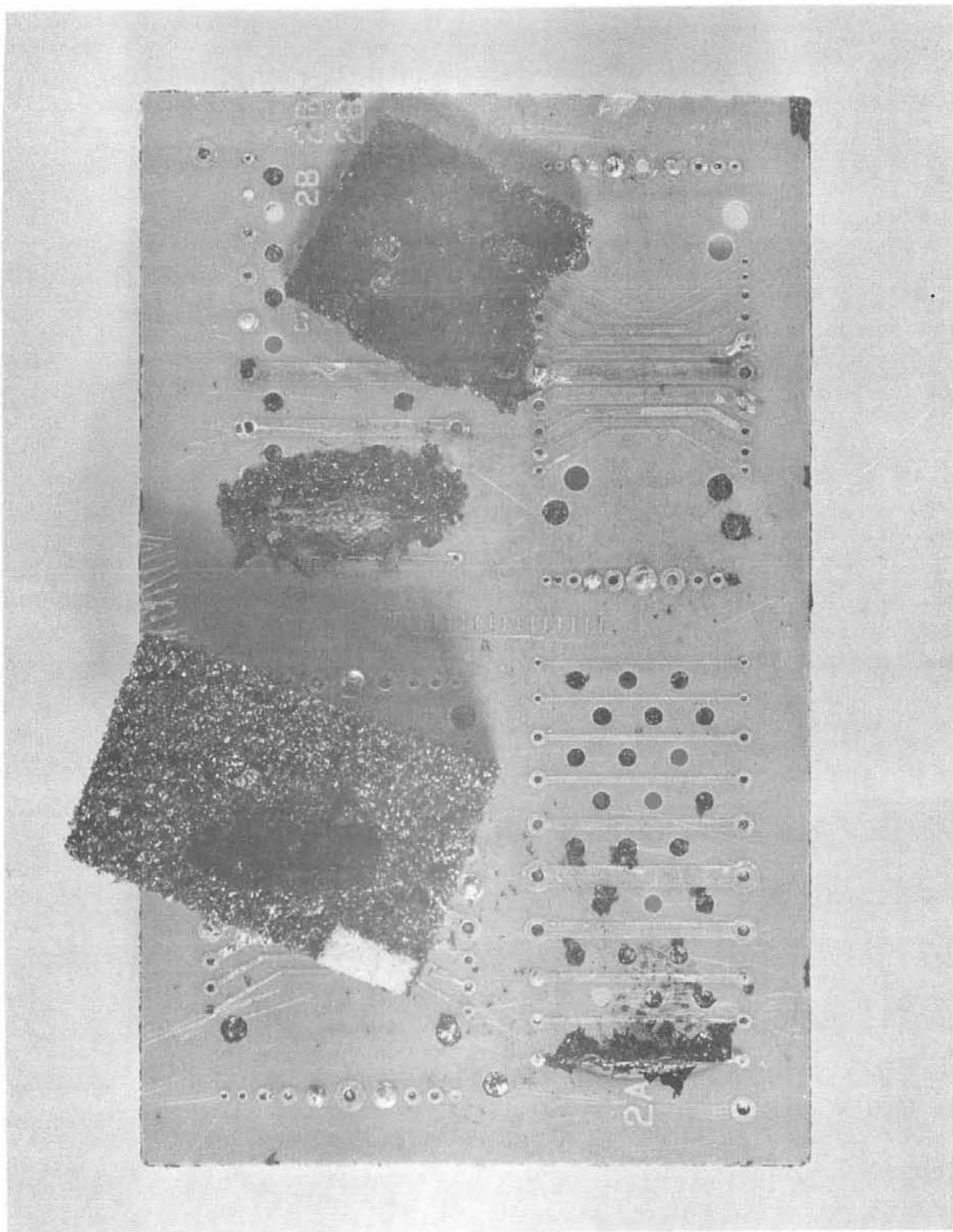


Figure 20  
Blowout Around Conductor on Epoxy Foam Board

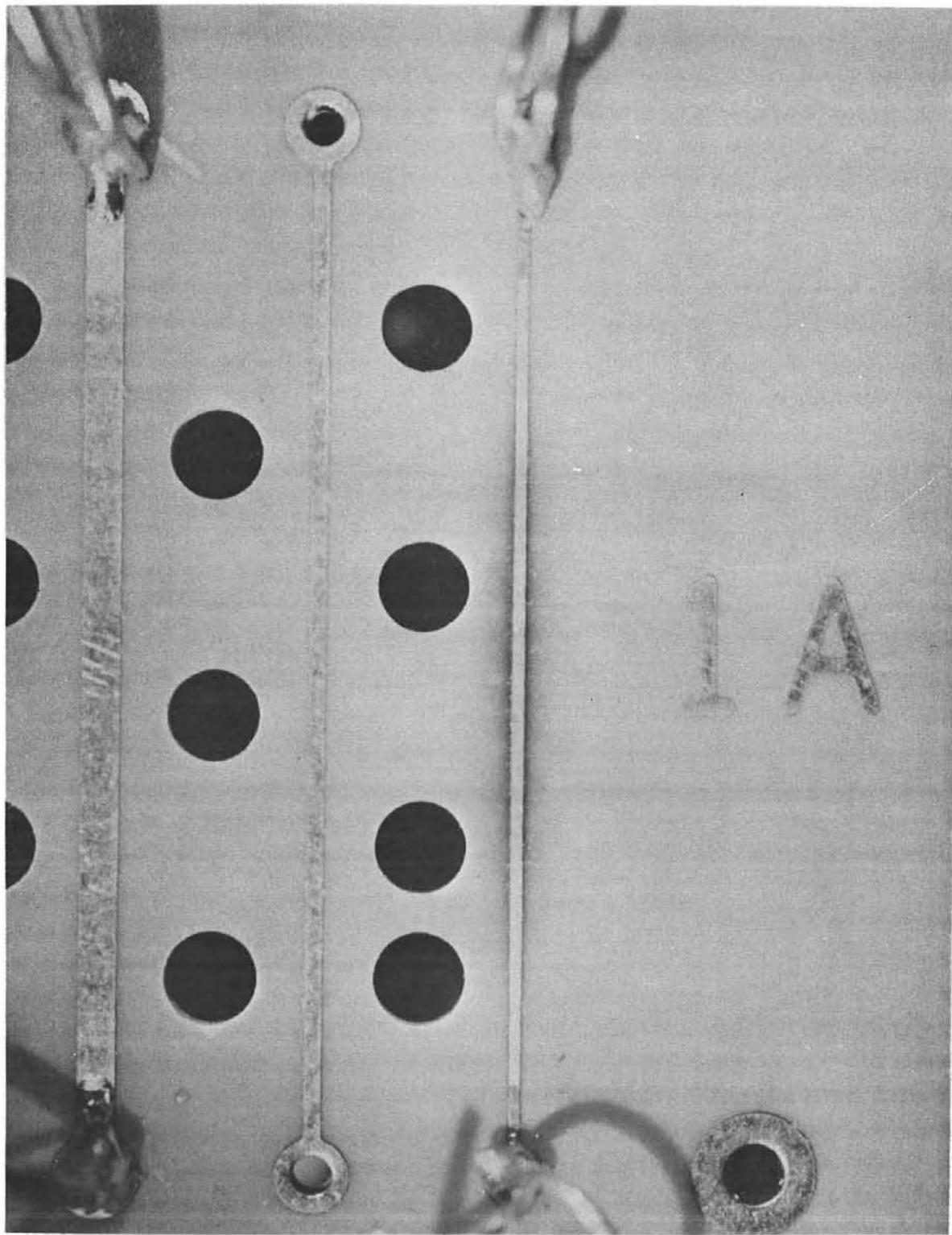


Figure 21  
Beginning of Thermal Degradation on Bare Board

## INSULATION RESISTANCE

Electrical resistance was measured, between the same conductors which were tested for voltage holdoff, in dry and humid environments. Dry environment was 10 to 30% RH; humid was 92 to 100% RH. All measurements were at room temperature, 22 to 24°C. Most of the measurements were made on a Guideline Model 9520 terahmmeter. A Keithly 610 CR was used for a few measurements and to confirm doubtful measurements made with the terahmmeter. Drift from capacitive effects was a problem for many of the measurements in the 10 to 100 teraohm region. A few minutes were allowed for stabilization in this region before the resistance was recorded. The values listed in Table 1<sup>4</sup> represent the average of 6 readings. Measurement voltage with the terahmmeter was 500 or 1000 volts. With the Keithly instrument, the measuring voltage could be as low as 20 volts. Measurement repeatability ranged from 10 to 50 percent in the high resistance region. During measurement the boards were either suspended in air or placed on a Teflon plate or on a glass rack.

The boards received no additional cleaning after a trichlorethylene vapor degrease at the end of the fabrication sequence. They received normal laboratory environment exposure. The flux from the resin cored solder (Kester SN 63, Core 58) used in attaching the leads was not removed. Two boards which were cleaned in isopropyl alcohol had resistances similar to those in the precleaned state. Boards which were coated or encapsulated were given a precleaning in trichloroethylene and isopropyl alcohol.

Table 1<sup>4</sup> lists resistances in teraohms for bare boards and the same boards after encapsulation. As there is no correlation between the separation and resistance for the same conductor length, resistivity calculations were not considered meaningful and only the factors for converting the resistances to

Table 14  
Insulation Resistance of Bare and Encapsulated Boards in Terachms

Board #	Dry (length/separation)							Humid (length/separation)							$\frac{\text{Hrs}}{\% \text{ RH}}$
	50/0.25	50/0.38	25/0.50	50/1.0	32/1.5	$\bar{x}$ /s.d.	50/0.25	50/0.38	25/0.50	50/1.0	32/1.5				
19	0.6	0.9	9	31	19	(12/13)									
43	9	7.5	7.5	7.5	6.5	(8/.9)									
108	12	24	5	15	19	(15/7)	0.004	-	0.02	0.02	0.23	72/93			
117	3.5	3	3	3	2.5	(3/.4)									
195	10	23	14	21	10	(16/6)									
202	2.5	3	3	4.5	6.5	(4/2)									
212	5.5	10	22	7	3.5	(10/7)	0.2	1	1	1.2	4	72/100			
X/s.d.	(6/4)	(10/10)	(9/6)	(13/10)	(10/7)	10									
19 + EF	1	1	1	17	10	(6/7)									
43 + GMB	26	20	17	19	15	(19/4)	-	-	43	4	15				
108 + UF	14	-	6	14	34	(17/12)	0.2	5	2	8	10	144/93			
117 + GMB	17	17	15	13	8	(14/4)									
202 + EF	1.5	1.5	1	2	2.5	(1.7/.6)									

$R \equiv (\text{length/separation}) = 200, 133, 50, 50, \text{ and } 21$  respectively for length to separation ratios listed above.

$\bar{x} = \text{mean resistance}$     s.d. = Standard Deviation

resistivities are listed. The lack of correlation between separation and resistance could be attributed to localized ionic concentrations instead of a uniform distribution of residual ions. These local or spot concentrations of ions could also account for the resistance variability between similarly processed boards.

Table 15 lists resistances for Parylene coated boards and Table 16 urethane coated boards. Resistance ranges for the different boards in dry environments are given below:

Bare Boards	1 to 31 teraohms
GMB Encapsulated	8 to 26
Urethane Foam	6 to 34
Epoxy Foam	1 to 17
Parylene (thick)	16 to 160
Parylene (thin)	2 to 230
Urethane	1 to 18

The epoxy foamed boards were in general slightly lower than bare boards while the GMB, and urethane foamed boards were higher. The thick Parylene boards were higher than the thinner Parylene or urethane coated boards. The use of a urethane or Parylene coating prior to foaming appears to be beneficial.

In the humid environment, 92 to 100% RH, resistances ranged from 0.0005 to 4 teraohms for the bare and coated boards. The most noticeable decrease was observed with the Parylene coated boards. The laminate source did not appear to have an influence on insulation resistance. Most of the boards showed rapid recovery of insulation resistance when transferred from the humid to the dry environment, as shown in Table 17.

The volume resistivity of the laminate, coating or encapsulant would not be expected to make significant contribution to insulation resistance at room temperature. (8), (9), (10)

Table 15

## Insulation Resistance of Parylene Coated Boards in Teraohms

Board	Dry (length/separation)						Humid (length/separation)						$\frac{\text{Hrs}}{\% \text{ RH}}$
	50/0.25	50/0.38	25/0.50	50/1.0	32/1.5	$\bar{x}/\text{s.d.}$	50/0.25	50/0.38	25/0.50	50/1.0	32/1.5		
67 P2	160	51	20	33	23	(57/58)							
113 P2	50	23	28	45	37	(37/11)	0.006	0.01	0.2	0.6	14		168/93
187 P2	51	37	26	40	60	(43/13)	0.001	0.001	0.0005	0.002	0.013		72/93
201 P2	38	62	68	91	113	(74/29)							
209 P2	16	25	30	29	20	(24/6)							
S-30 P2	68	49	34	50	50	(50/12)							
$\bar{x}/\text{sd}$ P2	(64/50)	(41/16)	(34/17)	(48/22)	(50/34)	(47)							
15 P1	5	8	100	28	170	(62/71)	0.6	0.9	5	7	3		24/100
87 P1	2	4	60	18	80	(33/35)	0.5	0.5	1	1	2		24/100
111 P1	8	8	133	17	230	(80/100)							
185 P1	3	5	11	5	30	(11/11)	0.008	0.001	-	0.03	0.02		72/100
I P1	3	4	60	90	16	(35/39)	1	1	2	1.2	0.06		24/100
$\bar{x}/\text{sd}$	(4/2)	(6/2)	(73/46)	(32/34)	(105/92)	44							
113P+UF	54	58	35	40	48	(47/10)	7	5	8	12	12		144/93
201P+UF	44	57	23	20	43	(37/16)							

$R \equiv (\text{length/separation}) = 200, 133, 50,$   
 $50, \text{ and } 21.$

P2 = 0.025 mm thick Parylene Coating  
 P1 = 0.013 mm thick Parylene Coating

Table 16  
Insulation Resistance of Urethane Coated Boards in Teraohms

Board & Coating	Dry (length/separation)						Humid (length/separation)						Hrs % RH
	50/0.25	50/0.38	25/0.50	50/1.0	32/1.5	$\bar{x}$ /s.d.	50/0.25	50/0.38	25/0.50	50/1.0	32/1.5		
21 U	3	5	3	7.5	3	(4/2)	-	-	1	2	1.5	100/100	
68 U	2	1	1	1.5	1.5	(1.5/.4)	0.006	0.2	0.4	0.4	0.6	48/100	
116 U	3	3	3.5	3.5	4	(3.5/.4)							
164 U	5	5	5	4.5	10.5	(6/2.5)	0.8	0.3	1	0.5	0.2	20/100	
194 U	4.5	4	5.5	11	8.5	(7/3)							
S-4 U	14	13	18	16	12	(15/2)	0.3	0.4	0.2	0.8	0.4	100/100	
S-38 U	-	3.5	4.5	3	5	(4/1)							
$\bar{x}$ /s.d.	(5/4)	(5/4)	(6/6)	(7/5)	(6/4)	6							
110U+EF	15	19	12	14	9	(12/5)							

$$R \equiv (\text{length/separation}) = 200, 133, 50, 50, 21$$

Table 17

## Effect of Time on Insulation Resistance in Different Humidity Environments

<u>Board #</u>	<u>Coating</u>	<u>Hours/Humidity</u>	Separation (mm) Resistance (Teraohms)				
			.25 (.010)	.38 (.015)	.50 (.020)	1.00 (0.039)	1.50 (0.059)
108	None	0.11%	12	24	5	15	19
		72/93%	0.004*	short*	0.02	0.02	0.2
		72/10%	.008*	short*	4	2	3
		0/10%	1.5	short*	6	14	34
		48/93%	2	short*	2	7	10
108 +	UF	144/93%	0.2	short*	2	8	10
		0/38%	6	10	22	7	33
		96/100%	0.2	0.3	0.7	0.8	2
		0/13%	50	23	28	45	37
		24/93%	0.09	0.05	0.3	1	2
113	Parylene	168/93%	0.006	0.01	0.2	0.6	1
		1/8%	8	17	35	40	48
		0/8%	54	0.58	35	40	48
		48/93%	8	15	12	12	12
		144/93%	7	5	8	12	12
187	Parylene	0/13%	51	37	26	40	60
		72/93%	0.001	0.001	0.0005	0.002	0.01
		0.1/8%	0.007	0.007	0.002	0.004	0.05
		0.5/8%	0.7	0.7	0.1	0.1	4
		1/8%	2	2	1	3	7
		24/10%	32	34	36	43	45

\*Filament Formation

The inadvertent presence of moisture film between conductors on one of the boards caused filament formation by electromigration during two of the measurements. Filament formation on PWBs is discussed in a separate report (11).

Waddell, Kirk, and Lewis (11) measured insulation resistances on PWBs made by the same process as those in this study. They used the pattern specified in ASTM 0257 with various gap widths, test voltages, temperatures and board materials. Their surface resistances on clean boards ranged from 5 to 25 terohms for 0.50 mm (0.020) separations at 80°C and in an environment of less than 10% RH. Of several contaminants intentionally applied to the boards finger prints caused the greatest resistance decrease. Resistances with such contamination were in the gigohm range in this dry environment. The effects of the finger prints could not be removed by spray cleaning with trichloroethylene. Contamination from rosin core solder had little effect on surface resistance in this environment.

Volume resistivity of the laminates measured above 100 terohms at 80°C. Surface resistance decreased by 50 percent for every 6.7°C increase from room temperature. Surface resistance decreased with decrease in conductor separation; however, the resistivity was not constant but decreased with separation. It was also relatively independent of test voltage in the 10 to 1000 volt range. Volume resistivity could be important where excessive currents in conductors cause appreciable heating of the laminate between conductors.

#### SUMMARY

No flashover or voltage breakdown between conductors occurred below 1000 volts at ambient conditions or below 400 volts at low pressure. At ambient pressure, 84 kPa (630 Torr), breakdown voltage for bare boards followed the relationship,  $V = 3.1 S^{0.51}$ , where S is the separation in millimeters. Boards

coated with Parylene or urethane and those encapsulated in GMB epoxy or urethane foam broke down at higher voltages than bare boards.

At low pressure, 660 Pa (5 Torr), breakdown voltage did not correlate with separation and breakdown paths were frequently between the voltage leads. This is attributed to the pressure-separation term being near the minimum of the Paschen Curve. The advantage obtained from a coating was much less at low pressure than at room pressure. Several low voltage breakdowns, 400 to 800 volts, on GMB encapsulated boards at low pressure were attributed to poor bonding between the GMB epoxy and the board laminate.

The extent of plating and etching which the conductors received in fabrication caused appreciable variations in current carrying capability of conductors. The effect of etching is especially noticeable for narrow conductors, while plating thickness variations have a greater relative effect for wide conductors. Thickness of uniformly deposited copper in plated through holes generally has little effect on the current carrying capability of a circuit. No significant differences in current capacity were associated with different sources of laminate or between equivalent cross sectional areas of single and parallel conductors.

From the maximum resistance change or temperature rise which can be tolerated for the circuit current, the designer can specify the minimum conductor cross sectional area he will accept in board fabrication. Conductor burn through and/or polymer degradation limit the current in a conductor.

Cross sectional areas of conductors obtained from resistance measurements were within 10 percent of those from optical and beta backscatter measurements. Resistance cross sectional measurements are considered more meaningful for circuit applications.

Log-log plots of temperature rise against current give an average slope of 2.25, i.e.,  $\Delta T_2/\Delta T_1 = (I_2/I_1)^{2.25}$ . Temperature rise is calculated from the resistance change with current and the temperature coefficient of resistance of copper.

The temperature rises obtained in this study were lower than published values for similar nominal widths and currents. Suggested sources for the lower values are differences in conductor cross section profile, shorter conductor lengths, and a shorter measurement period. A safety factor of 2 for temperature rises below 100°C is suggested to allow for measurement differences.

Temperature rise-current plots at -55°C and 74°C were similar to those at 25°C. In the 74°C environment the limiting or maximum current is lower as the system is closer to the temperature at which conductor burn through or polymer degradation is initiated. Pyrolysis and polymer degradation are time-temperature functions varying with separation distances of conductors carrying currents and ambient conditions.

Coated or encapsulated boards were similar to bare boards in temperature rise after 30 seconds. At currents at which conductors on bare boards burned through in 3 to 15 minutes, the same size conductors which were encapsulated, increased in temperature over longer intervals, 1 to 4 hours, until the encapsulant pyrolyzed. The pyrolysis caused sufficient pressure to rupture the encapsulant and expose the conductor to the atmosphere. When the conductors were so exposed they rapidly burned through.

Room temperature insulation resistance between bare or coated conductors ranged from 1 to 230 terohms in a laboratory environment of 10 to 30% RH, and 0.0005 to 4 terohms in a 92 to 100% RH environment.

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