2025 MAY 06

pGRAMS Electronics Meeting #XX

BayCat (Hub Computer) I/Os

Features

1. **Intel Atom "Bay Trail" Processor**
   Up to 1.9 GHz clock rate. Quad, dual or single core options. Low power consumption.
2. **High-performance Video**
   Integrated Intel Gen 7 graphics core supports DirectX 11, OpenGL 4, and H.264, MPEG-2 encoding/decoding. Analog VGA (2a) and mini DisplayPort video output (2b); both outputs support multiple display modes including Extended Desktop and Clone.
3. **Trusted Platform Module** *(on back side)*
   On-board TPM security chip can lock out unauthorized hardware and software
4. **RAM** *(on back side)*
   Up to 8 GB DDR3L socketed memory (one SO-DIMM).
5. **Network**
   Dual Ethernet interfaces, autodetect 10BaseT / 100BaseTX / 1000BaseT with remote boot support.
6. **Industrial I/O**
   One USB 3.0 port (6a *on back side*); Dual RS-232/422/485 serial ports (6b); four USB 2.0 ports support keyboard, mouse, and other devices, three 8254 timer/counters, I²C, and audio support (6c).
7. **Digital I/O**
   Twenty-four 3.3V digital I/O lines.
8. **SATA**
   3 Gb/s SATA port. Supports rotating or solid state SATA drive.
9. **Mini PCIe socket**
   Supports Wi-Fi modems, GPS receivers, flash data storage with auto-detect mSATA flash storage support, and other mini PCIe modules.
10. **MicroSD Socket**
    Supports removable microSD card solid-state drives.
11. **SPI Interface**
    Supports SPI and SPX devices, including low cost analog and digital modules.
12. **Main Power Input**
    5V Input ±5%
13. **PC/104 Expansion** *(on back side)*
    Legacy PCI connector, stack-down
14. **PC/104 Expansion** *(on back side)*
    Legacy ISA connector, stack-down

- **Industrial Temperature**
  -40° to +85°C operation for harsh environments
- **PC/104 Form Factor**
  Industry-standard PC/104-*Plus* expansion
- **MIL-STD-202G**
  Qualified for high shock/vibration environments

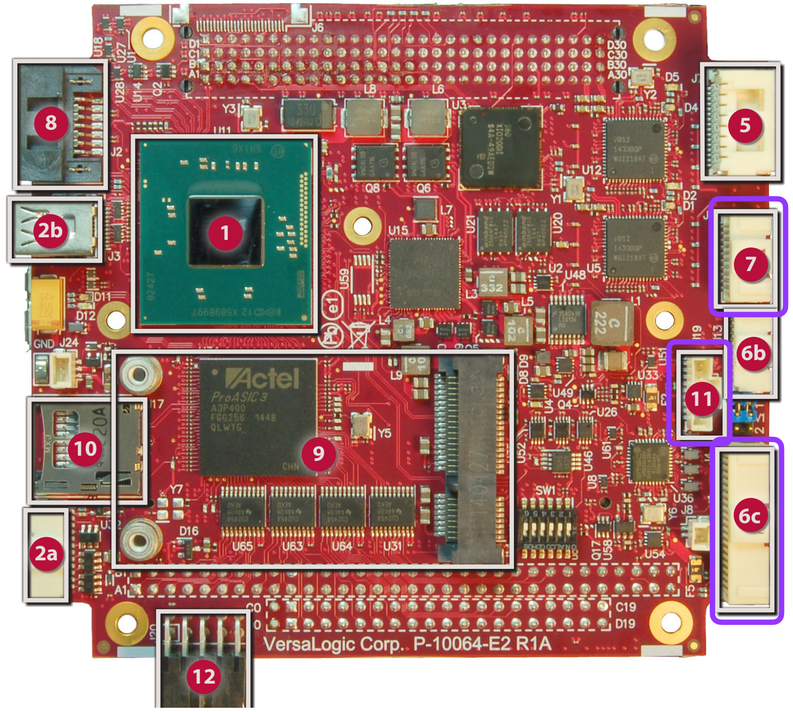
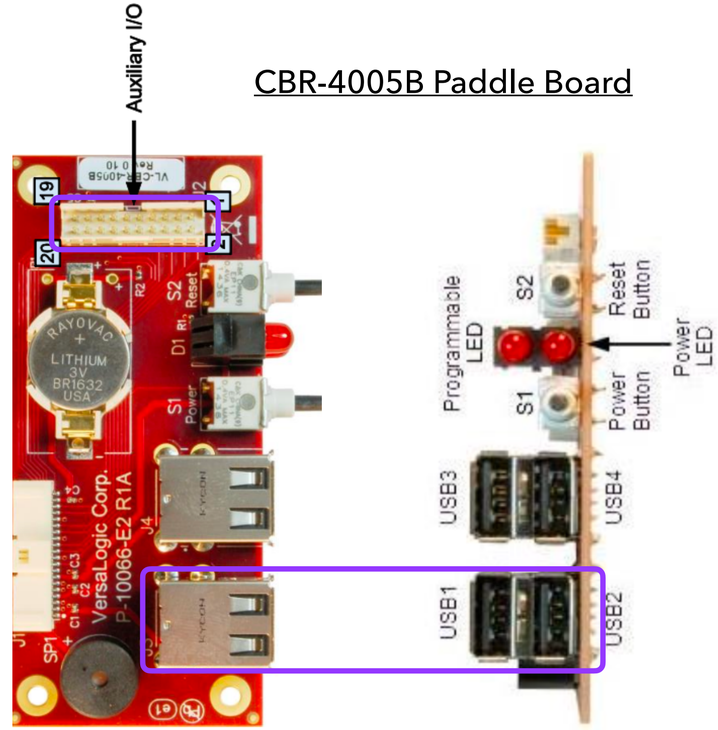


Table 20: Auxiliary I/O Connector Pinout

Pin	Signal	Pin	Signal
1	I2C Clock	2	V_BATT
3	I2C Data	4	V_BATT_RETURN
5	GND	6	GND
7	FPGA GPIO1	8	FPGA GPIO2
9	FPGA GPIO3	10	FPGA GPIO4
11	GND	12	GND
13	FPGA GPIO5	14	FPGA GPIO6
15	FPGA GPIO7	16	FPGA GPIO8
17	+3.3 V	18	GND
19	Ethernet Port 0 LED	20	Ethernet Port 1 LED

Adapter Cable
(CBR-4005A)

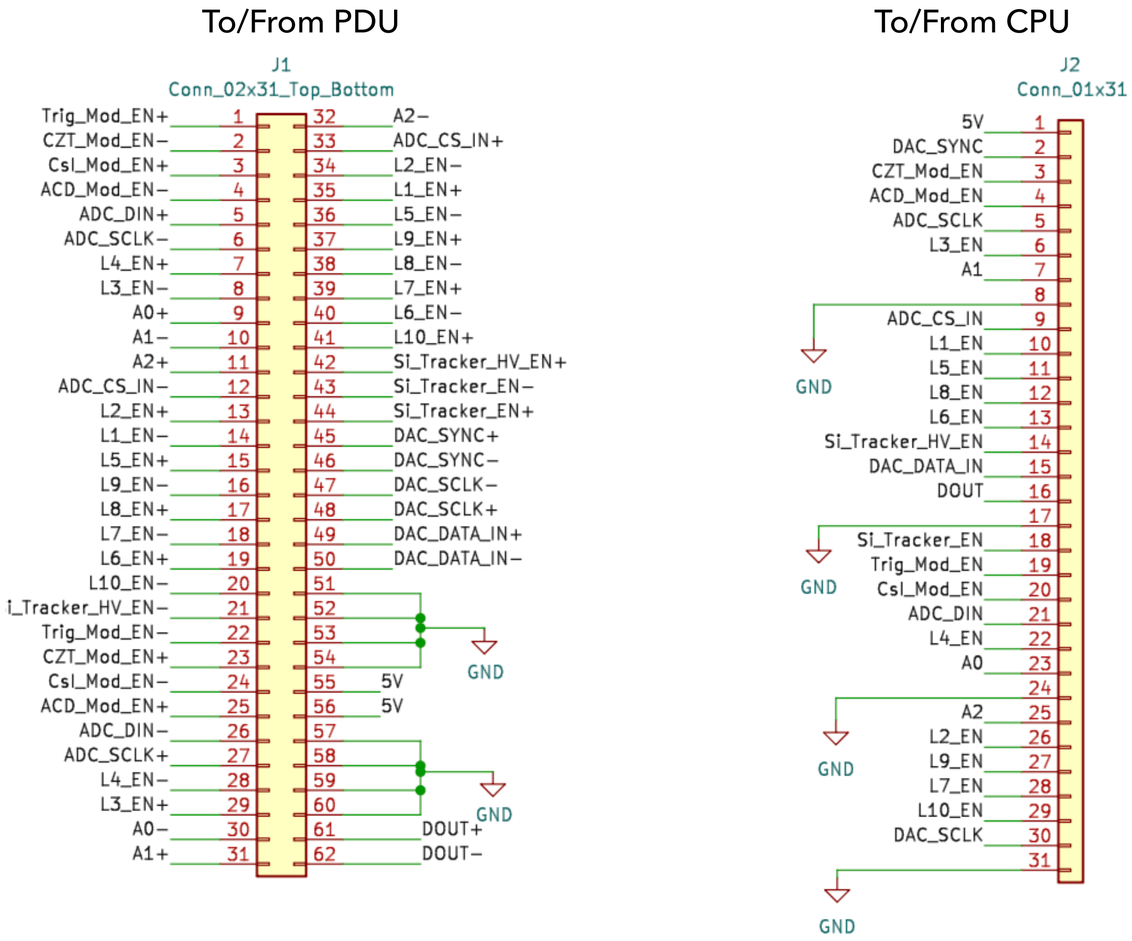
CBR-4005B Paddle Board



BayCat (Hub Computer) I/Os

- I/O Required for GSFC subsystems
  - For TOF/MPD bias control systems
    - 2 x USB 2.0 (on VL-CBR-4005 Paddle Board through connector-6C)
  - For PDU Interface Card (LVDS board)
    - 24 x 3.3V Digital I/O (16 on connector-7 + 8 on VL-CBR-4005 Paddle Board)
    - SPI for ADC and DAC (on connector-11)

ex) PDU Interface Card I/Os for ComPair



BayCat (Hub Computer) I/Os

Table 9: J21 I/O Connector Pinout

J21 Pin	Signal	VL-CBR-2005 Terminal Block	Terminal Block Pin
1	Digital I/O 1	J1	5
2	Digital I/O 2		4
3	Digital I/O 3		3
4	Digital I/O 4		1
5	Ground		2
6	Digital I/O 5	J2	5
7	Digital I/O 6		4
8	Digital I/O 7		2
9	Digital I/O 8		1
10	Ground		3
11	Digital I/O 9 (Optional Timer Channel 5 output)	J3	5
12	Digital I/O 10 (Optional Timer Channel 5 output)		3
13	Digital I/O 11 (Optional Timer Channel 4 Gate input)		2
14	Digital I/O 12 (Optional Timer Channel 3 Gate input)		1
15	Ground		4
16	Digital I/O 13 (Optional Timer 3 output)	J4	4
17	Digital I/O 14 (Optional Timer 3 input)		3
18	Digital I/O 15 (Optional Timer 4 output)		2
19	Digital I/O 16 (Optional Timer 4 input)		1
20	Ground		5

The SPI clock is derived from a 33 MHz PCI clock and can be software-configured to operate at the following frequencies:

- 8.25 MHz (33 MHz/4)
- 4.125 MHz (33 MHz/8)
- 2.0625 MHz (33 MHz/16)
- 1.03125 MHz (33 MHz/32)

Table 16: SPX Connector Pinout

Pin	Signal	Function
1	V5_SPX	+5.0 V
2	CLK	SPX Clock
3	GND	Ground
4	MISO	Master input, Slave output
5	GND	Ground
6	MOSI	Master output, Slave input
7	GND	Ground
8	SS0#	Chip Select 0
9	SS1#	Chip Select 1

Table 20: Auxiliary I/O Connector Pinout

Pin	Signal	Pin	Signal
1	I2C Clock	2	V_BATT
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5	GND	6	GND
7	FPGA GPIO1	8	FPGA GPIO2
9	FPGA GPIO3	10	FPGA GPIO4
11	GND	12	GND
13	FPGA GPIO5	14	FPGA GPIO6
15	FPGA GPIO7	16	FPGA GPIO8
17	+3.3 V	18	GND
19	Ethernet Port 0 LED	20	Ethernet Port 1 LED

PDU Required number of Digital I/Os for pGRAMS

- Power Enable (13)
    1. SiPM (6) Power EN
    2. Cold TPC HV EN
    3. Cold TPC Charge Pre-Amp EN
    4. Cold TPC SiPM Pre-Amp EN
    5. Warm TPC Shaper EN
    6. CAEN - NEVIS 3.3V EN
    7. CAEN - NEVIS 12V EN
    8. CAEN - NEVIS +/- 5V EN
    9. HUB CPU EN
    10. DAQ CPU EN
    11. TOF/MPD Readout +12V EN
    12. TOF/MPD Bias Control +12V (+6V?) EN
    13. TOF/MPD Bias DC-DC +12V (+6V?) EN

- PDU DAC MUX (3: A0 A1 A2)
    1. SiPM 0
    2. SiPM 1
    3. SiPM 2
    4. SiPM 3
    5. SiPM 4
    6. SiPM 5
    7. TPC HV

- PDU ADC MUX (3: A0 A1 A2)
    1. ???
    2. ???
    3. ???
    4. ???
    5. ???
    6. ???
    7. ???