Review of "Drowsy Caches: Simple Techniques for Reducing Leakage Power" [1]

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Key Ideas

These researchers seek to lower the power consumption of microprocessors. They target on-chip caches, which consume a large amount of power, for improvement. They seek to exploit locality to reduce power consumption by "dimming" areas of the cache that are not being heavily accessed. They claim to reduce the total energy consumed by caches by 50-75% with no more than a 1% decrease in performance.

Review

The claim made in their abstract is very impressive. 50-75% is a large energy savings with such a small impact to performance (1%). But they do not state the impact this will have on the energy consumption of the entire system. If making the caches more energy efficient has only a marginal effect on the overall energy consumption of the computer, then the work is not very useful. They evaluate their design thoroughly by testing many design corners, down to whether or not to put tags into drowsy mode along with data. I was also impressed at the degree to which they evaluated potential weaknesses in their novel designs, such as the DVS drowsy memory cell schematic. They saw the potential for memory corruption due to crosstalk, tested if their design was susceptible, and presented the results that prove it is not. This is very convincing.

Conclusion

Given the degree to which they tested their designs and explored every design corner, it's clear that a lot of thought was put into this project. My main concern remains that I haven't been convinced that making caches more power efficient will significantly benefit the whole system. While my searches online reinforce the idea that caches consume a large fraction of the total chip power, I would like to see measurements that make this clear. But overall, I agree with the approach this paper takes to reducing power consumption. At the time, DVFS was beginning to be applied to processor cores. It makes a lot of sense to extend this technique (at least the voltage scaling) to caches.

References

[1] K. Flautner, Nam Sung Kim, S. Martin, D. Blaauw, and T. Mudge. Drowsy caches: simple techniques for reducing leakage power. In *Computer Architecture, 2002. Proceedings. 29th Annual International Symposium on*, pages 148–157, 2002.