XXXX: A Multi-Accelerated Application To Evaluate Accelerator-Rich Architectures

Riley Wood

***Abstract*—This is my abstract. It will give an overview of the motivation for my work and what accomplishments I will present to the reader in this paper [1][2][3].**

With the recent end of Dennard scaling, the power density of CPUs has begun to grow as transistors scale down. To stay within power budgets, architects are forced to utilize only a portion of the processor's transistors at any given time, leaving the rest unpowered. This "utilization wall" will grow more dramatic as transistors get smaller in the future; it is estimated that in 10 years, 93.75% of the CPU will need to be kept dark Check this statistic, it's from [3].

One approach to this problem which is gaining traction is to move away from a centralized computing model wherein all computation stems from a general purpose processor, and instead compute specific workloads on one of many specialized, on-chip hardware accelerators such that computation bounces from block to block. Talk about the benefits of specialization, how it solves the utilization wall. Cite specific sources that present evidence as to the benefits of specialization. There are already examples of SoCs that use this model Cite the IBM computer I forget it's name and the Apple SoC.

Still, these systems use only a handful of accelerators, whereas industry leaders at ITRS expect systems by 2022 to contain approximately 1500 on-chip accelerators. Using the standard OS+driver model of accelerator management would introduce massive delays at this scale. For this reason, the research community has begun looking into ways of more effectively managing such accelerator-rich architectures. Some of these include the Accelerator Store [1] and AXRCMP [2].

References

[1] M. Lyons, M. Hempstead, G. Y. Wei, and D. Brooks. The accelerator store framework for high-performance, low-power accelerator-based systems. *IEEE Computer Architecture Letters*, 9(2):53–56, Feb 2010.

[2] J. Cong, M. A. Ghodrat, M. Gill, B. Grigorian, and G. Reinman. Architecture support for accelerator-rich cmps. In *Design Automation Conference (DAC), 2012 49th ACM/EDAC/IEEE*, pages 843–849, June 2012.

[3] M. B. Taylor. Is dark silicon useful? harnessing the four horsemen of the coming dark silicon apocalypse. In *Design Automation Conference (DAC), 2012 49th ACM/EDAC/IEEE*, pages 1131–1136, June 2012.