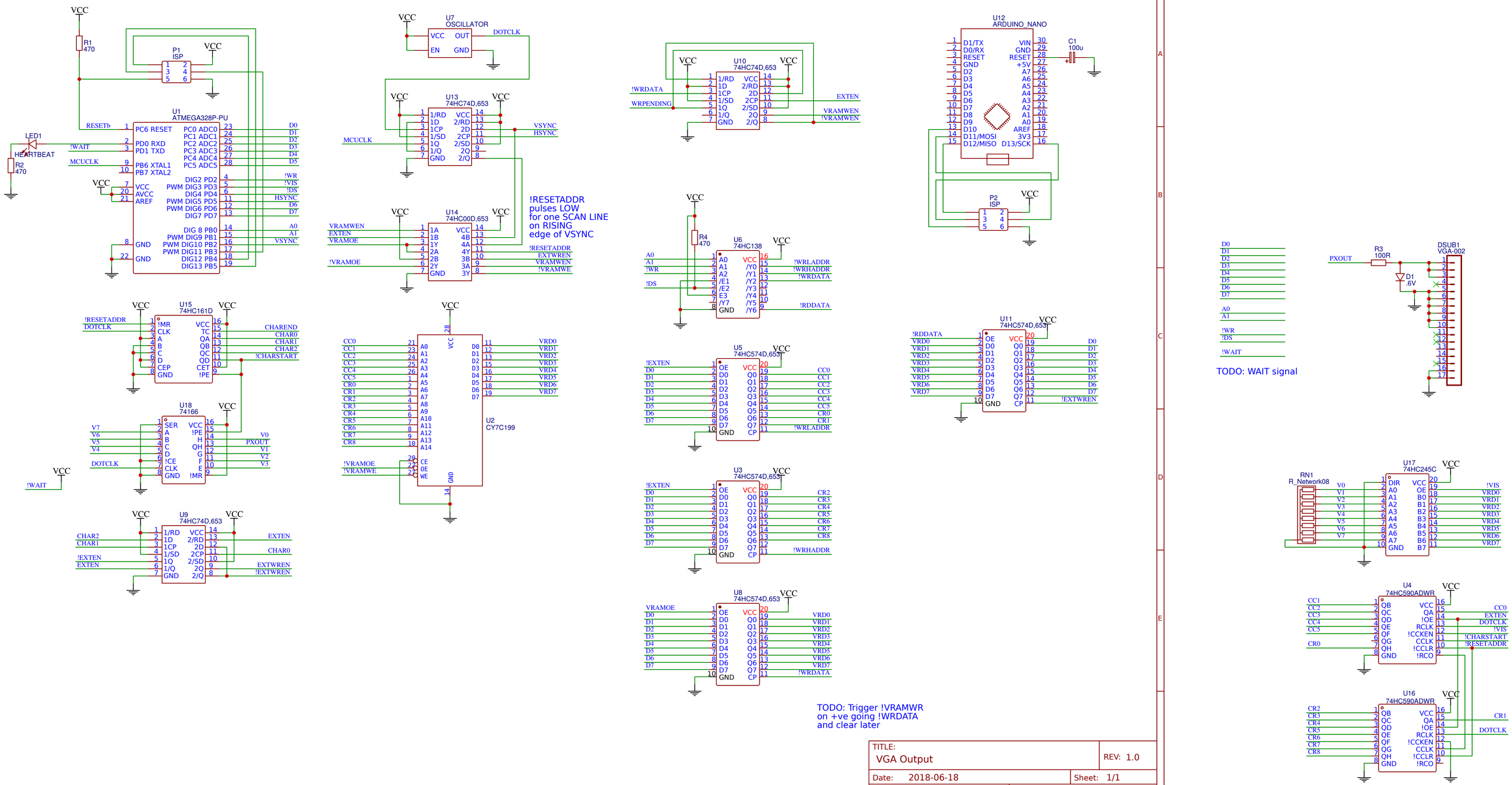
U1
ATMEGA328P-PU
U2
CY7C199
U3
74HC574D,653
U4
74HC590ADWR
U5
74HC574D,653
U6
74HC138
U7
OSCILLATOR
U8
74HC574D,653
U9
74HC74D,653
U10
74HC74D,653
U11
74HC574D,653
U12
ARDUINO_NANO
U13
74HC74D,653
U14
74HC00D,653
U15
74HC161D
U16
74HC590ADWR
U17
74HC245C
U18
74166
P1
ISP
P2
ISP
RN1
R_Network08
DSUB1
VGA-002
R1
470
R2
470
R3
100R
R4
470
C1
100u
D1
.6V
LED1
HEARTBEAT
VCC
!RESETADDR
pulses LOW
for one SCAN LINE
on RISING
edge of VSYNC
TODO: WAIT signal
TODO: Trigger !VRAMWR
on +ve going !WRDATA
and clear later
TITLE:
VGA Output
REV: 1.0
Date: 2018-06-18
Sheet: 1/1
EasyEDA V5.5.14
Drawn By: rjw57