

A Report On
“SODA DISPENSER MACHINE”

Mini Project 2-B (REV- 2019 ‘C’ Scheme) of Third Year, (TE Sem-VI)
in

Department of Electronics and Telecommunication Engineering

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CERTIFICATE

This is to certify that the project entitled Simple Vending Machine is a bonafide work of

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Guide

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Chapter 1

Introduction

1.1 Definition

A vending machine is an electronic device that dispenses goods when money or tokens are inserted. Field-Programmable Gate Array (FPGA) is a type of integrated circuit that can be programmed by a user after manufacturing. The aim of this project is to design and implement a vending machine using Field-Programmable Gate Array (FPGA) technology. The vending machine will be able to accept coins and bills, display available products and prices, and dispense the selected item. The FPGA will serve as the main control unit, managing the inputs and outputs and executing the necessary algorithms.

A vending machine is a machine which dispenses items such as snacks, beverages, lottery tickets, consumer products to customers automatically, after the customer inserts currency or credit into the machine. Nowadays, Vending Machines are well known among Japan, Malaysia, and Singapore. The usage of these machines is spread worldwide because of the modern lifestyle adapted. The objective here is to design Vending Machine Controller which accepts money inputs (1 and 0) in any sequence and delivers the products when the required amount has been deposited and gives back the change. Though the vending machine dispenses a lot of materials, the project only demonstrates a soda dispenser. This project has the potential to offer a flexible and customizable solution for dispensing various goods in different settings.

Chapter 2

Comparative Study

Year	Title	Description
2009	Fauziah Zainuddin, Norlin Mohd Ali, Roslina Mohd Sidek, Awanis Romli, Nooryati Talib & Mohd. Izham Ibrahim (2009) "Conceptual Modeling for Simulation: Steaming frozen Food Processing in Vending Machine" International Conference on Computer Science and Information Technology, University Malaysia Pahang, pp.145-149.	This paper proposes a vending machine for steaming frozen food using conceptual modeling. In which the process of three main states (user selection state, freezer state, and steaming state) has been modeled using the process approach, which emphasizes the process flow or control logic to construct the model for steamed buns vending machine application.
2012	M. Zhou, Q. Zhang & Z. Chen (2006), "What Can Be Done to Automate Conceptual Simulation Modelling?" Proceedings of the 2006 Winter Simulation Conference, pp. 809 – 814. International Journal of VLSI Design & Communication Systems (VLSICS) Vol.3, No.2, April 2012	In this paper coffee vending machine is designed using single electron encoded logic (SEEL). The designed circuit is tested and its power and switching time are compared with the CMOS technology.
2013	P Pradeepa, T Sudhalavanya, K Suganthi, N Suganthi, M Menagadevi, DESIGN AND IMPLEMENTATION OF VENDING MACHINE USING VERILOG HDL, International Journal of advanced engineering technology 4 (1), 51-53,2013	The machine can accept the coins of one rupees, two rupees, and five rupees in any possible sequence. There are coin slots and it is commonly connected to the FPGA. The user interface is used for coin dispensing and product dispense. Relay is used to control the product dispatch. The program has written on KCPSM3 processor and downloads into the FPGA Spartan-3A kit by using ELBERT configuration for selecting products, coin sum, and balance and it will be displayed on LCD.
2020	Edison Kho, Manoj Kumar 2020, Design and Implementation of FPGA-based Vending Machine for Integrated Circuit (IC), International Conference on Communication and Signal Processing (ICCSP), 0246-0251,2020	The paper gives the design and implementation of a multi-select state vending machine using a State Machine with which users can select the product and insert the desired token for respective products to dispense the Integrated Circuit or it will return the inserted token if the wrong token is inserted for each Integrated Circuit. We choose FPGA because FPGA-based vending gives a quicker response and absorbed less power and is reprogrammed anytime as compared to CMOS vending machines. The intended design is implemented in VHDL and simulated using Xilinx and it's implemented on FPGA Spartan 3A

Chapter 3

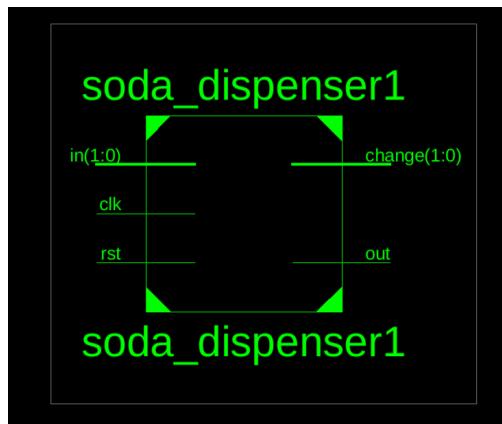
Problem Definition

The problem is defined as the design of vending machine that accepts coins of five and ten rupees and dispenses soda but doesn't give change when the required amount is unsatisfied. The machine should possess additional features of returning change when the input coin doesn't meet the required amount to dispense a soda. The machine asks the customer to insert coins as per the price of the product. The coin is a signal therefore input to the machine. The machine checks the inserted amount with the price of the product and dispenses the product if both are equal. If the customer inserts a coin of a higher amount or lower amount, the machine gives the product along with the change. Whenever a change is not available in the machine, it returns the total amount. Product and change are therefore outputs of the machine also return money is another output.

Chapter 4

Mini Project Design(Principle and Working)

4.1 Block Diagram and Description

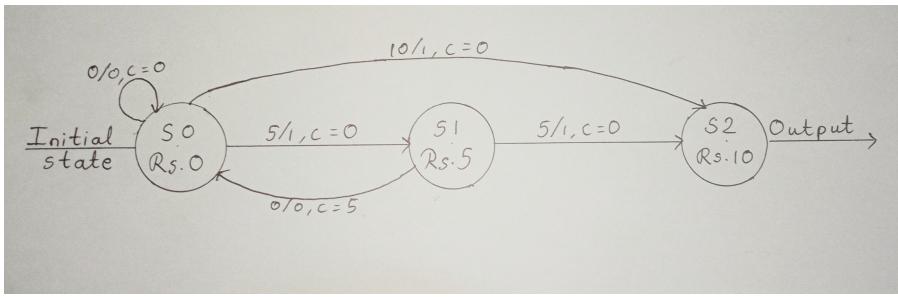


The block diagram shows the main module `sodadispenser` with its inputs `clk`, `rst`, and `in`, and outputs `out` and `change`.

The state machine inside the module changes state based on the inputs `in` and current state `currentstate`, and sets the next state `nextstate` and the outputs `out` and `change`.

The `change` output is a two-bit signal representing the amount of change to be given back to the user, and the `out` output is a one-bit signal indicating whether or not a soda has been dispensed.

4.2 State Diagram and State Transitions



The Verilog code implements a soda dispenser circuit that takes two inputs $\text{in}[1:1]$ to represent the amount of money deposited by a user (00 for no money, 01 for 5 Rs, and 10 for 10 Rs) and uses these inputs to control the output out to dispense soda and the two-bit output change[1:1] to indicate any change that needs to be returned to the user. The circuit is implemented using a Moore state machine. The circuit has three states:

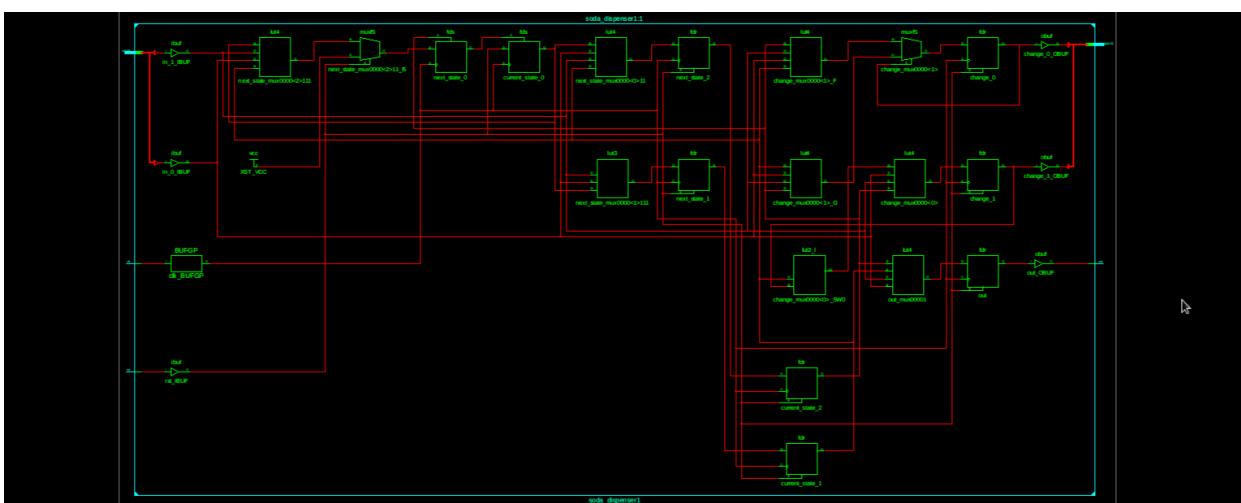
S0 - the initial state and the state that the circuit transitions to when a user has been served.
S1 - the state where the user has deposited 5 Rs, and the circuit waits for either more money or for the user to select a soda.

S2 - the state where the user has deposited 10 Rs, and the circuit waits for either more money or for the user to select a soda.

The circuit transitions between these states based on the input value of $\text{in}[1:1]$ and outputs a soda when the user has deposited enough money and selected a soda. If the user has deposited more money than needed, the circuit returns the change using the two-bit output change[1:1]. The reset input rst is used to bring the circuit to the initial state when activated.

The Universal Constraint File (UCF) maps the inputs and outputs of the Verilog code to the physical pins of the FPGA. The UCF file above maps the clk and rst signals to the pins G3 and G4, respectively. The $\text{in}[0]$ and $\text{in}[1]$ signals are mapped to the pins D1 and D2, respectively. The out signal is mapped to the pin B1, while the two-bit output change[0] and change[1] are mapped to the pins E1 and E2, respectively.

4.3 Circuit Diagram



4.4 Advantages and Disadvantages

Advantages:

-Simplicity: FSMs are relatively simple and easy to understand. They can be represented using state diagrams or tables, making them easy to visualize and analyze. This simplicity also makes FSMs easier to implement and test.

-Scalability: FSMs can be easily scaled up or down, depending on the complexity of the problem or system. This makes FSMs suitable for a wide range of applications, from simple control systems to complex software applications.

-Real-time operation: FSMs can operate in real-time, making them suitable for applications that require quick responses to changes in input. They can also handle multiple inputs and outputs, making them suitable for multi-tasking environments.

-Reduced complexity: FSMs can simplify complex systems by breaking them down into smaller, more manageable pieces. This can help reduce the overall complexity of the system and make it easier to understand and analyze.

-Reduced errors: FSMs can reduce the potential for errors in a system by enforcing strict rules and transitions between states. This can help ensure that the system operates correctly and consistently, even in complex environments.

Disadvantages:

While Finite State Machines (FSMs) offer several advantages, they also have some disadvantages that need to be considered when deciding whether to use them for a particular application.

Here are some of the disadvantages of FSMs:

-Limited flexibility: FSMs are designed to operate within a specific set of rules and transitions between states. If the rules or transitions need to be changed, the FSM may need to be completely re-designed, making it less flexible than other types of systems or algorithms.

-State explosion: As the number of states and transitions in an FSM increases, the complexity of the system can increase exponentially. This can make it difficult to design and maintain the FSM, and can also increase the risk of errors.

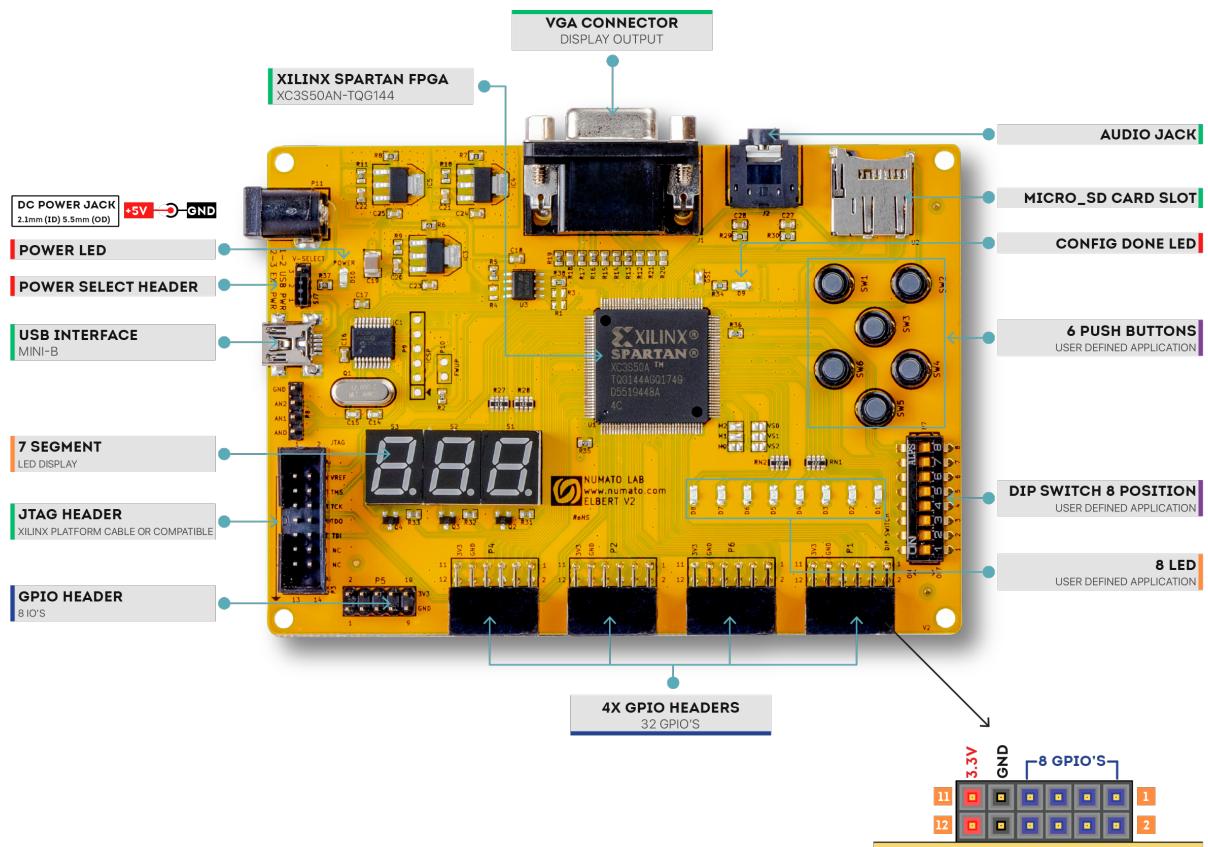
-Limited fault tolerance: FSMs are not fault-tolerant, meaning that if a component of the FSM fails, the entire system may fail. This can be a disadvantage in applications where reliability is critical.

Chapter 5

Components and Software

5.1 Components

Spartan 3-A



The Spartan-3A FPGA is a family of Field-Programmable Gate Arrays (FPGAs) manufactured by Xilinx. It is designed for low-power and high-performance applications, and is widely used in a variety of industries such as automotive, aerospace, telecommunications, and consumer electronics.

The technical specifications of the Spartan-3A FPGA family are as follows:

Number of logic cells: 1,888 to 33,192

Number of slices: 592 to 1,048

Number of block RAMs: 4 to 18

Memory capacity: 2.7 Kb to 486 Kb

Number of clock management tiles: 1 to 3

Maximum user I/O pins: 144 to 576

Maximum memory bandwidth: 400 Mbps to 800 Mbps

Maximum clock frequency: 375 MHz to 550 MHz

Operating voltage: 1.2V to 1.5V

Power consumption: 0.24W to 1.7W

Package types: QFP, BGA, and CSP

5.2 Software

Xilinx ISE Design Suite

Xilinx ISE Design Suite The Xilinx ISE (Integrated Synthesis Environment) Design Suite is a set of software tools used for designing and implementing digital circuits using Xilinx FPGAs. The ISE Design Suite includes a range of tools for designing, simulating, synthesizing, and implementing digital circuits. The Xilinx ISE Design Suite supports a wide range of Xilinx FPGAs, including the Spartan, Virtex, Artix, and Kintex families. It also supports a range of operating systems, including Windows, Linux, and Solaris.

Chapter 6

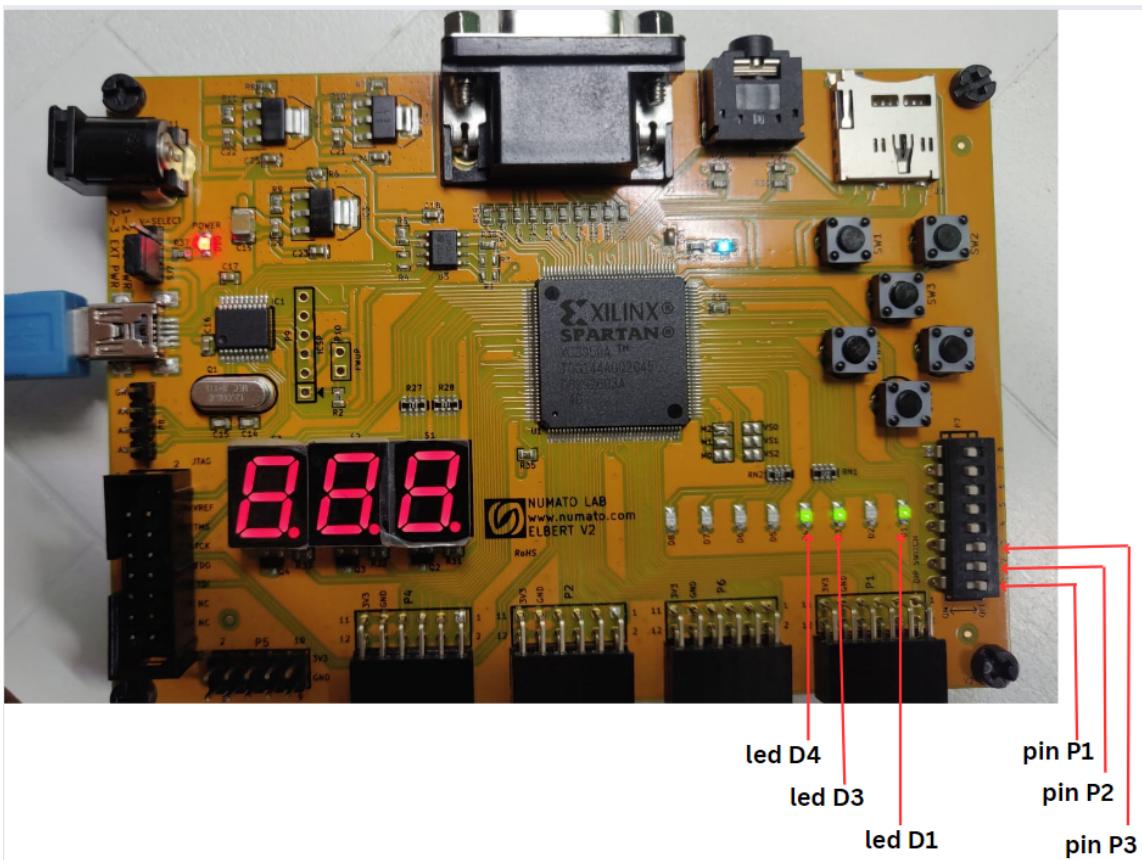
Proposed Execution Steps

6.1 Implemented Steps

Implemented Steps for FPGA

1. First of all, started a program file with Verilog module and then wrote code using FSM.
2. Performed syntax check and created post syntax file to generate testbench file.
3. Used Simulation behavioral model to create waveform.
4. Created User Constraint File to assign input and output pins to required variables.
5. Performed Implementation design → Translate → Map → Place and route → Generate programming file.
6. Uploaded .bit file into FPGA board using Elbert V2 configuration tool.

6.2 Hardware output



Dp switches used for input:

Pin P1: clock pin assigned

Pin P2: in[0] // first value of the bit, either 0 or 1

Pin P3: in[1] //second value of the bit, either 0 or 1

LED used for output:

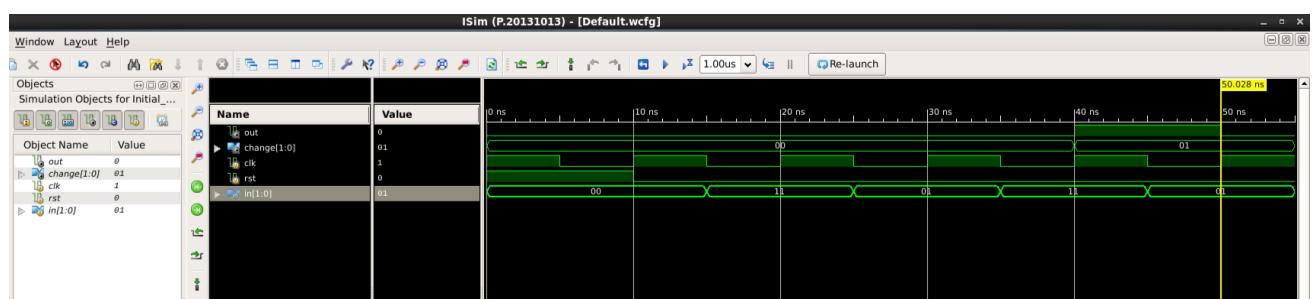
Led D1: glowing of this led states that the machine is in the S1 state

Led D1 and D3: glowing of this led states that the machine is in S1 and S2 state

Led D1, D3 and D4: glowing of this led states the machine's output state.

Note: There is no led glow for state S0.

6.3 Software Output



Chapter 7

Conclusion

In conclusion, the FPGA vending machine project presented a practical and functional implementation of a vending machine using a Finite State Machine (FSM) approach. The project successfully demonstrated how FPGA technology can be used to implement a vending machine that accepts coins and dispenses products according to user input.

The development of a soda dispenser vending machine using FPGA technology has been successfully implemented. The system design was based on a Moore machine architecture, which allowed the system to respond quickly to user inputs and accurately dispense the requested soda type and quantity. Throughout the design and implementation process, several challenges were encountered, such as ordering the state transitions, generating UCF file, etc. These challenges were addressed through careful system testing and debugging. The development of this vending machine soda dispenser demonstrates the potential of FPGA technology for creating customized digital systems for a range of applications. With further refinement and optimization, this technology could be applied to a variety of industries and use cases, including other types of vending machines, control systems, and industrial automation.

References

- [1] *P Pradeepa, T Sudhalavanya, K Suganthi, N Suganthi, M Menagadevi, DESIGN AND IMPLEMENTATION OF VENDING MACHINE USING VERILOG HDL, International Journal of advanced engineering technology 4 (1), 51-53,2013*
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