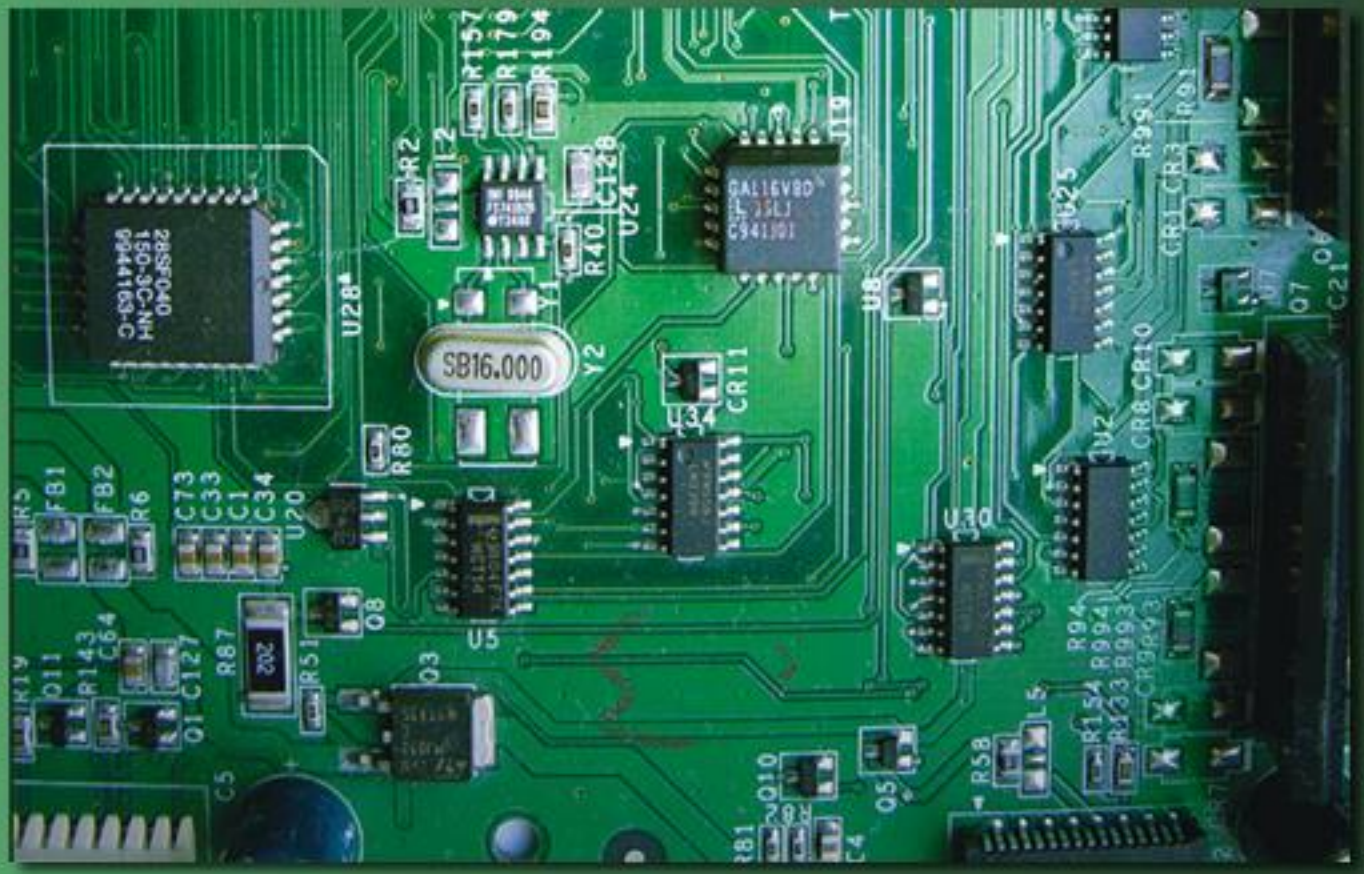
The Intel Microprocessors

8086/8088, 80186/80188, 80286, 80386, 80486 Pentium, Pentium Pro Processor, Pentium II, Pentium 4, and Core2 with 64-bit Extensions

Architecture, Programming, and Interfacing



EIGHTH EDITION

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PEARSON

Chapter 11: Basic I/O Interface

Introduction

- This chapter outlines some of the basic methods of communications, both serial and parallel, between humans or machines and the microprocessor.
- We first introduce the basic I/O interface and discuss decoding for I/O devices.
- Then, we provide detail on parallel and serial interfacing, both of which have a variety of applications.

Chapter Objectives

Upon completion of this chapter, you will be able to:

- Explain the operation of the basic input and output interfaces.
- Decode an 8-, 16-, and 32-bit I/O device so that they can be used at any I/O port address.
- Define handshaking and explain how to use it with I/O devices.
- Interface and program the 82C55 programmable parallel interface.

Chapter Objectives (*cont.*)

Upon completion of this chapter, you will be able to:

- Interface LCD displays, LED displays, keyboards, ADC, DAC, and various other devices to the 82C55.
- Interface and program the 16550 serial communications interface adapter.
- Interface and program the 8254 programmable interval timer.

Chapter Objectives (*cont.*)

Upon completion of this chapter, you will be able to:

- Interface an analog-to-digital converter and a digital-to-analog converter to the microprocessor.
- Interface both DC and stepper motors to the microprocessor.

11–4 8254 PROGRAMMABLE INTERVAL TIMER

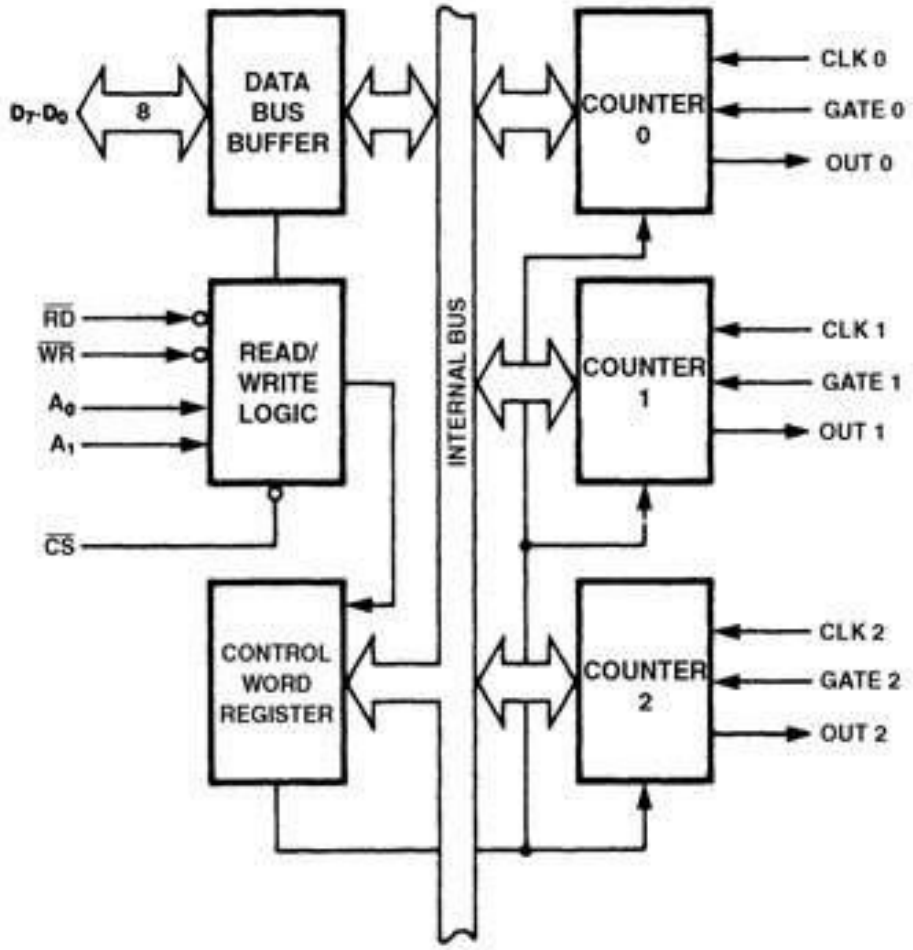
- The 8254 consists of three independent 16-bit programmable counters (**timers**).
- Each counter is capable of counting in binary or binary-coded decimal (BCD).
  - maximum allowable input frequency to any counter is 10 MHz
- Useful where the microprocessor must control real-time events.

- Usage includes real-time clocks, event counters, and motor speed/direction control.
- Timer appears in the PC decoded at ports 40H–43H to do the following:
  - 1. Generate a basic timer interrupt that occurs at approximately 18.2 Hz
  - 2. Cause the DRAM memory system to be refreshed
  - 3. Provide a timing source to the internal speaker and other devices.
- Timer in the PC is an 8253 instead of 8254.

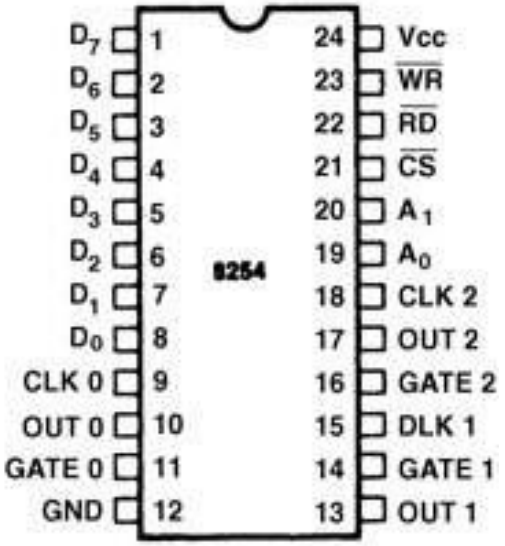
8254 Functional Description

- Figure 11–33 shows the pin-out of the 8254, a higher-speed version of the 8253, and a diagram of one of the three counters.
- Each timer contains:
  - a CLK input which provides the basic operating frequency to the timer
  - a gate input pin which controls the timer in some modes
  - an output (OUT) connection to obtain the output of the timer

Figure 11–33 The 8254 programmable interval timer. (a) Internal structure and (b) pin-out. (Courtesy of Intel Corporation.)



(a)



(b)

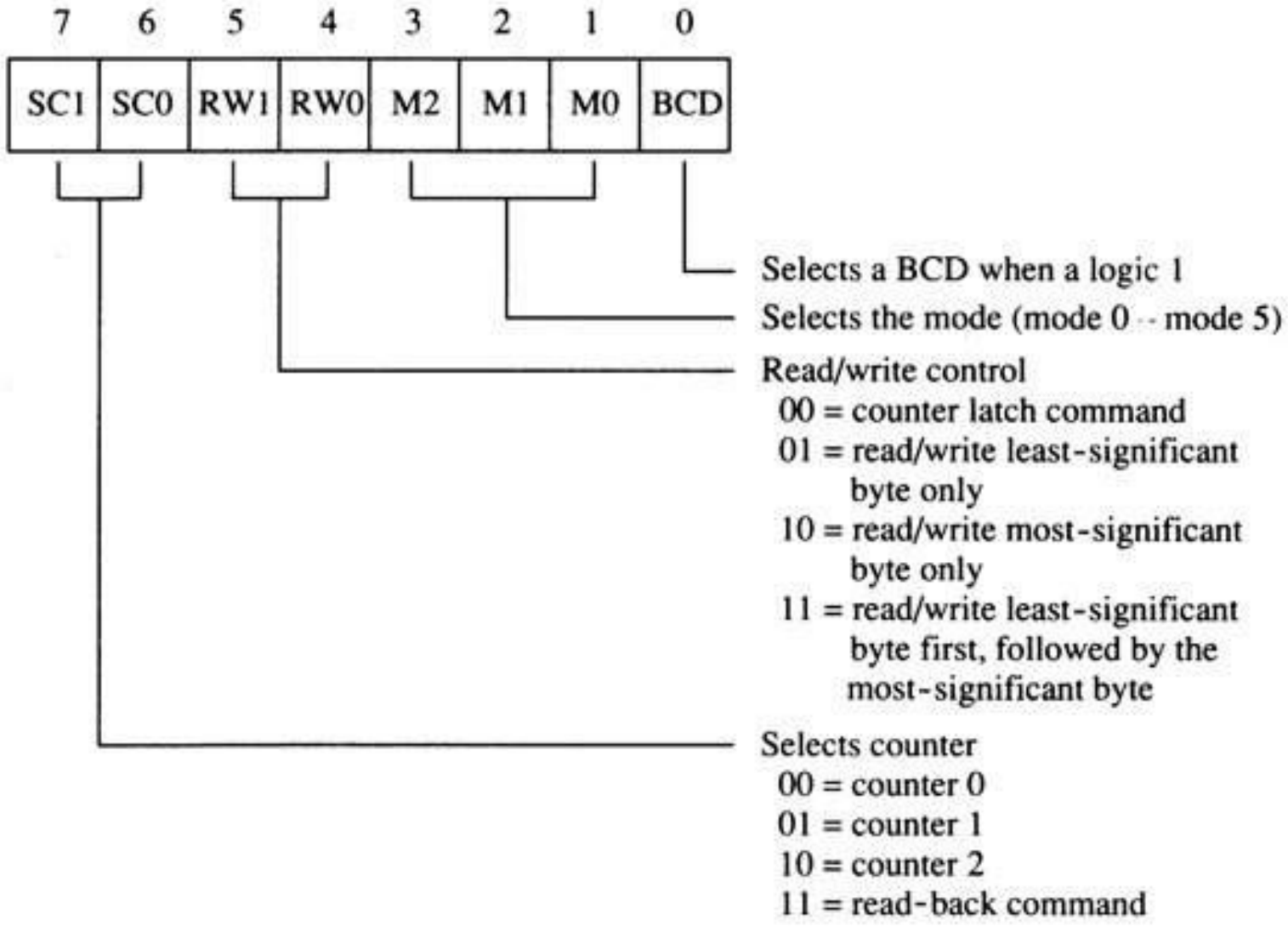
- The signals that connect to the processor are the data bus pins (D_7–D_0), $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, and address inputs A_1 and A_0.
- Address inputs are present to select any of the four internal registers.
  - used for programming, reading, or writing to a counter

- Timer zero generates an 18.2 Hz signal that interrupts the microprocessor at interrupt vector 8 for a clock tick.
  - often used to time programs and events in DOS
- Timer 1 is programmed for 15 μs, used on the PC to request a DMA action used to refresh the dynamic RAM.
- Timer 2 is programmed to generate a tone on the PC speaker.

Programming the 8254

- Each counter is programmed by writing a control word, followed by the initial count.
  - fig 11–34 lists the program control word structure
- The control word allows the programmer to select the counter, mode of operation, and type of operation (read/write).
  - also selects either a binary or BCD count

Figure 11–34 The control word for the 8254-2 timer.



- Each counter may be programmed with a count of 1 to FFFFH; A count of 0 is equal to FFFFH+l (65,536) or 10,000 in BCD.
- Timer 0 is used in the PC with a divide-by count of 64K (FFFFH) to generate the 18.2 Hz (18.196 Hz) interrupt clock tick.
  - timer 0 has a clock input frequency of 4.77 MHz + 4 or 1.1925 MHz
- The order of programming is important for each counter, but programming of different counters may be interleaved for better control.

EXAMPLE 10–21

```
PROGRAM CONTROL WORD 1          ;setup counter 1
PROGRAM CONTROL WORD 2          ;setup counter 2
PROGRAM LSB 1                   ;stop counter 1 and program LSB
PROGRAM LSB 2                   ;stop counter 2 and program LSB
PROGRAM MSB 1                   ;program MSB of counter 1 and start it
PROGRAM MSB 2                   ;program MSB of counter 2 and start it
```

or

```
PROGRAM CONTROL WORD 1          ;setup counter 1
PROGRAM LSB 1                   ;stop counter 1 and program LSB
PROGRAM MSB 1                   ;program MSB of counter 1 and start it
PROGRAM CONTROL WORD 2          ;setup counter 2
PROGRAM LSB 2                   ;stop counter 2 and program LSB
PROGRAM MSB 2                   ;program MSB of counter 2 and start it
```

Modes of Operation

- six modes (0–5) of available to each of the 8254 counters
- each mode functions with the CLK input, the gate (G) control signal, and OUT signal

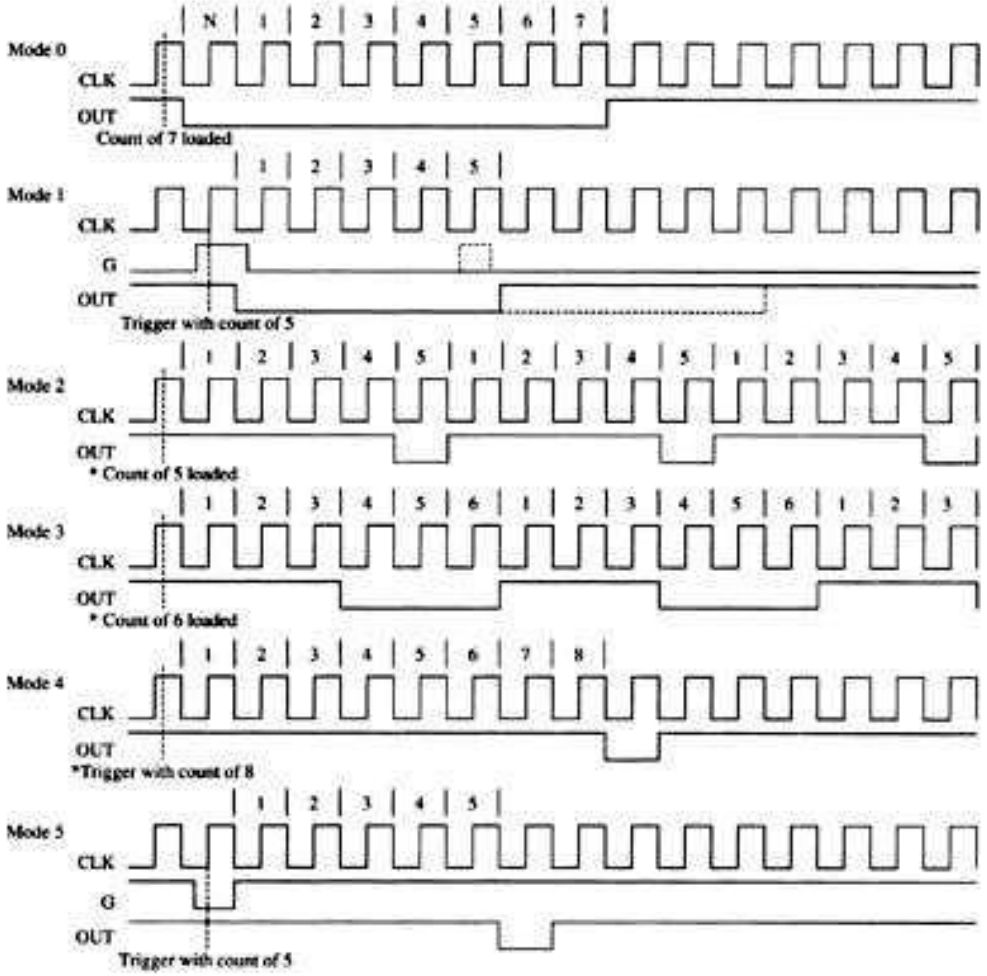


Figure 11–35 The six modes of operation for the 8254-2 programmable interval timer. The G input stops the count when 0 in modes 2, 3, and 4.

Mode 0

- Allows 8254 to be used as an event counter.
- Output becomes logic 0 when the control word is written and remains until N plus the number of programmed counts.
- Note that gate (G) input must be logic 1 to allow the counter to count.
- If G becomes logic 0 in the middle of the count, the counter will stop until G again becomes logic 1.

Mode 1

- Causes function as a retriggerable, monostable multivibrator (one-shot).
- G input triggers the counter so it develops a pulse at the OUT connection that becomes logic 0 for the duration of the count.
  - if the count is 10, the OUT connection goes low for 10 clocking periods when triggered
- If G input occurs within the output pulse, the counter is reloaded and the OUT connection continues for the total length of the count.

Mode 2

- Allows the counter to generate a series of continuous pulses one clock pulse wide.
  - pulse separation is determined by the count
- For a count of 10, output is logic 1 for nine clock periods and low for one clock period.
- The cycle is repeated until the counter is programmed with a new count or until the G pin is placed at logic 0.
  - G input must be logic 1 for this mode to generate a continuous series of pulses

Mode 3

- Generates a continuous square wave at the OUT connection, provided the G pin is logic 1.
- If the count is even, output is high for one half of the count and low for one half of the count.
- If the count is odd, output is high for one clocking period longer than it is low.
  - if the counter is programmed for a count of 5, the output is high for three clocks and low for two clocks

Mode 4

- Allows a single pulse at the output.
- If count is programmed as 10, output is high for 10 clocking periods and low for one period.
  - the cycle does not begin until the counter is loaded with its complete count
- Operates as a software triggered one-shot.
- As with modes 2 and 3, this mode also uses the G input to enable the counter.
  - G input must be logic 1 for the counter to operate for these three modes

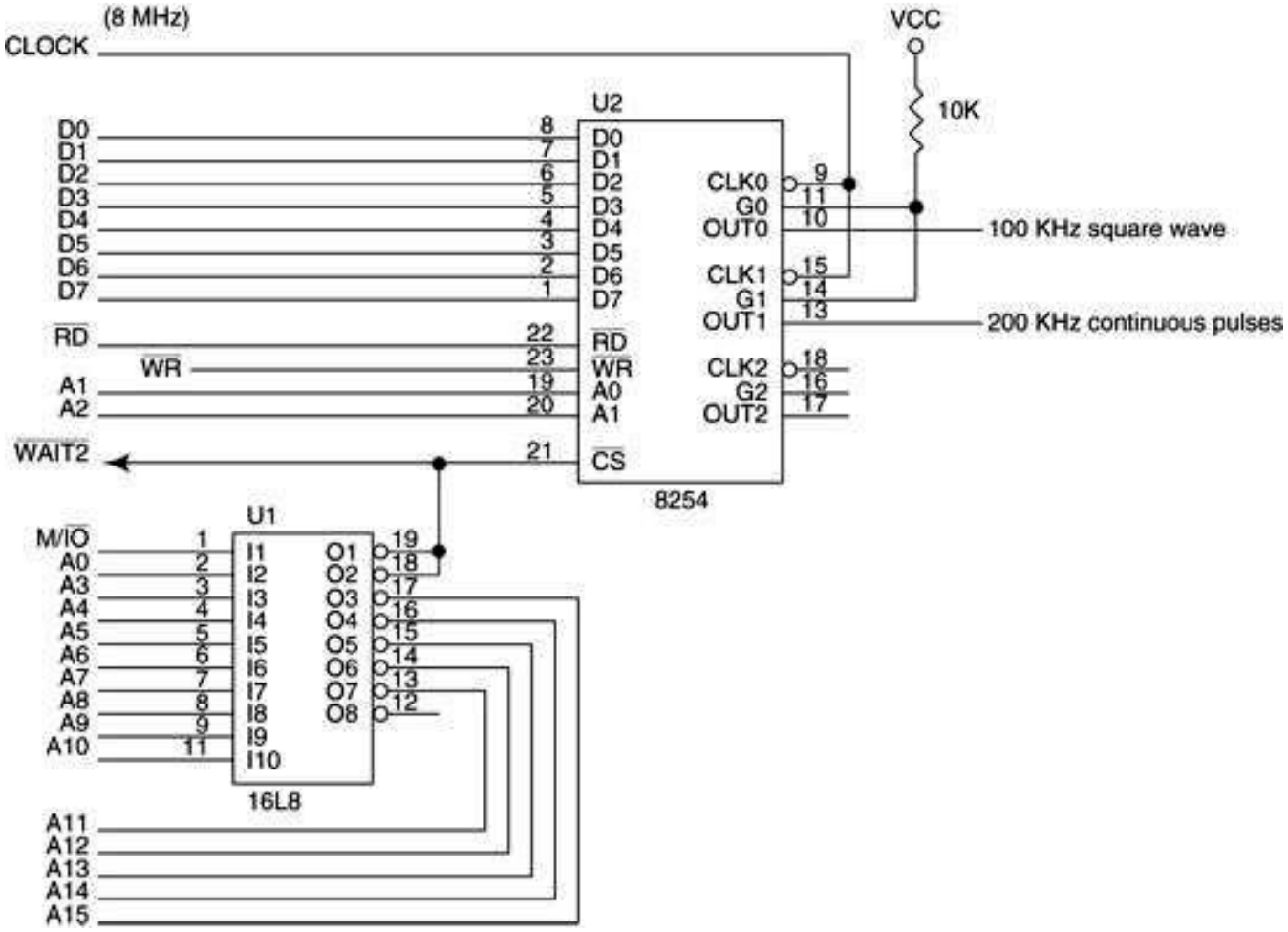
Mode 5

- A hardware triggered one-shot that functions as mode 4.
  - except it is started by a trigger pulse on the G pin instead of by software
- This mode is also similar to mode 1 because it is retriggerable.

Generating a Waveform with the 8254

- Fig 11–36 shows an 8254 connected to I/O ports 0700H, 0702H, 0704H, and 0706H of an 80386SX.
- The addresses are decoded by using a PLD that also generates a write strobe signal for the 8254, which is connected to the low-order data bus connections.

Figure 11–36 The 8254 interfaced to an 8 MHz 8086 so that it generates a 100 KHz square wave at OUT0 and a 200 KHz continuous pulse at OUT1.



- The PLD also generates a wait signal for the microprocessor that causes two wait states when the 8254 is accessed.
- The wait state generator connected to the microprocessor actually controls the number of wait states inserted into the timing.
- Example 11–24 lists the program that generates a 100 KHz square-wave at OUT0 and a 200 KHz continuous pulse at OUT1.

A procedure that programs the 8254 timer to function as illustrated in fig.- 11-36

```
TIME PROC NEAR USES AX DX
        MOV DX, 706H
        MOV AL, 00110110B
        OUT DX, AL
        MOV AL, 01110100B
        OUT DX, AL

        MOV DX, 700H
        MOV AL, 80
        OUT DX, AL
        MOV AL, 0
        OUT DX, AL
```

A procedure that programs the 8254 timer to function as illustrated in fig.- 11-34

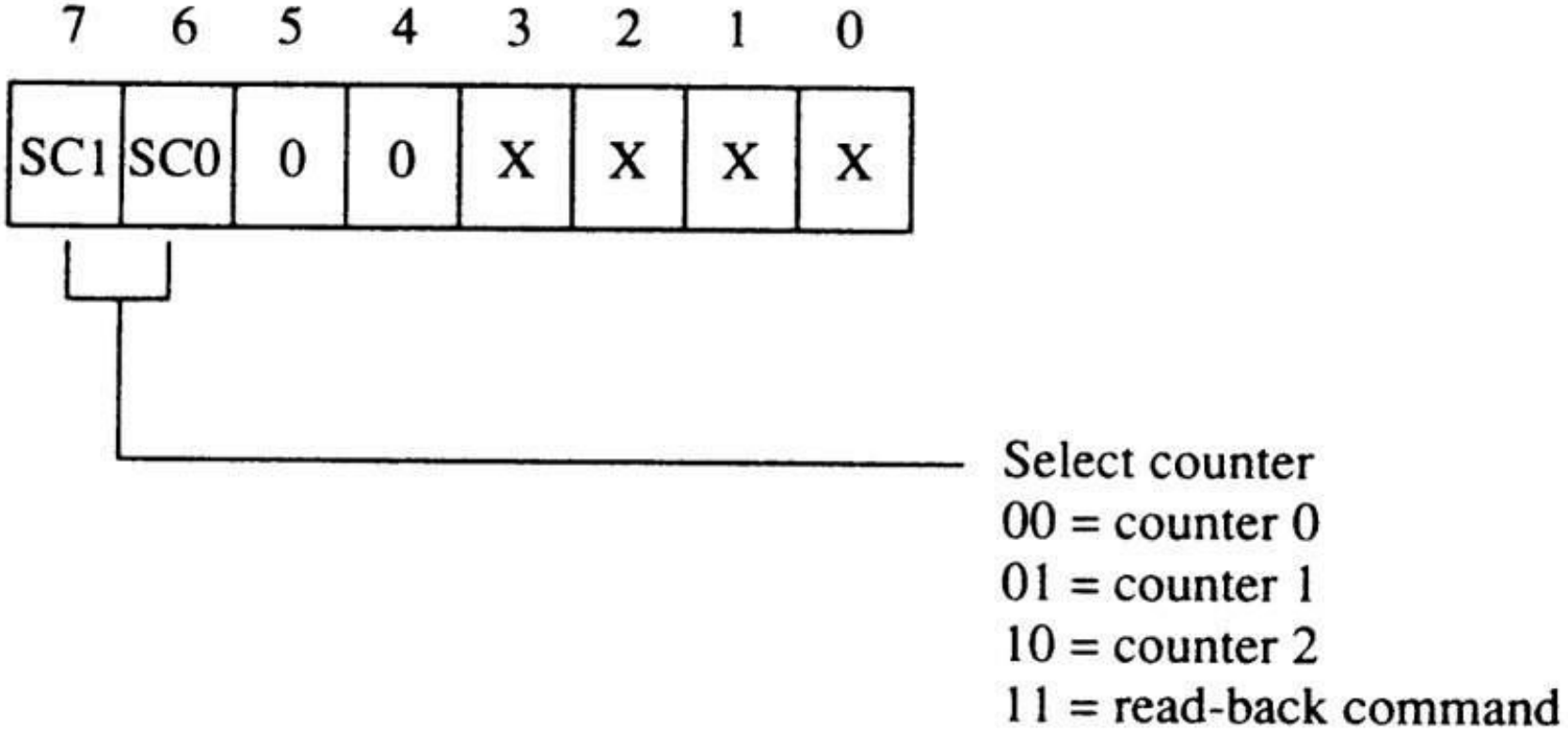
```
        MOV DX, 702H
        MOV AL, 40
        OUT DX, AL
        MOV AL, 0
        OUT DX, AL

        RET
TIME ENDP
```

Reading a Counter

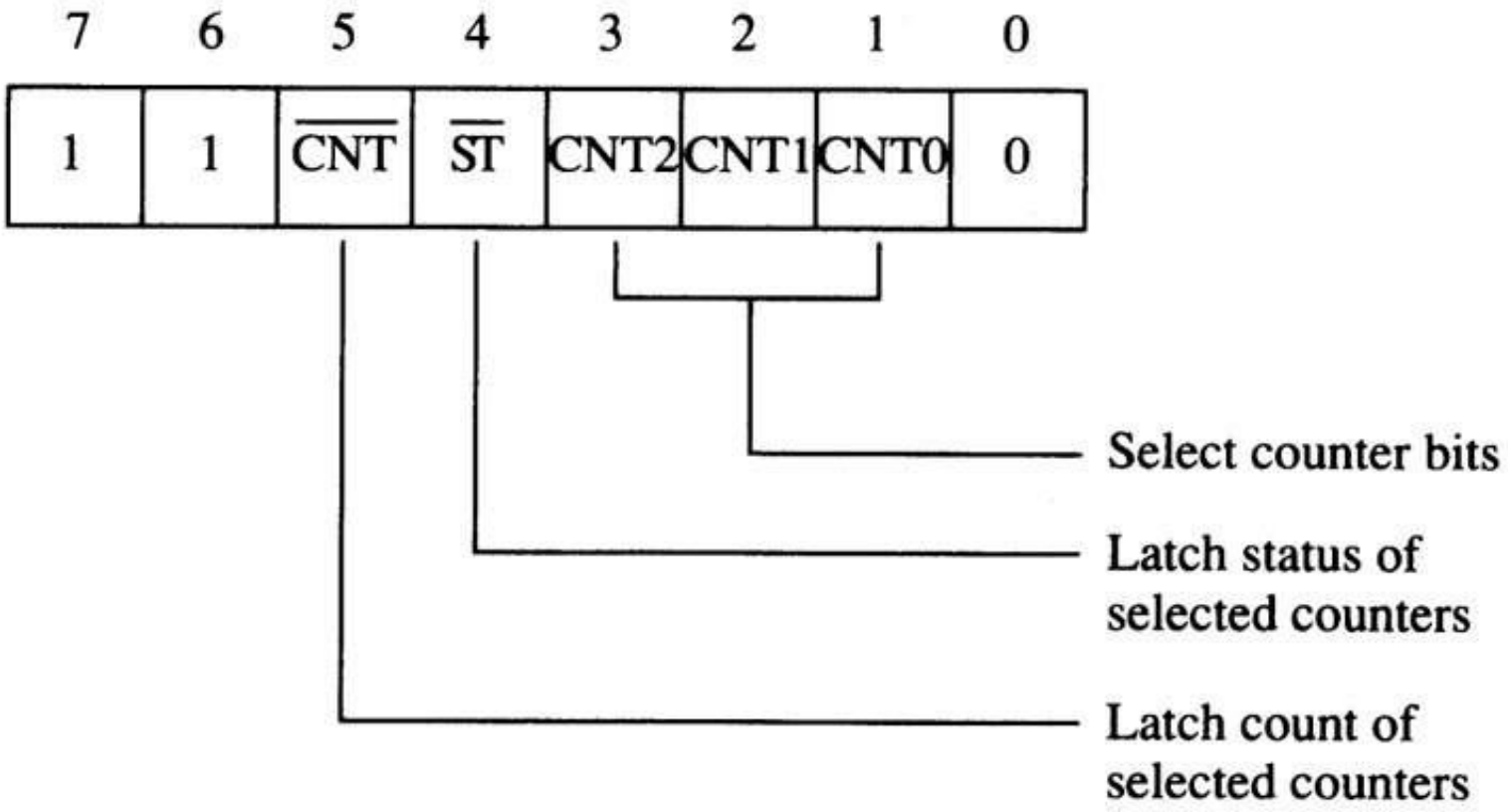
- Each counter has an internal latch read with the read counter port operation.
  - the latches will normally follow the count
- If counter contents are needed, the latch can remember the count by programming the counter latch control word.
- See Figure 11–37.
  - counter contents are held in a latch until read

Figure 11–37 The 8254-2 counter latch control word.



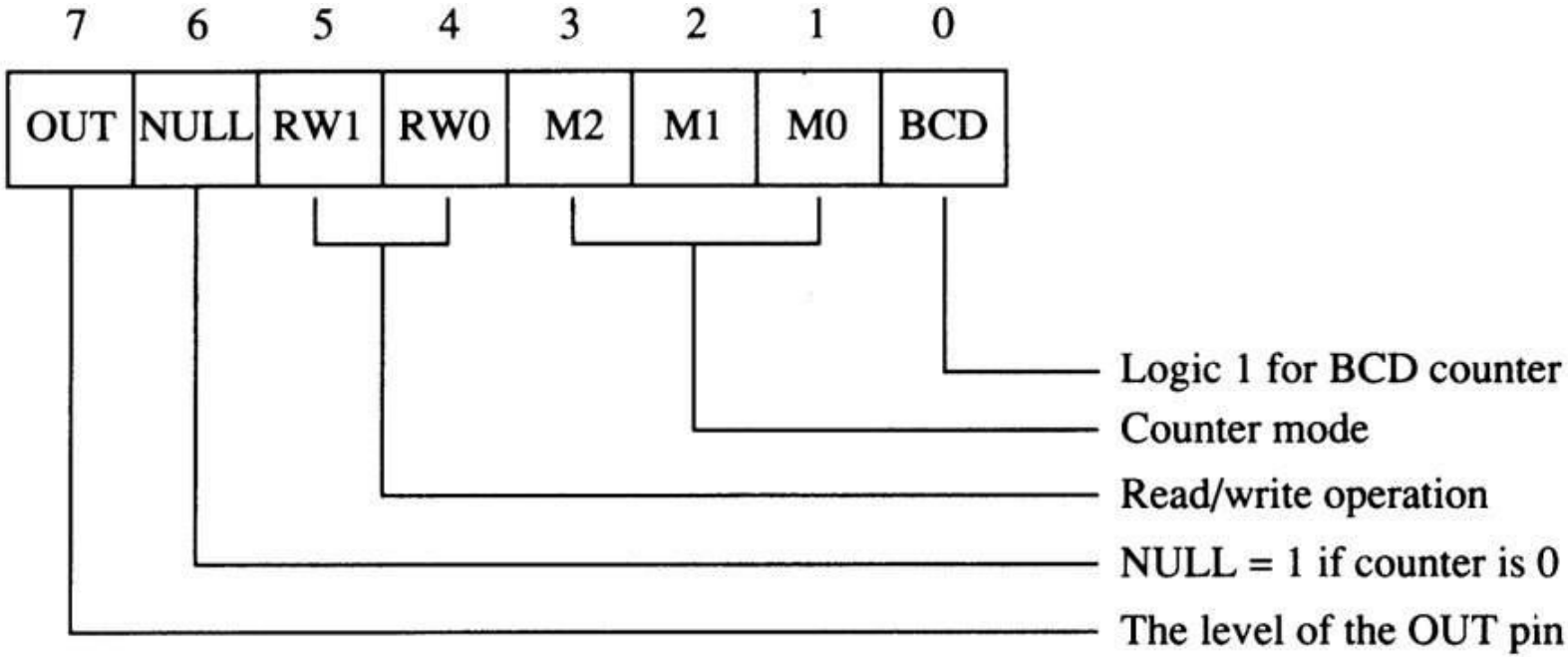
- When a read from the latch or counter is programmed, the latch tracks the contents.
- When necessary for contents of more than one counter to be read at the same time, the read-back control word is used
- Illustrated in Figure 11–38.

Figure 11–38 The 8254-2 read-back control word.



- With the read-back control word, the $\overline{\text{CNT}}$ bit is logic 0 to cause the counters selected by CNT0, CNT1, and CNT2 to be latched.
- If the status register is to be latched, then the bit is placed at logic 0.
- Figure 11–39 shows the status register, which shows:
  - the state of the output pin
  - whether the counter is at its null state (0)
  - how the counter is programmed

Figure 11–39 The 8254-2 status register.



DC Motor Speed and Direction Control

- An application of 8254 is as a motor speed controller for a DC motor.
- Fig 11–40 shows the schematic diagram of the motor and associated driver circuitry.
- It also illustrates the interconnection of the 8254, a flip-flop, and the motor and its driver.

Figure 11–40 Motor speed and direction control using the 8254 timer.

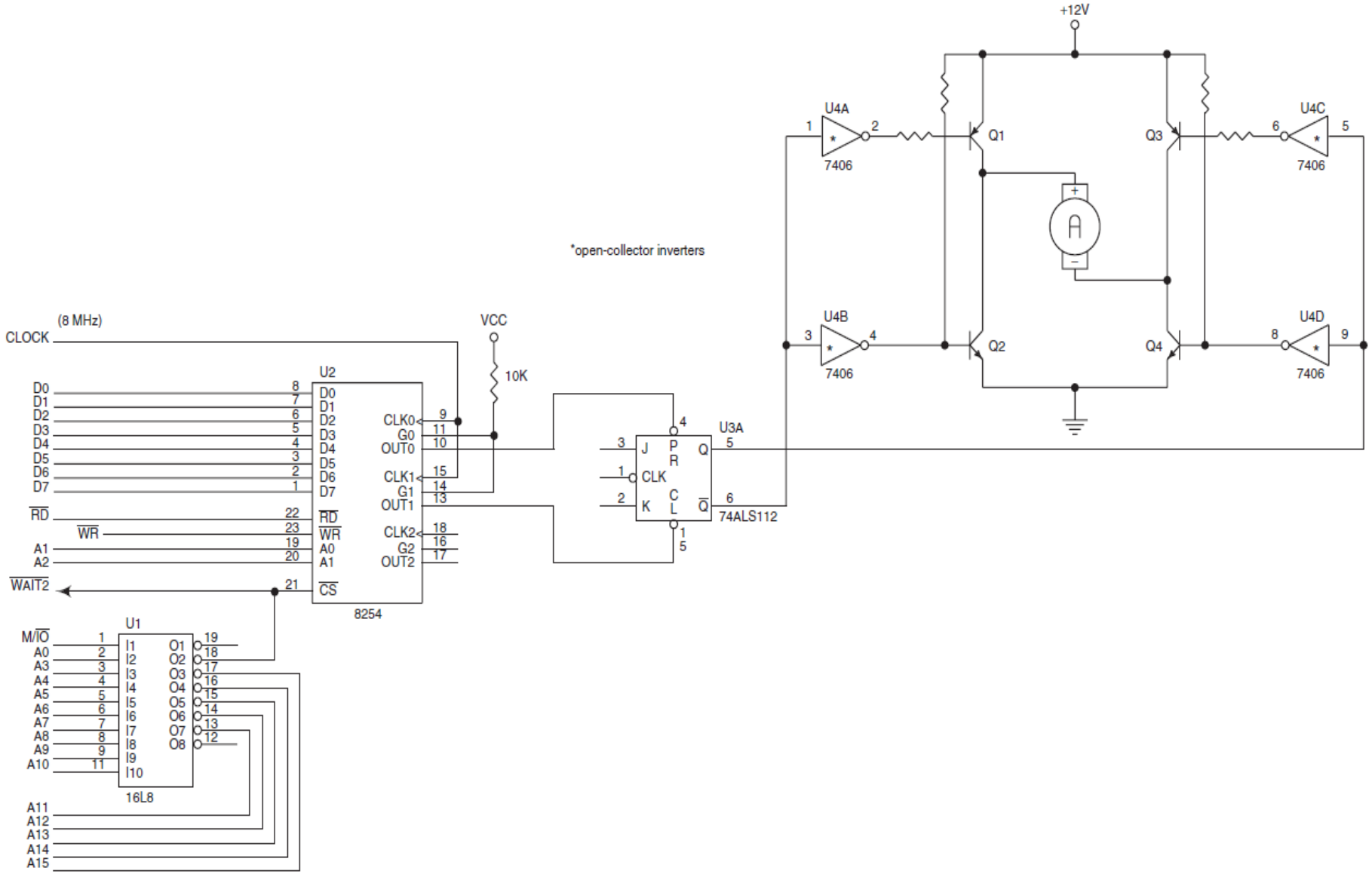
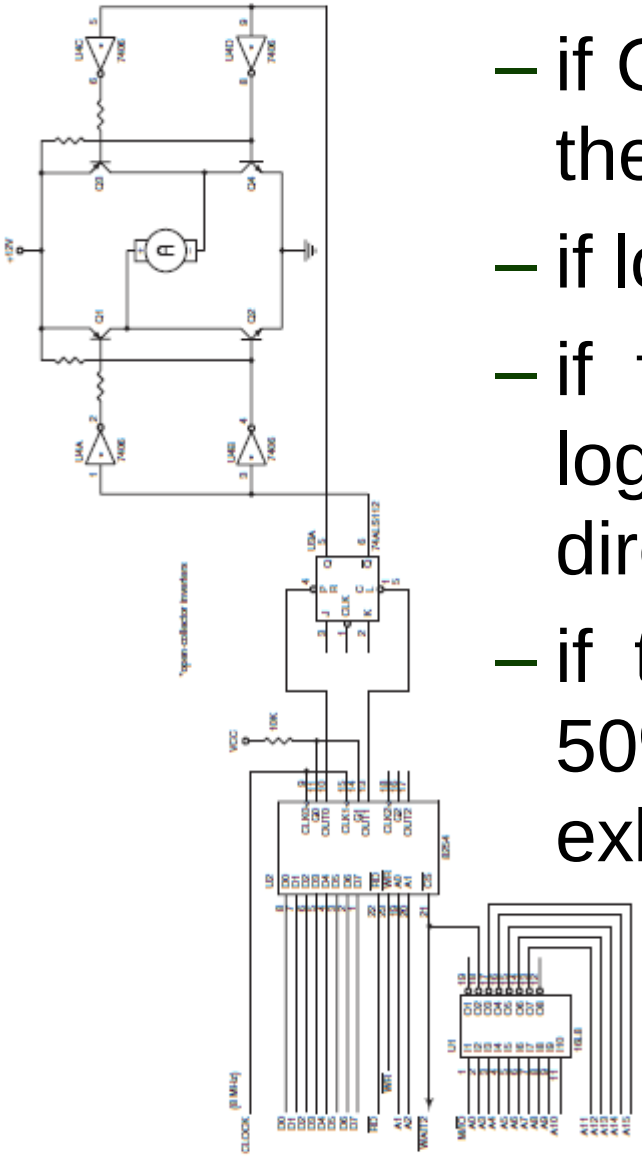


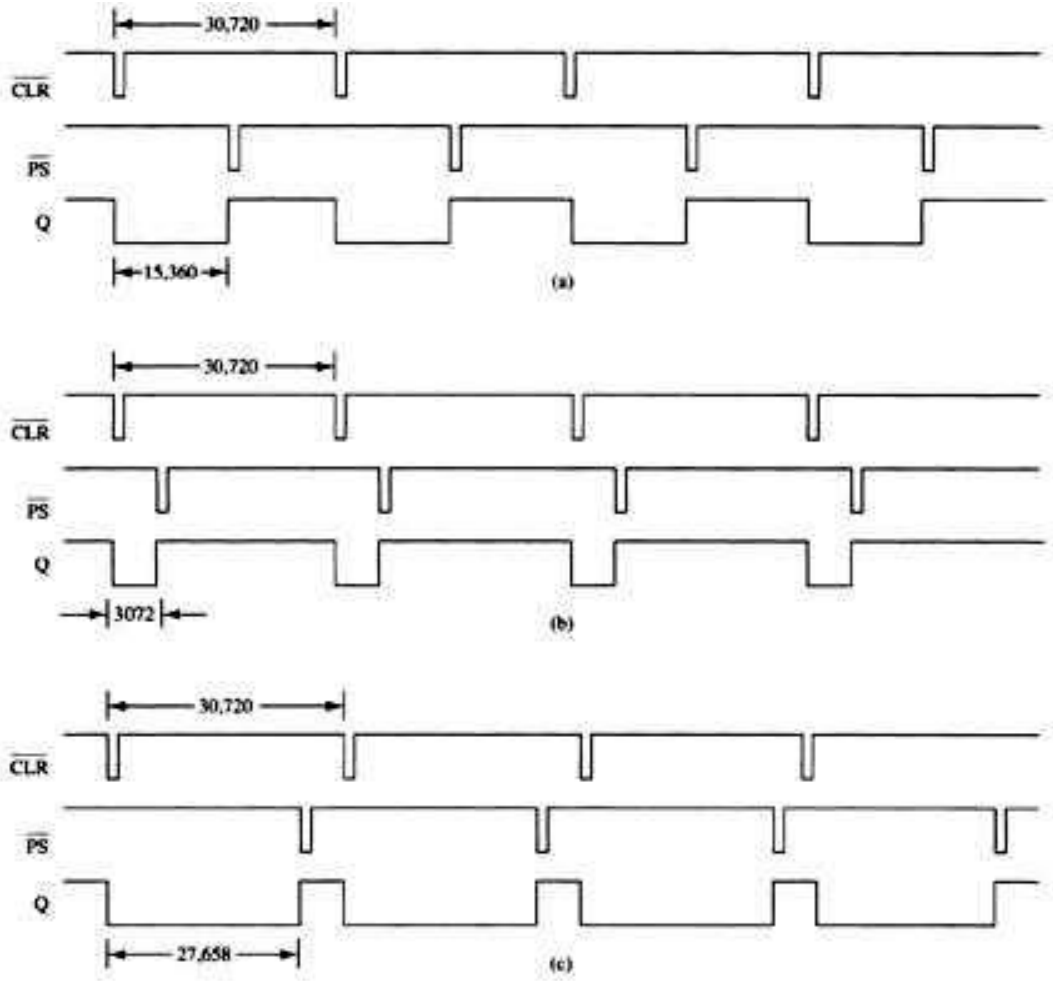
Figure 11–40 Motor speed and direction control using the 8254 timer.



- if Q output of the 74ALS112 is logic 1, the motor spins in its reverse direction
- if logic 0, the motor spins in forward
- if flip-flop output alternates between logic 1 and 0, the motor spins in either direction at various speeds
- if the duty cycle of the Q output is 50%, the motor will not spin at all and exhibits some holding torque

- Fig 11–41 shows some timing diagrams and effects on the speed/direction of the motor.
- Each counter generates pulses at different positions to vary the duty cycle at the Q output of the flip-flop.
- This output is also called *pulse width modulation.*
- Example 11–25 lists a procedure that controls the speed and direction of the motor.

Figure 11–41 Timing for the motor speed and direction control circuit of Figure 11–40. (a) No rotation, (b) high-speed rotation in the reverse direction, and (c) high-speed rotation in the forward direction.



A procedure that controls the speed and direction of the motor

```
CNTR   EQU    706H
CNT0   EQU    700H
CNT1   EQU    702H
COUNT EQU    30720

SPEED PROC NEAR USES BX DX AX

        MOV BL, AH
        MOV AX, 120
        MUL BL
        MOV BX, AX
        MOV AX, COUNT
        SUB AX, BX
        MOV BX, AX
```

A procedure that controls the speed and direction of the motor

```
MOV DX, CNTR
MOV AL, 00110100B
OUT DX, AL
MOV AL, 01110100B
OUT DX, AL

MOV DX, CNT1
MOV AX, COUNT
OUT DX, AL
MOV AL, AH
OUT DX, AL
```

A procedure that controls the speed and direction of the motor

```
.REPEAT
        IN AL, DX
        XCHG AL, AH
        IN AL, DX
        XCHG AL, AH
.UNTIL BX == AX

MOV DX, CNT0
MOV AX, COUNT
OUT  DX, AL
MOV AL, AH
OUT  DX, AL

RET

SPEED ENDP
```

SUMMARY

- The 8254 is a programmable interval timer with three 16-bit counters that count in binary or binary-coded decimal (BCD).
- Each counter is independent and operates in six different modes: (1) events counter, (2) retriggerable, monostable multivibrator, (3) pulse generator, (4) square-wave generator, (5) software-triggered pulse generator, and (6) hardware-triggered pulse generator.