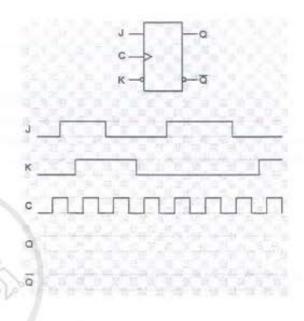


Daffodil International University

Department of Computer Science & Engineering Faculty of Science & Information Technology Final Examination Semester: Fall 2019

Course Code: CSE 212(Day) Course Title: Digital Electronics

Time: 2.0 hours Full Marks: 40 Answer any four(04) from the following questions 1. Suppose you have adders and some normal gates in your lab and your teacher asked you to construct a binary adder and subtractor in one circuit. How would you design it and explain its operation. b) Suppose you have J-K flip-flop in your lab and you want to construct a D flipflop from it. How can you design it? 2 c) Write down the differences between NAND and NOR latch. a) Construct a 2 to 4 decoder with its truth table and draw a circuit which stores 6 2. its output in one clock signal. 4 b) Implement a full adder circuit using multiplexers. a) Construct a 4 to 16 decoder using 3 to 8 decoders and explain how it works? 3 5 b) Differentiate between encoder and priority encoder. Explain the basic operation of priority encoder. a) Determine the output states for the J-K flip flop, given the following pulse 3 inputs; consider initial ouput is zero:



- b) Find out True/False:
 - Asynchronous inputs affect the state of the FF independent of the clock.

2

5

5

- A MUX is known as data distributor.
- III. An edge-triggered FF changes state always at the beginning.
- Decoders are used in Input/Output selection in computers.
- V. JK flip-flop has an ambiguity.
- c) What is the output of an XOR gate when a logic signal and its exact inverse are connected to its inputs?
- a) Implement the following function with a multiplexer:

$$F(W, X, Y, Z) = \sum (0, 1, 3, 4, 8, 9, 15)$$

b) Simplify the following Boolean function:

$$F(A, B, C, D) = \Sigma(1, 3, 7, 11, 15) + d\Sigma(0, 2, 5)$$