A NEW MULTILEVEL INVERTER TOPOLOGY USING LESS NUMBER OF SWITCHES

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A thesis submitted in partial fulfillment for the
Degree of Bachelor of Technology

in the Electrical and Electronic Engineering

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March 2013

ABSTRACT

The emergence of multilevel inverters has been in increase since the last decade. These new types of converters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum. Numerous topologies have been introduced and widely studied for utility and drive applications. Amongst these topologies, the multilevel cascaded inverter was introduced in Static VAR compensation and drive systems. This project presents a new technique for getting a multilevel output and also uses PWM control techniques. In this technique, the number of switches used for the dc to ac conversion is reduced. So this dc to ac conversion significantly reduces the initial cost. This technique exhibits some attractive features which suits industrial applications. MATLAB simulink environment is used to simulate the results. The hardware results are also presented for the proposed technique.

INTRODUCTION

Multilevel voltage source inverter is recognized as an important alternative to the normal two level voltage source inverter especially in high voltage application. Using multilevel technique, the amplitude of the voltage is increased, stress in the switching devices is reduced and the overall harmonics profile is improved. Among the familiar topologies, the most popular one is cascaded multilevel inverter. It exhibits several attractive features such as simple circuit layout, less components counts, modular in structure and avoid unbalance capacitor voltage problem. However as the number of output level increases, the circuit becomes bulky due to the increase in the number of power devices. In this project, it is proposed to employ a new technique to obtain a multilevel output using less number of power semiconductor switches when compared to ordinary cascaded multilevel inverter.

MULTILEVEL CONVERTER

INVERTER:

An inverter is an electrical device that converts direct current (DC) to alternating current (AC); the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits.

Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utility high-voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries.

The electrical inverter is a high-power electronic oscillator. It is so named because early mechanical AC to DC converters was made to work in reverse, and thus were "inverted", to convert DC to AC.

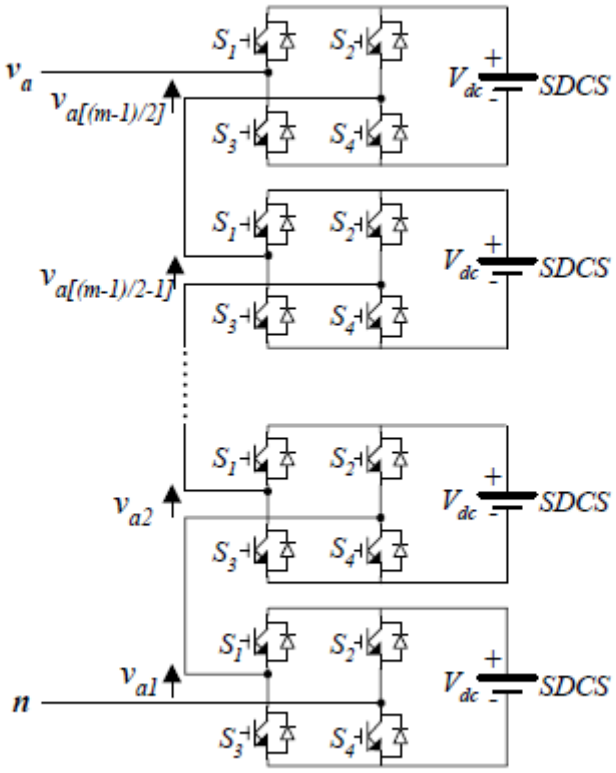
The inverter performs the opposite function of a rectifier

CASCADED H-BRIDGES INVERTER

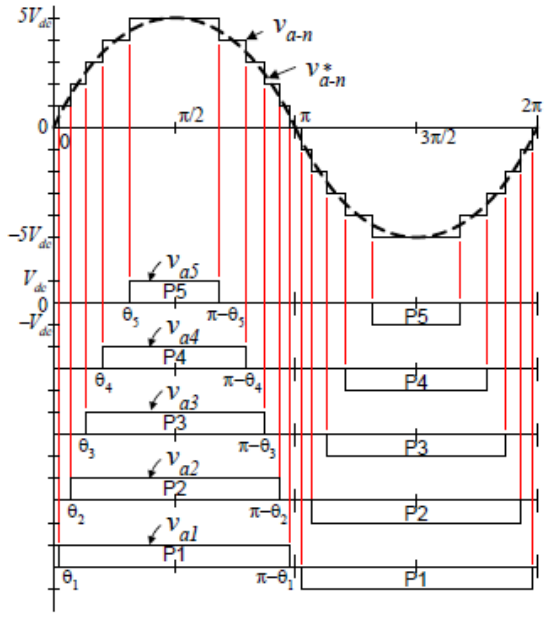
A single-phase structure of an m-level cascaded inverter is illustrated in Figure 31.1. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by $m = 2s+1$, where s is the number of separate dc sources. An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure 31.2. The phase voltage $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$.

For a stepped waveform such as the one depicted in Figure 31.2 with s steps, the Fourier Transform for this waveform follows

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_{n} \left[\cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s) \right] \frac{\sin(n\omega t)}{n}, \quad \text{where } n = 1, 3, 5, 7, \ldots$$



Single-phase structure of a multilevel cascaded H-bridges inverter



Output phase voltage waveform of an 11-level cascade inverter with 5 separate dc sources.

The magnitudes of the Fourier coefficients when normalized with respect to V_{dc} are as follows:

$$H(n) = \frac{4}{\pi n}\left[\cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s)\right], \quad \text{where } n = 1, 3, 5, 7, \ldots$$

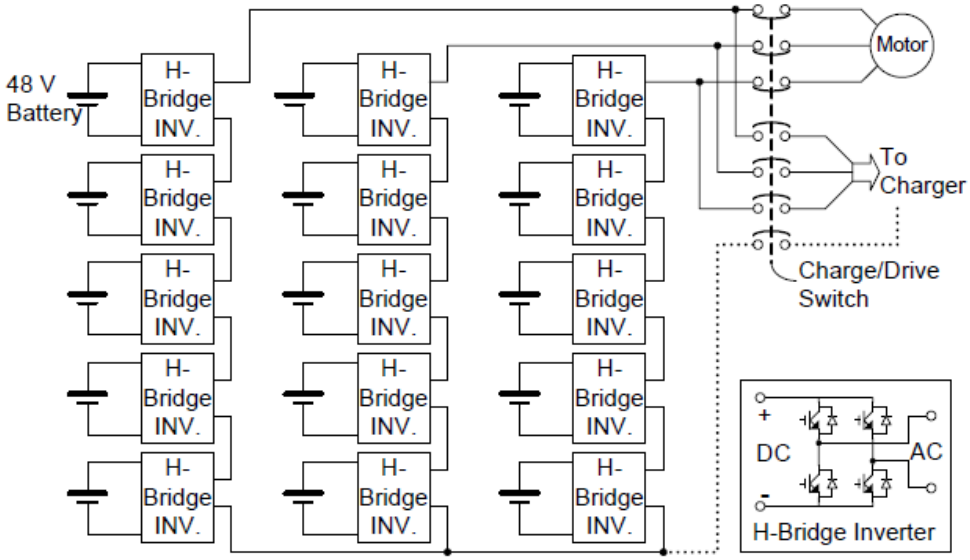
The conducting angles, θ_1, θ_2, ..., θ_s, can be chosen such that the voltage total harmonic distortion is a minimum. Generally, these angles are chosen so that predominant lower frequency harmonics, 5th, 7th, 11th, and 13th, harmonics are eliminated. More detail on harmonic elimination techniques will be presented in the next section.

Multilevel cascaded inverters have been proposed for such applications as static var generation, an interface with renewable energy sources, and for battery-based applications. Three-phase cascaded inverters can be connected in wye, as shown in Figure, or in delta. Peng has demonstrated a prototype multilevel cascaded static var generator connected in parallel with the electrical system that could supply or draw reactive current from an electrical system.

The inverter could be controlled to either regulate the power factor of the current drawn from the source or the bus voltage of the electrical system where the inverter was connected. Peng [20] and Joos [24] have also shown that a cascade inverter can be directly connected in series with the electrical system for static var compensation. Cascaded inverters are ideal for

connecting renewable energy sources with an ac grid, because of the need for separate dc sources, which is the case in applications such as photovoltaic's or fuel cells.

Cascaded inverters have also been proposed for use as the main traction drive in electric vehicles, where several batteries or ultra capacitors are well suited to serve as SDCSs. The cascaded inverter could also serve as a rectifier/charger for the batteries of an electric vehicle while the vehicle was connected to an ac supply as shown in Figure. Additionally, the cascade inverter can act as a rectifier in a vehicle that uses regenerative braking.



Three-phase wye-connection structure for electric vehicle motor drive and battery charging.

The main advantages and disadvantages of multilevel cascaded H-bridge converters are as follows

ADVANTAGES:

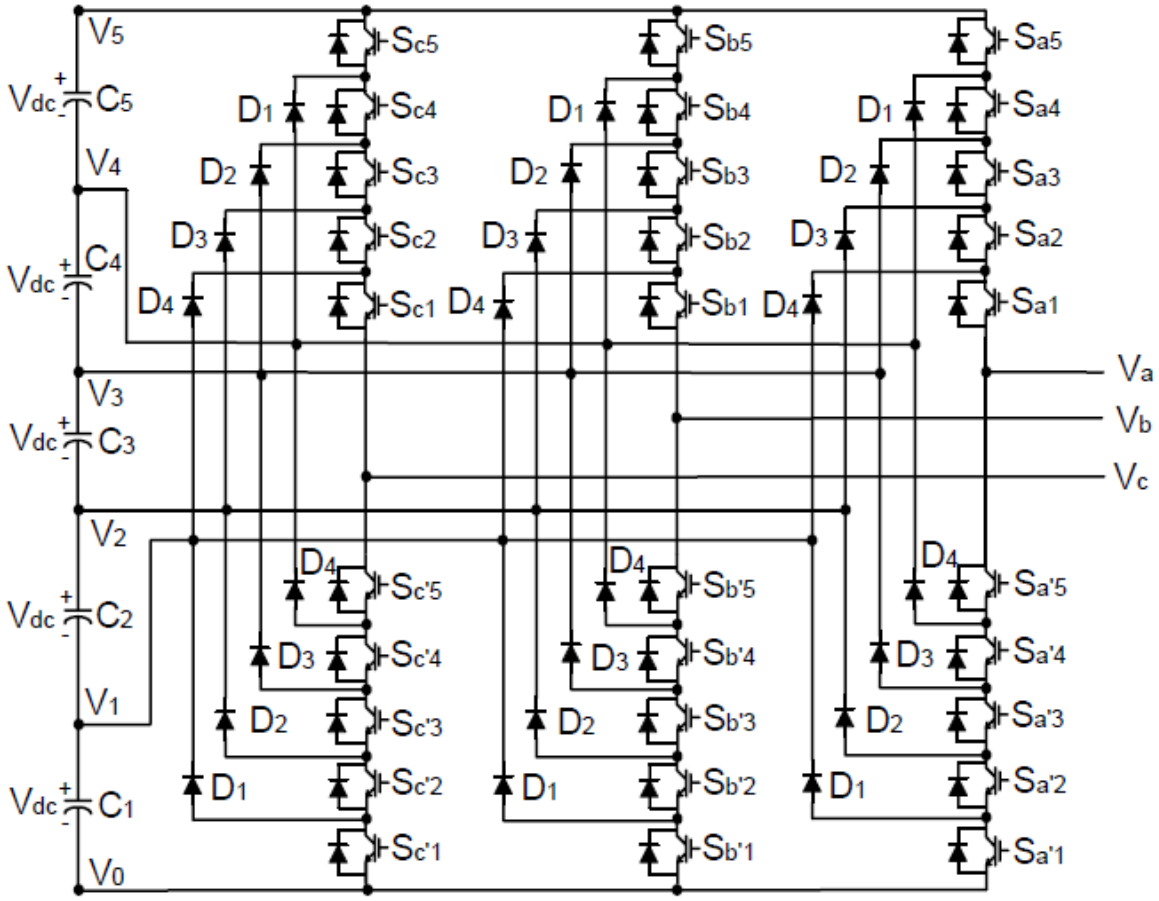
- The number of possible output voltage levels is more than twice the number of dc sources (m = 2s + 1).
- The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

DISADVANTAGES:

- Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple SDCSs readily available.

DIODE-CLAMPED MULTILEVEL INVERTER

The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter. In the 1990s several researchers published articles that have reported experimental results for four-, five-, and six-level diode-clamped converters for such uses as static var compensation, variable speed motor drives, and high-voltage system interconnections. A three-phase six-level diode-clamped inverter is shown in Figure. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is V_{dc}, and the voltage stress across each switching device is limited to V_{dc} through the clamping diodes. Table lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage V_0 as a reference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair requires that the other complementary switch be turned off. The complementary switch pairs for phase leg a are (S_{a1}, $S_{a'1}$), (S_{a2}, $S_{a'2}$), (S_{a3}, $S_{a'3}$), (S_{a4}, $S_{a'4}$), and (S_{a5}, $S_{a'5}$). Table also shows that in a diode-clamped inverter, the switches that are on for a particular phase leg are always adjacent and in series. For a six-level inverter, a set of five switches is on at any given time.



Three-phase six-level structure of a diode-clamped inverter.

Diode-clamped six-level inverter voltage levels and corresponding switch states.

Voltage V_{a0}	Switch State									
	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_5 = 5Vdc$	1	1	1	1	1	0	0	0	0	0
$V_4 = 4Vdc$	0	1	1	1	1	1	0	0	0	0
$V_3 = 3Vdc$	0	0	1	1	1	1	1	0	0	0
$V_2 = 2Vdc$	0	0	0	1	1	1	1	1	0	0
$V_1 = Vdc$	0	0	0	0	1	1	1	1	1	0
$V_0 = 0$	0	0	0	0	0	1	1	1	1	1

ADVANTAGES:

- All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back inter-connection or an adjustable speed drive.
- The capacitors can be pre-charged as a group.
- Efficiency is high for fundamental frequency switching.

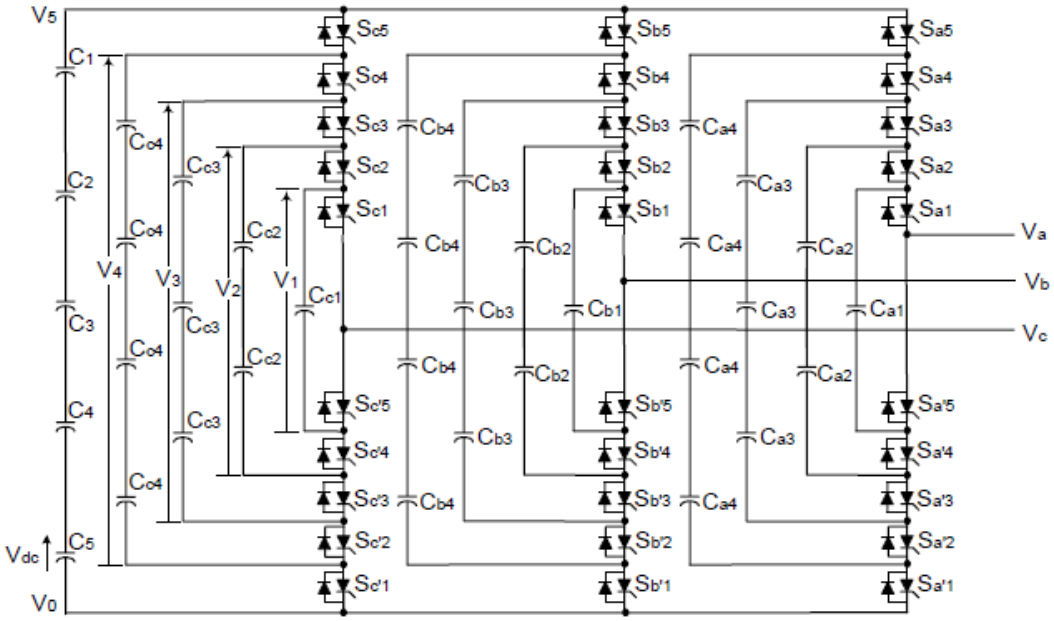
DISADVANTAGES:

- Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.
- The number of clamping diodes required is quadratically related to the number of levels, which can be cumbersome for units with a high number of levels.

FLYING CAPACITOR MULTILEVEL INVERTER

Meynard and Foch introduced a flying-capacitor-based inverter in 1992 [32]. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping

diodes, the inverter uses capacitors in their place. The circuit topology of the flying capacitor multilevel inverter is shown in Figure 31.7. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform.



Three-phase six-level structure of a flying capacitor inverter.

One advantage of the flying-capacitor-based inverter is that it has redundancies for inner voltage levels; in other words, two or more valid switch combinations can synthesize an output voltage. Table 31.2 shows a list of all the combinations of phase voltage levels that are possible for the six-level circuit shown in Figure 31.7. Unlike the diode-clamped inverter, the flying-capacitor inverter does not require all of the switches that are on (conducting) be in a consecutive series.

Moreover, the flying-capacitor inverter has phase redundancies, whereas the diode-clamped inverter has only line-line redundancies [2, 3, 33]. These redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels.

In addition to the (m-1) dc link capacitors, the m-level flying-capacitor multilevel inverter will require (m-1) × (m-2)/2 auxiliary capacitors per phase if the voltage rating of the capacitors is identical to that of the main switches. One application proposed in the literature for

the multilevel flying capacitor is static var generation [2, 3]. The main advantages and disadvantages of multilevel flying capacitor converters are as follows [2, 3].

ADVANTAGES:

- Phase redundancies are available for balancing the voltage levels of the capacitors.
- Real and reactive power flow can be controlled.
- The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.

DISADVANTAGES:

- Control is complicated to track the voltage levels for all of the capacitors. Also, precharging all of the capacitors to the same voltage level and startup are complex.
- Switching utilization and efficiency are poor for real power transmission.

The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Packaging is also more difficult in inverters with a high number of levels.

Flying-capacitor six-level inverter redundant voltage levels and corresponding switch states

Voltage V_{a0}	Switch State									
	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_{a0} = 5V_{dc}$ (no redundancies)										
$5V_{dc}$	1	1	1	1	1	0	0	0	0	0
$V_{a0} = 4V_{dc}$ (4 redundancies)										
$5V_{dc} - V_{dc}$	1	1	1	1	0	0	0	0	0	1
$4V_{dc}$	0	1	1	1	1	1	0	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc}$	1	0	1	1	1	0	1	0	0	0
$5V_{dc} - 3V_{dc} + 2V_{dc}$	1	1	0	1	1	0	0	1	0	0
$5V_{dc} - 2V_{dc} + V_{dc}$	1	1	1	0	1	0	0	0	1	0
$V_{a0} = 3V_{dc}$ (5 redundancies)										
$5V_{dc} - 2V_{dc}$	1	1	1	0	0	0	0	0	1	1
$4V_{dc} - V_{dc}$	0	1	1	1	0	1	0	0	0	1
$3V_{dc}$	0	0	1	1	1	1	1	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc} - V_{dc}$	1	0	1	1	0	0	1	0	0	1
$5V_{dc} - 3V_{dc} + V_{dc}$	1	1	0	0	1	0	0	1	1	0
$4V_{dc} - 2V_{dc} + V_{dc}$	0	1	1	0	1	1	0	0	1	0
$V_{a0} = 2V_{dc}$ (6 redundancies)										
$5V_{dc} - 3V_{dc}$	1	1	0	0	0	0	0	1	1	1
$5V_{dc} - 4V_{dc} + V_{dc}$	1	0	0	0	1	0	1	1	1	0
$4V_{dc} - 2V_{dc}$	0	1	1	0	0	1	0	0	1	1
$4V_{dc} - 3V_{dc} + V_{dc}$	0	1	0	0	1	1	0	1	1	0
$3V_{dc} - V_{dc}$	0	0	1	1	0	1	1	0	0	1
$3V_{dc} - 2V_{dc} + V_{dc}$	0	0	1	0	1	1	1	0	1	0
$2V_{dc}$	0	0	0	1	1	1	1	1	0	0
$V_{a0} = V_{dc}$ (4 redundancies)										
$5V_{dc} - 4V_{dc}$	1	0	0	0	0	0	1	1	1	1
$4V_{dc} - 3V_{dc}$	0	1	0	0	0	1	0	1	1	1
$3V_{dc} - 2V_{dc}$	0	0	1	0	0	1	1	0	1	1
$2V_{dc} - V_{dc}$	0	0	0	1	0	1	1	1	0	1
V_{dc}	0	0	0	0	1	1	1	1	1	0
$V_{a0} = 0$ (no redundancies)										
0	0	0	0	0	0	1	1	1	1	1

NUETRAL POINT CLAMPED (NPC) INVERTERS

NPC converters also known as three-level inverters.

Problems of 2-level inverter in high-power applications.

- High DC link voltage requires series connection of devices.

- Difficulty in dynamic voltage sharing during switching.

These problems are solved by using NPC inverter or multilevel inverter.

The below fig shows the NPC inverter circuit.

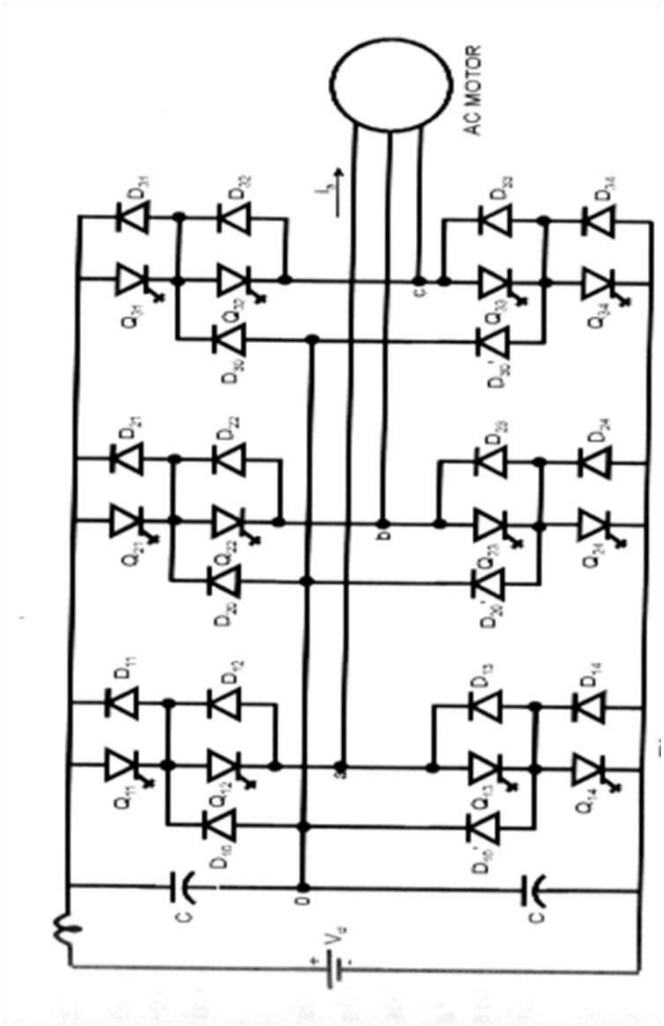


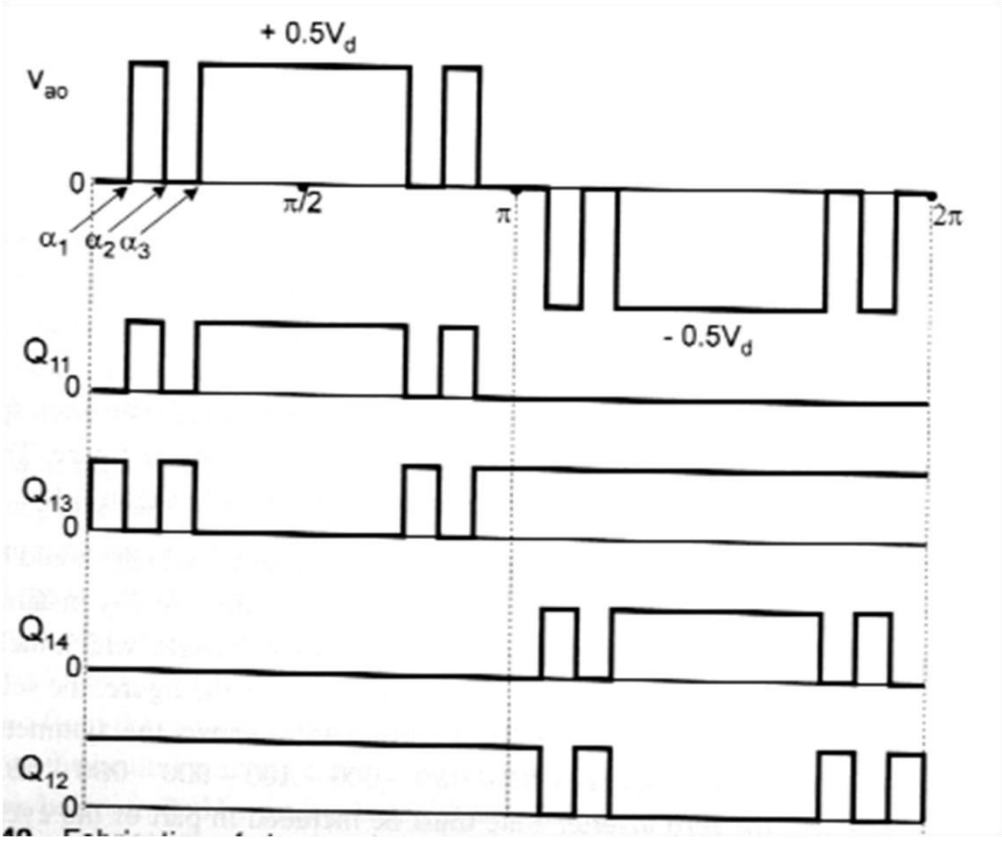
fig. NPC inverter

- DC link capacitor split to create neutral point 0
- Q_{11}, Q_{14} : main devices (2-level inverter)
- Q_{12}, Q_{13} : auxiliary devices – clamp output potential to neutral point with help of clamping diodes D_{10} D_{10}'
- Apply all PWM techniques

NPC inverter operation

- Consider HEPWM technique to eliminate 2 lowest significant harmonics (5^{th} and 7^{th}) and control fundamental voltage

- Phase voltage waveform (v_{a0}) and corresponding gate signals



- Each output potential clamped to neutral potential in off periods of PWM control
- For positive phase current +ia,

  Q_{11}, Q_{12} : when v_{a0} positive

  D_{13}, D_{14} : when v_{a0} negative

  D_{10}, Q_{12} : at neutral clamping condition
- For negative phase current -ia,

  D_{11}, D_{12} : when v_{a0} positive

  Q_{13}, Q_{14} : when v_{a0} negative

  O_{13}, D_{10}' : at neutral clamping condition
- Operation mode gives :

  3 levels waveform for phase voltage (v_{a0}) → +0.5 Vd, 0 , -0.5 Vd
- Levels of line voltage (v_{ab}) waveform of → +Vd, -Vd, +0.5 Vd, -0.5 Vd and 0
- Prove that each device has to withstand 0.5 V_d voltage

- D_{10}, D_{10}' conducting : voltage across main device clamped to +0.5 Vd
- When lower devices conducting : V_d appears across the upper devices in series (devices share 0.5 V_d statically)
- At any switching, voltage step size across the series string = 0.5 V_d $\rightarrow$ permits series connection of devices without exceeding 0.5 V_d rating

- Each leg has 3 switching states
  - State A : Upper switches ON
  - State B : Lower switches ON
  - State C : Auxiliary switches ON
- Available switching states = $3^3 = 27$ (8 for two-level inverters)

ADVANTAGES

- Allows voltage clamping
- Improve PWM harmonic quality
  - Based on HEPWM technique, lower significant harmonics of NPC inverter attenuated considerably compared to two-level inverter
  - Can be extended to more voltage levels for higher voltage/power levels

DISADVANTAGES

- Extra devices required
- Fluctuation of neutral point voltages with finite size of DC link capacitors (voltage level redundancies permits manipulation of PWM signals without diminishing quality)

APPLICATIONS

- Multi Megawatt induction /synchronous motor drives for industrial applications

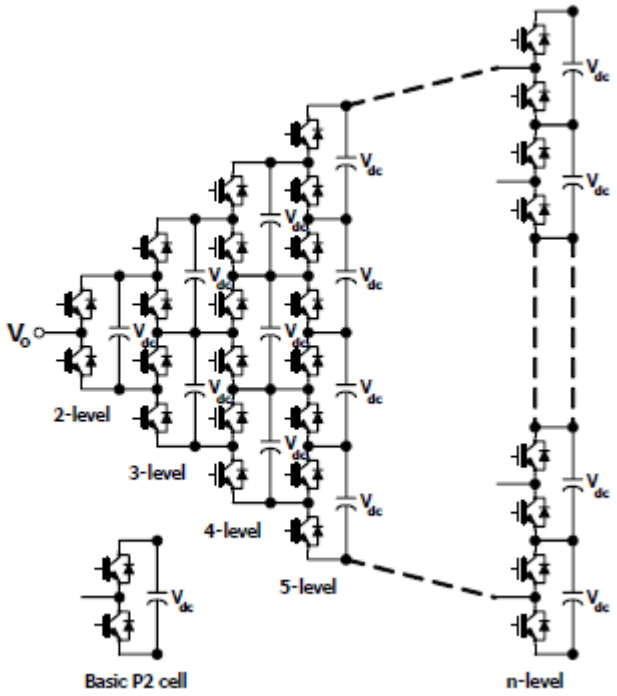
OTHER MULTILEVEL INVERTER STRUCTURES

Besides the three basic multilevel inverter topologies previously discussed, other multilevel converter topologies have been proposed; however, most of these are "hybrid" circuits that are combinations of two of the basic multilevel topologies or slight variations to them. Additionally, the combination of multilevel power converters can be designed to match with a specific application based on the basic topologies. In the interest of completeness, some of these will be identified and briefly described.

A. GENERALIZED MULTILEVEL TOPOLOGY

Existing multilevel converters such as diode-clamped and capacitor-clamped multilevel converters can be derived from the generalized converter topology called P2 topology proposed by Peng as illustrated in Figure. The generalized multilevel converter topology can balance each voltage level by itself regardless of load characteristics, active or reactive power conversion and without any assistance from other circuits at any number of levels automatically. Thus, the topology provides a complete multilevel topology that embraces the existing multilevel converters in principle.

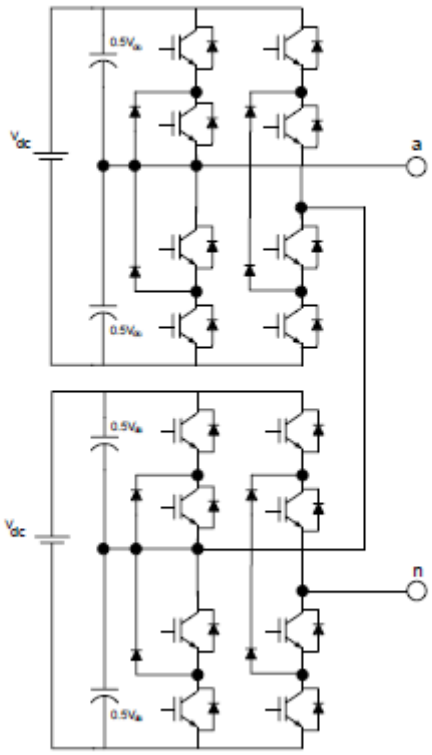
Figure shows the P2 multilevel converter structure per phase leg. Each switching device, diode, or capacitor's voltage is $1V_{dc}$, for instance, 1/ (m-1) of the DC-link voltage. Any converter with any number of levels, including the conventional bi-level converter can be obtained using this generalized topology.



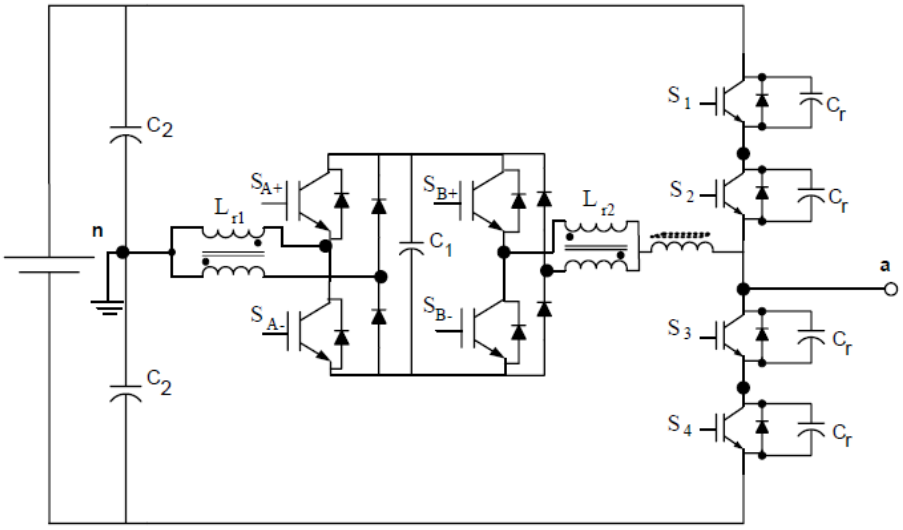
Generalized P2 multilevel converter topology for one phase leg.

B. MIXED-LEVEL HYBRID MULTILEVEL CONVERTER

To reduce the number of separate DC sources for high-voltage, high-power applications with multilevel converters, diode-clamped or capacitor-clamped converters could be used to replace the full-bridge cell in a cascaded converter [35]. An example is shown in Figure 31.9. The nine-level cascade converter incorporates a three-level diode-clamped converter as the cell. The original cascaded H-bridge multilevel converter requires four separate DC sources for one phase leg and twelve for a three-phase converter. If a five-level converter replaces the full-bridge cell, the voltage level is effectively doubled for each cell. Thus, to achieve the same nine voltage levels for each phase, only two separate DC sources are needed for one phase leg and six for a three-phase converter. The configuration has mixed-level hybrid multilevel units because it embeds multilevel cells as the building block of the cascade converter. The advantage of the topology is it needs less separate DC sources. The disadvantage for the topology is its control will be complicated due to its hybrid structure.



Mixed-level hybrid unit configuration using the three-level diode-clamped converter as the cascaded converter cell to increase the voltage levels.



Zero-voltage switching capacitor-clamped inverter circuit.

C. SOFT-SWITCHED MULTILEVEL CONVERTER

Some soft-switching methods can be implemented for different multilevel converters to reduce the switching loss and to increase efficiency. For the cascaded converter, because each converter cell is a bi-level circuit, the implementation of soft switching is not at all different from that of conventional bi-level converters. For capacitor-clamped or diode-clamped converters, soft-switching circuits have been proposed with different circuit combinations. One of soft-switching circuits is a zero-voltage-switching type which includes auxiliary resonant commutated pole (ARCP), coupled inductor with zero-voltage transition (ZVT), and their combinations [1, 36] as shown in Figure.

D. BACK-TO-BACK DIODE-CLAMPED CONVERTER

Two multilevel converters can be connected in a back-to-back arrangement and then the combination can be connected to the electrical system in a series-parallel arrangement as shown in Figure 31.11. Both the current demanded from the utility and the voltage delivered to the load can be controlled at the same time. This series-parallel active power filter has been referred to as a universal power conditioner [37-43] when used on electrical distribution systems and as a universal power flow controller [44-48] when applied at the transmission level. Previously, Lai and Peng [30] proposed the back-to-back diode-clamped topology shown in Figure 31.12 for use as a high-voltage dc inter connection between two asynchronous ac systems or as a rectifier/inverter for an adjustable speed drive for high-voltage motors. The diode-clamped inverter has been chosen over the other two basic multilevel circuit topologies for use in a universal power conditioner for the following reasons:

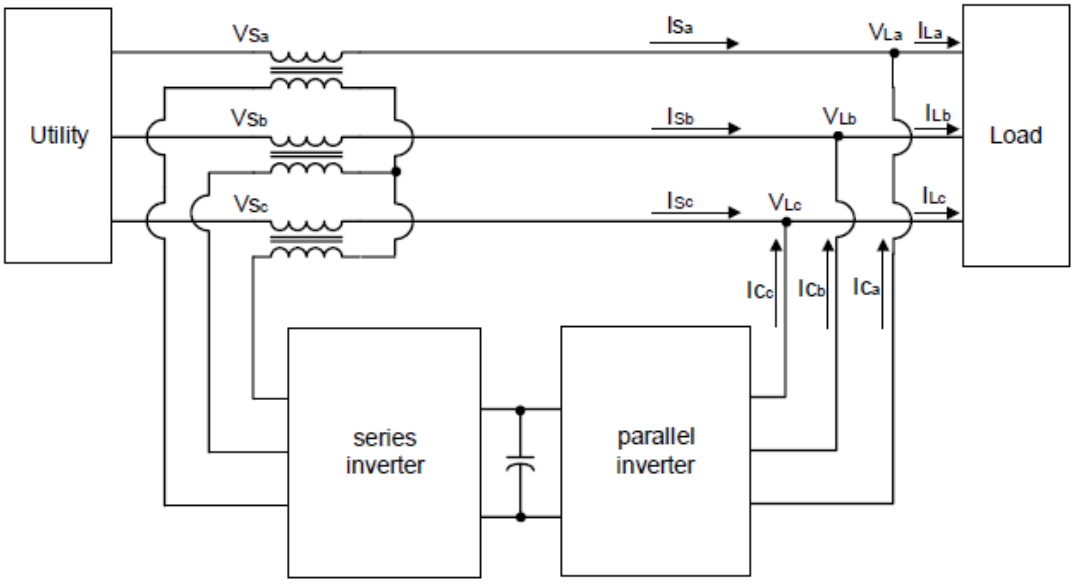
- All six phases (three on each inverter) can share a common dc link. Conversely, the cascade inverter requires that each dc level be separate, and this is not conducive to a back-to-back arrangement.
- The multilevel flying-capacitor converter also shares a common dc link; however, each phase leg requires several additional auxiliary capacitors. These extra capacitors would add substantially to the cost and the size of the conditioner.

Because a diode-clamped converter acting as a universal power conditioner will be expected to compensate for harmonics and/or operate in low amplitude modulation index regions, a more sophisticated, higher-frequency switch control than the fundamental frequency

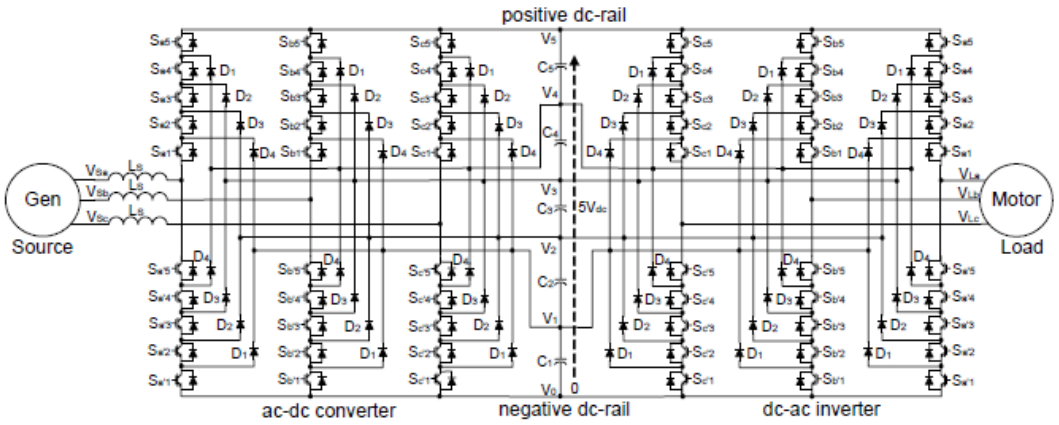
switching method will be needed. For this reason, multilevel space vector and carrier-based PWM approaches are compared in the next section, as well as novel carrier-based PWM methodologies.

MULTILEVEL CONVERTER PWM MODULATION STRATEGIES

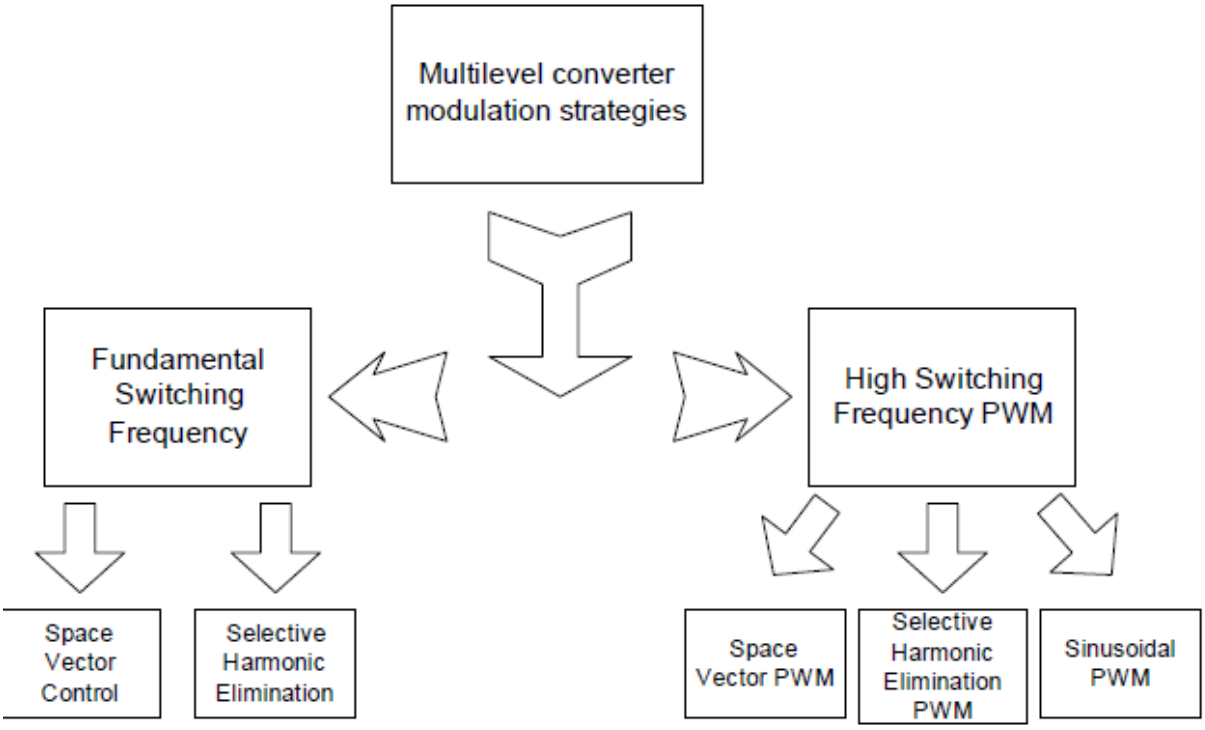
Pulse width modulation (PWM) strategies used in a conventional inverter can be modified to use in multilevel converters. The advent of the multilevel converter PWM modulation methodologies can be classified according to switching frequency as illustrated in Figure 31.13. The three multilevel PWM methods most discussed in the literature have been multilevel carrier-based PWM, selective harmonic elimination, and multilevel space vector PWM; all are extensions of traditional two-level PWM strategies to several levels. Other multilevel PWM methods have been used to a much lesser extent by researchers; therefore, only the three major techniques will be discussed in this chapter.



Series-parallel connection to electrical system of two back-to-back inverters.



Six-level diode-clamped back-to-back converter structure.



Classification of PWM multilevel converter modulation strategies

MULTILEVEL CONVERTER DESIGN EXAMPLE

NUMBER OF LEVELS AND VOLTAGE RATING OF ACTIVE DEVICES

In a multilevel inverter, determining the number of levels will be one of the most important factors because this affects many of the other sizing factors and control techniques. Tradeoffs in specifying the number of levels that the power conditioner will need and the advantages and complexity of having multiple voltage levels available are the primary differences that set a multilevel filter apart from a single level filter.

As a starting point, known is the nominal RMS voltage rating, V_{nom}, of the electrical system to which the diode clamped power conditioner will be connected. The dc link voltage must be at least as high as the amplitude of the nominal line-neutral voltage at the point of connection, or2·Vnom.

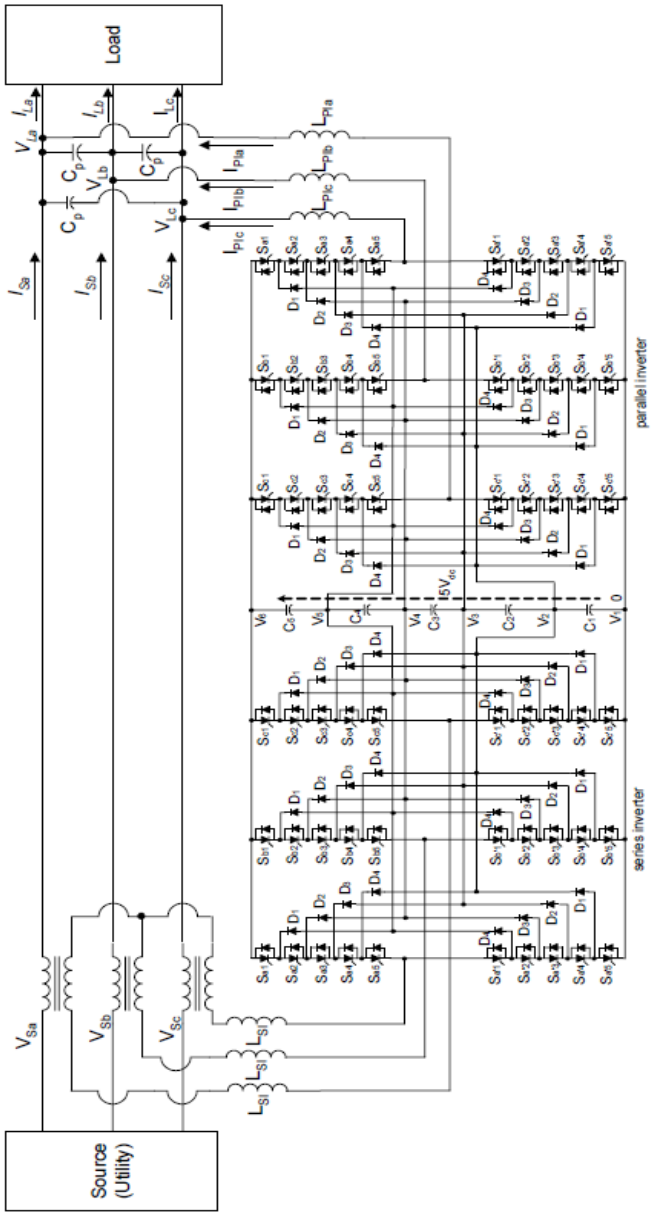
The parallel inverter must be able to inject currents by imposing a voltage across the parallel inductors, L_{PI}, that is the difference between the load voltage V_L and parallel inverter output voltage V_{PI}. The most difficult time to impose a voltage across the inductors is when the load voltage waveform is at its maximum or minimum. Simulation results have shown that the amplitude of the desired load voltage V_{nom} should not be more than 70 percent of the overall dc link voltage for the parallel inverter to have sufficient margin to inject appropriate compensation currents. Without this margin, complete compensation of reactive currents may not be possible. This margin can be incorporated into a design factor for the inverter. Because the dc link voltage and the voltage at the connection point can both vary, the design factor used in the rating selection process incorporates these elements as well as the small voltage drops that occur in the inverters during active device conduction.

The product of the number of the active devices in series (m-1) and the voltage rating of the devices V_{dev} must then be such that

$$V_{\substack{device \\ rating}} \cdot (m-1) \geq \sqrt{2} \cdot V_{nom} \cdot D_{\substack{design \\ factor}}.$$

The minimum number of levels and the voltage rating of the active devices (IGBTs, GTOs, power MOSFETs, etc.) are inversely related to each other. More levels in the inverter will

lower the required voltage device rating of individual devices; or looking at it another way, a higher voltage rating of the devices will enable a fewer minimum number of levels to be used.



Electrical system connection of multilevel diode-clamped power conditioner.

Increasing the number of levels does not affect the total voltage blocking capability of the active devices in each phase leg because lower device ratings can be used. Some of the benefits

of using more than the minimum required number of levels in a diode clamped inverter are as follows:

1. Voltage stress across each device is lower. Both active devices and dc link capacitors could be used that have lower voltage ratings (which sometimes are much cheaper and have greater availability).
2. The inverter will have a lower EMI because the dV/dt during each switching will be lower.
3. The output of the waveform will have more steps, or degrees of freedom, which enables the output waveform to more closely track a reference waveform.
4. Lower individual device switching frequency will achieve the same results as an inverter with a fewer number of levels and higher device switching frequency. Or the switching frequency can be kept the same as that in an inverter with a fewer number of levels to achieve a better waveform.

The drawbacks of using more than the required minimum number of levels are as follows:

1. Six active device control signals (one for each phase of the parallel inverter and the series inverter) are needed for each hardware level of the inverter – i.e., $6\cdot(m-1)$ control signals. Additional levels require more computational resources and add complexity to the control.
2. If the blocking diodes used in the inverter have the same rating as the active devices, their number increases dramatically because $6\cdot(m-2)\cdot(m-1)$ diodes would be required for the back-to-back structure.

Considering the trade-offs between the number of levels and the voltage rating of the devices will generally lead the designer to choose an appropriate value for each.

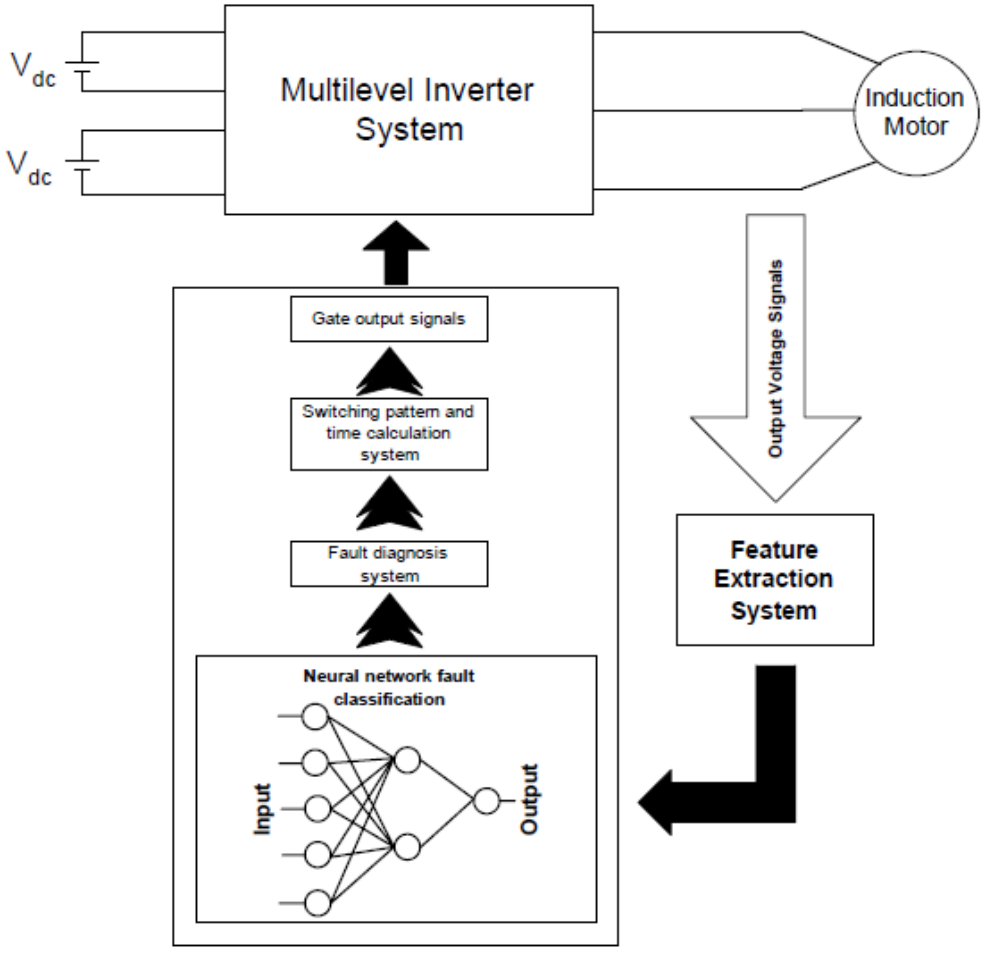
FAULT DIAGNOSIS IN MULTILEVEL CONVERTERS

Since a multilevel converter is normally used in medium to high power applications, the reliability of the multilevel converter system is very important. For instance industrial drive applications in manufacturing plants are dependent upon induction motors and their inverter systems for process control. Generally, the conventional protection systems are passive devices

such as fuses, overload relays, and circuit breakers to protect the inverter systems and the induction motors. The protection devices will disconnect the power sources from the multilevel inverter system whenever a fault occurs, stopping the operated process. Downtime of manufacturing equipment can add up to be thousands or hundreds of thousands of dollars per hour, therefore fault detection and diagnosis is vital to a company's bottom line. In order to maintain continuous operation for a multilevel inverter system, knowledge of fault behaviors, fault prediction, and fault diagnosis are necessary. Faults should be detected as soon as possible after they occur, because if a motor drive runs continuously under abnormal conditions, the drive or motor may quickly fail.

The possible structure for a fault diagnosis system is illustrated in Figure 31.33. The system is composed of four major states: feature extraction, neural network classification, fault diagnosis, and switching pattern calculation with gate signal output. The feature extraction performs the voltage input signal transformation, with rated signal values as important features, and the output of the transformed signal is transferred to the neural network classification. The networks are trained with both normal and abnormal data for the MLID; thus, the output of this network is nearly 0 and 1 as binary code. The binary code is sent to the fault diagnosis to decode the fault type and its location. Then, the switching pattern is calculated to reconfigure the multilevel inverter.

Switching patterns and the modulation index of other active switches can be adjusted to maintain voltage and current in a balanced condition after reconfiguration recovers from a fault. The MLID can continuously operate in a balanced condition; of course, the MLID will not be able to operate at its rated power. Therefore, the MLID can operate in balanced condition at reduced power after the fault occurs until the operator locates and replaces the damaged switch.



Structure of fault diagnosis system of a multilevel cascaded H-bridges inverter.

APPLICATIONS:

DC POWER SOURCE UTILIZATION

Inverter designed to provide 115 VAC from the 12 VDC source provided in an automobile. The unit shown provides up to 1.2 amperes of alternating current, or enough to power two sixty watt light bulbs.

An inverter converts the DC electricity from sources such as batteries, solar panels, or fuel cells to AC electricity. The electricity can be at any required voltage; in particular it can operate AC equipment designed for mains operation, or rectified to produce DC at any desired voltage.

Grid tie inverters can feed energy back into the distribution network because they produce alternating current with the same wave shape and frequency as supplied by the distribution system. They can also switch off automatically in the event of a blackout.

Micro-inverters convert direct current from individual solar panels into alternating current for the electric grid.

UNINTERRUPTIBLE POWER SUPPLIES

An uninterruptible power supply (UPS) uses batteries and an inverter to supply AC power when main power is not available. When main power is restored, a rectifier is used to supply DC power to recharge the batteries.

INDUCTION HEATING

Inverters convert low frequency main AC power to a higher frequency for use in induction heating. To do this, AC power is first rectified to provide DC power. The inverter then changes the DC power to high frequency AC power.

HVDC POWER TRANSMISSION

With HVDC power transmission, AC power is rectified and high voltage DC power is transmitted to another location. At the receiving location, an inverter in a static inverter plant converts the power back to AC.

VARIABLE-FREQUENCY DRIVES

A variable-frequency drive controls the operating speed of an AC motor by controlling the frequency and voltage of the power supplied to the motor. An inverter provides the controlled power. In most cases, the variable-frequency drive includes a rectifier so that DC power for the inverter can be provided from main AC power. Since an inverter is the key component, variable-frequency drives are sometimes called inverter drives or just inverters.

ELECTRIC VEHICLE DRIVES

Adjustable speed motor control inverters are currently used to power the traction motors in some electric and diesel-electric rail vehicles as well as some battery electric vehicles and hybrid electric highway vehicles such as the Toyota Prius. Various improvements in inverter technology are being developed specifically for electric vehicle applications.[2] In vehicles with regenerative braking, the inverter also takes power from the motor (now acting as a generator) and stores it in the batteries.

AIR CONDITIONING

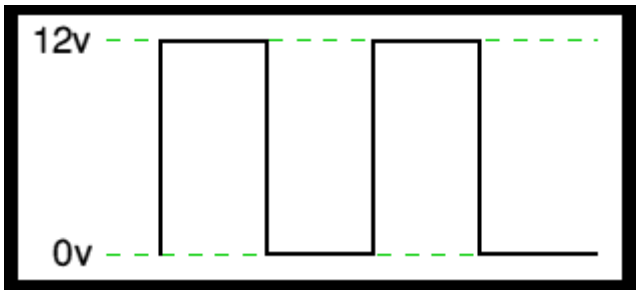
An air conditioner bearing the inverter tag uses a variable-frequency drive to control the speed of the motor and thus the compressor.

THE GENERAL CASE

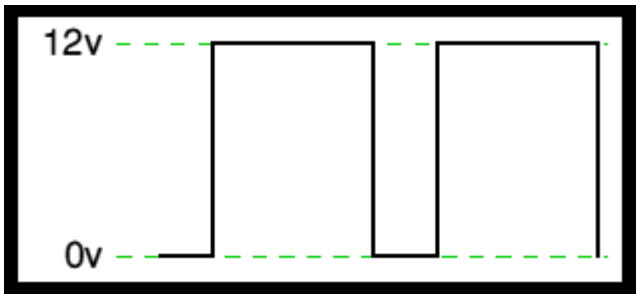
A transformer allows AC power to be converted to any desired voltage, but at the same frequency. Inverters, plus rectifiers for DC, can be designed to convert from any voltage, AC or DC, to any other voltage, also AC or DC, at any desired frequency. The output power can never exceed the input power, but efficiencies can be high, with a small proportion of the power dissipated as waste heat.

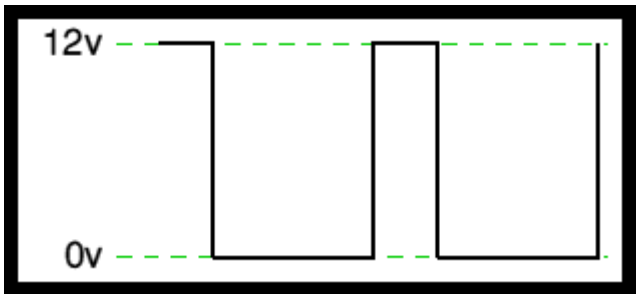
PULSE WIDTH MODULATION (PWM)

Pulse Width Modulation (PWM) is the most effective means to achieve constant voltage battery charging by switching the solar system controller's power devices. When in PWM regulation, the current from the solar array tapers according to the battery's condition and recharging needs Consider a waveform such as this: it is a voltage switching between 0v and 12v. It is fairly obvious that, since the voltage is at 12v for exactly as long as it is at 0v, then a 'suitable device' connected to its output will see the average voltage and think it is being fed 6v - exactly half of 12v. So by varying the width of the positive pulse - we can vary the 'average' voltage.



Similarly, if the switches keep the voltage at 12 for 3 times as long as at 0v, the average will be 3/4 of 12v - or 9v, as shown below and if the output pulse of 12v lasts only 25% of the overall time, then the average is

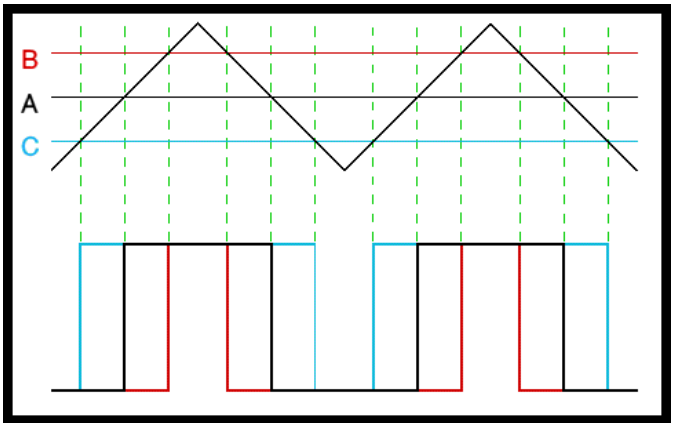




By varying - or 'modulating' - the time that the output is at 12v (i.e. the width of the positive pulse) we can alter the average voltage. So we are doing 'pulse width modulation'. I said earlier that the output had to feed 'a suitable device'. A radio would not work from this: the radio would see 12v then 0v, and would probably not work properly. However a device such as a motor will respond to the average, so PWM is a natural for motor control.

PULSE WIDTH MODULATOR

So, how do we generate a PWM waveform? It's actually very easy, there are circuits available in the TEC site. First you generate a triangle waveform as shown in the diagram below. You compare this with a d.c voltage, which you adjust to control the ratio of on to off time that you require. When the triangle is above the 'demand' voltage, the output goes high. When the triangle is below the demand voltage, the



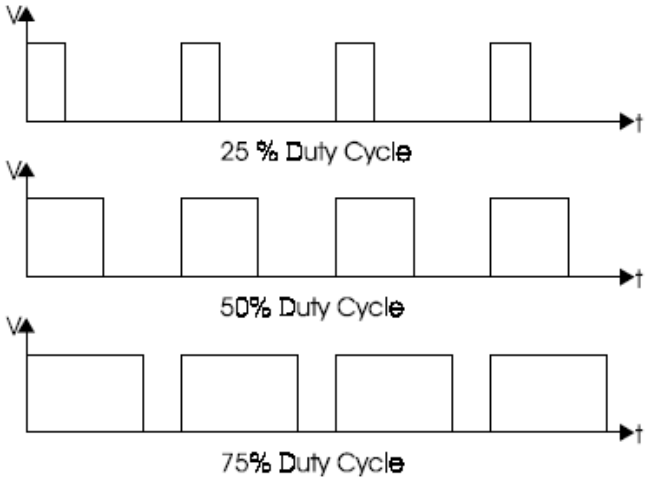
When the demand speed it in the middle (A) you get a 50:50 output, as in black. Half the time the output is high and half the time it is low. Fortunately, there is an IC (Integrated circuit) called a comparator: these come usually 4 sections in a single package. One can be used as the

oscillator to produce the triangular waveform and another to do the comparing, so a complete oscillator and modulator can be done with half an IC and maybe 7 other bits.

The triangle waveform, which has approximately equal rise and fall slopes, is one of the commonest used, but you can use a saw tooth (where the voltage falls quickly and rinses slowly). You could use other waveforms and the exact linearity (how good the rise and fall are) is not too important.

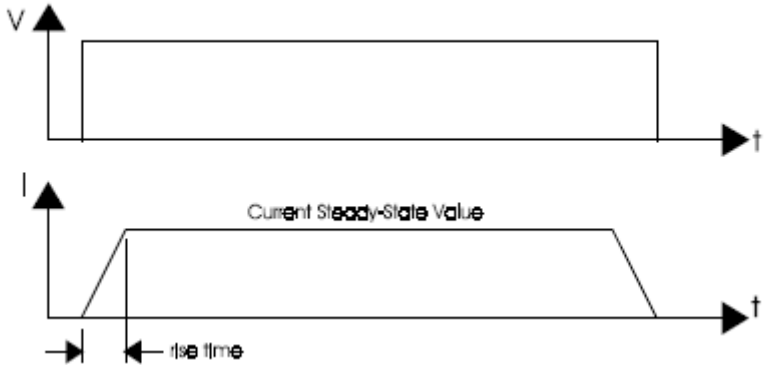
Traditional solenoid driver electronics rely on linear control, which is the application of a constant voltage across a resistance to produce an output current that is directly proportional to the voltage. Feedback can be used to achieve an output that matches exactly the control signal. However, this scheme dissipates a lot of power as heat, and it is therefore very inefficient.

A more efficient technique employs pulse width modulation (PWM) to produce the constant current through the coil. A PWM signal is not constant. Rather, the signal is on for part of its period, and off for the rest. The duty cycle, D, refers to the percentage of the period for which the signal is on. The duty cycle can be anywhere from 0, the signal is always off, to 1, where the signal is constantly on. A 50% D results in a perfect square wave. (Figure 1)



A solenoid is a length of wire wound in a coil. Because of this configuration, the solenoid has, in addition to its resistance, R, a certain **inductance**, L. When a voltage, V, is applied across an inductive element, the current, I, produced in that element does not jump up to its constant value, but gradually rises to its maximum over a period of time called the **rise time** (Figure 2).

Conversely, I does not disappear instantaneously, even if V is removed abruptly, but decreases back to zero in the same amount of time as the rise time.



Therefore, when a low frequency PWM voltage is applied across a solenoid, the current through it will be increasing and decreasing as V turns on and off. If D is shorter than the rise time, I will never achieve its maximum value, and will be discontinuous since it will go back to zero during V's off period (Figure 3).* In contrast, if D is larger than the rise time, I will never fall back to zero, so it will be continuous, and have a DC average value. The current will not be constant, however, but will have a ripple.

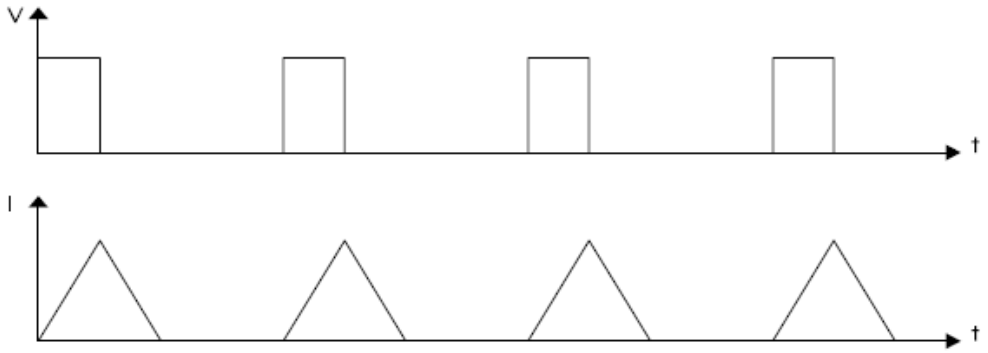
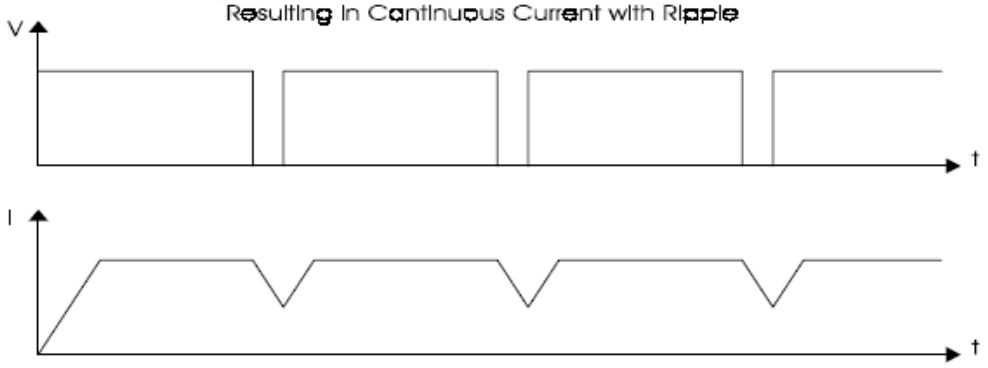
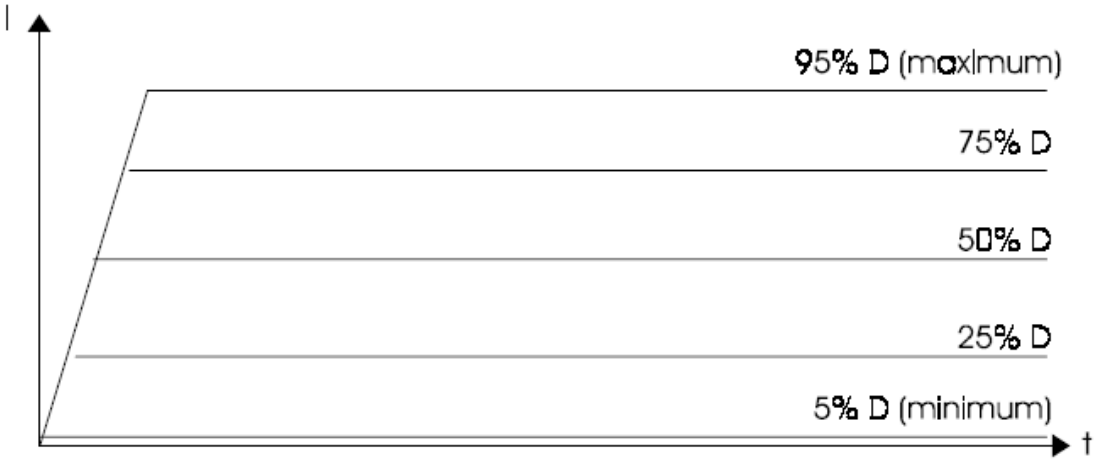


Figure 4 - Low Frequency PWM with D>rise time Resulting in Continuous Current with Ripple



At high frequencies, V turns on and off very quickly, regardless of D, such that the current does not have time to decrease very far before the voltage is turned back on. The resulting current through the solenoid is therefore considered to be constant. By adjusting the D, the amount of output current can be controlled. With a small D, the current will not have much time to rise before the high frequency PWM voltage takes effect and the current stays constant. With a large D, the current will be able to rise higher before it becomes constant.



WHY THE PWM FREQUENCY IS IMPORTANT:

The PWM is a large amplitude digital signal that swings from one voltage extreme to the other. And, this wide voltage swing takes a lot of filtering to smooth out. When the PWM frequency is close to the frequency of the waveform that you are generating, then any PWM filter will also smooth out your generated waveform and drastically reduce its amplitude. So, a good rule of thumb is to keep the PWM frequency much higher than the frequency of any waveform you generate.

Finally, filtering pulses is not just about the pulse frequency but about the duty cycle and how much energy is in the pulse. The same filter will do better on a low or high duty cycle pulse compared to a 50% duty cycle pulse. Because the wider pulse has more time to integrate to a stable filter voltage and the smaller pulse has less time to disturb it the inspiration was a request to control the speed of a large positive displacement fuel pump. The pump was sized to allow full power of a boosted engine in excess of 600 Hp.

At idle or highway cruise, this same engine needs far less fuel yet the pump still normally supplies the same amount of fuel. As a result the fuel gets recycled back to the fuel tank, unnecessarily heating the fuel. This PWM controller circuit is intended to run the pump at a low speed setting during low power and allow full pump speed when needed at high engine power levels.

MOTOR SPEED CONTROL (POWER CONTROL)

Typically when most of us think about controlling the speed of a DC motor we think of varying the voltage to the motor. This is normally done with a variable resistor and provides a limited useful range of operation. The operational range is limited for most applications primarily because torque drops off faster than the voltage drops.

Most DC motors cannot effectively operate with a very low voltage. This method also causes overheating of the coils and eventual failure of the motor if operated too slowly. Of course, DC motors have had speed controllers based on varying voltage for years, but the range of low speed operation had to stay above the failure zone described above.

Additionally, the controlling resistors are large and dissipate a large percentage of energy in the form of heat. With the advent of solid state electronics in the 1950's and 1960's and this technology becoming very affordable in the 1970's & 80's the use of pulse width modulation (PWM) became much more practical. The basic concept is to keep the voltage at the full value and simply vary the amount of time the voltage is applied to the motor windings. Most PWM circuits use large transistors to simply allow power On & Off, like a very fast switch.

This sends a steady frequency of pulses into the motor windings. When full power is needed one pulse ends just as the next pulse begins, 100% modulation. At lower power settings the pulses are of shorter duration. When the pulse is On as long as it is Off, the motor is operating at 50% modulation. Several advantages of PWM are efficiency, wider operational range and longer lived motors. All of these advantages result from keeping the voltage at full scale resulting in current being limited to a safe limit for the windings.

PWM allows a very linear response in motor torque even down to low PWM% without causing damage to the motor. Most motor manufacturers recommend PWM control rather than the older voltage control method. PWM controllers can be operated at a wide range of frequencies. In theory very high frequencies (greater than 20 kHz) will be less efficient than lower frequencies (as low as 100 Hz) because of switching losses.

The large transistors used for this On/Off activity have resistance when flowing current, a loss that exists at any frequency. These transistors also have a loss every time they "turn on" and

every time they “turn off”. So at very high frequencies, the “turn on/off” losses become much more significant. For our purposes the circuit as designed is running at 526 Hz. Somewhat of an arbitrary frequency, it works fine.

Depending on the motor used, there can be a hum from the motor at lower PWM%. If objectionable the frequency can be changed to a much higher frequency above our normal hearing level (>20,000Hz).

PWM CONTROLLER FEATURES:

This controller offers a basic “Hi Speed” and “Low Speed” setting and has the option to use a “Progressive” increase between Low and Hi speed. Low Speed is set with a trim pot inside the controller box. Normally when installing the controller, this speed will be set depending on the minimum speed/load needed for the motor. Normally the controller keeps the motor at this Lo Speed except when Progressive is used and when Hi Speed is commanded (see below). Low Speed can vary anywhere from 0% PWM to 100%.

Progressive control is commanded by a 0-5 volt input signal. This starts to increase PWM% from the low speed setting as the 0-5 volt signal climbs. This signal can be generated from a throttle position sensor, a Mass Air Flow sensor, a Manifold Absolute Pressure sensor or any other way the user wants to create a 0-5 volt signal. This function could be set to increase fuel pump power as turbo boost starts to climb (MAP sensor). Or, if controlling a water injection pump, Low Speed could be set at zero PWM% and as the TPS signal climbs it could increase PWM%, effectively increasing water flow to the engine as engine load increases.

This controller could even be used as a secondary injector driver (several injectors could be driven in a batch mode, hi impedance only), with Progressive control (0-100%) you could control their output for fuel or water with the 0-5 volt signal.

Progressive control adds enormous flexibility to the use of this controller. Hi Speed is that same as hard wiring the motor to a steady 12 volt DC source. The controller is providing 100% PWM, steady 12 volt DC power. Hi Speed is selected three different ways on this controller: 1) Hi Speed is automatically selected for about one second when power goes on. This gives the motor full torque at the start. If needed this time can be increased (the value of C1

would need to be increased). 2) High Speed can also be selected by applying 12 volts to the High Speed signal wire. This gives Hi Speed regardless of the Progressive signal.

When the Progressive signal gets to approximately 4.5 volts, the circuit achieves 100% PWM – Hi Speed.

HOW DOES THIS TECHNOLOGY HELP?

The benefits noted above are technology driven. The more important question is how the PWM technology Jumping from a 1970's technology into the new millennium offers:

• LONGER BATTERY LIFE:

– reducing the costs of the solar system

– reducing battery disposal problems

• MORE BATTERY RESERVE CAPACITY:

– increasing the reliability of the solar system

– reducing load disconnects

– Opportunity to reduce battery size to lower the system cost

• GREATER USER SATISFACTION:

– get more power when you need it for less money

MATLAB

Matlab is a high-performance language for technical computing. It integrates computation, visualization, and programming in an easy-to-use environment where problems and solutions are expressed in familiar mathematical notation. Typical uses include Math and computation Algorithm development Data acquisition Modeling, simulation, and prototyping Data analysis, exploration, and visualization Scientific and engineering graphics Application development, including graphical user interface building.

Matlab is an interactive system whose basic data element is an array that does not require dimensioning. This allows you to solve many technical computing problems, especially those with matrix and vector formulations, in a fraction of the time it would take to write a program in a scalar no interactive language such as C or Fortran.

The name matlab stands for matrix laboratory. Matlab was originally written to provide easy access to matrix software developed by the linpack and eispack projects. Today, matlab engines incorporate the lapack and blas libraries, embedding the state of the art in software for matrix computation.

Matlab has evolved over a period of years with input from many users. In university environments, it is the standard instructional tool for introductory and advanced courses in mathematics, engineering, and science. In industry, matlab is the tool of choice for high-productivity research, development, and analysis.

Matlab features a family of add-on application-specific solutions called toolboxes. Very important to most users of matlab, toolboxes allow you to learn and apply specialized technology. Toolboxes are comprehensive collections of matlab functions (M-files) that extend the matlab environment to solve particular classes of problems. Areas in which toolboxes are available include signal processing, control systems, neural networks, fuzzy logic, wavelets, simulation, and many others.

The matlab system consists of five main parts:

Development Environment**.** This is the set of tools and facilities that help you use matlab functions and files. Many of these tools are graphical user interfaces. It includes the matlab desktop and Command Window, a command history, an editor and debugger, and browsers for viewing help, the workspace, files, and the search path.

The matlab Mathematical Function Library. This is a vast collection of computational algorithms ranging from elementary functions, like sum, sine, cosine, and complex arithmetic, to

more sophisticated functions like matrix inverse, matrix eigenvalues, Bessel functions, and fast Fourier transforms.

The matlab Language**.** This is a high-level matrix/array language with control flow statements, functions, data structures, input/output, and object-oriented programming features. It allows both "programming in the small" to rapidly create quick and dirty throw-away programs, and "programming in the large" to create large and complex application programs.

Matlab has extensive facilities for displaying vectors and matrices as graphs, as well as annotating and printing these graphs. It includes high-level functions for two-dimensional and three-dimensional data visualization, image processing, animation, and presentation graphics. It also includes low-level functions that allow you to fully customize the appearance of graphics as well as to build complete graphical user interfaces on your matlab applications.

The matlab Application Program Interface (API). This is a library that allows you to write C and Fortran programs that interact with matlab. It includes facilities for calling routines from matlab (dynamic linking), calling matlab as a computational engine, and for reading and writing MAT-files.

SIMULINK:

Introduction:

Simulink is a software add-on to matlab which is a mathematical tool developed by The Math works,(http://www.mathworks.com) a company based in Natick. Matlab is powered by extensive numerical analysis capability. Simulink is a tool used to visually program a dynamic system (those governed by Differential equations) and look at results. Any logic circuit, or control system for a dynamic system can be built by using standard building blocks available in Simulink Libraries. Various toolboxes for different techniques, such as Fuzzy Logic, Neural Networks, dsp, Statistics etc. are available with Simulink, which enhance the processing power of the tool. The main advantage is the availability of templates / building blocks, which avoid the necessity of typing code for small mathematical processes.

Concept of signal and logic flow:

In Simulink, data/information from various blocks are sent to another block by lines connecting the relevant blocks. Signals can be generated and fed into blocks dynamic / static).Data can be fed into functions. Data can then be dumped into sinks, which could be scopes, displays or could be saved to a file. Data can be connected from one block to another, can be branched, multiplexed etc. In simulation, data is processed and transferred only at Discrete times, since all computers are discrete systems. Thus, a simulation time step (otherwise called an integration time step) is essential, and the selection of that step is determined by the fastest dynamics in the simulated system.

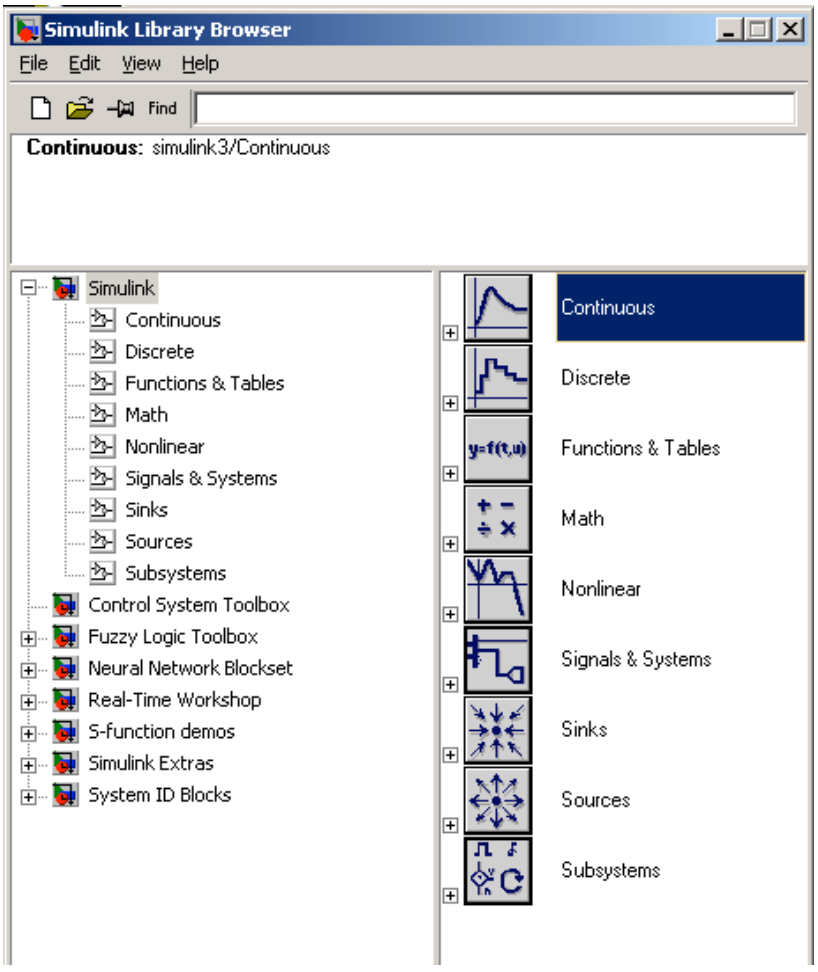


Fig 4.1 Simulink library browser

Connecting blocks:

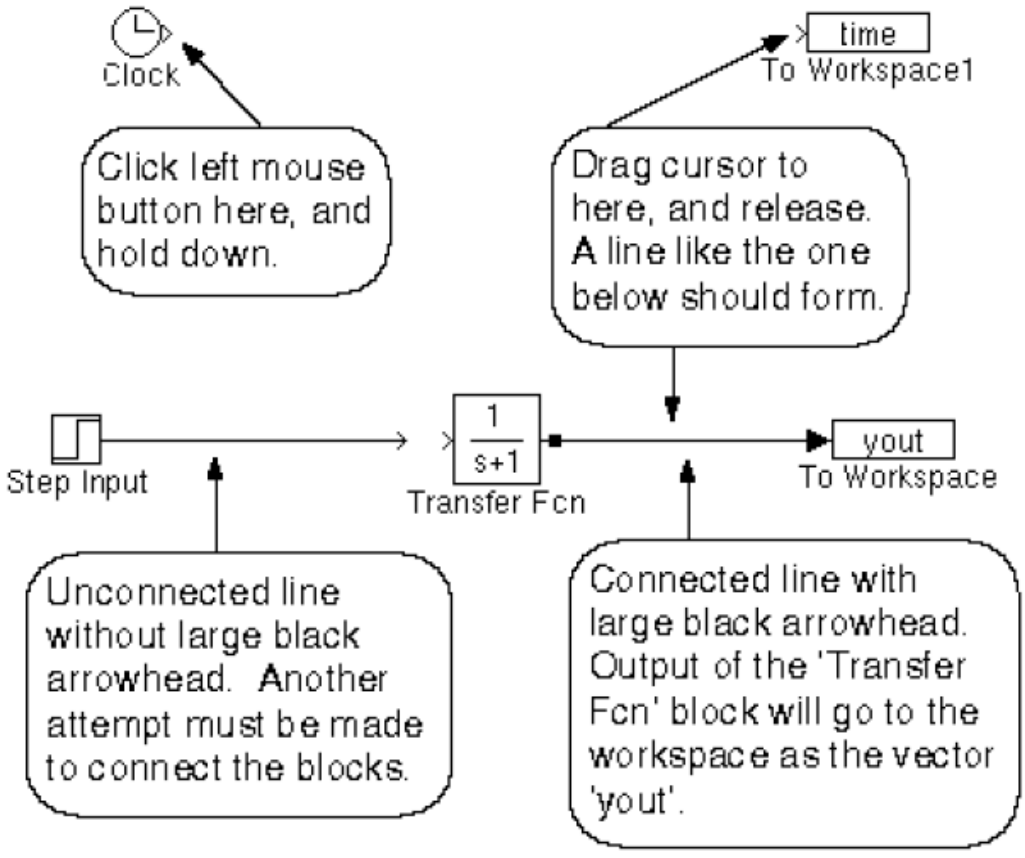


fig 4.2 Connectung blocks

To connect blocks, left-click and drag the mouse from the output of one block to the input of another block.

Sources and sinks:

The sources library contains the sources of data/signals that one would use in a dynamic system simulation. One may want to use a constant input, a sinusoidal wave, a step, a repeating sequence such as a pulse train, a ramp etc. One may want to test disturbance effects, and can use the random signal generator to simulate noise. The clock may be used to create a time index for plotting purposes. The ground could be used to connect to any unused port, to avoid warning messages indicating unconnected ports.

The sinks are blocks where signals are terminated or ultimately used. In most cases, we would want to store the resulting data in a file, or a matrix of variables. The data could be displayed or even stored to a file. the stop block could be used to stop the simulation if the input to that block (the signal being sunk) is non-zero. Figure 3 shows the available blocks in the sources and sinks libraries. Unused signals must be terminated, to prevent warnings about unconnected signals.

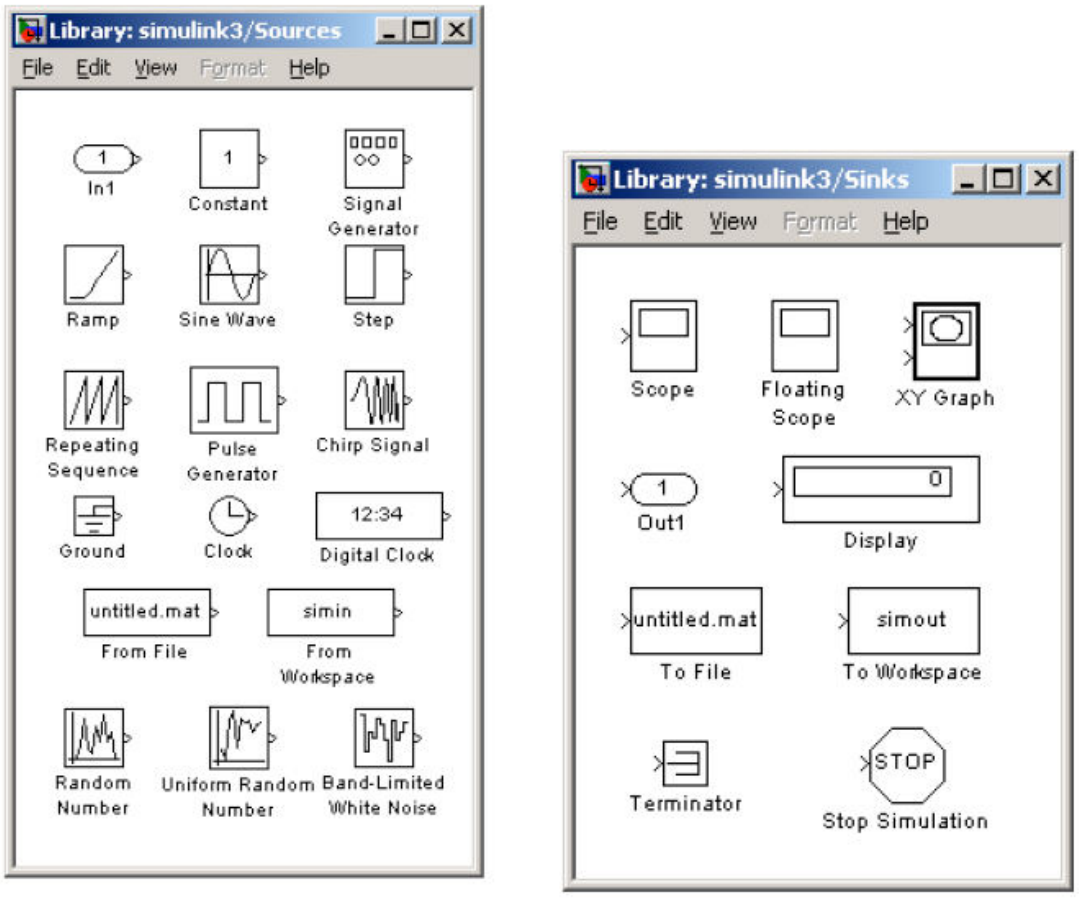


fig 4.3 Sources and sinks

Continuous and discrete systems:

All dynamic systems can be analyzed as continuous or discrete time systems. Simulink allows you to represent these systems using transfer functions, integration blocks, delay blocks etc.

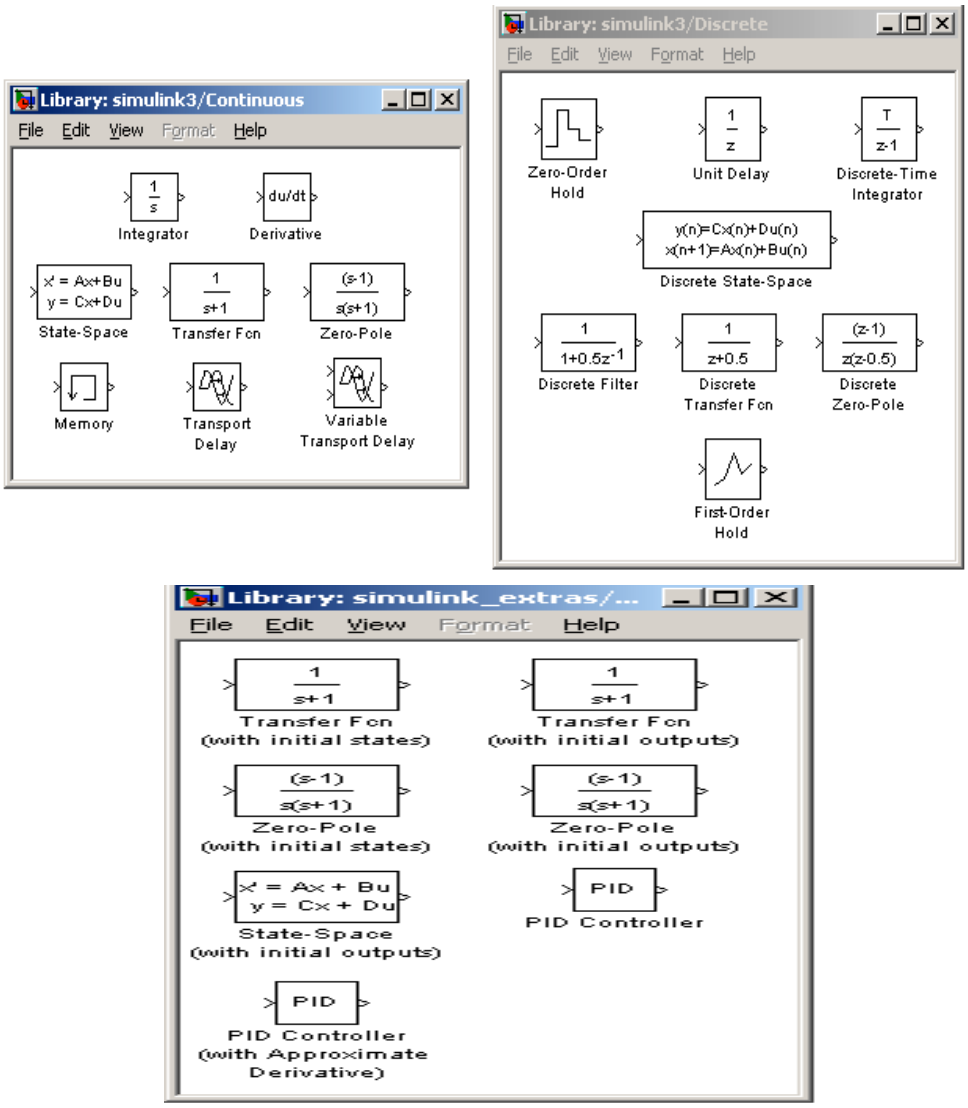


fig 4.4 continous and descrete systems

Non-linear operators:

A main advantage of using tools such as Simulink is the ability to simulate non-linear systems and arrive at results without having to solve analytically. It is very difficult to arrive at an analytical solution for a system having non-linearities such as saturation, signup function,

limited slew rates etc. In Simulation, since systems are analyzed using iterations, non-linearities are not a hindrance. One such could be a saturation block, to indicate a physical limitation on a parameter, such as a voltage signal to a motor etc. Manual switches are useful when trying simulations with different cases. Switches are the logical equivalent of if-then statements in programming.

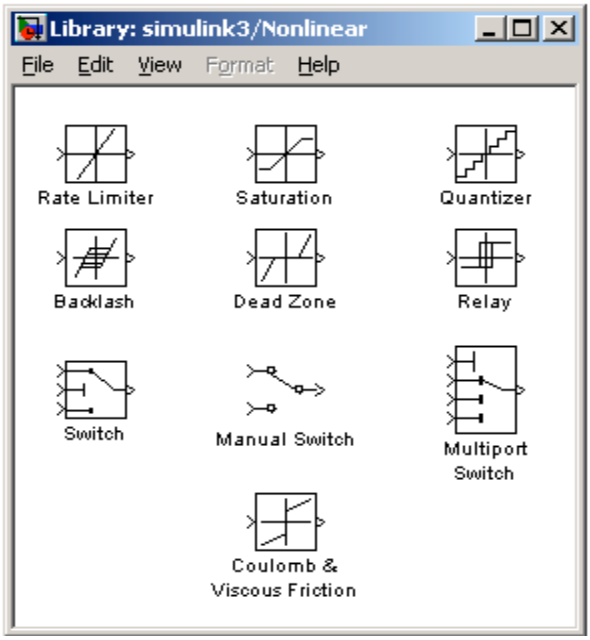


fig 4.5 simulink blocks

Mathematical operations:

Mathematical operators such as products, sum, logical operations such as and, or, etc. .can be programmed along with the signal flow. Matrix multiplication becomes easy with the matrix gain block. Trigonometric functions such as sin or tan inverse (at an) are also available. Relational operators such as ‘equal to’, ‘greater than’ etc. can also be used in logic circuits

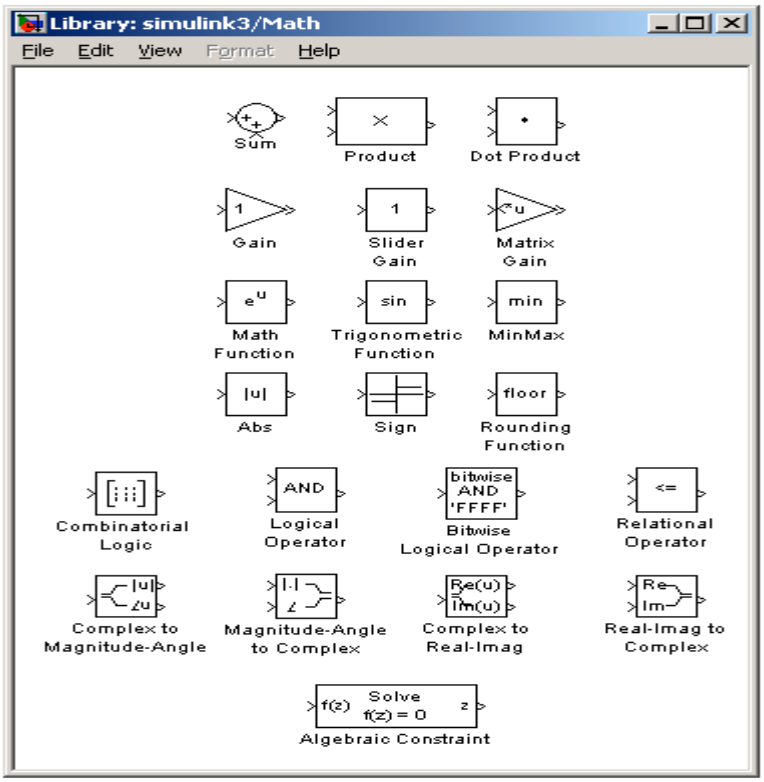


fig 4.6 Simulink math blocks

SIGNALS & DATA TRANSFER:

In complicated block diagrams, there may arise the need to transfer data from one portion to another portion of the block. They may be in different subsystems. That signal could be dumped into a goto block, which is used to send signals from one subsystem to another.

Multiplexing helps us remove clutter due to excessive connectors, and makes matrix(column/row) visualization easier.

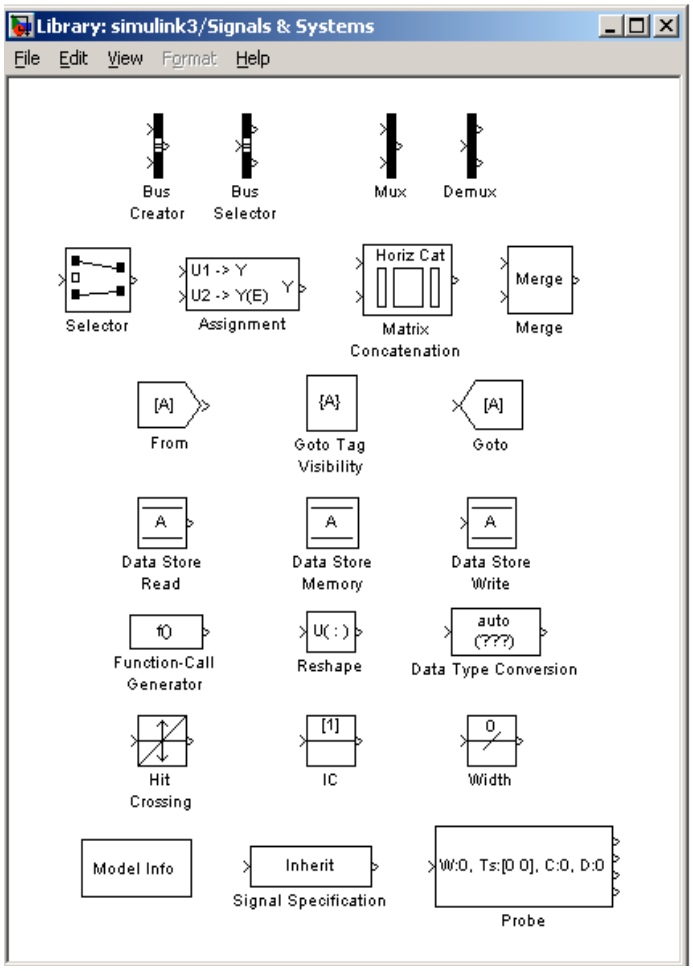


fig 4.7 signals and systems

Making subsystems

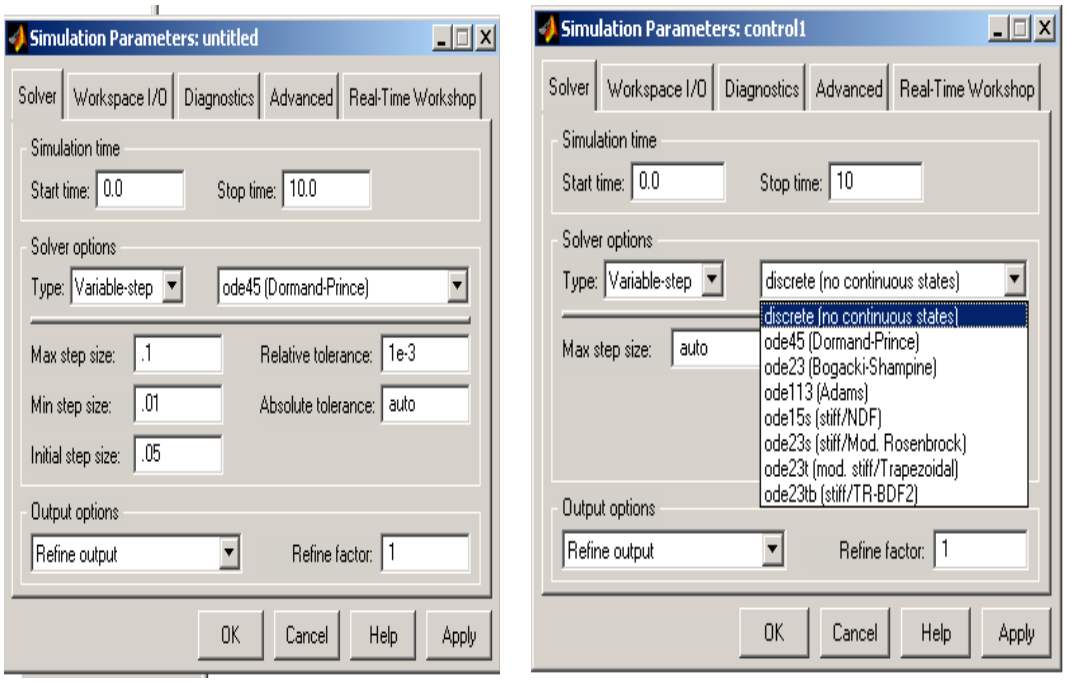
Drag a subsystem from the Simulink Library Browser and place it in the parent block where you would like to hide the code. The type of subsystem depends on the purpose of the block. In general one will use the standard subsystem but other subsystems can be chosen. For instance, the subsystem can be a triggered block, which is enabled only when a trigger signal is received.

Open (double click) the subsystem and create input / output PORTS, which transfer signals into and out of the subsystem. The input and output ports are created by dragging them

from the Sources and Sinks directories respectively. When ports are created in the subsystem, they automatically create ports on the external (parent) block. This allows for connecting the appropriate signals from the parent block to the subsystem.

Setting simulation parameters:

Running a simulation in the computer always requires a numerical technique to solve a differential equation. The system can be simulated as a continuous system or a discrete system based on the blocks inside. The simulation start and stop time can be specified. In case of variable step size, the smallest and largest step size can be specified. A Fixed step size is recommended and it allows for indexing time to a precise number of points, thus controlling the size of the data vector. Simulation step size must be decided based on the dynamics of the system. A thermal process may warrant a step size of a few seconds, but a DC motor in the system may be quite fast and may require a step size of a few milliseconds.



MODELING OF CASE STUDY

MULTILEVEL INVERTER

Basic concept of Multilevel Inverter:

Multilevel inverters are significantly different from the ordinary inverter where only two levels are generated. The semiconductor devices are not connected in series to for one single high-voltage switch. In which each group of devices contribute to a step in the output voltage waveform. The steps are increased to obtain an almost sinusoidal waveform. The number of switches involved is increased for every level increment. Figure 2.1 shows the block diagram of the general multilevel inverter.

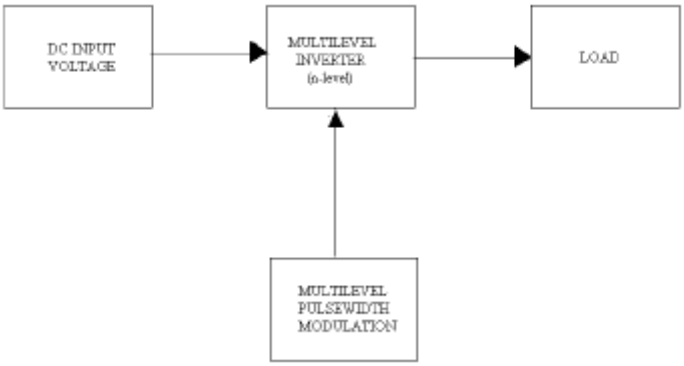


Figure 2.1 Multilevel Inverter System

Generally, the output waveform of the multilevel inverter is generated from different voltage sources obtained from the capacitor voltage sources. In the past two decades, several multilevel voltage source converters have been introduced. In that some of the topologies are popular and some are not popular. Consider a three phase inverter system as shown in the figure 2.2 with DC voltage Vdc. Series connected capacitors constitute the energy tank for the inverter, providing some nodes to which the multilevel inverter can be connected. Each capacitor has the same voltage Em, which is given by

$$Em = Vdc /(m-1)$$

Where m denotes the number of the level is referred to as the number of nodes to which the inverter can be accessible. An m level inverter needs (m-1) capacitors. Output phase voltages can be defined as voltage across output terminals of the inverter and the ground point denoted by 0 as shown in figure 2.2

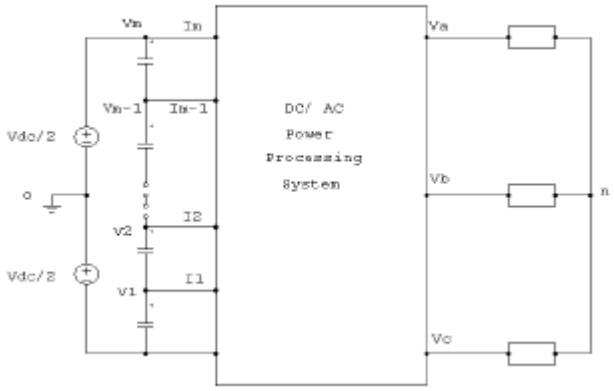


Figure 2.2 Three Phase Multilevel Power Processing System

Types of Multilevel Inverter

The general purpose of the multilevel inverter is to synthesize a nearly sinusoidal voltage from several levels of dc voltages, typically obtained from capacitor voltage sources. As the number of level increases, the synthesized output waveform has more steps, which produce a staircase wave that approaches a desired waveform. Also as more steps added to the waveform, the harmonic distortion of the output waveform decreases, approaching zero as the level increases. As the number of level increases, the voltage that can be summing multiple voltage levels also increases. Three converter topologies have been considered to have commercial potential. They are

A) Diode-clamped multilevel inverter
B) Flying-capacitor multilevel inverter
C) Cascaded inverter with separate DC sources

Among the three familiar topologies, cascaded multilevel inverter is an effective one. So by skipping the other topologies, the cascaded multilevel inverter is explained below. Cascaded multilevel inverter is having an unique and attractive topology such as simplicity in structure, usage of less number of components,etc.

Cascaded Multilevel Inverter with Separate DC Source:

The multilevel inverter using the cascaded converters with separate DC sources is discussed here. The cascaded multilevel inverter synthesizes a desired voltage from several independent sources of DC voltages which may be obtained from batteries, fuel cells or solar cells. This configuration has recently become very popular in high-power AC supplies and adjustable-speed drive applications. This converter can avoid extra clamping diodes or voltage-balancing capacitors. A single phase, m-level configuration of the cascaded multilevel inverter shown in the figure 2.3 Each single DC sources is associated with a single H-bridge converter. The AC terminal voltages of differentlevel converters are connected in series. Through different combinations of the four switches, S1-S4, each converter level can generate three different voltage outputs ,+Vdc, -Vdc and zero. The AC outputs of different full-bridge converters in the same phase are connected in series such that the synthesized voltage waveform is the sum of the individual converter outputs .Note that the number of output waveform is the sum of the individual converter outputs .Note that the number of output-phase voltage levels is defined in a different way from those of the two previous converters .In this topology, the number of output-phase voltage levels is defined by m=2N+1,where N is the number of DC sources .A five level cascaded converter ,For example ,consists of two DC sources and two full bridge converters. Minimum harmonic distortion can be obtained by controlling the conduction angles at different converter levels.

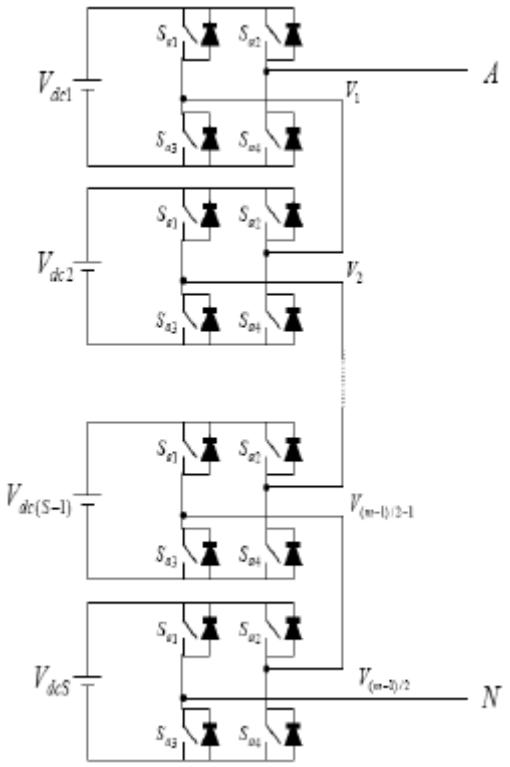


Figure 2.3 Single Phase Structure of Cascaded Multilevel Inverter

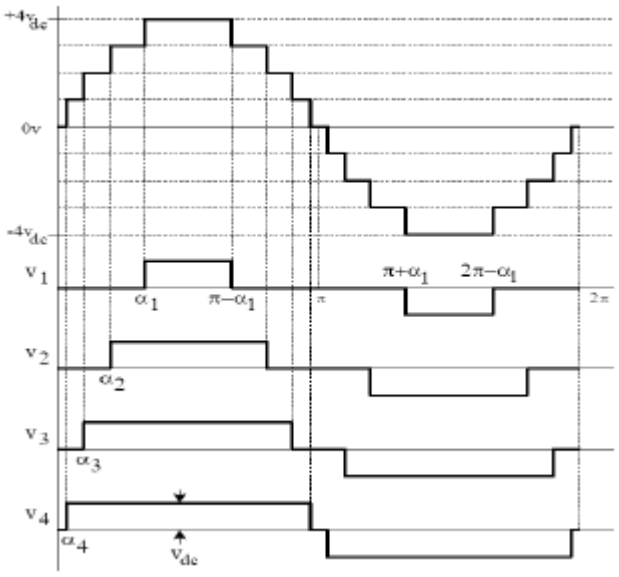


Figure 2.4 Waveform of a Nine-Level Output Phase Voltage and each H-Bridge Output Voltage.

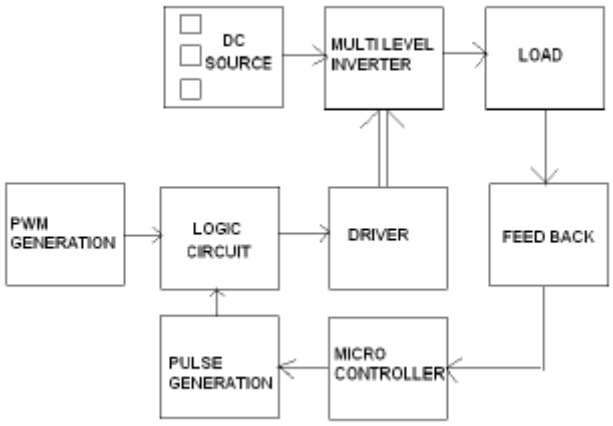


Figure 3.1 Block Diagram of the Proposed Multilevel Inverter

Advantages

1. The series structure allows a scalable, modularized circuit layout and packaging since each bridge has the same structure.

2. Switching redundancy for inner voltage level is possible because the phase voltage output sum of each bridges output.
3. Potential of electrical shock is reduced due to separate DC sources.
4. Requires less number of components when compared to other two types.

Disadvantages

1. Limited to certain applications where separate DC sources are available.

2. Usage of the power semiconductor switches increases exponentially whenever the level is to be increased

PROPOSED MULTILEVEL INVERTER

The proposed converter consists of less number of switches when compared to the other familiar topologies. The initial cost reduces because of the switch reduction. So, it looks attractive and an apt one for industrial applications. The block diagram of the proposed

multilevel inverter is shown in the The general circuit diagram of the proposed multilevel inverter is shown in the figure 3.2. The switches are arranged in the manner as shown in the figure. For the proposed topology, we just need to add only one switch for every increase in levels. So initial cost get reduced. Let us see operation in the next subdivision in detail for the seven-level inverter.

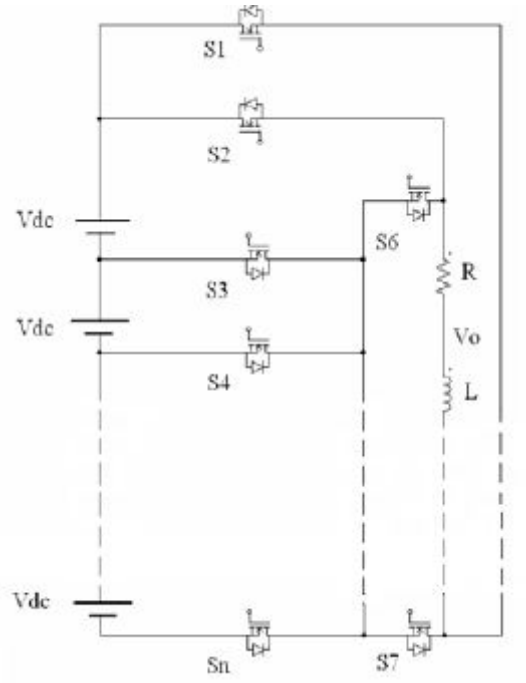


Figure 3.2 General Circuit Diagram of the Proposed Multilevel Inverter Topology

Proposed Multilevel Inverter For Seven Levels

The proposed multilevel inverter for seven levels is shown figure 3.3.The inverter consists of seven MOSFET switches and three separate DC sources with a load. By switching the MOSFETS at the appropriate firing angles, we can obtain the seven level output voltage. MOSFET is preferred because of its fast switching nature.

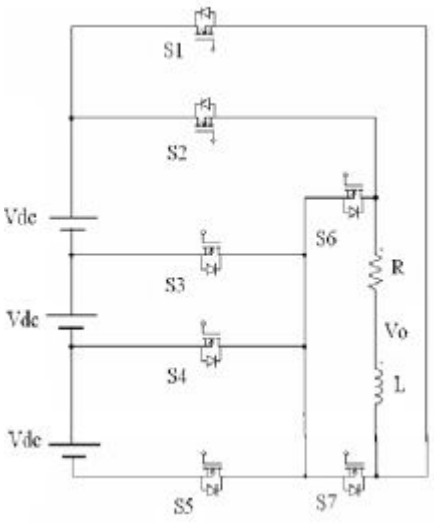


Figure 3.3 Circuit Diagram of the Seven Level Proposed Multilevel Inverter

Table 3.1 Switching Conditions

SINO	Conducting Switches	Amplitude Of the Output Voltage
1	S_2, S_7, S_3	+Vdc
2	S_2, S_7, S_4	+2Vdc
3	S_2, S_7, S_5	+3Vdc
4	Nil	0
5	S_1, S_6, S_3	-Vdc
6	S_1, S_6, S_4	-2Vdc
7	S_1, S_6, S_5	-3Vdc

The figure 3.4 shows the expected waveform of the proposed converter. Consider the input supply as 100volts DC supply. Three various supplies are given individually. By switching the MOSFETs, according the table 3.1 given above ,the various levels of output is obtained.

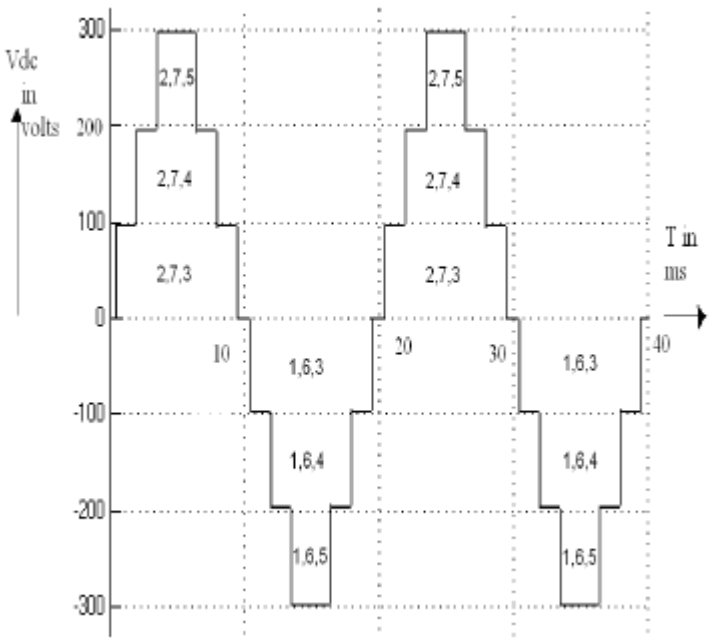


Figure 3.4 Output Waveform of the Proposed Multilevel Inverter

Advantages

1. Because of the reduction in the number of switches the initial cost reduces.
2. Controlling becomes easier.
3. Losses becomes less due to the elimination of the harmonics.
4. Apt structure for industrial applications.
5. Overall weight reduces because of the usage of less number of components.

Comparison between the Proposed Multilevel Inverter and the Cascaded Multilevel Inverter

The table 3.2 shows the comparison between the proposed inverter with the cascaded multilevel inverter. The proposed converter exhibits a significant outcome such as reduction in the number of switches and an easy control is possible.

Parameters	Cascaded				Proposed			
Levels	3	4	5	6	3	4	5	6
Switches required	12	16	20	24	7	8	9	10

SIMULATION RESULTS

Simulation results of the proposed converter for seven levels using MATLAB/simulink. The PWM technique is used for pulse generation. The MOSFET switches are used because of its fast switching capability. The input supply for each DC source is 100V. The load used is a R-L load. The output waveform is phase voltage and it comprises seven levels.The PWM technique is used to produce the control signal .

Simulation of the Proposed Multilevel Inverter for Seven Levels

The MATLAB simulation circuit for the proposed inverter which comprises only seven MOSFET switches for producing seven levels is shown in the figure 4.1. The MATLAB circuit used for generating gate pulse without using PWM technique is shown in the figure 4.2. The MATLAB circuit used for generating gate pulse using PWM technique is shown in the figure 4.3. The pulse generated by the circuit shown in the figure 4.4. The output waveform of the proposed inverter for seven levels without PWM technique is shown in the figure 4.5. The output waveform of the proposed inverter for seven levels with PWM technique is shown in the figure 4.6. The pulse is generated using comparison between constant DC voltage and power supply .The comparison is done using operational amplifiers. For the first pulse we give a DC voltage of lesser amplitude and moderate amplitude for the second pulse. Likewise we have to increase the amplitude to reduce the pulse width. The PWM technique is used to obtain a good harmonic spectrum. The gating pulse is generated from the above mentioned process and given separately to the respective MOSFETs. The supply is given through three separate DC sources. The R-L load is used for the simulation purpose. The simulation results show that the circuit is operating properly. The output waveform has three levels in the positive side and three levels in the

negative side and a zero level. Totally there are seven levels. Thus the proposed multilevel inverter for seven levels is successfully simulated. And the results are shown below in sequential manner.

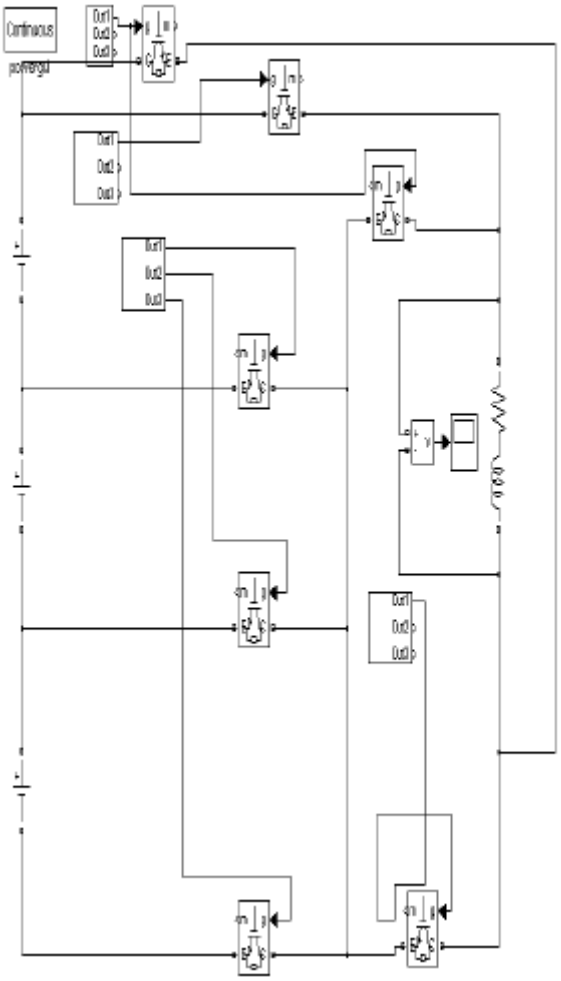


Figure 4.1 Proposed Multilevel Inverter for Seven Levels

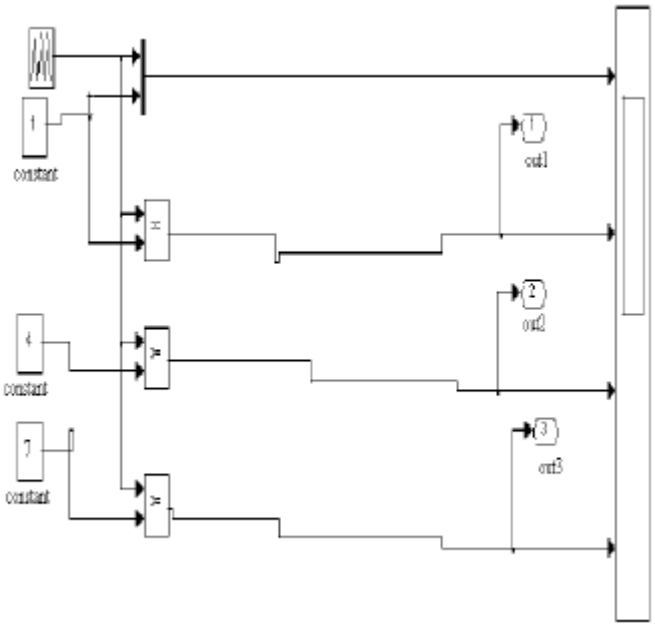


Figure 4.2 Gate Pulse Generation Circuit Without PWM Technique

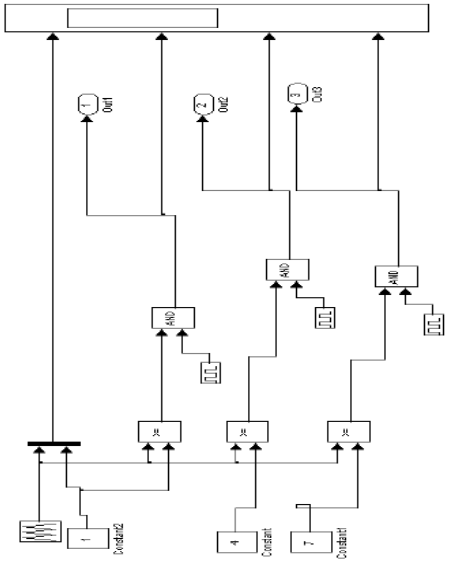


Figure 4.3 Gate Pulse Generation Circuit With PWM Technique

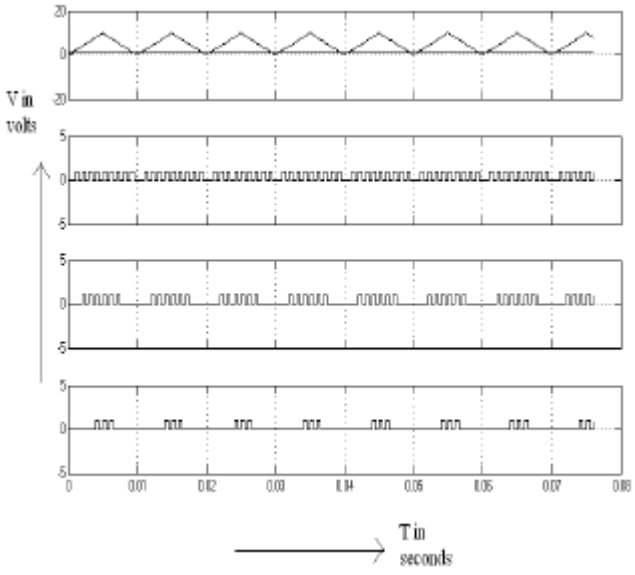


Figure 4.4 Pulses Generated Using PWM Technique

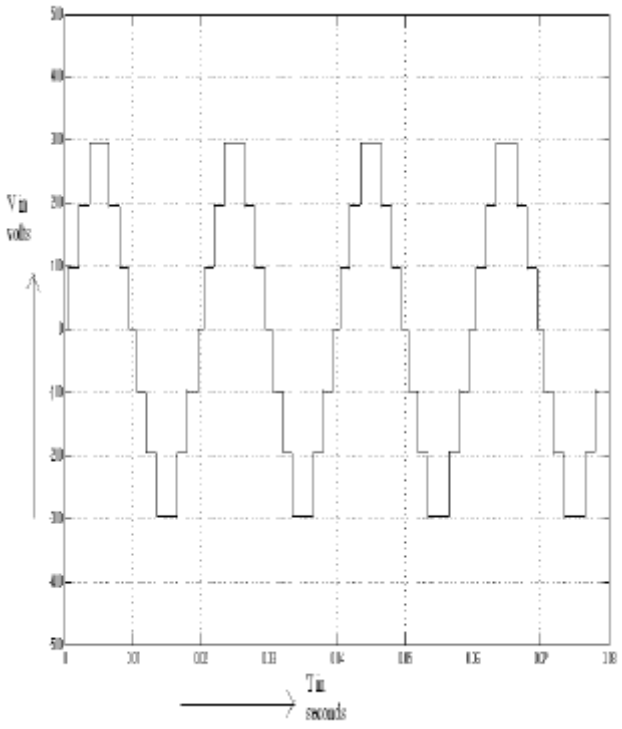


Figure 4.5 Output Voltage Waveform With out Using PWM Technique

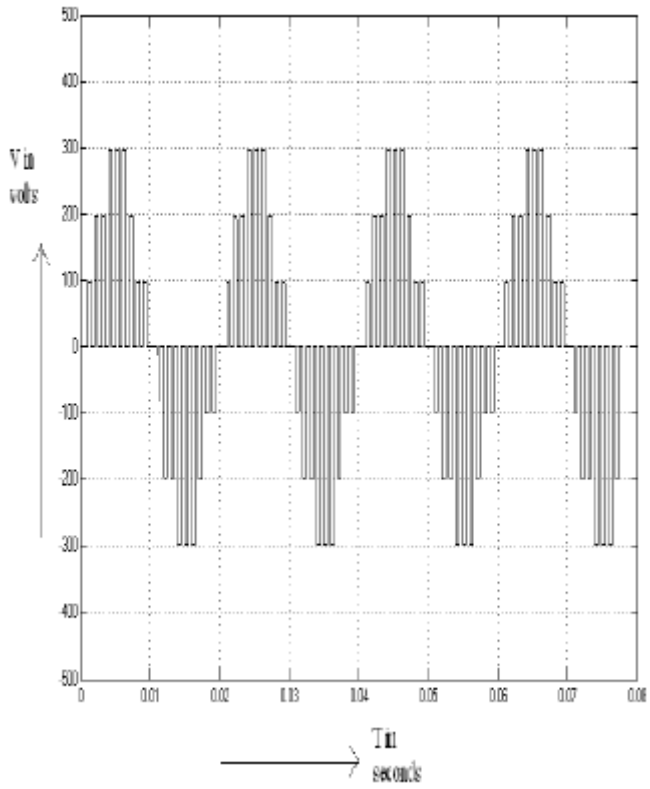


Figure 4.6 Output Voltage Waveform Using PWM Technique

CONCLUSION

The simulation of the seven-level multilevel inverter is successfully done using pulse width modulation technique. From the simulation, it is noted that the new multilevel inverter topology works well and shows hope to reduce the initial cost and complexity. When we increase the levels, the number of switches used is very less compared to the other topology.

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