Kathmandu University

Department of Computer Science and Engineering

Dhulikhel, Kavre

Lab Work-2

Half Adder, Full Adder & Multiplexer

[COMP 306]

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Submitted to:

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1. **Design a half added and realize it. Design and realize a full address using half adder you have designed above. Simulate 4:1 MUX**

Objective:

To Design Half Adder Full Adder and 4:1 Multiplexer

Components Required:

- Probe
- Wire
- Gates (AND, XOR, OR, NOT)
- Digital Constant
- LED Light
- Resistor
- 4:1 Multiplexer

Circuit Diagram

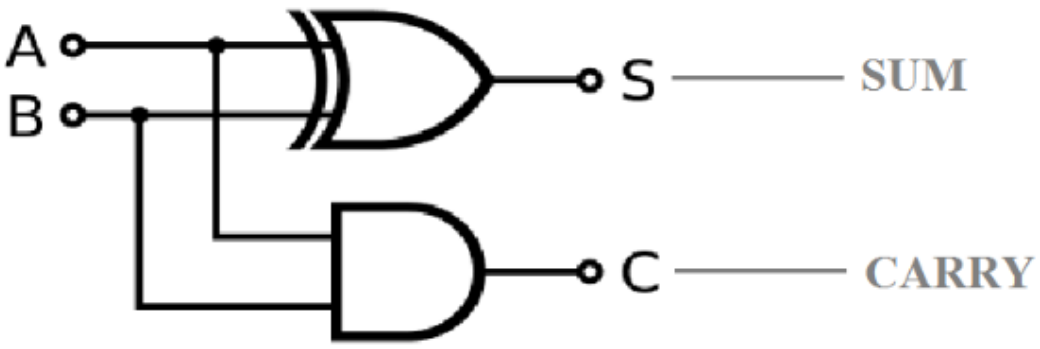


Fig 1: Half-Adder Circuit

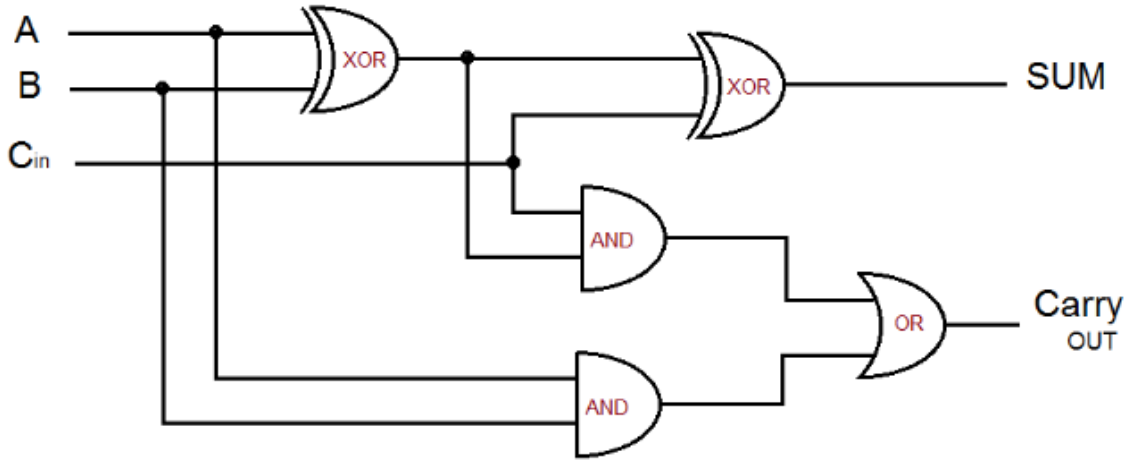


Fig 2: Full-Adder Circuit

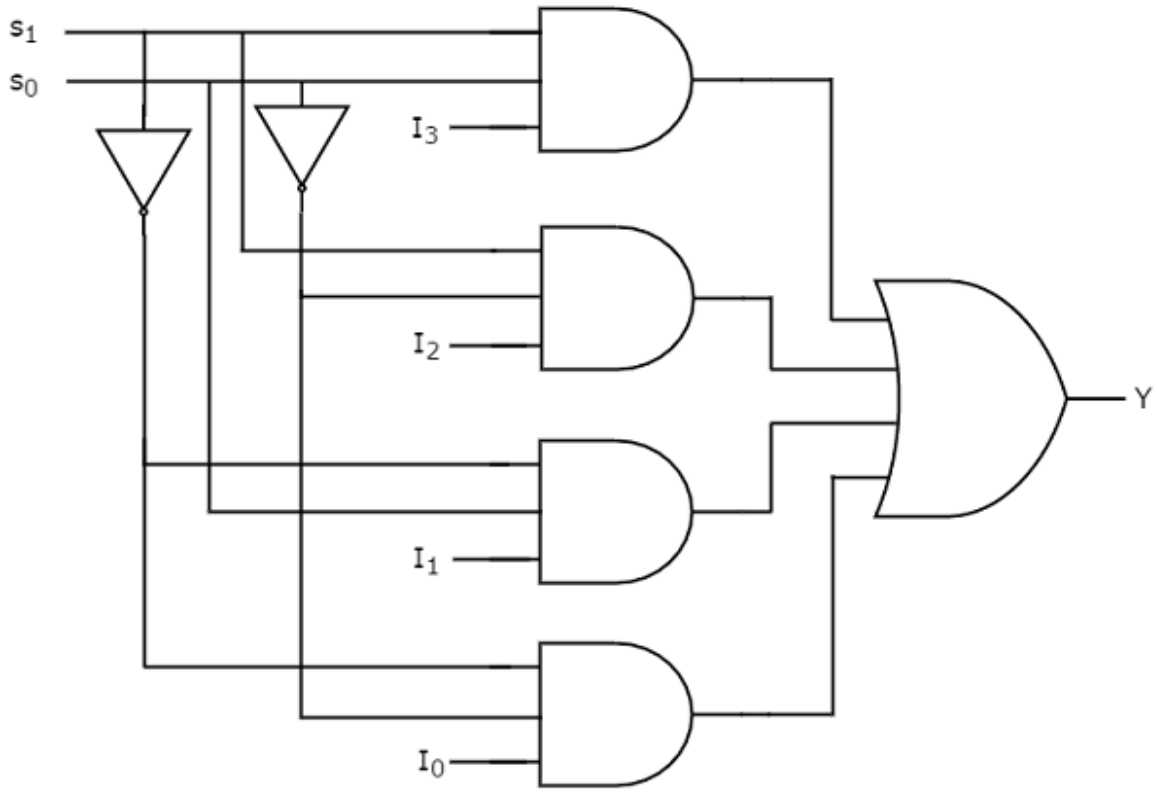


Fig 3 4:1 Multiplexer Circuit

Truth Table:

The truth table obtained for the Half Adder, Full Adder and MUX after varying their input parameters during simulation are shown in the table below:

Half Adder

A	B	C Out	Sum
0	0	0	0
1	0	0	1
0	1	0	1
1	1	1	0

Fig 4: Truth Table Half-Adder

Full Adder

A	B	C	C Out	Sum
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

Fig 5: Truth Table Full-Adder

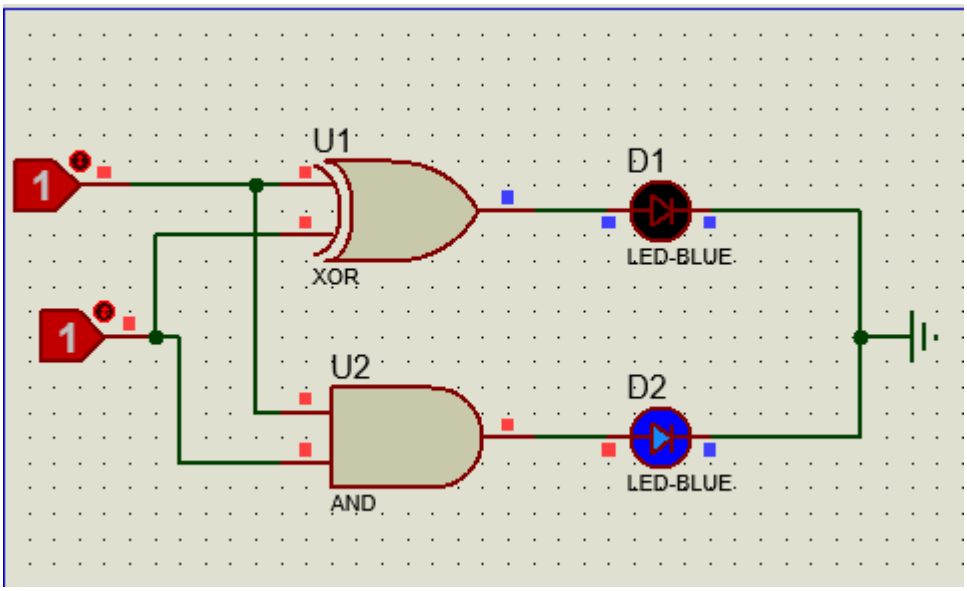
S0	S1	Output
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Fig 6: Truth Table 4:1 MUX

Conclusion:

Both Half Adder, Full Adder and 4:1 MUX were successfully simulated using Proteus Simulation and the truth tables were determined by checking multiple combinations of inputs and their effects on the probe.

Screenshots:



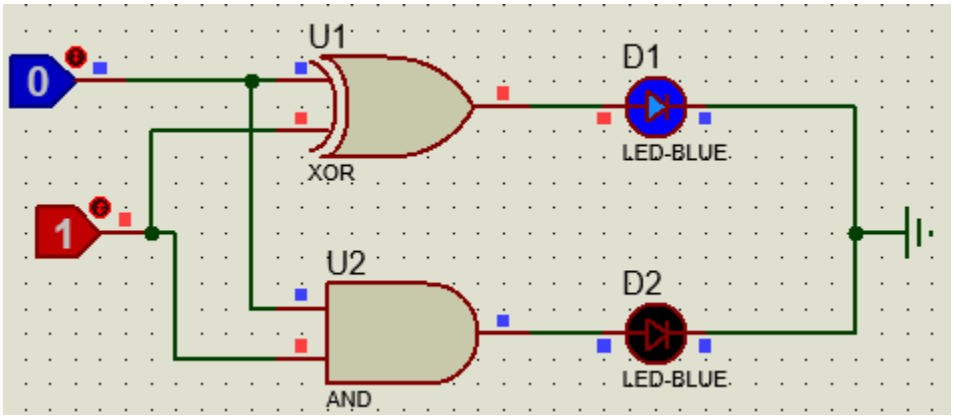
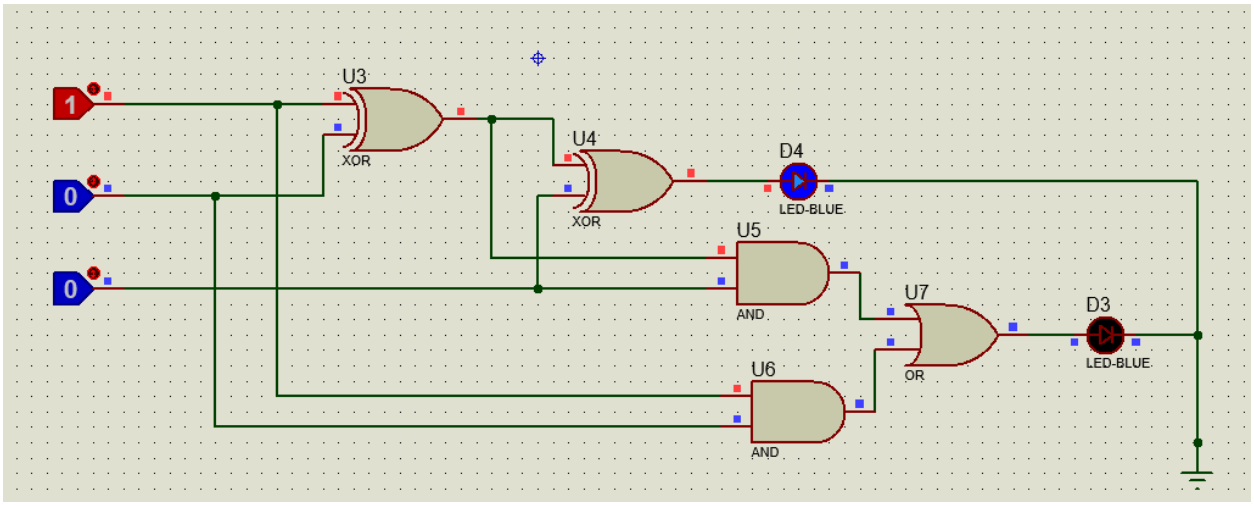


Fig 7: half-adder circuit



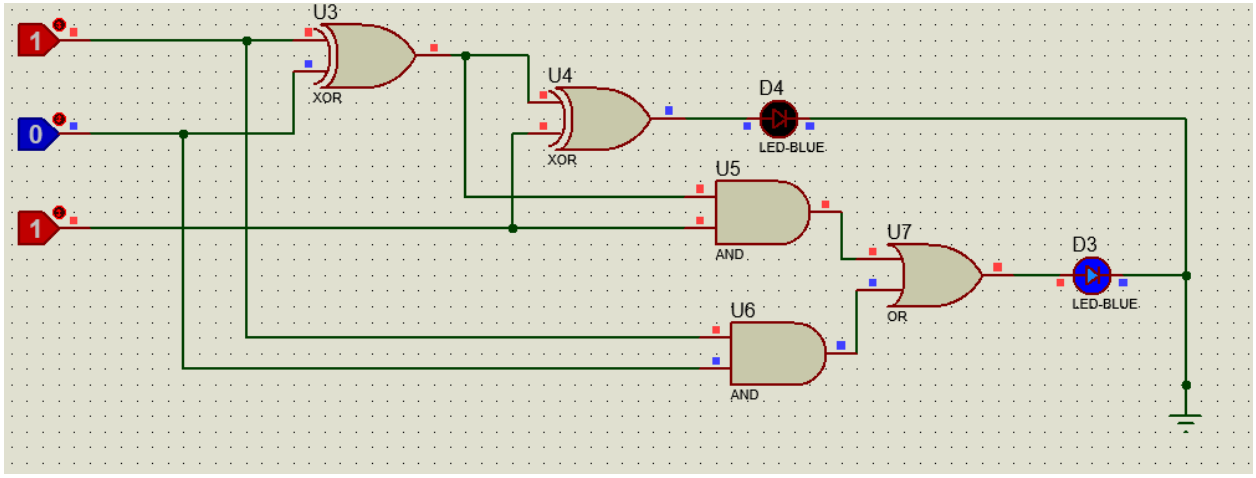


Fig 8: Full-adder Circuit

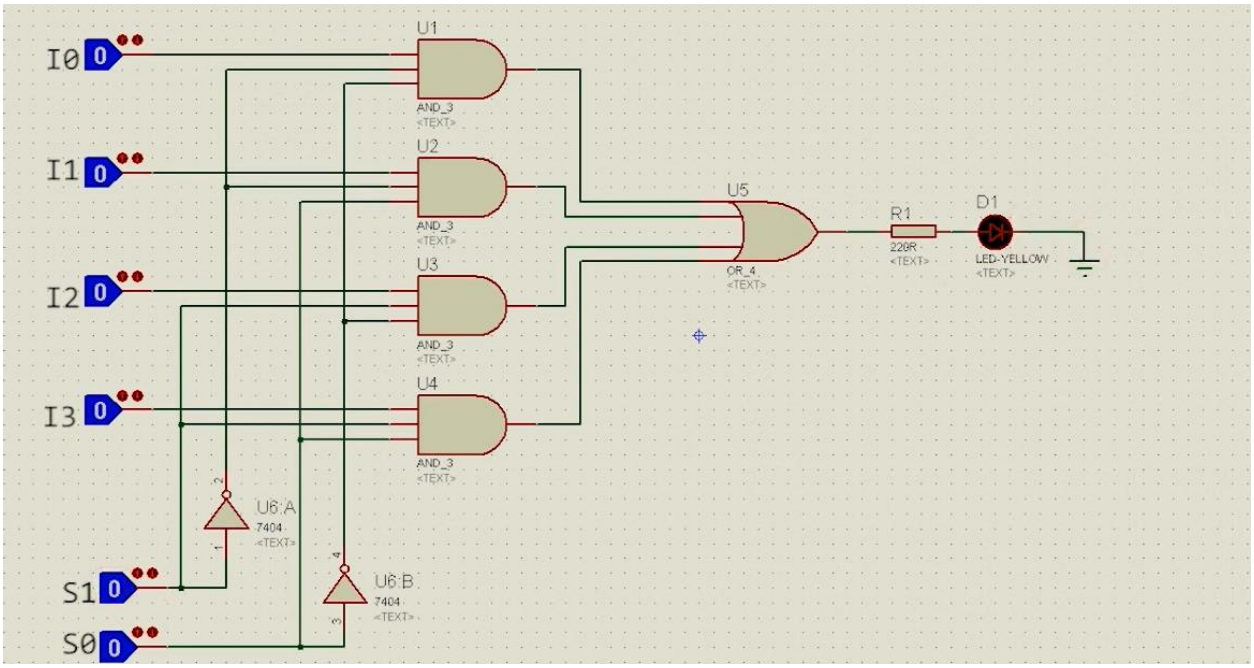


Fig 9: 4:1 Multiplexer