Test Environment

CSI-2 Transmitter AHB IP

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Revision History

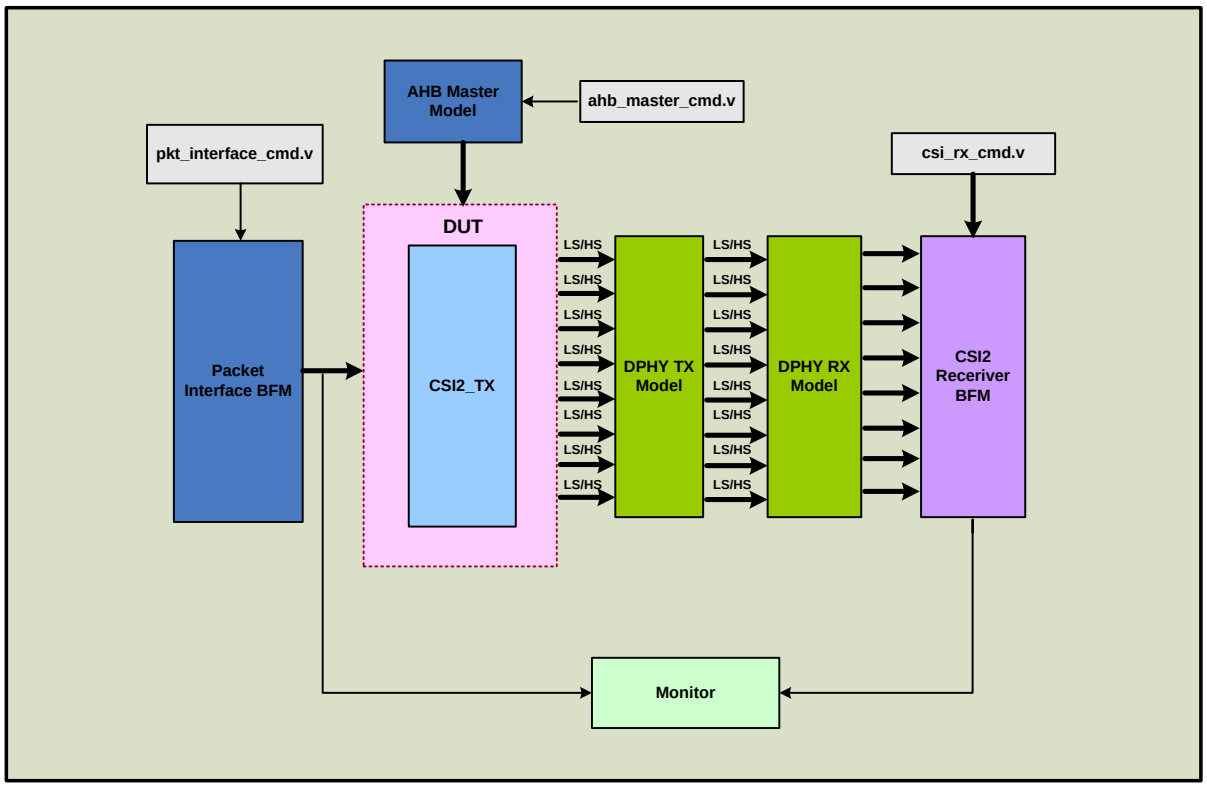
Revision	Date	Author	Summary Of Changes
1.0	24.04.2014	Dinesh Kumar	Original Document
1.1	16.05.2014	Pramod Kumar	Test tree is updated due to addition of new testcases
1.2	23.05.2014	Pramod Kumar	1. Test tree is updated due to addition of new testcases 2. Description for csi decoder bfm has been added

1 CSI-2 Transmitter Test Architecture

1.1 Test Environment

The Figure 1 shows the block diagram of CSI-2 Transmitter Test Environment architecture.

Figure 1 : Test Environment



1.1.1 AHB Master Model

Functionality of the AHB Master model is described below:

- AHB Master Model interacts with the CSI core and Tx BFM.
- AHB Master model handles the interrupt service routines for the generated interrupts from the CSI receiver
- AHB Master model configuration can be done in to modes:

A. Default Mode (Configures the Operational registers with default values specified in the user guide)
B. User Config Mode (Configures the Operational registers values as per the values specified in the ahb_master_cmd.v)

- The process is started by the master asserting a request (hbusreq) signal to the arbiter. Then arbiter indicates when the master will be granted to use the bus.
- A granted bus master starts an AHB transfer by driving the address and control signals.
- These signals provide information on the address, direction and width of the transfer, as well as an indication if the transfer forms part of a burst (single transfer).
- AHB Master Model supports burst transfer – single transfer
- AHB Master Model supports one master and one slave
- AHB Master Model data transfer size 8 / 16 / 32 bits

1.1.2 Packet Interface BFM

Functionality of the Packet Interface BFM model is described below:

- This module is used for sending the payload data based on color formats defined by the user.
- The pixel elements are transmitted to the CSI-2 transmitter as per the command file in the verification environment (pkt_interface_cmd.v)
- Interacts with CSI-2TX transmitter block and transmits the pixel level information, following standard CSI-2 specification
- Transmits short and long packets including generic data type
- Data byte count can be randomized.
- Interacts with CSI-2 monitor and transmits pixel level data.

1.1.3 D-PHY Transceiver Model

Functionality of the D-PHY transceiver model is described below:

- The D-PHY Transmitter and Receiver model emulates the functionality of a D-PHY transceiver.
- Derives differential signaling on high speed lanes from high speed clock or high speed data signal.
- Splits up the low power differential signals into low power transmitter differential signals and low power receiver differential signals.
- Supports calibration process which is enabled by transmitter bfm.
- Supports continuous clock mode and non continuous clock mode D-PHY operation.
- Supports minimum and maximum D-PHY timing parameters value configuration.

1.1.4 CSI-2 Receiver BFM

Functionality of the CSI-2 Receiver BFM is described below:

- This model reads commands from a command file, namely csi_rx_cmd.v
- CSI2-Receiver BFM Interacts with the D-PHY Rx.
- It receives the byte data from the D-PHY Rx & stores it depending upon the valid signal.
- It validates the packet header data; it flags error if it finds any unsupported/Reserved data Id.
- It does ECC checking for the Short & Long packet header & asserts error for any mismatch.
- It flags error if the word count field doesn't obey the number of bytes to be transmitted for the corresponding Data Id (i.e., Less than min bytes & Not in multiples).
- It computes the CRC for the received bytes & asserts error for any mismatch with the received CRC value.
- It performs byte to pixel packing for Long packet whenever the minimum byte count is reached for the corresponding Data Type.
- Receiver BFM transmits the packet header (Short, Long) to the monitor along with the header enable for the header data comparison.
- Receiver BFM transmits the Pixel Data to the monitor along with the pixel enable for the pixel data comparison.

1.1.5 Monitor

Functionality of the Monitor model is described below:

- This module monitors and store the packet information between Packet Interface BFM and DUT, it compares stored information (i.e., pixel and short packet) with the data transmitted from receiver BFM.
- Monitor detects Frame Start, Line start, Line End, Frame end & stores it in the short memory.
- Similarly monitor stores the Generic Short packet & the Header information of Long packet into the same short memory.
- The pixel data is detected & stored in the Long memory as per the reception.
- Monitor compares the Sync short packet's (FS, LS, LE, FE) , Generic short packet's & Long packet header data depending on an enable signal(csi_header_en) from CSI Receiver BFM along with data. It flags error for mismatch.
- Similarly monitor does the pixel comparison depending upon the enable signal (csi_long_pkt_data_en) from the CSI Receiver BFM along with pixel data. It flags error for mismatch.

- Monitor does the check for protocol violations, Frame Sync, Line Sync errors along with Illegal change of Virtual channel number during the packet transmission.

1.1.6 CSI Decoder Bfm

Functionality of the CSI Decoder Bfm model is described below:

- This module decompress the data sent by the DUT w.r.t the compression scheme
- It transmits the decompressed data to the CSI receiver bfm using a valid (dec_data_vld) & data (dec_data_op).
- CSI decoder bfm supports the following compression schemes with prediction-1 & prediction-2
    - 10-6-10
    - 10-7-10
    - 10-8-10
    - 12-6-12
    - 12-7-12
    - 12-8-12

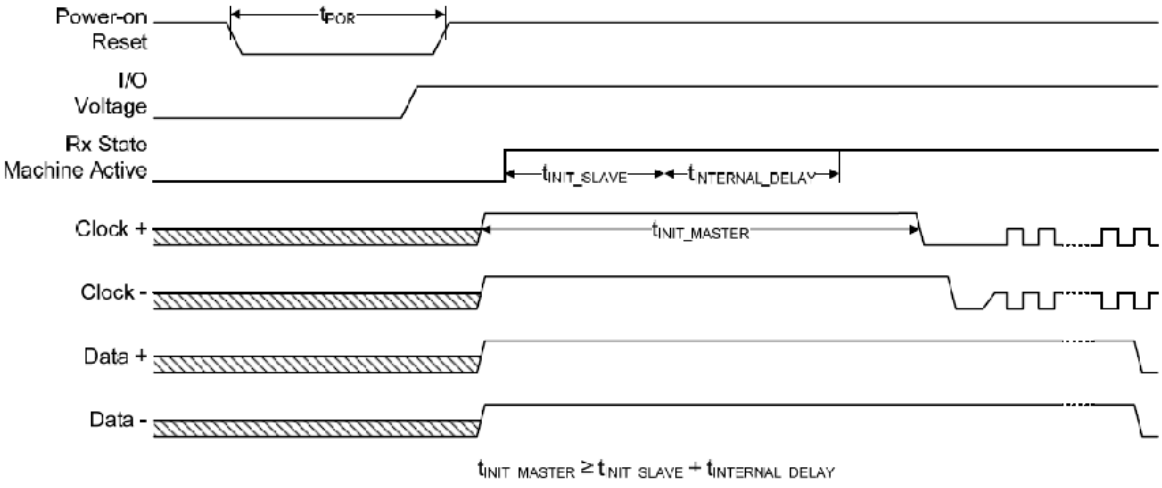
2 Test scenario Descriptions

2.1 D-PHY power up sequence

- After Power-up, the transmitter shall observe an initialization period, tinit, during which it shall drive a TX-Stop state (LP-11) on all lanes.
- The Receiver shall power up in the Stop state and monitor the lines to determine if the transmitter has asserted Stop state for at least the tinit period.
- The Receiver shall ignore all line states prior to detection of a tinit event. The Receiver shall be ready to accept us transactions immediately following the end of the tinit period.

In the following figure, power-on-reset mechanism is assumed for initialization. Here, tinit_slave represents the minimum initialization period specified in MIPI D-PHY Specification.ie.100 us. The Receiver may need some time to reach a functional state after power-up. This time is represented in the following figure as tinternal_delay.

The period of tinit_master is selected as greater than or equal to 1ms to suit for any high level protocol like CSI.

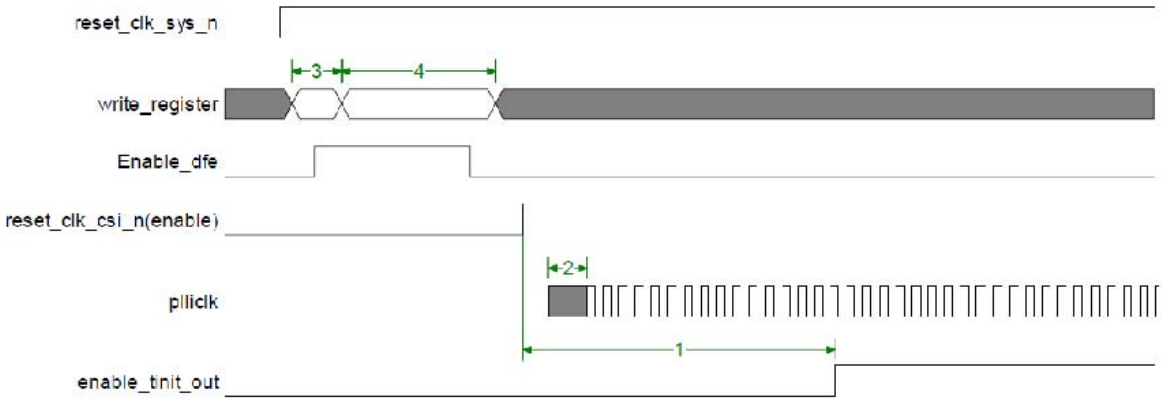


D-PHY power-up sequence

2.2 Power up Sequences for processor interface

- After power on reset, all the registers are programmed with their corresponding values.
- DFE related registers are written first. After writing DFE parameters related registers (trim_7 and trim_6[30]), DFE enable bit is written high(“1”) by writing trim_6[31].
- AFE related register write operation is completed. Then DFE enable bit is written as low.(“0”)
- After completing register configurations, reset is asserted for 1us and then de-asserted.
- After Tinit time period (1 ms) completion, device is ready for normal/ULPS operation.

This sequence is illustrated in the following figure.



Power-up sequence with register write operation

NOTE:
1. This is the time period in which txddrclkhs_i and pllqclk will become stable. In this period, all the AFE and DFE configurations become stable.
2. This is the PLL settling time.
3. DFE related trim values are written in the register set.
4. AFE related trim values are written in the register set.

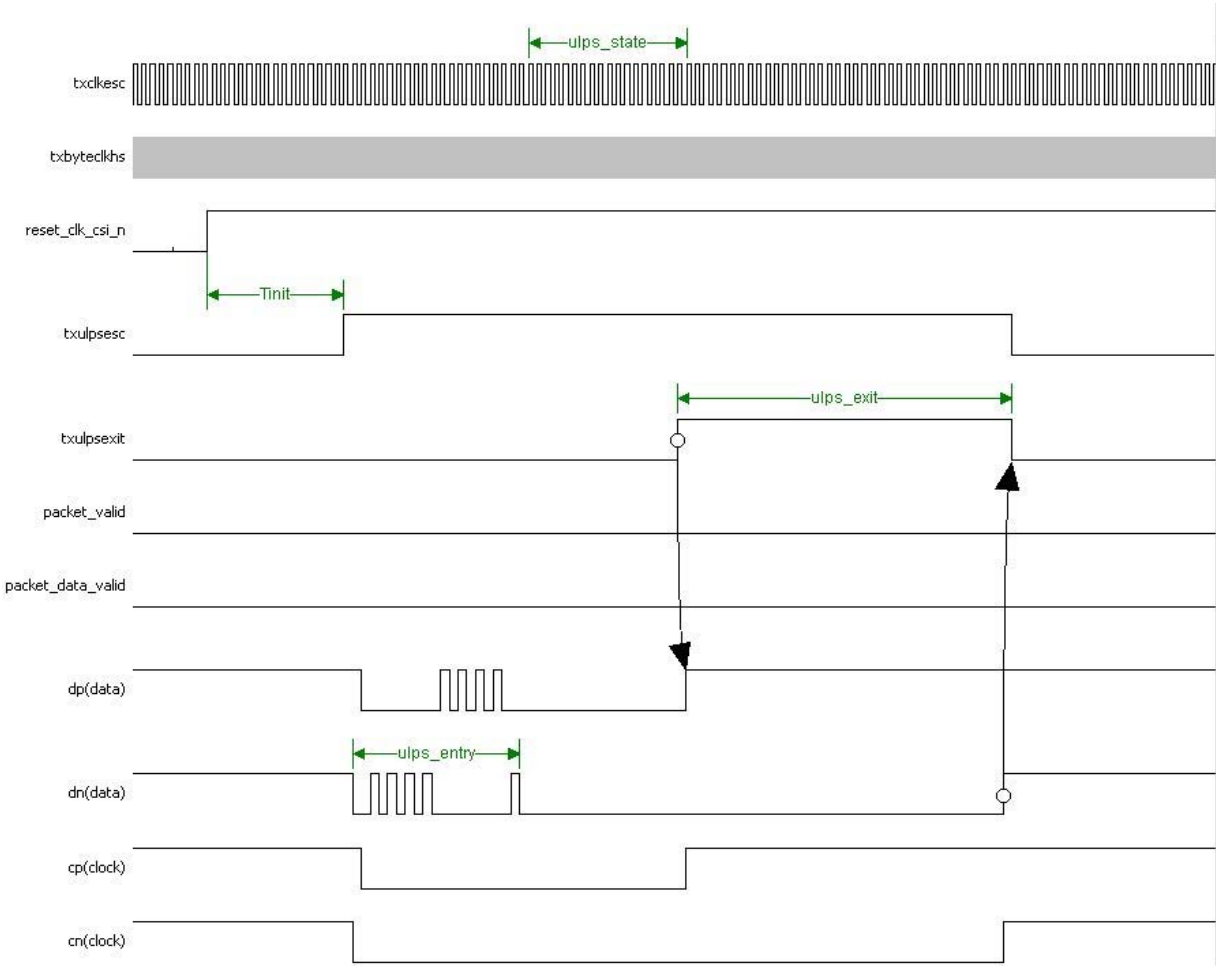
In the figure, shaded areas are invalid.

2.3 ULPS entry and exit

ULPS mode is the power saving state and it should occur only when there is no data to transfer. The entry and exit of ULPS can be controlled in the following manner.

- Initially, both the txulpsesc and txulpsexit signals are low. It indicates the D-PHY is in normal mode.
- To enter into ULPS mode, txulpsesc signal is asserted as high. It dictates the CSI controller to generate the control signals for the D-PHY to enter into ULPS mode.
- To exit from ULPS mode, both the txulpsesc and txulpsexit signals are driven as high for a minimum time period of minimum.
- After exiting from ULPS mode, both the txulpsesc and txulpsexit signals are driven low.

ULPS entry and exit flow is illustrated in the following figure.



ULPS entry and exit

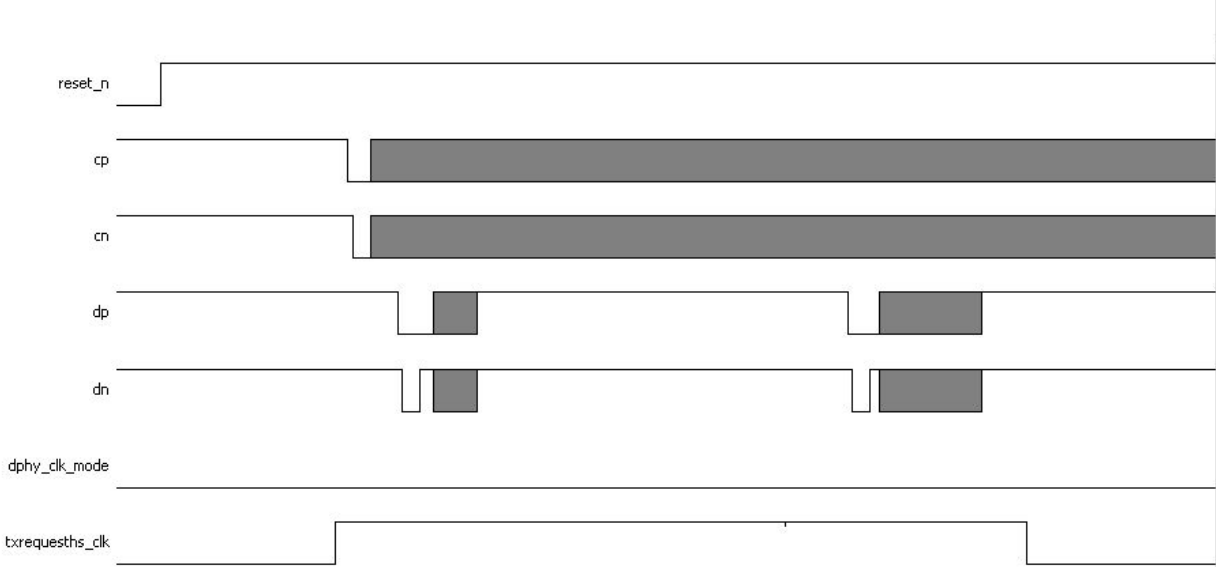
2.4 Clock Mode

There are two options available to handle clocking scheme in D-PHY. They are listed below,

- Continuous clock
- Non-continuous clock

2.4.1 Continuous clock

In this mode, the bit (rxddrclkhs) and byte (txbyteclkhs and rxbyteclkhs) clocks are generated from D-PHY as a continuous signal. There is no need to de-assert the clock request signal from CSI/BIST Controller in between packet transmissions. The following figure illustrates the behavior of this mode for two consecutive packets.

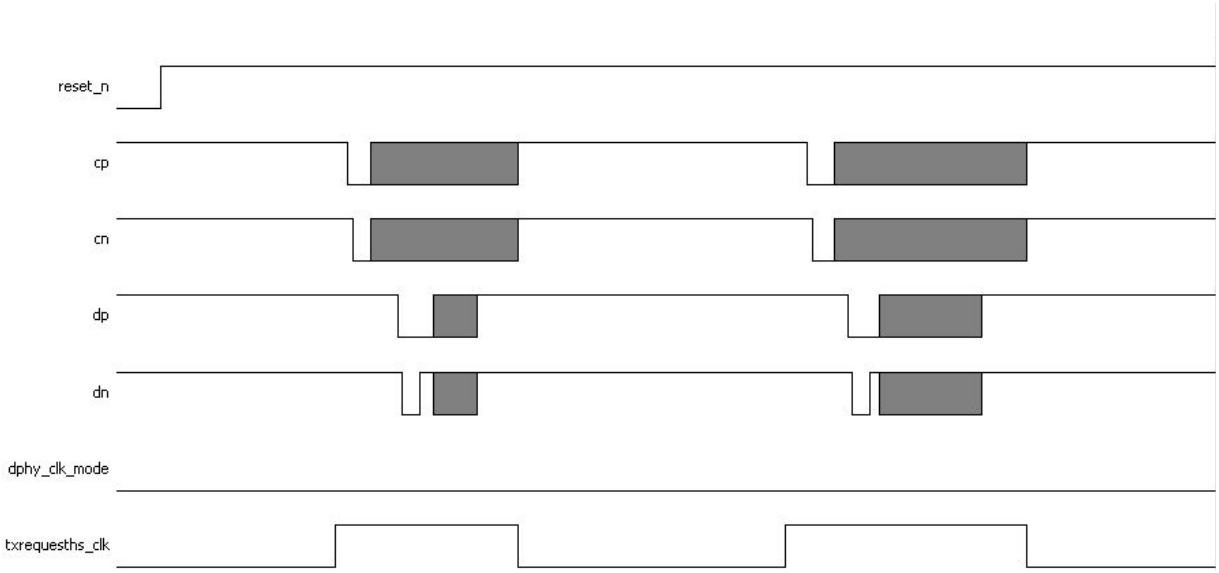


Continuous clock mode

NOTE: The shaded areas in the above figure indicate valid transitions.

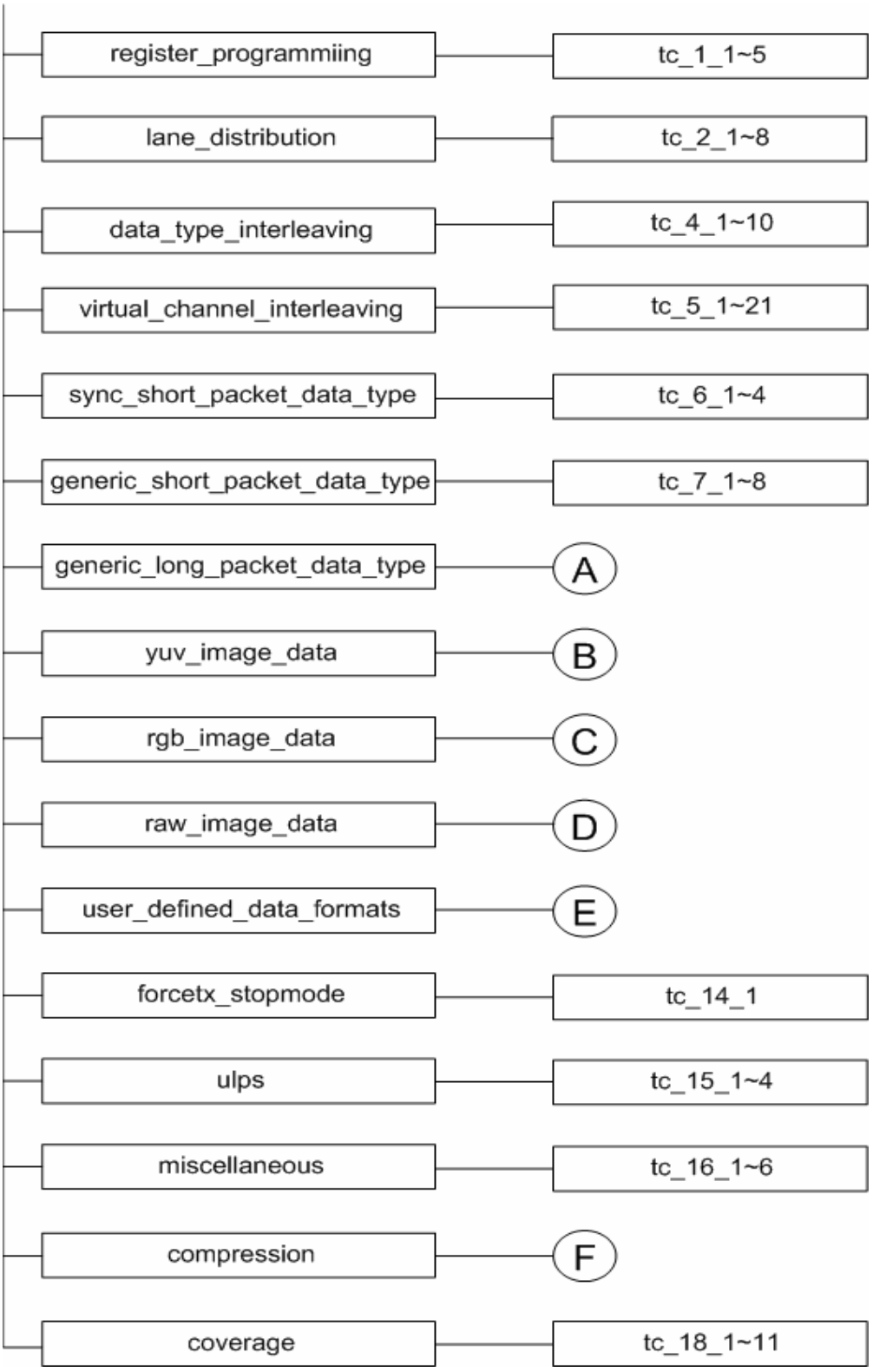
2.4.2 Non-continuous clock

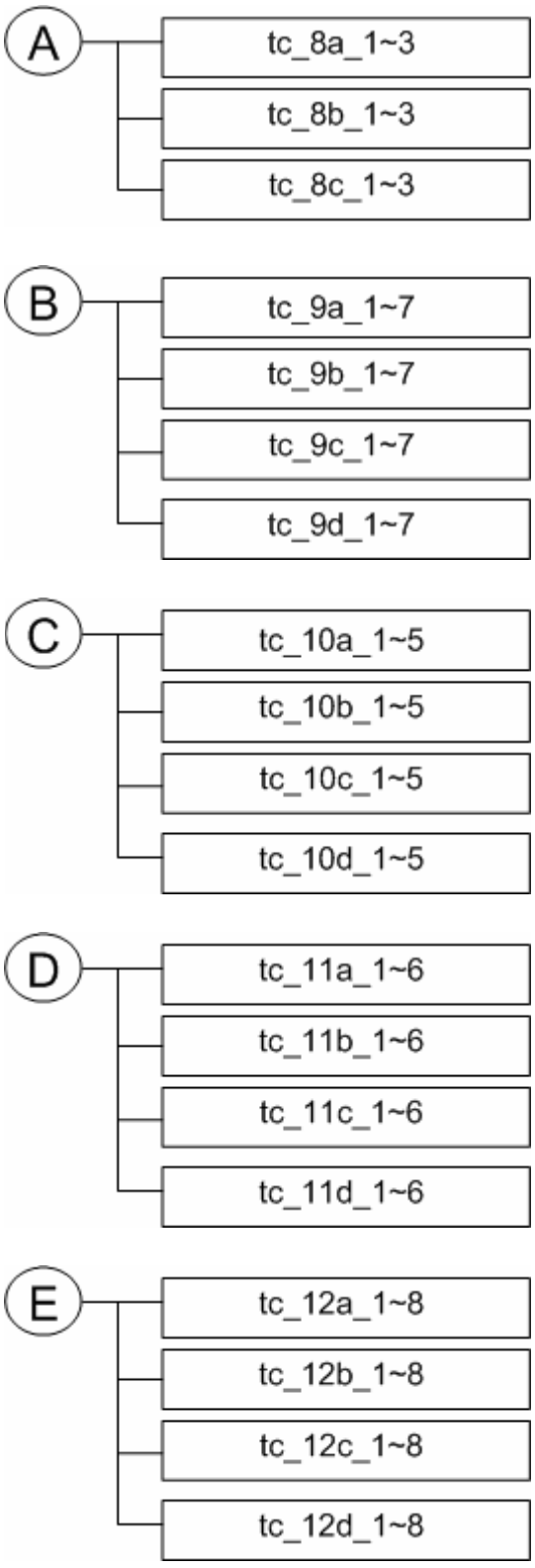
In this mode, the bit (RxDDRClkHS) and byte (txbyteclkhs and RxByteClkHS) clocks are generated from D-PHY as a non-continuous signal. CSI/BIST Controller should assert and de-assert clock request signal for each and every packet transmission. The following figure illustrates the behavior of this mode.

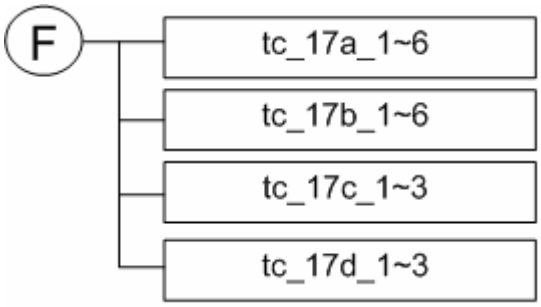


Non-continuous clock mode

3 Test Tree







4 Directory Structure

5 Test Plans and Tasks

NOTE: *For details on individual test case and task please refer to the test case excel sheet "CSI2_Transmitter_Testplan.xls" in docs directory*

