User Guide

CSI-2 Transmitter AHB IP

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Revision History

Table 1 : Revision History

Revision	Date	Change Description
1.0	06-May-2014	Initial Version
1.1	16-May-2014	-Lane configuration default value is changed to eight lane -DPHY Lane polarity swap register is updated for eight lanes

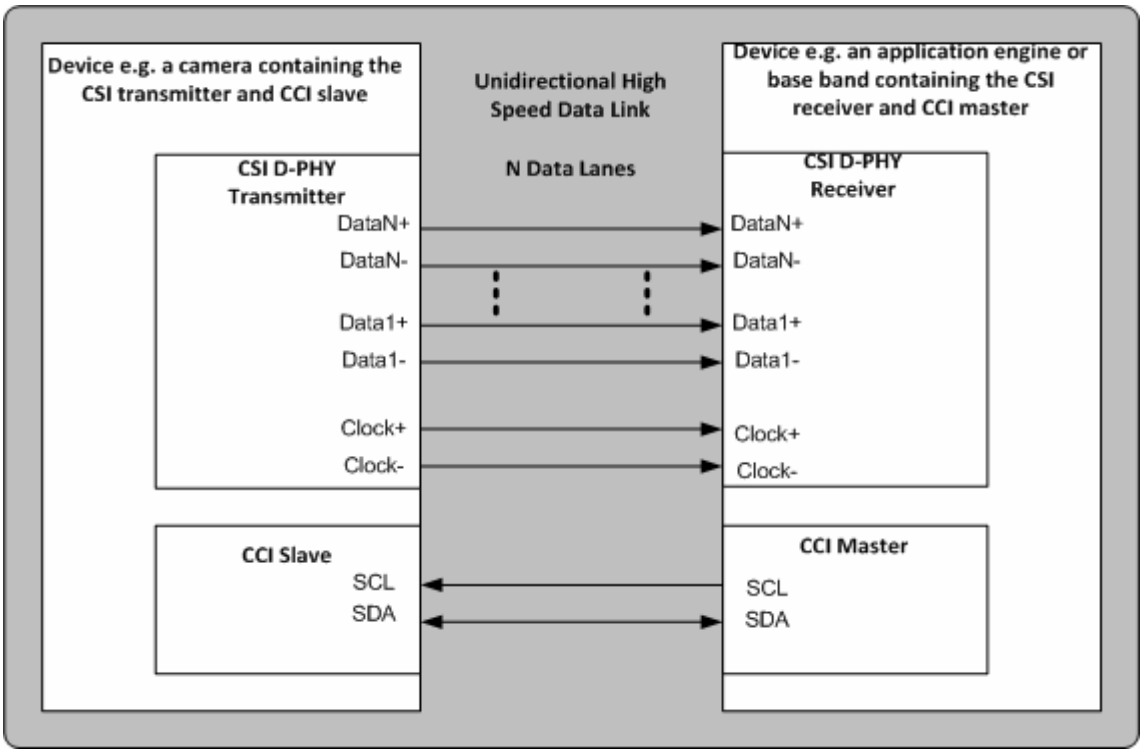
1 Introduction

1.1 Overview of CSI-2 Devices

The CSI2 devices are camera serial interface devices. It is categorized into two types namely, a CSI transmitter with a CCI slave and another as a CSI receiver device with a CCI master. Data transfer via CSI is unidirectional, that is from transmitter to receiver. CCI data transfer is bidirectional between the CCI slave and master.

CSI (Camera serial interface Bus) is a type of serial bus that enables transfer of data between a Transmitter device and a receiver device. The CSI device has point-to-point connections with CSI devices via D- PHY and as shown in Figure. Similarly, CCI [Camera Control Interface bus] is a type of serial bus that enables transfer back and forth between the master CCI and a Slave CCI unit.

Figure 1 : CSI-2 Transmitter and Receiver Interface



D-PHY data lane signals are transferred point-to-point as differential signals using two signal lines. It has a clock lane to transfer clock. There are two signaling modes like high speed mode and a low power mode. The mode is set to a Low power mode and a stop state at start up (or) during power up. Depending on the desired data transfer type, the data/clock lanes switches between high and low power modes.

CCI interface ends via I2C bus which has a clock line and a bidirectional data line.

The CSI-2 devices operate in a layered fashion. There are 5 layers identified both at receiver and transmitter ends.

1.1.1 CSI-2 Layered Structure

Figure 2 : CSI-2 Layered Structure

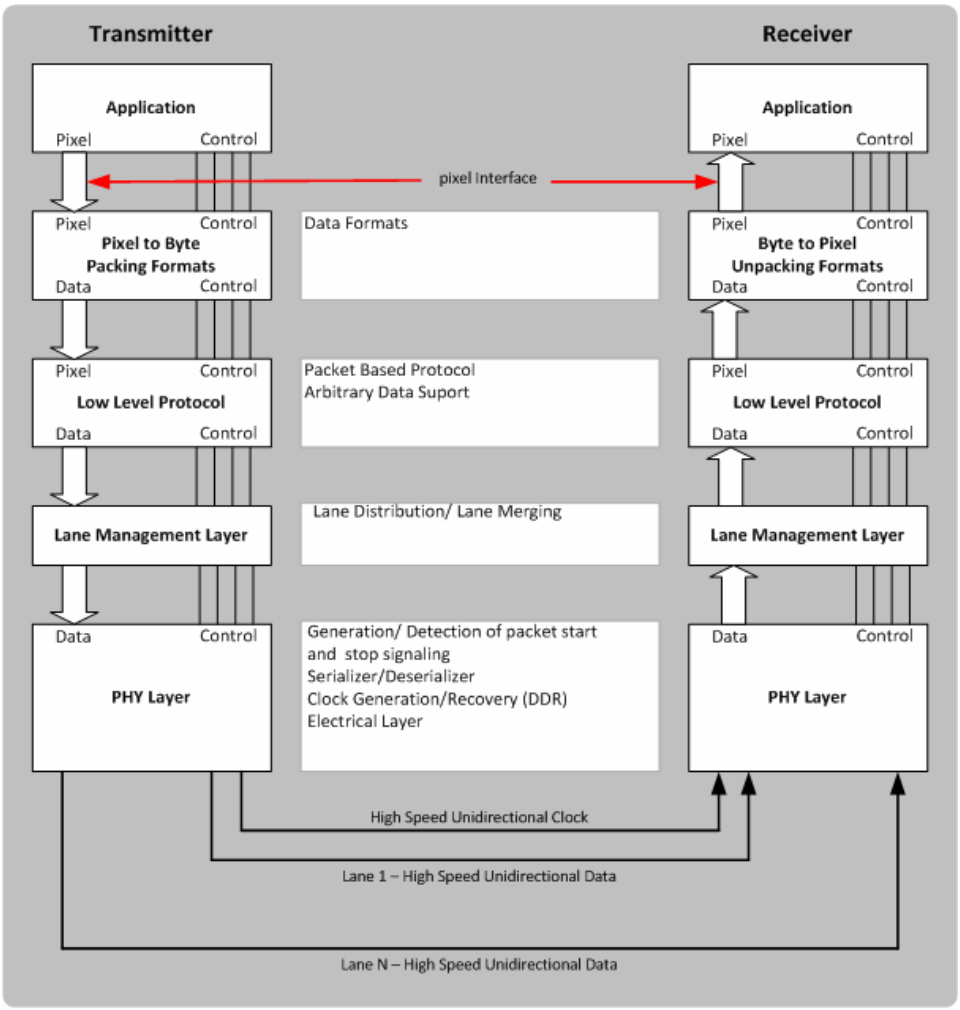


Table 2: CSI-2 Layered Structure

Layer	Description
PHY Layer	It has an embedded electrical layer and sends and detects start of packet signaling and end of packet signaling on the data lanes. It has a serializer and de-serializer unit to dialogue with the PPI / lane management unit. It also has a clock divider unit to transmit and to receive clock pulse during different modes of operation.

Lane Management Layer	This layer does the lane buffer and distributes the data in the lanes programmed in a round robin manner and also merges them to streamline it to the LLP/ PLI unit.
Low Level Protocol Layer	This layer packetizes as well as de-packetizes data with respect to channels, frames, colors and line formats. There is an ECC generator and corrector unit to recover the data free from errors in the packet headers. It has a CRC checker or CRC generator unit to pack the payload data with CRC checksum bits for payload data protection.
Pixel/ Byte to Byte/ Pixel Packing Formats	Porting of pixel formats to data bytes in the payload data is done depending on the type of image data supported by the application.
Application	Depending on the type of formats, camera types, capability of the camera used by the transmitter, the application recovers the image formats and reproduces the image in the display unit. It also works on de-framing the data into pixel formats that is understandable to pixel to packing formats. High level encoding and decoding of image data is handled in the application unit.

1.2 Features

The Arasan CSI-2 Transmitter supports the following features

1.2.1 CSI-2 Controller Features

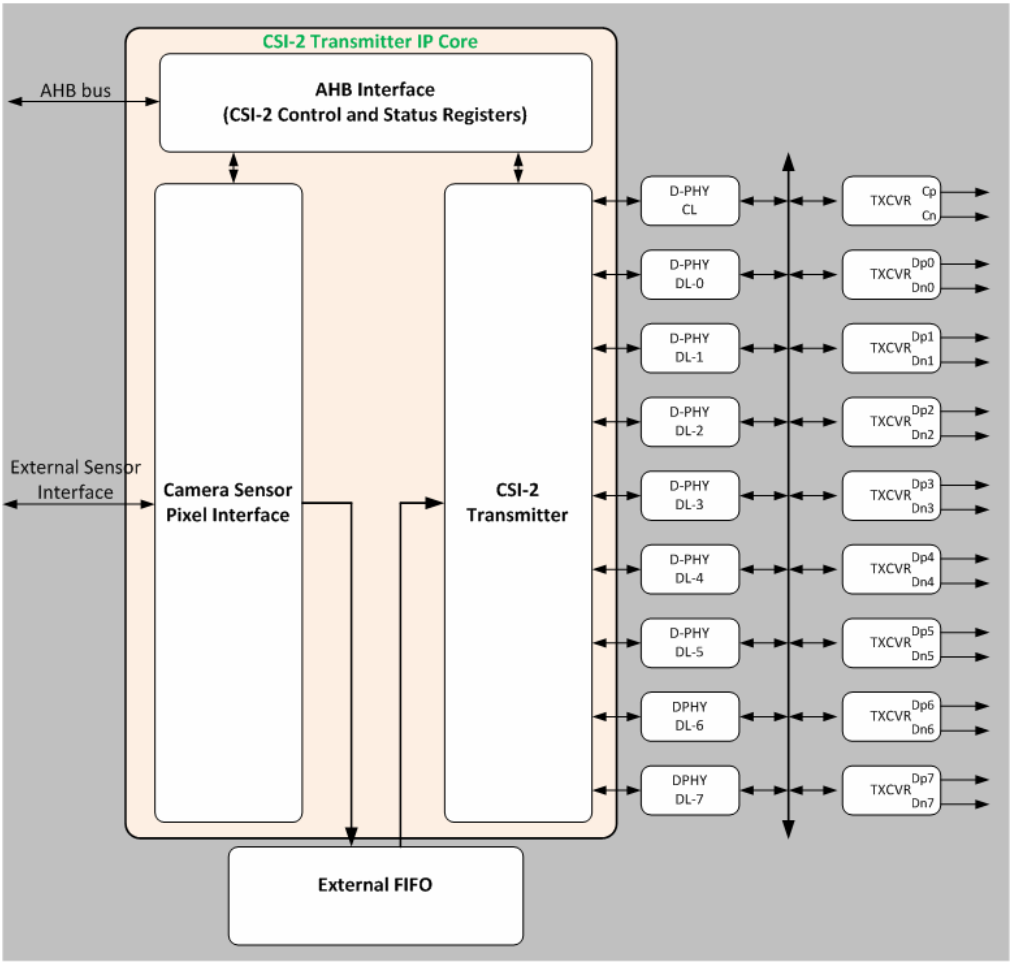
- Compliance to MIPI specification ***mipi_CSI-2_specification_v1-1***
- *Compliance to MIPI specification* ***mipi_CSI-2_specification_v1-2_r05***
- Standard D-PHY PPI interface compliant to MIPI specification ***mipi_D-PHY_specification_v1-2_r03***
- Supports PHY lane configurability up to ***Eight*** lanes
- AHB processor interface / Micro Controller interface for register programming
- Support Image sensor interface at pixel level
- Supports data type interleaving
- Supports virtual channel interleaving
- Support for all MIPI spec. defined compression and prediction techniques
- Pixel format supported
  - RAW data type
  - YUV data type
  - RGB data type
  - User Defined data type – 8-bit
  - Generic 8-bit long packets (Null, Blanking, Embedded data)
- Supports ECC and CRC calculations
- Store and Forward Architecture – Stores the full pixel packet before forwarding.

2 Architecture

The Figure below shows the architectural block diagram of CSI-2 transmitter core. The preference of system bus in this architecture is AHB. This is primarily used for register configuration. This system bus interface could be changed to other interface like Micro-controller bus interface. In this document, the system bus interface will be limited to AHB interface.

In CSI-2 transmitter core, the PHY layer uses high speed clock (in phase) for HS data transfer and high speed clock (quadrature) for clock transmission on clock lane. The core supports HS mode and ULPS operations. The PPI interface operates with Byte Clock (HS speed Clk/4) driven out from the D-PHY.

Figure 3 : System Architecture



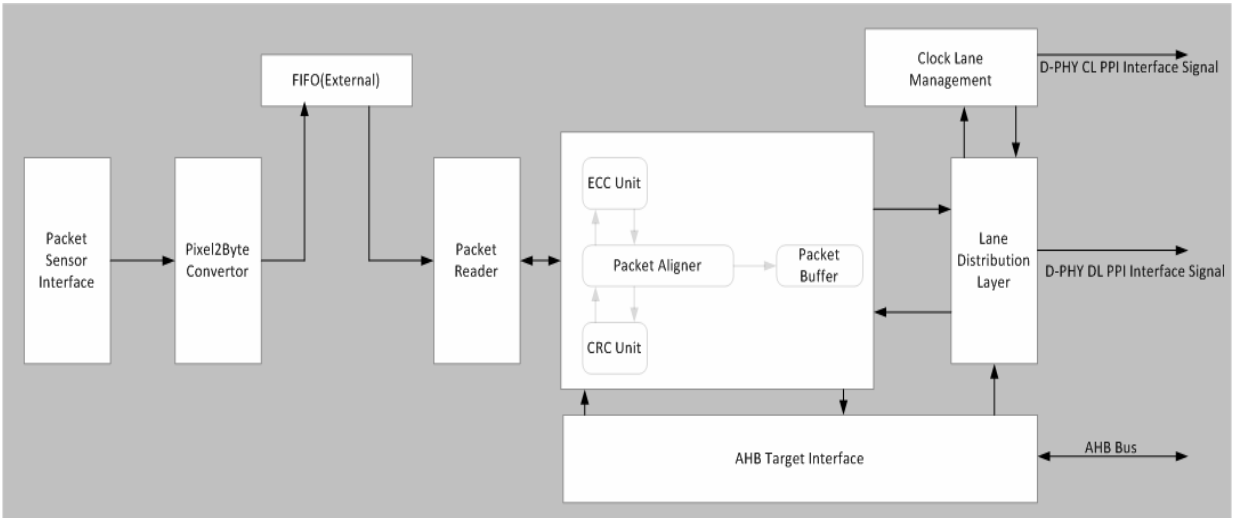
2.1 Functional Block Diagram of CSI-2 Transmitter IP

The CSI-2 transmitter IP is partitioned into following sub-modules to accomplish the required functionality,

- AHB Target Interface
- Sensor Interface
- Pixel to Byte Convertor
- FIFO (External)
- Packet Reader
- Low Level Protocol
- Lane Distribution Layer Unit
- Clock Lane Management Unit

The Figure shows the functional block diagram of CSI-2 Transmitter IP core.

Figure 4 : CSI-2 Transmitter IP Core



2.1.1 AHB Target Interface

This module connects the CSI-2 transmitter core to external AHB processor. The module provides interface to DPHY/AFE and CSI-2 controller register set. The user can configure the different application specific attributes through set of registers. The various programmable registers are listed in section “Registers”

2.1.2 Packet Sensor Interface

This module interfaces to external sensor. The module provides a handshake mechanism to accept the long pixel data packet and the synchronization packets like Frame Start, Line Stat, Line End and Frame End. This also controls the data flow from the external sensor interface to CSI-2 transmitter controller.

2.1.3 Pixel to Byte Convertor

This module converts the received pixel information to byte as per the CSI-2 specification. The respective pixel to byte convertor will get enabled based on the received data type. This module converts the received pixel information and sync packet information to 64-bit and forwards it to external memory. This module also takes care of compression of the pixel information.

2.1.4 FIFO (External)

This is library specific dual Port (or) Two port RAM of size 64-width x 8K deep, which is instantiated outside the CSI-2 IP. This is used as temporary storage buffer. The size of the buffer can be reduced / increased based on the application. This FIFO parameter is provided as configurable parameter in “csi2tx_defines.v” file. Based on the user requirement, the user can change the FIFO size (depth only).

The write interface of this FIFO operates with respect to clk_csi and the read interface operates with respect to TxByteclkHS.

Note: In store and forward mechanism the depth of the FIFO should be 2 * MAX Line size required.

2.1.5 Packet Reader

This module keeps track the number of packet being written to FIFO and read out from FIFO. As the architecture supports only store and forward mechanism, this module waits for the complete packet to be stored in the FIFO before forwarding it to the low level protocol layer for further processing.

2.1.6 Low Level Protocol

This module includes following sub-modules to perform the required functionality

- CRC

- ECC
- Packet Aligner
- Packet Buffer

2.1.6.1 CRC

The CRC modules calculates the CRC for the received byte aligned data and on receiving the end of packet validates the appropriate CRC value to the upper layer in order to append it to the CSI-2 packet as packet footer.

2.1.6.2 ECC

The ECC module calculated the ECC for the short packet and packet header of the long packet. Once the ECC is ready, signals the upper layer to append the ECC to the packet header.

2.1.6.3 Packet Aligner

This module supports the following features,

- Appends the packet footer to the packet
- Appends the ECC to the packet header
- Aligns the Long packet header and data information in the 64-bit format to support up to eight lanes
- Calculates the CRC appending byte positions
- Write the received packet to the packet buffer

2.1.6.4 Packet Buffer

This is register based FIFO of size 64-width X 8-deep. This is used as elastic buffer to the DPHY. This is a synchronous FIFO, where in the write and read interface operates with respect to TxByteClkHS.

2.1.7 Lane Distribution Layer

This module supports the following features,

- Maintains the one packet processing concept for the CSI-2 – Will not read any other packet until the current packet is completely processed by the DPHY and all the DPHY parameter are met.
- Takes care of the bytes distribution on to different D-PHY data lanes based on the user lane configuration
- Provides the Data Lane PPI interface for the DPHY

2.1.8 Clock Lane Management Layer

This module supports the following features,

- Provides the Clock lane PPI interface to the DPHY
- Control the request for the clock lane based on the continuous and non-continuous clock mode
- Controls the clock and data lane of DPHY, when ULPS is enabled by the user
- Controls the Calibration of the DPHY as per user requirement

3 Signals

3.1 Pin Description

Table 3: Top Level Port Interface

Port	Width	Dir.	Description	Clock Domain
Global Interface SIgnals				
pwr_on_rst_n	1	IN	Active low Asynchronous reset	N.A
sysclk	1	IN	The clock with which the AHB Interface operates.	N.A
txbyteclkhs	1	IN	Byte Clock derived from TxDDRClkHS. This clock is used to synchronize all high speed PPI Interface signals	N.A
sensor_clk	1	IN	Pixel clock. Clock with which the pixel data is received from sensor. Requirement : sensor_clk should be >= TxByteClkHS	N.A
txclkesc	1	IN	Low Speed clock of DPHY. This clock is used to synchronize all the low speed PPI interface signal	N.A
test_mode	1	IN	Active HIGH test mode signal used internally to mux the Power On Reset during DFT mode	N.A
DPHY Interface Signals				
dfe_pll_locked	1	IN	When '1' Indicates that the PLL of the DPHY is locked and indication for the CSI-2 to initiate transfer if any	Aynchronous
txreadyhs	8	IN	This signal indicates if the DPHY is ready to accept data on the PPI interface for respective lane. A successful data transfer is complete when txreadyhs and txrequesths is valid for one clock cycle for respective lane. The LSb of this bus corresponds to data lane 0 and the MSb of this bus corresponds to data lane 7	txbyteclkhs
stopstate	8	IN	Indicates a reception of STOP state on the data lane. The LSb of this bus corresponds to data lane 0 and the MSb of this bus corresponds to data lane 7	Asynchronous
ulpsactivenot_clk_n	1	IN	This signal indicates if the clock lane transmitter is not in ULPS active state.	txclkesc
ulpsactivenot_n	8	IN	This signal indicates if the transmit data lane is not in ULPS state. The LSb of this bus correspond to the data lane 0, and the MSb of this bit correspond to the data lane 7.	txclkesc
stopstate_clk	1	IN	Indicates the STOP state sequence on the clock lane	Asynchronous

txrequesths	8	OUT	TheHS request signal that correspond to the DATA lines. The LSb of this bus correspond to the data lane 0, and the MSb of this bit correspond to the data lane 7.	txbyteclkhs
txdatahs	64	OUT	The data to be transmitted on the Data lanes. The LSB of the data bus correspond to the data lane 0, and MSB correspond to the data lane 7.	txbyteclkhs
txulpsesc_entry	8	OUT	This signal indicates if the DPHY has to initiate a ULPS sequence on the data lane. The LSb of this bus correspond to the data lane 0, and the MSb of this bit correspond to the data lane 7.	txclkesc
txulpsesc_entry_clk	1	OUT	This signal indicates if the DPHY has to initiate a ULPS sequence on the clock lane	txclkesc
txulpsesc_exit	8	OUT	This signal indicates if the DPHY has to exit out of a ULPS state on the data lanes. The LSb of this bus correspond to the data lane 0, and the MSb of this bit correspond to the data lane 7.	txclkesc
txulpsesc_exit_clk	1	OUT	This signal indicates if the DPHY has to exit out of a ULPS state on the clock lane.	txclkesc
txrequestesc	8	OUT	Valid signal for any ESC mode request on the data lanes. The LSb of this bus correspond to the data lane 0, and the MSb of this bit correspond to the data lane 7.	txclkesc
txskewcalhs	8	OUT	High-Speed Transmit Skew Calibration. A low-to-high transition on TxSkewCalHS causes the PHY to initiate a de-skew calibration. A high-to-low transition on TxSkewCalHS causes the PHY to stop deskew pattern transmission and initiate an end-of-transmission sequence. The LSb of this bus correspond to the data lane 0, and the MSb of this bit correspond to the data lane 7.	txbyteclkhs
DPHY/AFE Configuration interface signals				
afe_trim_0	32	OUT	AFE trim register-0	sysclk
afe_trim_1	32	OUT	AFE trim register-1	sysclk
afe_trim_2	32	OUT	AFE trim register-2	sysclk
afe_trim_3	32	OUT	AFE trim register-3	sysclk
dfe_dln_reg_0	32	OUT	Register to DPHY for data lane control	sysclk
dfe_dln_reg_1	32	OUT	Register to DPHY for data lane control	sysclk
dfe_cln_reg_0	32	OUT	Register to DPHY for clock lane control	sysclk
dfe_clk_reg_1	32	OUT	Register to DPHY for clock lane control	sysclk
pll_cnt_reg	16	OUT	PLL count value	sysclk
dfe_dln_lane_swap	8	OUT	Register control to DPHY for lane swap	sysclk
AHB Interface Signals				

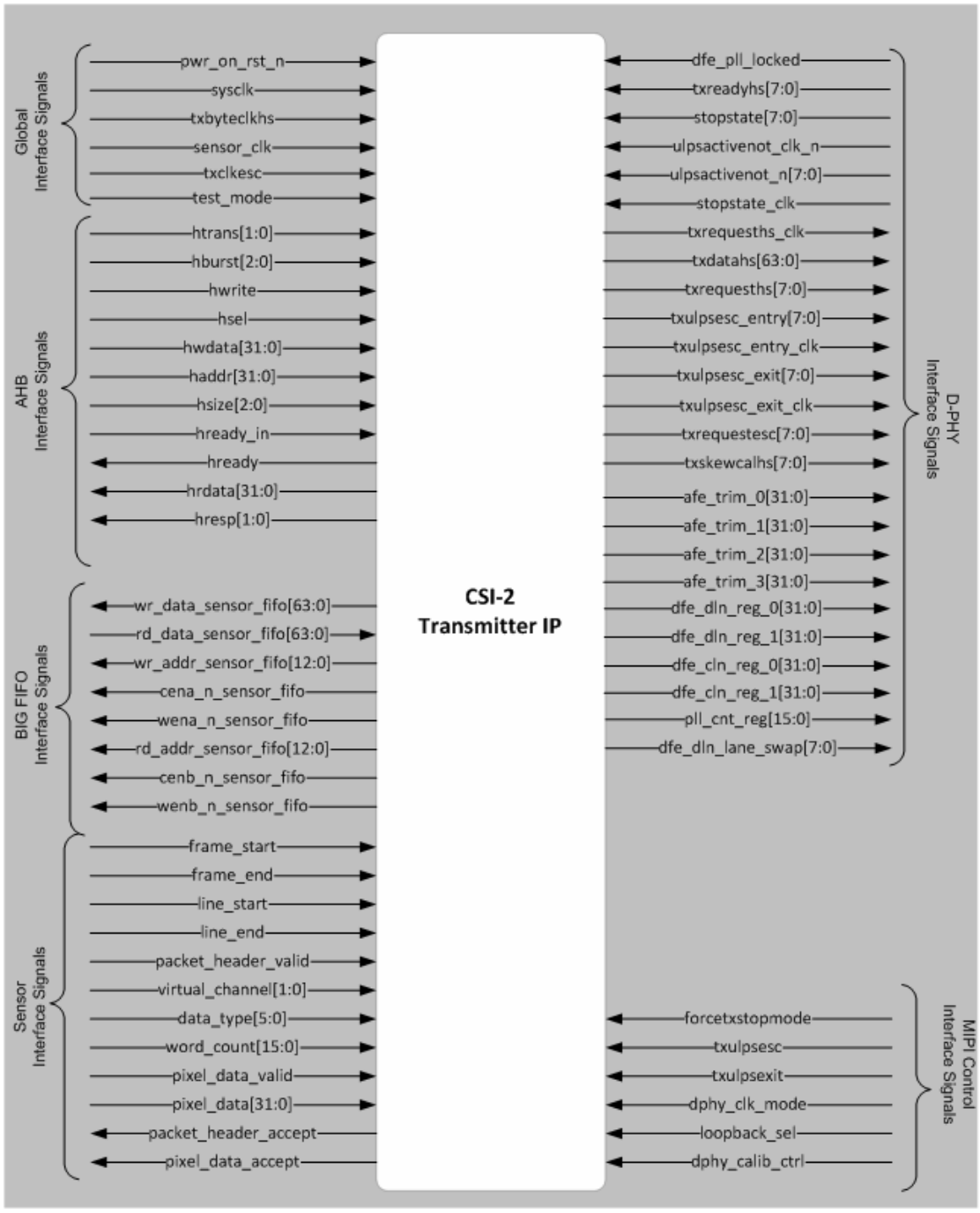
hwrite	1	IN	Read/Write from AHB master When '0' : Read operation When '1' : Write operation	sysclk
hsel	1	IN	Select signal from AHB master	sysclk
hready_in	1	IN	Ready signal from AHB master	sysclk
haddr	32	IN	Address bus from AHB master	sysclk
hsize	3	IN	Indicate Double Word from AHB master	sysclk
hburst	3	IN	Indicates sequential transfer from mater	sysclk
htrans	2	IN	Non-seq or seq transaction from AHB master	sysclk
hwdata	32	IN	Write data from AHB master	sysclk
hrdata	32	OUT	Read data from AHB slave	sysclk
hresp	2	OUT	Transfer response from AHB slave	sysclk
hready	1	OUT	Ready signal from AHB slave	sysclk
Camera Sensor Interface Signals				
frame_start	1	IN	Indicates the frame start from the corresponding virtual channel. This is a pulse which is asserted for one clock cycle for each frame start. Min of two clock should be maintained after the de-assertion of frame start to the assertion of line start/packet_header_valid	sensor_clk
frame_end	1	IN	Indicates the frame end for the corresponding virtual channel. This is a pulse which is asserted for one clock cycle for each frame end. Minimum of 2 clock should be maintained from the de-assertion to the next packet assertion	sensor_clk
line_start	1	IN	Indicates the line start for the corresponding virtual channel. This is a pulse which is asserted for one clock cycle for each line start. Minimum of 2 clock should be maintained from the de-assertion to the next packet assertion	sensor_clk
line_end	1	IN	Indicates the line end for the corresponding virtual channel. This is a pulse which is asserted for one clock cycle for each frame end. Minimum of 2 clock should be maintained from the de-assertion to the next packet assertion	sensor_clk
packet_header_valid	1	IN	Signal to indicate that the data type is accepted. Data type is validated only if both the packet_header_valid and packet_header_accept is asserted	sensor_clk
virtual_channel	2	IN	Indicates the virtual channel for which the packet needs to be transmitted 00 → Virtual Channel-0 01 → Virtual Channel-1 10 → Virtual Channel-2 11 → Virtual Channel-3	sensor_clk

data_type	6	IN	For long packets, indicates the data type of the pixel data from camera sensor For short packets, it indicates the data type that needs to be transmitted	sensor_clk
word_count	16	IN	Indicates the word count of the long packet to be transmitted Note: If the compression scheme is programmed by the processor for User Defined data type, the word count should be with respect to the compressed format	sensor_clk
pixel_data_valid	1	IN	When asserted indicates that the pixel data is valid	sensor_clk
pixel_data	32	IN	32-bit pixel data from camera sensor. If the pixel size is less than 32-bit then the MSB bits are discarded	sensor_clk
packet_header_accept	1	OUT	When asserted indicates that the data type, word count and the virtual channel are valid	sensor_clk
pixel_data_accept	1	OUT	Signal to indicate that the pixel data is accepted. Pixel data is validated only if both the pixel_data_valid and pixel_data_accept is asserted. Minimum of 2 clock should be maintained from the de-assertion to the next packet assertion	sensor_clk
MIPI Control Signals				
forcetxstopmode	1	IN	This signal indicates if the transmitter engine should drive STOP state on the data lane. This is configured by the application requesting D-PHY to drive STOP STATE Note: This signal should be stable at least for two clock cycles of txbyteclkhs	Asynchronous
txulpsesc	1	IN	This signal indicates if the DPHY has to initiates the ULPS sequence. If this is asserted the CSI-2 Tx will drive ULPS entry enable for D-PHY(Clock and Data Lanes) This is configured by application for driving the D-PHY to ULPS mode	Asynchronous
txulpsexit	1	IN	This signal indicates if the DPHY has to exit out of a ULPS state. If this is asserted the CSI-2 Tx will drive ULPS exit enable for D-PHY(Clock and Data lanes) This is configured by the application to exit the DPHY from ULPS mode	Asynchronous
dphy_clk_mode	1	IN	When ‘0’ : Continuous Clock Mode When ‘1’ : Non Continuous Clock Mode This is configured by the application based on the mode in which MIPI PHY clock lane need to operate	Asynchronous

loopback_sel	1	IN	This signal is used as a valid signal to the LOOP BACK MODE When '1' : Indicates that the core is in LOOPBACK MODE When '0' : Indicates that the core is in Functional mode Note: This signal should be tied low, if the MIPI D-PHY does not support loop back Note: This feature not applicable for third party D-PHY	Asynchronous
dphy_calib_ctrl	1	IN	This signal indicates if the DPHY has to start the Skew calibration or not. When this signal rises from 0 to 1 – Skew calibration is enabled to DPHY When this signal falls from 1 to 1 – Skew calibration is disabled to DPHY This is configured by the application to enter/exit the DPHY from Calibration Note: This signal should be stable at least for two clock cycles of txbyteclkhs	Asynchronous
Sensor FIFO Interface signals				
cena_n_sensor_fifo	1	OUT	Chip enable for Port-A	sensor_clk
wena_n_sensor_fifo	1	OUT	This port is used only for Write. When '0' : Write When '1' : Read	sensor_clk
wr_addr_sensor_fifo	13	OUT	Write address bus for sensor RAM	sensor_clk
wr_data_sensor_fifo	64	OUT	32-bit write data bus to Sensnor RAM	sensor_clk
rd_data_sensor_fifo	64	IN	Read data bus from sensor RAM	txbyteclkhs
rd_addr_sensor_fifo	13	OUT	Read address bus for sensor RAM	txbyteclkhs
cenb_n_sensor_fifo	1	OUT	Chip enable for Port-B	txbyteclkhs
wenb_n_sensor_fifo	1	OUT	This port is used only for Read. When '0' : Write When '1' : Read	txbyteclkhs

Pin Diagram

Figure 5: CSI-2 Transmitter Top Level Port Interface



4 Register

4.1 CSI-2 Transmitter Controller Register

The CSI-2 Tx register set provides memory mapped registers on the system bus interface. The reserved bits defined in this specification may be allocated in later revisions. Software shall not modify these reserved bits and assume the reserve bits are all zeros. CSI-2 Tx registers are used to control the operation of the IP. A read access to all the reserved memory space gives zeros on read data bus. A write access to all the reserved memory space gets ignored.

The following notation is used to describe the register access attributes

- RO : Read only. If a register is read only, write has no affect
- WO : Write Only. If a register is write only, read returns a zero for all bit positions
- R/W : Read/Write. A register with this attribute can be read and written
- R/WC : Read/Write Clear. A register with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect

Number	Register Offset	Register Name
AFE Registers		
1.	0x0000H	Trim Register-0
2.	0x0004H	Trim Register-1
3.	0x0008H	Trim Register-2
4.	0x000CH	Trim Register-3
5.	0x0010H	Reserved
6.	0x0014H	Reserved
7.	0x0018H	Reserved
8.	0x001CH	Reserved
DFE/CSI-2 Tx Controller Register		
1.	0x0020H	DPHY DFE DLN Register-0
2.	0x0024H	DPHY DFE DLN Register-1
3.	0x0028H	DPHY DFE CLN Register-0
4.	0x002CH	DPHY DFE CLN Register-1
5.	0x0030H	DPHY Lane Polarity Swap Register
7.	0x0034H	Reserved
8.	0x0038H	Status Register
9.	0x003CH	Lane Configuration Register
10.	0x0040H	Reserved
11.	0x0044H	Reserved

12.	0x0048H	Reserved
13.	0x004CH	VC0 Compression/Prediction Register-1
14.	0x0050H	VC0 Compression/Prediction Register-2
15.	0x0054H	VC1 Compression/Prediction Register-1
16.	0x0058H	VC1 Compression/Prediction Register-2
17.	0x005CH	VC2 Compression/Prediction Register-1
18.	0x0060H	VC2 Compression/Prediction Register-2
19.	0x0064H	VC3 Compression/Prediction Register-1
20.	0x0068H	VC3 Compression/Prediction Register-2
21.	0x006CH	PLL Count Register

Note : For AFE Register settings, please refer to Arasan DPHY User Guide

4.2 DPHY DFE DLN Register-0

Register Name	DPHY DFE DLN Register-0
Address	0x0020H
Default Value	0x0A0D_0716H

Bit Value Mapping

[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	0	0	0	0	1	1	1	0	0	0	1	0	1	1	0
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
0	0	0	0	1	0	1	0	0	0	0	0	1	1	0	1

Bit	Field	Access		Description
		S/W	H/W	
[7:0]	DFE_DLN_HS_ZERO_CNT	R/W	RO	This parameter specifies the number of byte clocks cycles the data lane shall wait to complete the HS-ZERO time
[15:8]	DFE_DLN_HS_PREPARE	R/W	RO	This parameter specifies the number of byte clock cycles the data lane shall wait to complete the HS PREPARE time
[23:16]	DFE_DLN_HS_EXIT	R/W	RO	This parameter specifies the number of byte clock cycles the data lane shall wait to complete the HS-EXIT time
[31:24]	DFE_DLN_HS_TRIAL	R/W	RO	This parameter specifies the number of byte clock cycles the data lane shall wait to complete the HS TRIAL time

4.3 DPHY DFE DLN Register-1

Register Name	DPHY DFE DLN Register-1

Address	0x0024H
Default Value	0x0006_1E07H

Bit Value Mapping

[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bit	Field	Access		Description
		S/W	H/W	
[7:0]	DFE_DLN_RX_CNT	R/W	RO	This parameter specifies the number of byte clocks cycles the data lane shall wait before enabling the HS receiver
[15:8]	DFE_DLN_SYNC_CNT	R/W	RO	This parameter specifies the number of byte clock cycles the data lane shall wait before announcing an error on the timeout of the SYNC pattern
[23:16]	DFE_DLN_LPX_HS_CNT	R/W	RO	This parameter specifies the number of byte clock cycles required to accommodate an LP- xx state on the data lane
[31:24]	RSVD	R/W	RO	Reserved

4.4 DPHY DFE CLN Register-0

Register Name	DPHY DFE CLN Register-0
Address	0x0028H
Default Value	0x080D_0521H

Bit Value Mapping

[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	1
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	1

Bit	Field	Access		Description
		S/W	H/W	
[7:0]	DFE_CLN_ZERO	R/W	RO	This parameter specifies the number of byte clocks cycles the clock lane transmitter module shall wait during the HS-ZERO sequence of the high speed clock transmission

[15:8]	DFE_CLN_PREPARE	R/W	RO	This parameter specifies the number of byte clock cycles the clock lane transmitter module shall wait during the prepare sequence of the high speed clock transmission
[23:16]	DFE_CLN_HS_EXIT	R/W	RO	This parameter specifies the number of byte clock cycles the clock lane transmitter module shall wait during the exit sequence of the high speed clock transmission
[31:24]	DFE_CLN_HS_TRIAL	R/W	RO	This parameter specifies the number of byte clock cycles the clock lane transmitter module shall wait during the TRIAL sequence of the high speed clock transmission

4.5 DPHY DFE CLN Register-1

Register Name	DPHY DFE CLN Register-1
Address	0x002CH
Default Value	0x0000_0006H

Bit Value Mapping

[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Field	Access		Description
		S/W	H/W	
[7:0]	DFE_CLN_LPX_HS_CNT	R/W	RO	This parameter specifies the number of byte clocks required to accommodate an LP-xx stat on the clock lane
[15:8]	TCLK_PRE	R/W	RO	This parameter specifies that the HS clock shall be driven by the transmitter prior to any associated data lane beginning the transition from LP to HS mode. The parameter is in terms of number of TxByteClkHS
[23:16]	TCLK_POST	R/W	RO	This parameter specifies the number of byte clock cycles the clock lane transmitter module shall wait before removing the clock lane request after the last associated data lane has transitioned to LP mode
[31:24]	RSVD	NA	NA	Reserved

4.6 DPHY Lane polarity swap register

Register Name	DPHY lane polarity swap register
Address	0x0030H

Default Value	0x0000_0000H

Bit Value Mapping															
[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Field	Access		Description
		S/W	H/W	
[0]	DLN0_SWAP	R/W	RO	D-PHY data lne-0 swap logic enable When '1' : Dp/Dn lines are swapped When '0' : Dp/Dn lines are not swapped
[1]	DLN1_SWAP	R/W	RO	D-PHY data lane-1 swap logic enable When '1' : Dp/Dn lines are swapped When '0' : Dp/Dn lines are not swapped
[2]	DLN2_SWAP	R/W	RO	D-PHY data lane-2 swap logic enable When '1' : Dp/Dn lines are swapped When '0' : Dp/Dn lines are not swapped
[3]	DLN3_SWAP	R/W	RO	D-PHY data lane-3 swap logic enable When '1' : Dp/Dn lines are swapped When '0' : Dp/Dn lines are not swapped
[4]	DLN4_SWAP	R/W	RO	D-PHY data lane-4 swap logic enable When '1' : Dp/Dn lines are swapped When '0' : Dp/Dn lines are not swapped
[5]	DLN5_SWAP	R/W	RO	D-PHY data lane-5 swap logic enable When '1' : Dp/Dn lines are swapped When '0' : Dp/Dn lines are not swapped
[6]	DLN6_SWAP	R/W	RO	D-PHY data lane-6 swap logic enable When '1' : Dp/Dn lines are swapped When '0' : Dp/Dn lines are not swapped
[7]	DLN7_SWAP	R/W	RO	D-PHY data lane-7 swap logic enable When '1' : Dp/Dn lines are swapped When '0' : Dp/Dn lines are not swapped
[31:8]	RSVD	NA	NA	Reserved

Note : Lane polarity is performed only on data lane

4.7 CSI-2 Tx FIFO Status Register

Register Name	FIFO status Register
Address	0x0038H

Default Value	0x0000_0000H

Bit Value Mapping															
[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Field	Access		Description
		S/W	H/W	
[0]	SYNC_FIFO_EMPTY	R/W	WO	Indicates the SYNC FIFO empty status
[1]	SYNC_FIFO_ALMOST_FULL	R/W	WO	Indicates the SYNC FIFO threshold full status
[2]	SYNC_FIFO_FULL	R/W	WO	Indicates the SYNC FIFO full status
[3]	ASYNC_FIFO_EMPTY	R/W	WO	Indicates the ASYNC FIFO empty status
[4]	AYNC_FIFO_FULL	R/W	WO	Indicates the ASYNC FIFO full status
[5]	DATA_ID_ERR	R/W	WO	When '1' Indicates the un-recognized data type
[31:5]	RSVD	NA	NA	Reserved

4.8 Lane Configuration Register

Register Name	Lane Configuration Register
Address	0x003CH
Default Value	0x0000_0007H

Bit Value Mapping															
[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Field	Access		Description
		S/W	H/W	

[2:0]	NUMBER_OF_LANES	R/W	RO	When [2:0] is "000" → CSI-2 Tx is configured as ONE lane "001" → CSI-2 Tx is configured as TWO lane "010" → CSI-2 Tx is configured as THREE lane "011" → CSI-2 Tx is configured as FOUR lane "100" → CSI-2 Tx is configured as FIVE lane "101" → CSI-2 Tx is configured as SIX lane "110" → CSI-2 Tx is configured as SEVEN lane "111" → CSI-2 Tx is configured as EIGHT lane
[31:3]	RSVD	NA	NA	Reserved

4.9 VC0 Compression/Prediction Scheme Register-1

Register Name	VC0 Compression/Prediction Scheme Register-1
Address	0x004CH
Default Value	0x0000_0000H

Bit Value Mapping															
[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Field	Access		Description
		S/W	H/W	
[4:0]	CMPRS_SCHM_FR_USD_TYPE0	R/W	RO	To be configured by processor as per the requirement. The [2:0] bits select the type of compression When "000" → No Compression When "001" → 10-6-10 Type When "010" → 10-7-10 Type When "011" → 10-8-10 Type When "100" → 12-6-12 Type When "101" → 12-7-12 Type When "110" → 12-8-12 Type When "111" → Reserved Bit[4:3] Selects Type of Prediction When "00" → Not allowed(Reserved) When "01" → Prediction-1 When "10" → Prediction-2 When "11" → Not allowed(Reserved)

[9:5]	CMPRS_SCHM_FR_USD_TYPE1	R/W	RO	To be configured by processor as per the requirement. The [7:5] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[9:8] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11” → Not allowed(Reserved)
[19:15]	CMPRS_SCHM_FR_USD_TYPE3	R/W	RO	To be configured by processor as per the requirement. The [17:15] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[19:18] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11”→ Not allowed(Reserved)
[24:20]	CMPRS_SCHM_FR_USD_TYPE4	R/W	RO	To be configured by processor as per the requirement. The [22:20] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[24:23] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11”→ Not allowed(Reserved)

[29:25]	CMPRS_SCHM_FR_USD_TYPE5	R/W	RO	To be configured by processor as per the requirement. The [27:25] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[29:28] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11”→ Not allowed(Reserved)
[31:30]	RSVD	NA	NA	Reserved

4.10 VC0 Compression/Prediction Scheme Register-2

Register Name	VC0 Compression/Prediction Scheme Register-2
Address	0x0050H
Default Value	0x0000_0000H

Bit Value Mapping															
[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Field	Access		Description
		S/W	H/W	

[4:0]	CMPRS_SCHM_FR_USD_TYPE6	R/W	RO	To be configured by processor as per the requirement. The [2:0] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[4:3] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When “11” → Not allowed(Reserved)
[9:5]	CMPRS_SCHM_FR_USD_TYPE7	R/W	RO	To be configured by processor as per the requirement. The [7:5] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[9:8] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11” → Not allowed(Reserved)
[31:10]	RSVD	NA	NA	Reserved

4.11 VC1 Compression/Prediction Scheme Register-1

Register Name	VC1 Compression/Prediction Scheme Register-1
Address	0x0054H
Default Value	0x0000_0000H

Bit Value Mapping															
[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Field	Access		Description
		S/W	H/W	
[4:0]	CMPRS_SCHM_FR_USD_TYPE0	R/W	RO	To be configured by processor as per the requirement. The [2:0] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[4:3] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When “11” → Not allowed(Reserved)
[9:5]	CMPRS_SCHM_FR_USD_TYPE1	R/W	RO	To be configured by processor as per the requirement. The [7:5] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[9:8] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11” → Not allowed(Reserved)

[19:15]	CMPRS_SCHM_FR_USD_TYPE3	R/W	RO	To be configured by processor as per the requirement. The [17:15] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[19:18] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11”→ Not allowed(Reserved)
[24:20]	CMPRS_SCHM_FR_USD_TYPE4	R/W	RO	To be configured by processor as per the requirement. The [22:20] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[24:23] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11”→ Not allowed(Reserved)
[29:25]	CMPRS_SCHM_FR_USD_TYPE5	R/W	RO	To be configured by processor as per the requirement. The [27:25] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[29:28] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11”→ Not allowed(Reserved)

[31:30]	RSVD	NA	NA	Reserved

4.12 VC1 Compression/Prediction Scheme Register-2

Register Name	VC1 Compression/Prediction Scheme Register-2
Address	0x0058H
Default Value	0x0000_0000H

Bit Value Mapping															
[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Field	Access		Description
		S/W	H/W	
[4:0]	CMPRS_SCHM_FR_USD_TYPE6	R/W	RO	To be configured by processor as per the requirement. The [2:0] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[4:3] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When “11” → Not allowed(Reserved)

[9:5]	CMPRS_SCHM_FR_USD_TYPE7	R/W	RO	To be configured by processor as per the requirement. The [7:5] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[9:8] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11” → Not allowed(Reserved)
[31:10]	RSVD	NA	NA	Reserved

4.13 VC2 Compression/Prediction Scheme Register-1

Register Name	VC2 Compression/Prediction Scheme Register-1
Address	0x005CH
Default Value	0x0000_0000H

Bit Value Mapping															
[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Field	Access		Description
		S/W	H/W	

[4:0]	CMPRS_SCHM_FR_USD_TYPE0	R/W	RO	To be configured by processor as per the requirement. The [2:0] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[4:3] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When “11” → Not allowed(Reserved)
[9:5]	CMPRS_SCHM_FR_USD_TYPE1	R/W	RO	To be configured by processor as per the requirement. The [7:5] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[9:8] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11” → Not allowed(Reserved)
[19:15]	CMPRS_SCHM_FR_USD_TYPE3	R/W	RO	To be configured by processor as per the requirement. The [17:15] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[19:18] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11”→ Not allowed(Reserved)

[24:20]	CMPRS_SCHM_FR_USD_TYPE4	R/W	RO	To be configured by processor as per the requirement. The [22:20] bits select the type of compression When "000" → No Compression When "001" → 10-6-10 Type When "010" → 10-7-10 Type When "011" → 10-8-10 Type When "100" → 12-6-12 Type When "101" → 12-7-12 Type When "110" → 12-8-12 Type When "111" → Reserved Bit[24:23] Selects Type of Prediction When "00" → Not allowed(Reserved) When "01" → Prediction-1 When "10" → Prediction-2 When"11"→ Not allowed(Reserved)
[29:25]	CMPRS_SCHM_FR_USD_TYPE5	R/W	RO	To be configured by processor as per the requirement. The [27:25] bits select the type of compression When "000" → No Compression When "001" → 10-6-10 Type When "010" → 10-7-10 Type When "011" → 10-8-10 Type When "100" → 12-6-12 Type When "101" → 12-7-12 Type When "110" → 12-8-12 Type When "111" → Reserved Bit[29:28] Selects Type of Prediction When "00" → Not allowed(Reserved) When "01" → Prediction-1 When "10" → Prediction-2 When"11"→ Not allowed(Reserved)
[31:30]	RSVD	NA	NA	Reserved

4.14 VC2 Compression/Prediction Scheme Register-2

Register Name	VC2 Compression/Prediction Scheme Register-2
Address	0x0060H
Default Value	0x0000_0000H

Bit Value Mapping															
[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Field	Access		Description
		S/W	H/W	
[4:0]	CMPRS_SCHM_FR_USD_TYPE6	R/W	RO	To be configured by processor as per the requirement. The [2:0] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[4:3] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When “11” → Not allowed(Reserved)
[9:5]	CMPRS_SCHM_FR_USD_TYPE7	R/W	RO	To be configured by processor as per the requirement. The [7:5] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[9:8] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11” → Not allowed(Reserved)
[31:10]	RSVD	NA	NA	Reserved

4.15 VC3 Compression/Prediction Scheme Register-1

Register Name	VC3 Compression/Prediction Scheme Register-1
Address	0x0064H
Default Value	0x0000_0000H

Bit Value Mapping															
[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Field	Access		Description
		S/W	H/W	
[4:0]	CMPRS_SCHM_FR_USD_TYPE0	R/W	RO	To be configured by processor as per the requirement. The [2:0] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[4:3] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When “11” → Not allowed(Reserved)
[9:5]	CMPRS_SCHM_FR_USD_TYPE1	R/W	RO	To be configured by processor as per the requirement. The [7:5] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[9:8] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11” → Not allowed(Reserved)

[19:15]	CMPRS_SCHM_FR_USD_TYPE3	R/W	RO	To be configured by processor as per the requirement. The [17:15] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[19:18] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11”→ Not allowed(Reserved)
[24:20]	CMPRS_SCHM_FR_USD_TYPE4	R/W	RO	To be configured by processor as per the requirement. The [22:20] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[24:23] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11”→ Not allowed(Reserved)
[29:25]	CMPRS_SCHM_FR_USD_TYPE5	R/W	RO	To be configured by processor as per the requirement. The [27:25] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[29:28] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11”→ Not allowed(Reserved)

[31:30]	RSVD	NA	NA	Reserved

4.16 VC3 Compression/Prediction Scheme Register-2

Register Name	VC3 Compression/Prediction Scheme Register-2
Address	0x0068H
Default Value	0x0000_0000H

Bit Value Mapping															
[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Field	Access		Description
		S/W	H/W	
[4:0]	CMPRS_SCHM_FR_USD_TYPE6	R/W	RO	To be configured by processor as per the requirement. The [2:0] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[4:3] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When “11” → Not allowed(Reserved)

[9:5]	CMPRS_SCHM_FR_USD_TYPE7	R/W	RO	To be configured by processor as per the requirement. The [7:5] bits select the type of compression When “000” → No Compression When “001” → 10-6-10 Type When “010” → 10-7-10 Type When “011” → 10-8-10 Type When “100” → 12-6-12 Type When “101” → 12-7-12 Type When “110” → 12-8-12 Type When “111” → Reserved Bit[9:8] Selects Type of Prediction When “00” → Not allowed(Reserved) When “01” → Prediction-1 When “10” → Prediction-2 When“11” → Not allowed(Reserved)
[31:10]	RSVD	NA	NA	Reserved

4.17 PLL Count Register

Register Name	PLL Count Register
Address	0x006CH
Default Value	0x0000_4E20H

Bit Value Mapping															
[15]	[14]	[13]	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	[00]
0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0
[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Field	Access		Description
		S/W	H/W	
[15:0]	PLL_CNT	R/W	RO	Programmed by the processor. Default time period is set for 1ms. This is set in terms of txbyteclkhs
[31:16]	RSVD	NA	NA	Reserved

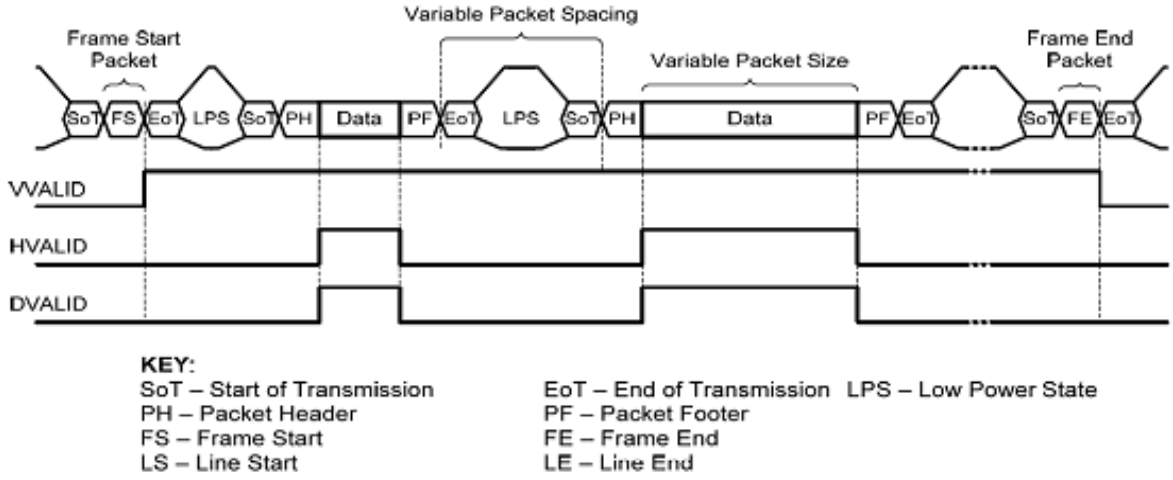
5 Protocol

5.1 Packet Transmission

5.1.1 User Defined Data

The user defined data type values shall be used to transmit arbitrary byte-based data such as JPEG and MPEG data over the CSI-2 bus. A typical frame is shown below.

Figure 6 Packet Transmission



5.2 DPHY Power up Sequence

After Power-up, the transmitter shall observe an initialization period, TINIT, during which it shall drive a TX-Stop state (LP-11) on all lanes.

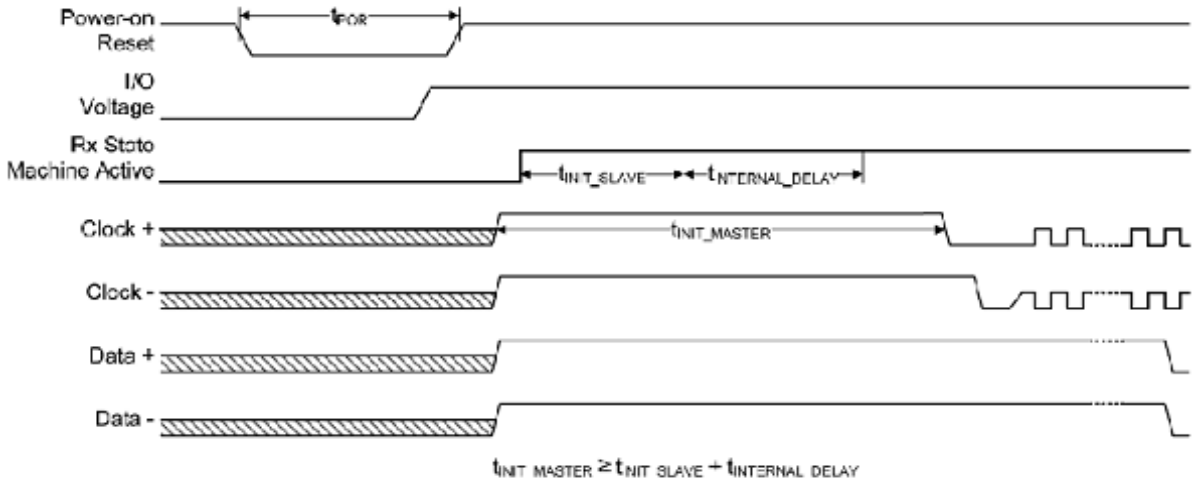
The Receiver shall power up in the Stop state and monitor the lines to determine if the transmitter has asserted Stop state for at least the TINIT period.

The Receiver shall ignore all line states prior to detection of a TINIT event. The Receiver shall be ready to accept us transactions immediately following the end of the TINIT period.

In the following figure, power-on-reset mechanism is assumed for initialization. Here, T_{INIT_SLAVE} represents the minimum initialization period specified in MIPI D-PHY Specification.ie.100 us. The receiver may need some time to reach a functional state after power-up. This time is represented in the following figure as $T_{INTERNAL\_DELAY}$.

The period of T_{INIT_MASTER} is selected as greater than or equal to 1ms to suit for any high level protocol like CSI.

Figure 7 DPHY Power Up Sequence



5.3 ULPS Entry and Exit

ULPS mode is the power saving state and it should occur only when there is no data to transfer. The entry and exit of ULPS can be controlled in the following manner,

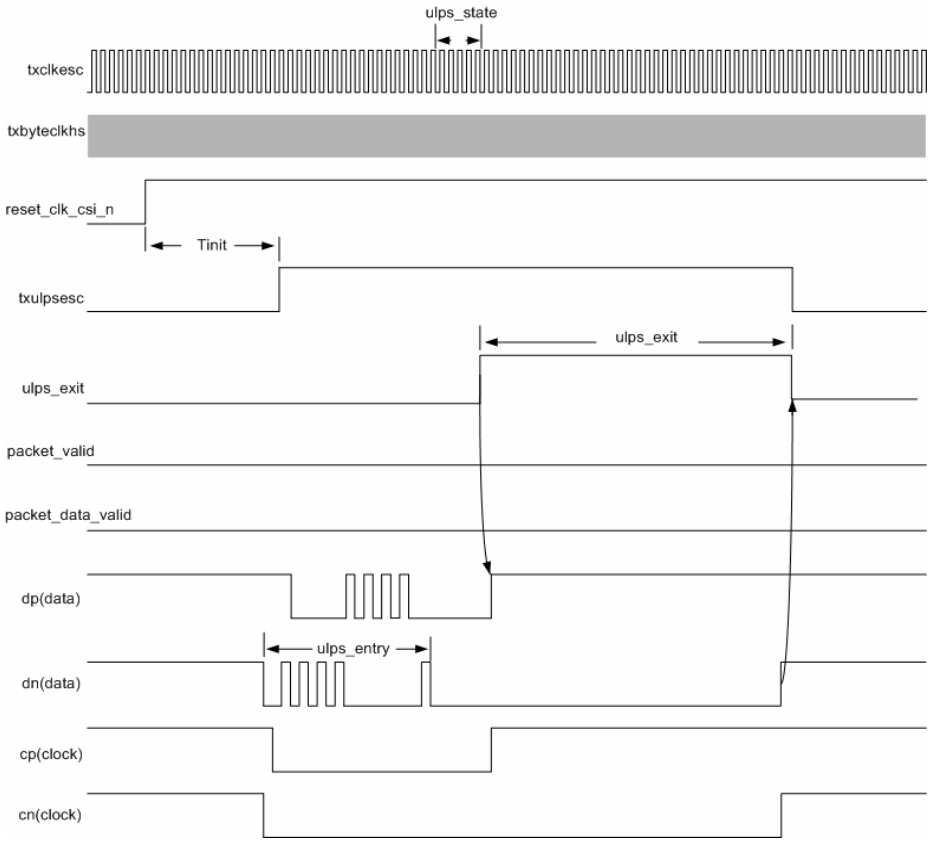
Initially, both the TxulpsEsc and TxulpsExit signals are low. It indicates the D-PHY is in normal mode.

- To enter into ULPS mode, TxulpsEsc signal is asserted as high. It dictates the CSI controller to generate the control signals for the D-PHY to enter into ULPS mode.
- To exit from ULPS mode, both the TxulpsEsc and TxulpsExit signals are driven as high for a minimum time period of TWAKEUP

After exiting from ULPS mode, both the TxulpsEsc and TxulpsExit signals are driven low.

ULPS entry and exit flow is illustrated in the following figure,

Figure 8 ULPS Entry and Exit



5.4 Clock Mode

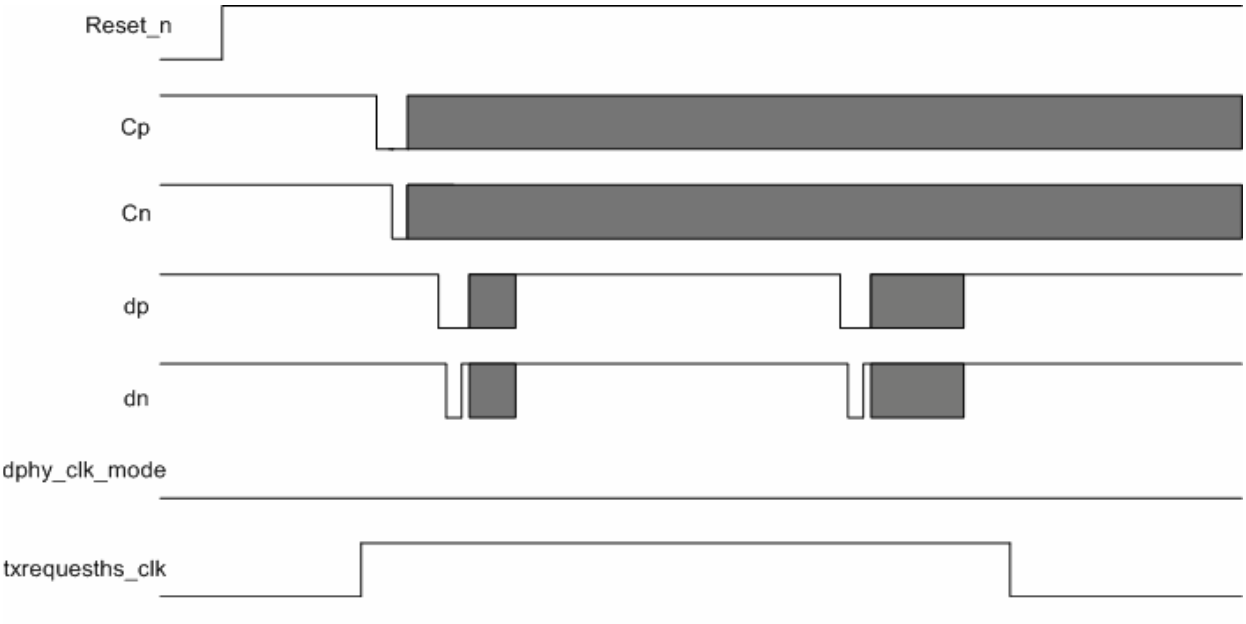
There are two options available to handle clocking scheme in D-PHY. Which are controlled by “dphy_clk_mode” in CSI2-Tx. They are listed below

1. Continuous Clock
2. Non-continuous Clock

5.4.1 Continuous Clock

In this mode, the bit (TxDDRClkHS) and byte (TxByteClkHS and RxByteClkHS) clocks are generated from D-PHY as a continuous signal. There is no need to de-assert the clock request signal from CSI Controller in between packet transmissions. The following figure illustrates the behavior of this mode for two consecutive packets.

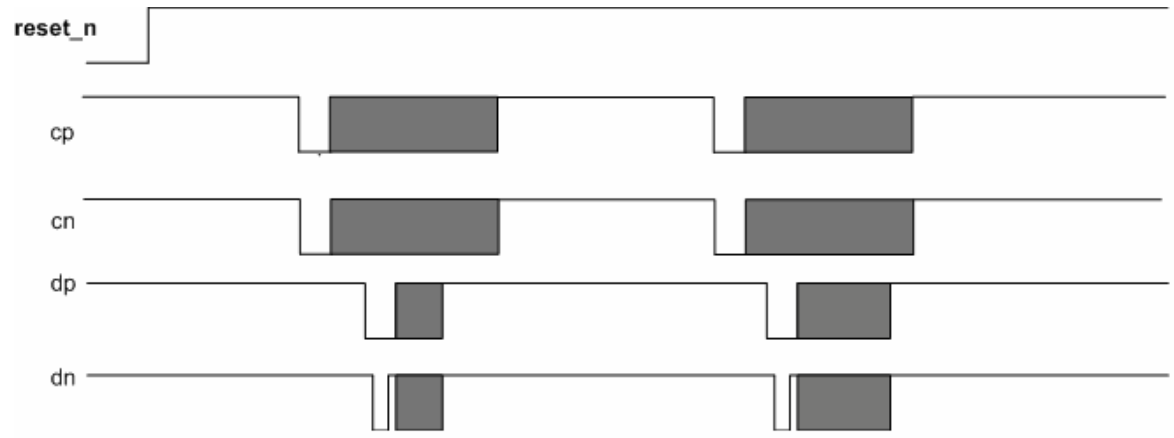
Figure 9: Continuous clock mode



5.4.2 Non-continuous Clock

In this mode, the bit (TxDDRClkHS) and byte (TxByteClkHS and RxByteClkHS) clocks are generated from D-PHY as a non-continuous signal. CSI Controller should assert and de-assert clock request signal for each and every packet transmission. The following figure illustrates the behavior of this mode.

Figure 10: Non-continuous clock mode



5.5 FIFO Utilization

The below table lists the FIFO utilization in IP

Table 4 : FIFO Utilization

Serial #	Size		Description
	Width	Depth	
1	64	8192	Asynchronous FIFO. This is a library specific RAM and instantiated outside the CSI-2 Transmitter core. The Depth of this FIFO is provided as compile time attribute so that the user can configure this as per the requirement
2	32	8	This is register based FIFO, resides with in the CSI-2 transmitter core.

5.6 Compile Time Attributes

The following compile time attribute is used to fix the size of the sensor FIFO. The sensor FIFO is a library specific memory. The size of the sensor FIFO can be adjusted as per the user application. The minimum depth of the sensor FIFO could be as low as 16 in deep. The compile time attribute is provided in the file csi2tx_defines.v

For store and forward mechanism the size of the FIFO should be two times the max line size required in the application.

Attribute Name	Description
SENSOR_FIFO_ADDR_WIDTH	This defines the width of the address bus and the depth of the FIFO will be 2 ** SENSOR_FIFO_ADDR_WIDTH. For example : If BIG_FIFO_ADDR_WIDTH = 4, the depth of the FIFO will be 16

5.7 Pixel Mapping from Sensor Interface

The CSI-2 transmitter IP provides a 32-bit data bus interface to external sensor. However, based on the pixel that is getting received, only few of the bits in the data bus is valid. This pixel mapping will vary based on the data type. The following section descries the pixel mapping for the supported data types.

5.7.1 YUV Pixel Formats

5.7.1.1 LEGACY YUV 420 8-bit

Table 5: Mapping with respect to pixel data of camera sensor BFM

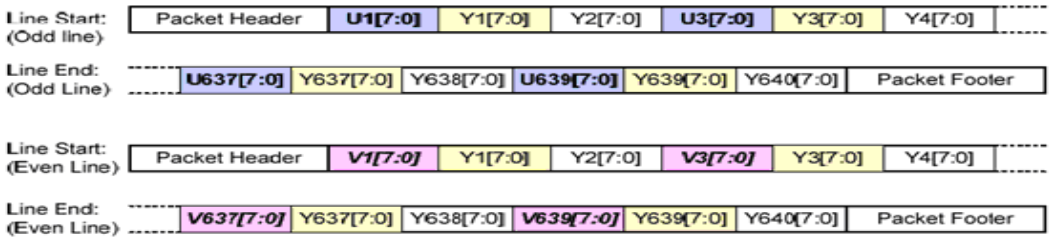
Color Component	No of Bits	Pixel Data
V	8	[7:0]
U	8	[17:10]
Y	8	[27:20]

Packing for even and odd lines: Legacy YUV 420 8-bit data transmission is performed by transmitting UYY.../VYY... sequence in odd/even lines. U component is transferred in odd lines (1, 3, 5…) and V component is transferred in even lines (2,4,6,..).
For example, U1Y1Y2, U3Y3Y4... will be transmitted in the odd lines and V1Y1Y2; V3Y3Y4... will be transmitted in the even lines

Table 6: Packing for even and odd lines

Line	Pixel	Bytes	Packing
Odd	2	3	Y and U components are transmitted from odd pixel Only Y component is transmitted from even pixel Odd Pixel - U and Y (Pixel Data[27:20], Pixel Data[17:10]) Even Pixel - Y(Pixel Data[27:20])
Even	2	3	Y and V components are transmitted from odd pixel Only Y component is transmitted from even pixel Odd Pixel - V and Y (Pixel Data[27:20], Pixel Data[7:0]) Even Pixel - Y(Pixel Data[27:20])

Packet format: Below diagram shows the packetisation of the color components done in the CSI Transmitter



5.7.1.2 YUV 420 8-bit

Table 7: Mapping with respect to pixel data of camera sensor BFM

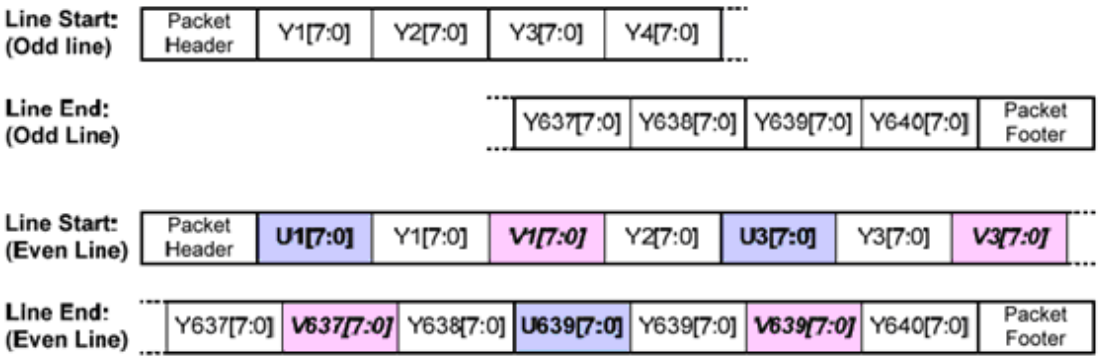
Color Component	No of Bits	Pixel Data
V	8	[7:0]
U	8	[17:10]
Y	8	[27:20]

Packing for even and odd lines: YUV 420 8-bit data transmission is performed by transmitting YYYY.../YVYUYVY... sequence in odd/even lines. Only luminance component(Y) is transferred in odd lines (1, 3, 5,..) and both luminance(Y) and chrominance component (U and V) is transferred in even lines (2, 4, 6,..)
For example, Y1Y2Y3Y4... will be transmitted in the odd lines and U1Y1V1Y2, U3Y3V3Y4... will be transmitted in the even lines

Table 8: Packing for even and odd lines

Line	Pixel	Bytes	Packing
Odd	2	2	Only Y component is transmitted from odd and even pixel Odd Pixel - Y (Pixel Data[27:20]) Even Pixel - Y(Pixel Data[27:20])
Even	2	4	Y, U and V components are transmitted from odd pixel Only Y component is transmitted from even pixel Odd Pixel - U, V and Y Component (Pixel Data[7:0], Pixel Data[27:20], Pixel Data[17:10]) Even Pixel - Y Component (Pixel Data[27:20])

Packet format: Below diagram shows the packetisation of the color components done in the CSI Transmitter



5.7.1.3 YUV 420 10-bit

Table 9: Mapping with respect to pixel data of camera sensor BFM

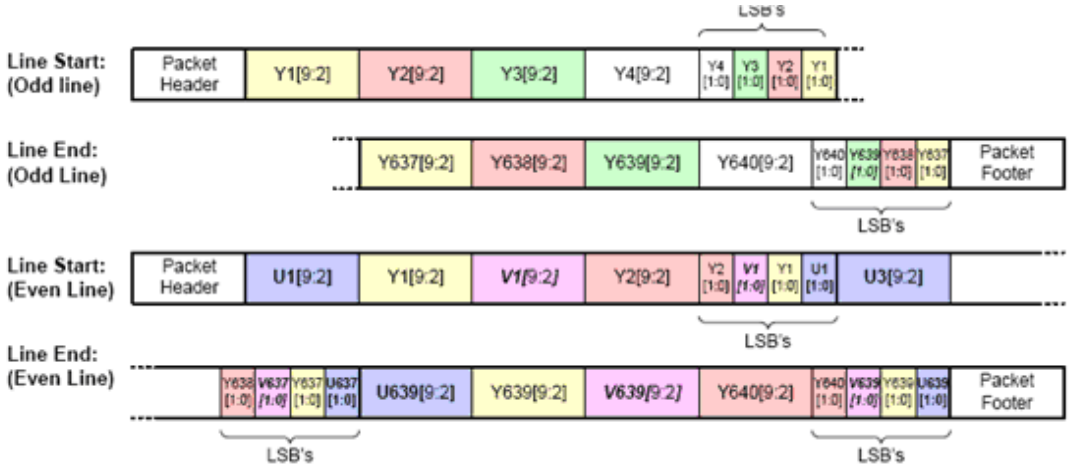
Color Component	No of Bits	Pixel Data
V	10	[9:0]
U	10	[19:10]
Y	10	[29:20]

Packing for even and odd lines: YUV 420 10-bit data transmission is performed by transmitting YYYY.../UYVYUYVY... sequence in odd/even lines. Only luminance component(Y) is transferred in odd lines (1,3,5,..) and both luminance(Y) and chrominance component (U and V) is transferred in even lines(2,4,6,..)
For example, Y1Y2Y3Y4... will be transmitted in the odd lines and U1Y1V1Y2, U3Y3V3Y4... will be transmitted in the even lines

Table 10: Packing for even and odd lines

Line	Pixel	Bytes	Packing
Odd	4	5	Only Y component is transmitted from odd and even pixel Odd Pixel - Y (Pixel Data[23:16]) Even Pixel - Y(Pixel Data[23:16])
Even	4	10	Y, U and V components are transmitted from odd pixel Only Y component is transmitted from even pixel Odd Pixel - U, V and Y Component (Pixel Data[9:0], Pixel Data[29:20], Pixel Data[19:10]) Even Pixel - Y Component (Pixel Data[29:20])

Packet format: Below diagram shows the packetisation of the color components done in the CSI Transmitter



5.7.1.4 YUV 422 8-bit

Table 11: Mapping with respect to pixel data of camera sensor BFM

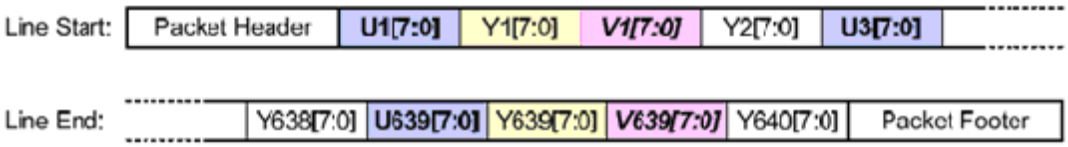
Color Component	No of Bits	Pixel Data
V	8	[7:0]
U	8	[17:10]
Y	8	[27:20]

Packing for even and odd lines: YUV 422 8-bit data transmission is performed by transmitting UYVY... sequence. For example, U1Y1V1Y2, U3Y3V3Y4... will be transmitted in the odd lines and even lines

Table 12: Packing for even and odd lines

Line	Pixel	Bytes	Packing
Odd	2	4	Y, U and V component are transmitted from odd pixel. Only Y component is transmitted from even pixel. Odd Pixel - Y , U and V (Pixel Data[7:0], Pixel Data[17:10], Pixel Data[27:20]) Even Pixel - Y(Pixel Data[27:20])

Packet format: Below diagram shows the packetisation of the color components done in the CSI Transmitter



5.7.1.5 YUV 422 10-bit

Table 13: Mapping with respect to pixel data of camera sensor BFM

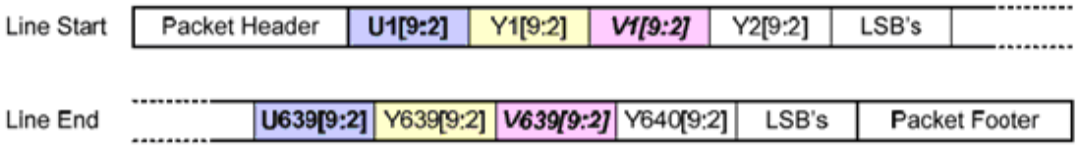
Color Component	No of Bits	Pixel Data
V	10	[9:0]
U	10	[19:10]
Y	10	[29:20]

Packing for even and odd lines: YUV 422 10-bit data transmission is performed by transmitting UYVY... sequence. For example, U1Y1V1Y2, U3Y3V3Y4... will be transmitted in the odd lines and even lines

Table 14: Packing for even and odd lines

Line	Pixel	Bytes	Packing
Odd	2	5	Y, U and V component are transmitted from odd pixel Only Y component is transmitted from even pixel Odd Pixel - Y , U and V Pixel Data[9:0], Pixel Data[19:10], Pixel Data[29:20 Even Pixel - Y Pixel Data[29:20]

Packet format: Below diagram shows the packetisation of the color components done in the CSI Transmitter



5.7.2 RGB Pixel Formats

5.7.2.1 RGB888

Table 15: Mapping with respect to pixel data of camera sensor BFM

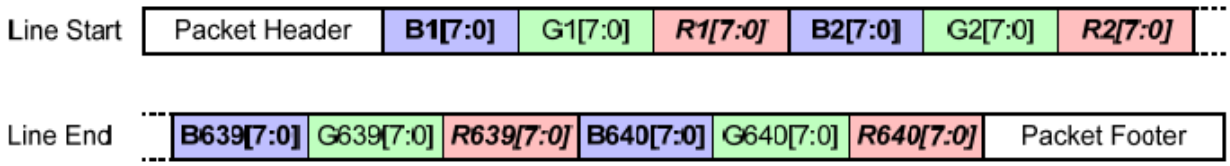
Color Component	No of Bits	Pixel Data
B	8	[7:0]
G	8	[15:8]
R	8	[23:16]

Packing: RGB888 data transmission is performed by transmitting B1G1R1.... sequence. For example, R1G1B1, R2G2B2... will be transmitted as B1G1R1, B2G2R2.

Table 16: Packing of RGB888

Pixel	Bytes	Packing
1	3	R G and B components are transmitted in each pixel Pixel - R G and B (Pixel Data[23:16], Pixel Data[15:8] and Pixel Data[7:0])

Packet format: Below diagram shows the packetisation of the color components done in the CSI Transmitter



5.7.2.2 RGB666

Table 17: Mapping with respect to pixel data of camera sensor BFM

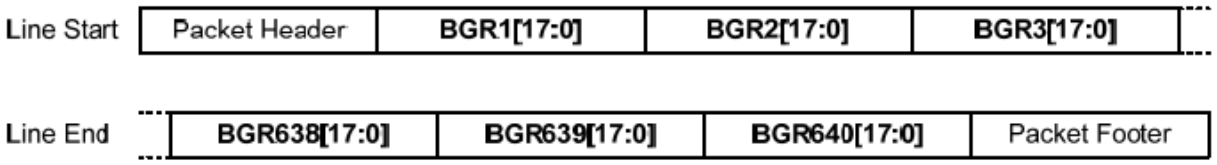
Color Component	No of Bits	Pixel Data
B	6	[5:0]
G	6	[11:6]
R	6	[17:12]

Packing: RGB666 data transmission is performed by transmitting B1G1R1.... sequence. For example, R1G1B1, R2G2B2... will be transmitted as B1G1R1, B2G2R2.

Table 18: Packing of RGB666

Pixel	Bytes	Packing
4	9	R G and B components are transmitted in each pixel Pixel - R G and B (Pixel Data[17:12], Pixel Data[11:6] and Pixel Data[5:0])

Packet format: Below diagram shows the packetisation of the color components done in the CSI Transmitter



5.7.2.3 RGB565

Table 19: Mapping with respect to pixel data of camera sensor BFM

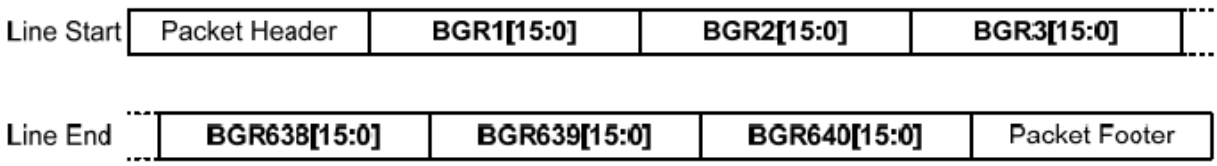
Color Component	No of Bits	Pixel Data
B	5	[4:0]
G	6	[10:5]
R	5	[15:11]

Packing: RGB565 data transmission is performed by transmitting B1G1R1.... sequence. For example, R1G1B1, R2G2B2... will be transmitted as B1G1R1, B2G2R2.

Table 20: Packing of RGB565

Pixel	Bytes	Packing
1	2	R G and B components are transmitted in each pixel Pixel - R G and B (Pixel Data[15:11], Pixel Data[10:5] and Pixel Data[4:0])

Packet format: Below diagram shows the packetisation of the color components done in the CSI Transmitter



5.7.2.4 RGB555

Table 21: Mapping with respect to pixel data of camera sensor BFM

Color Component	No of Bits	Pixel Data
B	5	[4:0]
G	5	[9:5]
R	5	[14:10]

Packing: RGB555 data transmission is performed by transmitting B1G1R1.... sequence. For example, R1G1B1, R2G2B2... will be transmitted as B1G1R1, B2G2R2.

Table 22: Packing of RGB555

Pixel	Bytes	Packing
1	2	R G and B components are transmitted in each pixel Pixel - R G and B {Pixel Data[14:10], Pixel Data[9:5],1'b0,Pixel Data[4:0]}

5.7.2.5 RGB444

Table 23: Mapping with respect to pixel data of camera sensor BFM

Color Component	No of Bits	Pixel Data
B	4	[3:0]
G	4	[7:4]
R	4	[11:8]

Packing: RGB444 data transmission is performed by transmitting B1G1R1.... sequence. For example, R1G1B1, R2G2B2... will be transmitted as B1G1R1, B2G2R2.

Table 24: Packing of RGB444

Pixel	Bytes	Packing
1	2	R G and B components are transmitted in each pixel Pixel - R G and B {Pixel Data[11:8],1'b1,Pixel Data[7:4],2'b10,Pixel Data[3:0],1'b1}

5.7.3 RAW Pixel Formats

5.7.3.1 RAW6

Table 25: Mapping with respect to pixel data of camera sensor BFM

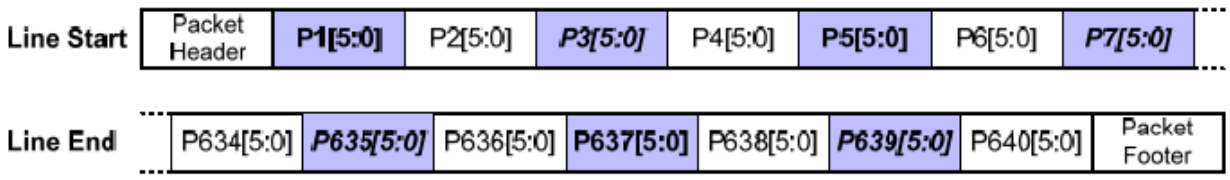
Pixel Component	No of Bits	Pixel Data
P	6	[5:0]

Packing: RAW6 data transmission is performed by transmitting pixel data.

Table 26: Packing of RAW6

Pixel	Bytes	Packing
4	3	Pixel component is transmitted in each pixel Pixel - (Pixel Data[5:0])

Packet format: Below diagram shows the packetisation of the color components done in the CSI Transmitter



5.7.3.2 RAW7

Table 27: Mapping with respect to pixel data of camera sensor BFM

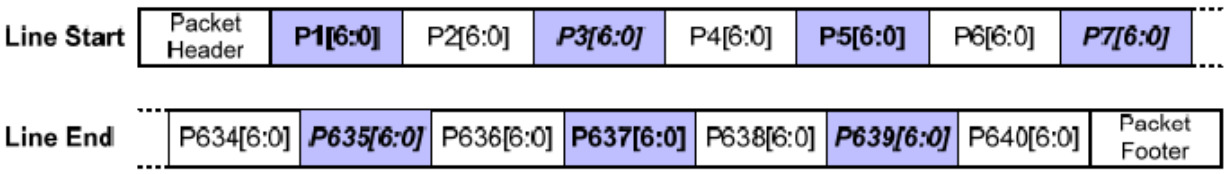
Pixel Component	No of Bits	Pixel Data
P	7	[6:0]

Packing: RAW7 data transmission is performed by transmitting pixel data.

Table 28: Packing of RAW7

Pixel	Bytes	Packing
8	7	Pixel component is transmitted in each pixel Pixel - (Pixel Data[6:0])

Packet format: Below diagram shows the packetisation of the color components done in the CSI Transmitter



5.7.3.3 RAW8

Table 29: Mapping with respect to pixel data of camera sensor BFM

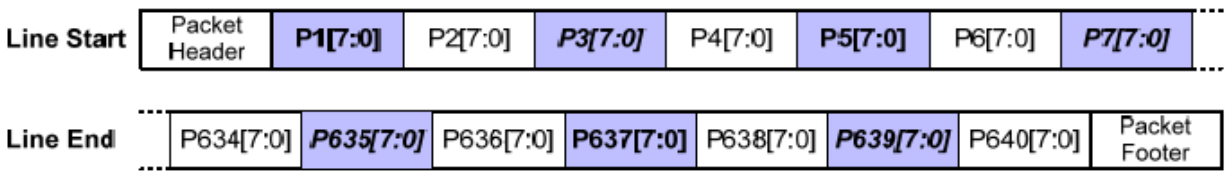
Pixel Component	No of Bits	Pixel Data
P	8	[7:0]

Packing: RAW8 data transmission is performed by transmitting pixel data.

Table 30: Packing of RAW8

Pixel	Byte	Packing
1	1	Pixel component is transmitted in each pixel Pixel - (Pixel Data[7:0])

Packet format: Below diagram shows the packetisation of the color components done in the CSI Transmitter



5.7.3.4 RAW10

Table 31: Mapping with respect to pixel data of camera sensor BFM

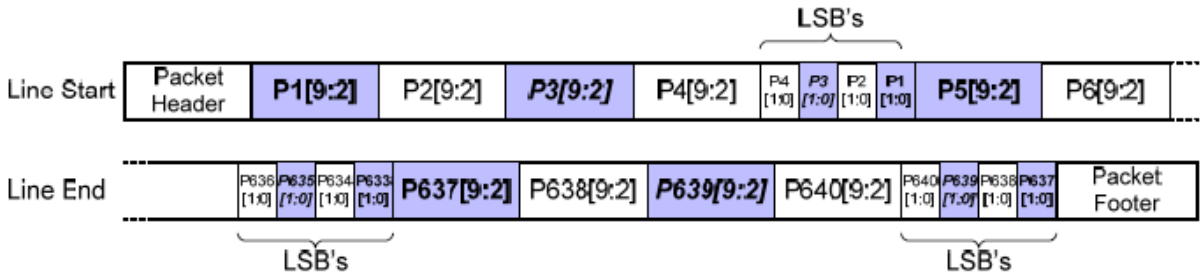
Pixel Component	No of Bits	Pixel Data
P	10	[9:0]

Packing: RAW10 data transmission is performed by transmitting pixel data.

Table 32: Packing of RAW10

Pixels	Bytes	Packing
4	5	Pixel component is transmitted in each pixel Pixel - (Pixel Data[9:0])

Packet format: Below diagram shows the packetisation of the color components done in the CSI Transmitter



5.7.3.5 RAW12

Table 33: Mapping with respect to pixel data of camera sensor BFM

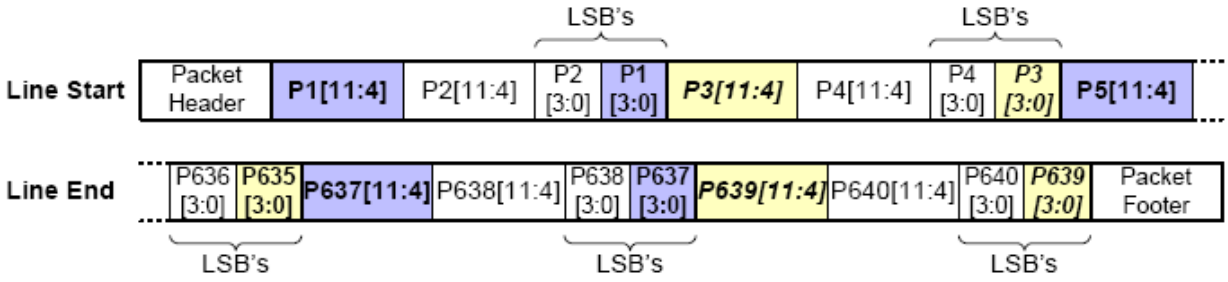
Pixel Component	No of Bits	Pixel Data
P	12	[11:0]

Packing: RAW12 data transmission is performed by transmitting pixel data

Table 34 Packing of RAW12

Pixels	Bytes	Packing
2	3	Pixel component is transmitted in each pixel Pixel - (Pixel Data[11:0])

Packet format: Below diagram shows the packetisation of the color components done in the CSI Transmitter



5.7.3.6 RAW14

Table 35: Mapping with respect to pixel data of camera sensor BFM

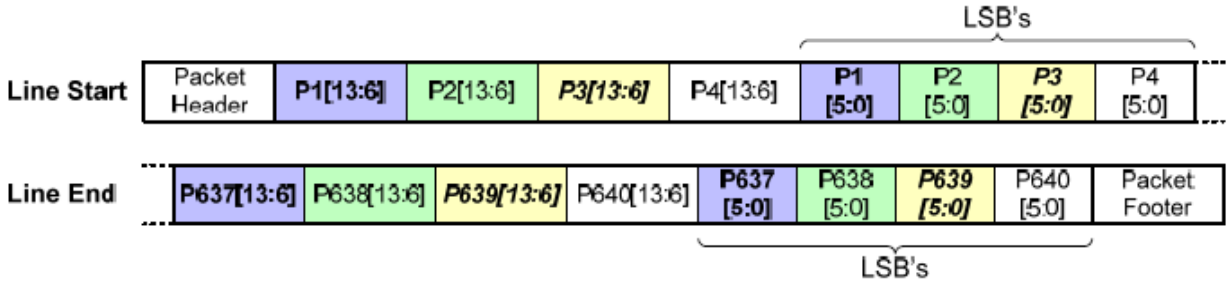
Pixel Component	No of Bits	Pixel Data
P	14	[13:0]

Packing: RAW14 data transmission is performed by transmitting pixel data

Table 36: Packing of RAW14

Pixels	Bytes	Packing
4	7	Pixel component is transmitted in each pixel Pixel - (Pixel Data[13:0])

Packet format: Below diagram shows the packetisation of the color components done in the CSI Transmitter



5.7.4 User Defined Pixel Formats

5.7.4.1 USD Type 1

Table 37: Mapping with respect to pixel data of camera sensor BFM

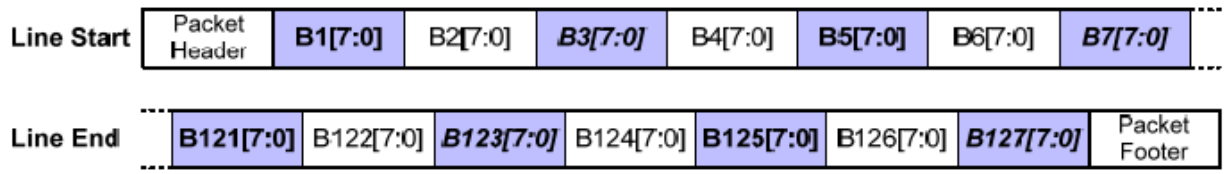
Pixel Component	No of Bits	Pixel Data
P	8	[7:0]

Packing: USD Type 1 data transmission is performed by transmitting pixel data

Table 38: Packing of USD Type 1

Pixels	Bytes	Packing
1	1	Pixel component is transmitted in each pixel Pixel - (Pixel Data[7:0])

Packet format: Below diagram shows the packetisation of the color components done in the CSI Transmitter



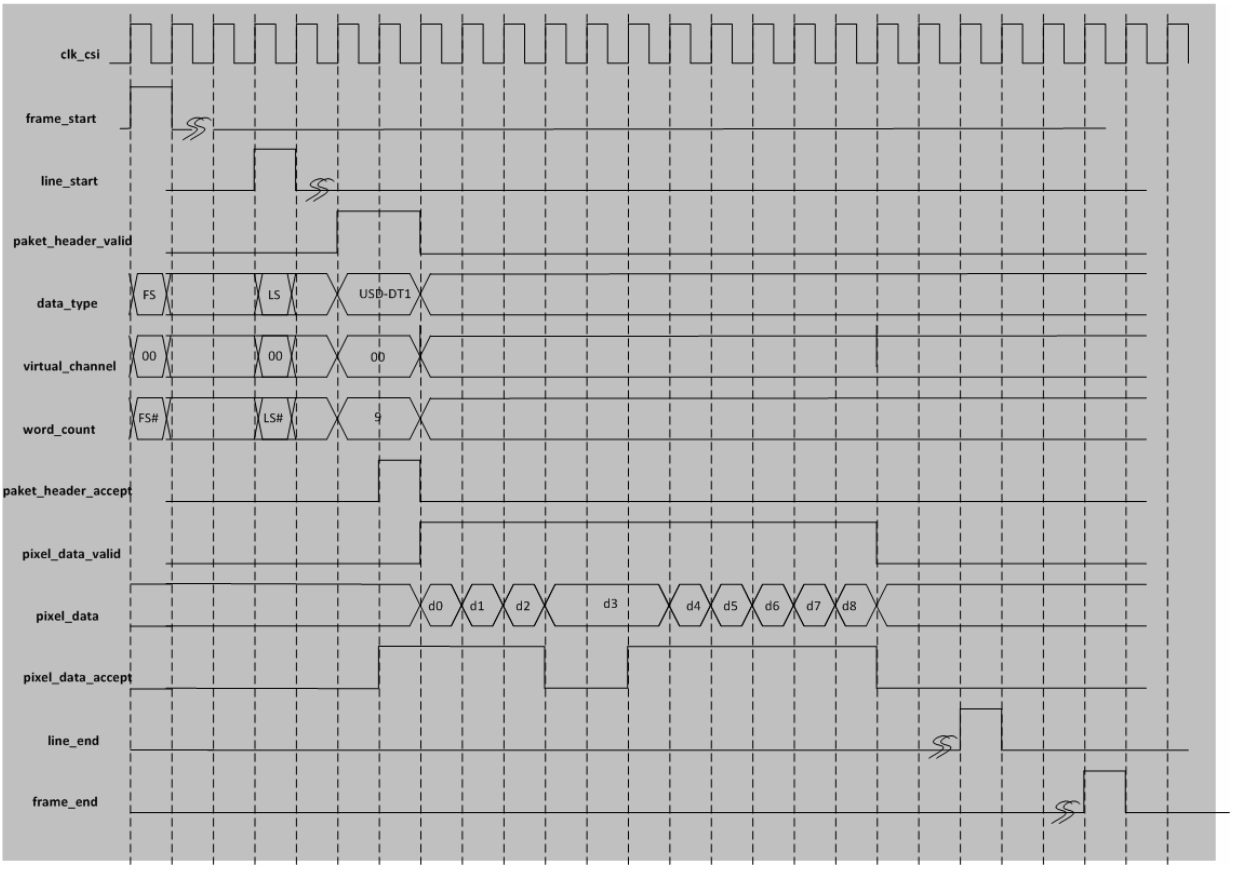
NOTE: *Same pattern holds good for User Defined Data Type 2 to User Defined Data Type 8*

6 Timing

6.1 Image acquisition (Image Sensor Interface)

The waveform below represents the sensor interface

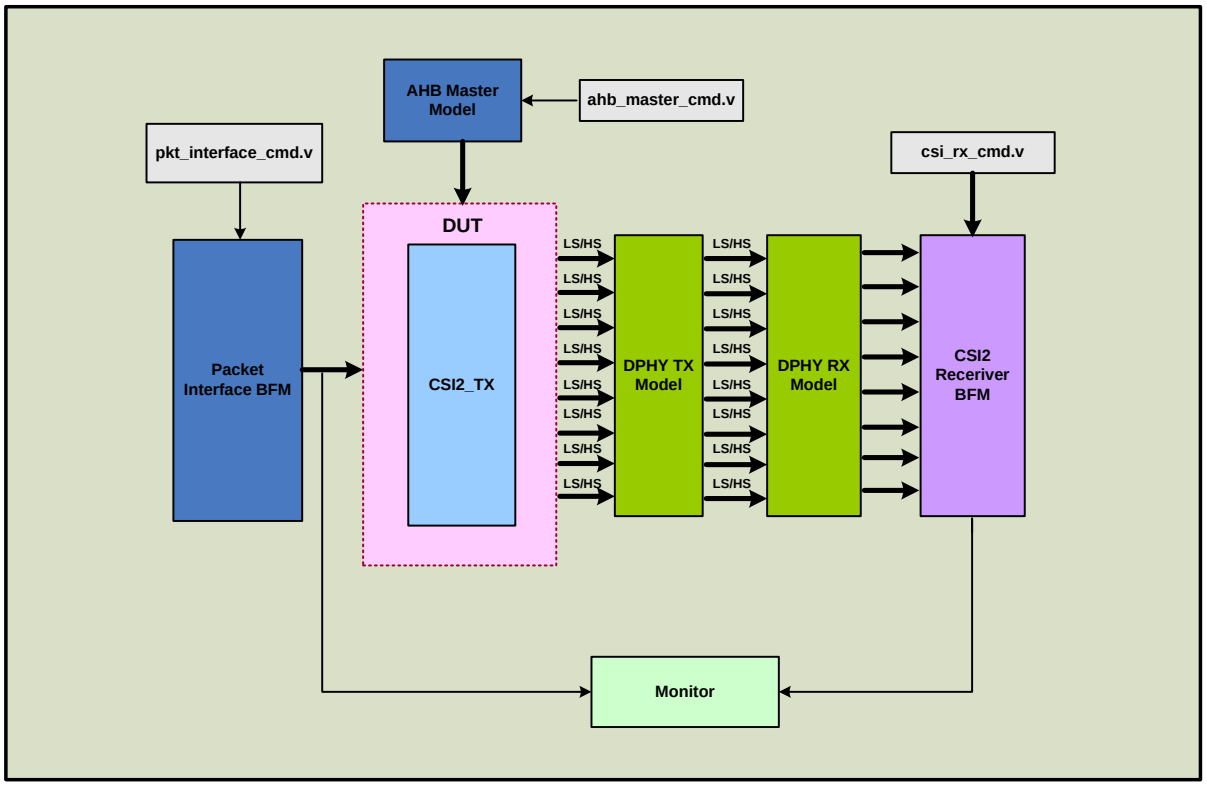
Figure 11: Sensor Interface Timing Diagram



7 Verification

The CSI-2 Transmitter IP has been verified in the simulation environment using the behavioral model of the surrounding component. The verification environment is shown in the Figure

Figure 12: CSI-2 Transmitter IP Test Environment



7.1.1 AHB Master Model

Functionality of the AHB Master model is described below:

- AHB Master Model interacts with the CSI core and Tx BFM.
- AHB Master model handles the interrupt service routines for the generated interrupts from the CSI receiver
- AHB Master model configuration can be done in to modes:
  A. Default Mode (Configures the Operational registers with default values specified in the user guide)

B. User Config Mode (Configures the Operational registers values as per the values specified in the ahb_master_cmd.v)

- The process is started by the master asserting a request (hbusreq) signal to the arbiter. Then arbiter indicates when the master will be granted to use the bus.
- A granted bus master starts an AHB transfer by driving the address and control signals.
- These signals provide information on the address, direction and width of the transfer, as well as an indication if the transfer forms part of a burst (single transfer).
- AHB Master Model supports burst transfer – single transfer
- AHB Master Model supports one master and one slave
- AHB Master Model data transfer size 8 / 16 / 32 bits

7.1.2 Packet Interface BFM

Functionality of the Packet Interface BFM model is described below:

- This module is used for sending the payload data based on color formats defined by the user.
- The pixel elements are transmitted to the CSI-2 transmitter as per the command file in the verification environment(pkt_interface_cmd.v)
- Interacts with CSI-2TX transmitter block and transmits the pixel level information, following standard CSI-2 specification
- Transmits short and long packets including generic data type
- Data byte count can be randomized.
- Interacts with CSI-2 monitor and transmits pixel level data.

7.1.3 D-PHY Transceiver Model

Functionality of the D-PHY transceiver model is described below:

- The D-PHY Transmitter and Receiver model emulates the functionality of a D-PHY transceiver.
- Derives differential signaling on high speed lanes from high speed clock or high speed data signal.
- Splits up the low power differential signals into low power transmitter differential signals and low power receiver differential signals.
- Supports calibration process which is enabled by transmitter bfm.
- Supports continuous clock mode and non continuous clock mode D-PHY operation.
- Supports minimum and maximum D-PHY timing parameters value configuration.

7.1.4 CSI-2 Receiver BFM

Functionality of the CSI-2 Receiver BFM is described below:

- This model reads commands from a command file, namely csi_rx_cmd.v
- CSI2-Receiver BFM Interacts with the D-PHY Rx.
- It receives the byte data from the D-PHY Rx & stores it depending upon the valid signal.
- It validates the packet header data; it flags error if it finds any unsupported/Reserved data Id.
- It does ECC checking for the Short & Long packet header & asserts error for any mismatch.
- It flags error if the word count field doesn't obey the number of bytes to be transmitted for the corresponding Data Id (i.e Less than min bytes & Not in multiples).
- It computes the CRC for the received bytes & asserts error for any mismatch with the received CRC value.
- It performs byte to pixel packing for Long packet whenever the minimum byte count is reached for the corresponding Data Type.
- Receiver BFM transmits the packet header (Short, Long) to the monitor along with the header enable for the header data comparison.
- Receiver BFM transmits the Pixel Data to the monitor along with the pixel enable for the pixel data comparison.

7.1.5 Monitor

Functionality of the Monitor model is described below:

- This module monitors and store the packet information between Packet Interface BFM and DUT, it compares stored information (i.e pixel and short packet) with the data transmitted from receiver BFM.
- Monitor detects Frame Start, Line start, Line End, Frame end & stores it in the short memory.
- Similarly monitor stores the Generic Short packet & the Header information of Long packet into the same short memory.
- The pixel data is detected & stored in the Long memory as per the reception.
- Monitor compares the Sync short packet's (FS, LS, LE, FE) , Generic short packet's & Long packet header data depending on an enable signal(csi_header_en) from CSI Receiver BFM along with data. It flags error for mismatch.
- Similarly monitor does the pixel comparison depending upon the enable signal (csi_long_pkt_data_en) from the CSI Receiver BFM along with pixel data. It flags error for mismatch.

- Monitor does the check for protocol violations, Frame Sync, Line Sync errors along with Illegal change of Virtual channel number during the packet transmission.

8 Appendix

8.1 Power up Sequence for CSI2 Transmitter

The following steps needs to be followed for initializing the CSI2 transmitter to accept the image data from the external image source.

- Apply power on reset
- After power on reset, all the registers listed in section 4.1 needs to programmed with appropriate value that is suitable for user application
- Once the registers are programmed, the CSI2 transmitter will wait for assertion of "dfe_pll_locked" from MIPI DPHY. Until and unless this signal is asserted, the CSI2 transmitter will not start the transmission. The assertion of "dfe_pll_locked" indicates the completion of MIPI PHY power up sequence and it is ready to accept transaction on PPI. The signal "dfe_pll_locked" should be held high unless POR occurs.
- Once the CSI2 Transmitter samples the "dfe_pll_locked" as high, it gets into functional mode

Note: Please note that the register configurations listed in section 4.1 are with respect to Arasan CSI2 Transmitter with Arasan MIPI PHY as CSI2 controller is used to configure the DPHY and AFE. Some of these register may be irrelevant in case where the Arasan CSI2 Transmitter getting connect to 3rd party MIPI PHY.

8.2 D-PHY Integration Guide

CSI-2 Transmitter controller is used to drive the required register configuration for Arasan MIPI PHY. When 3rd party MIPI PHY is connected to Arasan CSI-2 Tx controller few of the register configuration/ports can be left open/tied to appropriate value as listed in the Table.

Port	Width	Direction	Description	Clock Domain
Clock and Reset Interface Signals				
TxClkEsc	1	Input	Slow speed clock used by the transmitter module. This clock is used to drive all low power PPI interface signals. This should be connected to D-PHY LP transmit clock.	External
TxByteClkHS	1	Input	Byte clock derived from the TxDDRClkHS. This clock is used to synchronize all high speed signals on the PPI interface between the controller and DPHY. This clock should be generated from DPHY. This clock should be 1/4 of TxDDRClkHS_I	TxDDRClkHS_I
Control Signals				

dfe_pll_locked	1	Input	This signal indicates that DPHY is ready to accept the data and transmit the data. Upon the reception of this signal CSI2 TX Controller starts processing the data. Note: This signal can be tied to logic '1' if not used when 3rd party D-PHY is connected However it the responsibility of the MIPI PHY to make sure that it accepts the data from the controller only after MIPI PHY initialization	Asynchronous
dfe_dln_reg_0	32	Output	Register carrying the global timing parameter for DPHY to control the TX data lane [7:0] : DFE_DLN_HS_ZERO_CNT [15:8] : DFE_DLN_HS_PREPARE [23:16] : DFE_DLN_HS_EXIT [31:24] : DFE_DLN_HS_TRIAL Note: This signal can be left open, if the MIPI PHY as it own register programming interface. However the application should make sure that the parameter programmed for DPHY should be the same that is programmed for the CSI2 Tx controller	sysclk
dfe_dln_reg_1	32	Output	Register carrying the global timing parameter for DPHY to control the RX data lane [7:0] : DFE_DLN_RX_CNT [15:8] : DFE_DLN_SYNC_CNT [23:16] : DFE_DLN_LPX_HS_CNT [31:24] : Reserved Note: This signal can be left open, if the MIPI PHY as it own register programming interface. However the application should make sure that the parameter programmed for DPHY should be the same that is programmed for the CSI2 Tx controller	sysclk
dfe_cln_reg_0	32	Output	Register carrying the global timing parameter for DPHY to control the TX clock lane [7:0] : DFE_CLN_ZERO [15:8] : DFE_CLN_PREPARE [23:16] :DFE_CLN_HS_EXIT [31:24] : DFE_CLN_HS_TRIAL Note : This signal can be left open, if the MIPI PHY as it own register programming interface. However the application should make sure that the parameter programmed for DPHY should be the same that is programmed for the CSI2 Tx controller	sysclk

dfe_cln_reg_1	32	Output	Register carrying the global timing parameter for DPHY to control the RX clock lane [7:0] : DFE_CLN_LPX_HS_CNT [15:8] : TCLK_PRE [23:16] : TCLK_POST [31:24] : Reserved Note: This signal can be left open, if the MIPI PHY as it own register programming interface. However the application should make sure that the parameter programmed for DPHY should be the same that is programmed for the CSI2 Tx controller	sysclk
pll_cnt_reg	32	Output	This register carry the TINIT period for the DPHY. Initialization period Note: This signal can be left open, if the MIPI PHY as it own register programming interface.	sysclk
dfe_dln_lane_swap	8	Output	This is Arasan Customization register used for the DPHY lane polarity swapping [0] : DLN0_SWAP [1] : DLN1_SWAP [2] : DLN2_SWAP [3] : DLN3_SWAP [4] : DLN4_SWAP [5] : DLN5_SWAP [6] : DLN6_SWAP [7] : DLN7_SWAP Note: This signal be left open	sysclk
Analog Interface Signals **The Analog interface signals are specific to Arasan AFE. These signals should be left open.**				
afe_trim_0	32	Output	AFE trim register0. This register is used only for Arasan AFE model. In case of User Specific DPHY, this register value can be ignored	sysclk
afe_trim_1	32	Output	AFE trim register1. This register is used only for Arasan AFE model. In case of User Specific DPHY, this register value can be ignored	sysclk
afe_trim_2	32	Output	AFE trim register2. This register is used only for Arasan AFE model. In case of User Specific DPHY, this register value can be ignored	sysclk

afe_trim_3	32	Output	AFE trim register3. This register is used only for Arasan AFE model. In case of User Specific DPHY, this register value can be ignored	sysclk
PPI Interface Signals				
txrequestesc	[7:0]	Output	It is a standard signal according **MIPI - DPHY** specification	TxClkEsc
txdatahs	[63:0]	Output	The data to be transmitted on the data lanes. It is a standard signal according **MIPI - DPHY** specification	TxByteClkHS
txrequesths	[7:0]	Output	The HS request signal for data lane0~7. A low-to-high transition on TxRequestHS causes the Lane Module to initiate a Start-of-Transmission sequence. A high-to-low transition on TxRequestHS causes the Lane Module to initiate an End-of-Transmission sequence. For Clock Lanes, this active high signal causes the Lane Module to begin transmitting a High-Speed clock. For Data Lanes, this active high signal also indicates that the protocol is driving valid data on txdatahs to be transmitted. The Lane Module accepts the data when both txrequesths and txreadyhs are active on the same rising txbyteclkhs clock edge. The protocol always provides valid transmit data when txrequesths is active. Once asserted, txrequesths remains high until the data has been accepted, as indicated by txreadyhs. txrequesths is only asserted while txrequestesc is low. It is a standard signal according **MIPI - DPHY** specification	TxByteClkHS
txreadyhs	[7:0]	Input	This signal indicates if the DPHY is ready to accept data on the PPI Interface. It is a standard signal according **MIPI -DPHY** specification	TxByteClkHS
txulpsesc	[7:0]	Output	This signal indicates if the DPHY has to initiate a ULPS sequence on the data lanes. This active high signal is asserted with txrequestesc to cause the Lane Module to enter the Ultra-Low Power State. The Lane Module remains in this mode until txrequestesc is de-asserted. It is a standard signal according **MIPI - DPHY** specification	TxClkEsc

txulpsexit	[7:0]	Output	This signal indicates if the DPHY has to exit out of a ULPS state on data lane0~7. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. This signal is ignored when the Lane is not in the ULPS state. It is a standard signal according **MIPI - DPHY** specification	TxClkEsc
txulpsclk	1	Output	The signal initiates a ULPS entry sequence on the clock lane. It is a standard signal according **MIPI - DPHY** specification	TxClkEsc
txulpsexit_sclk	1	Output	The signal initiates a ULPS exit sequence on the clock lane. It is a standard signal according **MIPI - DPHY** specification	TxClkEsc
txrequesths_clk	1	Output	This active high signal causes the clock lane module to begin transmitting a high-speed clock. It is a standard signal according **MIPI - DPHY** specification	TxByteClkHS
ulpsactivenot_n	[7:0]	Input	This signal indicates if the transmit data lane is not in ULPS state It is a standard signal according **MIPI - DPHY** specification	TxClkEsc
ulpsactivenot_clk_n	1	Input	This signal indicates if the clock lane transmitter is not in ULPS active state It is a standard signal according **MIPI - DPHY** specification	TxClkEsc
stopstate	[7:0]	Input	Indicates a reception of STOP state on the data lanes0~7. It is a standard signal according **MIPI - DPHY** specification	Asynchronous
stopstate_clk	1	Input	Indicates a reception of STOP state on the clock lane It is a standard signal according **MIPI - DPHY** specification	Asynchronous
txskewcalhs	[7:0]	Output	High-Speed Transmit Skew Calibration. A low-to-high transition on TxSkewCalHS causes the PHY to initiate a de-skew calibration. A high-to-low transition on TxSkewCalHS causes the PHY to stop deskew pattern transmission and initiate an end-of-transmission sequence. The LSb of this bus correspond to the data lane 0, and the MSb of this bit correspond to the data lane 7. This is optional feature, if not used left oprn	Txbyteclkhs

