YAMAHA *LSI*

YM3O12

2-Channel Serial Input  
Floating D/A Converter (DAC-MS)

* **OUTLINE**

YM3012: DAC-MS (hereinafter referred to as DAC) is a floating D/A converter with serial input for two channels . It can generate analog output (dynamic range 16 bits) of 10-bit mantissa section and 3-bit exponent section on the basis of input digital signal.

* **FEATURES**
* An external buffer operational amplifier is provided to obtain analog output easily.
* A wide dynamic range with 16 bits.
* Compatible with PCM audio sources of up to 2 channels
* Built-in sample hold analog switches
* It is possible to obtain low noise, low harmonic distortion and good temperature char­acteristics.
* Monolithic chip with high precision thin film resister and CMOS and contained in a 16 pin plastic DIL package.

YAMAHA CORPORATION

■ 55MSS2M 000303b 735 ■

YM3012 CATALOG  
CATALOG No.: LSI-2130123  
1992. 4

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■ PIN DIAGRAM

Vdd C

G>

**ANALOG**

**GND(Vss)**

**CLOCK/IC**

**<n**

**Re**

■ BLOCK DIAGRAM

**DIG**

**GND(Vss) L**

**S D (DATA)**

**SAM2**

**SAMI**

**ICL**

**ANALOG**

**GND(Vss)**

**in**

<0

**co**

W

N>

□

**BC**

**MP**

N

**(ANALOG OUT)**

**□ ToBUFF**

**(ANALOG IN)**

**I COM**

□

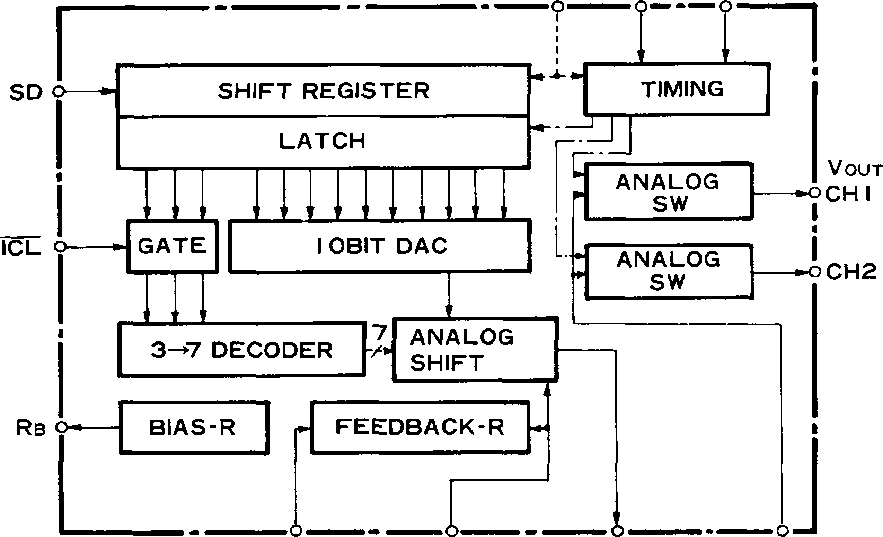
**CH-2**

**VOUT**

**CH-1**

**YM3012**

**CLOCKS I SAM I SAM2**



**BC MP To BUFF COM**

**(ANALOG-OUT) (ANALOG-IN)**

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**YM3012**

MM

■ PIN DISIGNATION

|  |  |  |
| --- | --- | --- |
| **Pin No.** | **Symbol** | **Function** |
| 1 | Vdd | Reference power source on high potential side |
| 2 | CLOCK | Clock (01) for operation of shift register and timing generator |
| 3 | DIG- Vss | Digital section power source on low potential side (GND) |
| 4 | SD | Serial input of converted digital signal |
| 5 | SAM2 | “ 1 ” section becomes CH2 sampling period |
| 6 | SAMI | “1” section becomes CHI sampling period, Trailing edge of SAMI and SAM2 are used |
|  |  | to generate internal signal for latching serial data |
| 7 | ICL | “1” -normal operation; “0” - analog output becomes equal (S2 = St = 0, So = 1), regardless of SD signal |
| 8 | ANALOG vss | Analog section power source on low potential side (GND) |
| 9 | Vout CHI | CHI sample hold analog switch output |
| 10 | Vout  CH2 | CH2 sample hold analog switch output |
| 11 | COM | Analog switch common input for CHI and CH2 |
| 12 | To BUFF | Analog output from DAC, input to buffer operational amplifier |
| 13 | MP | Normally biased to 1 /2 Vdd, exponential analog output obtained on the base of MP potential by S signal |
| 14 | BC | Resistance eliminating error due to buffer operational amplifier input bias current, present between this pin and 13 pin. It is recommended to externally connect a Cc capacitor for phase compensation |
| 15 | Rb | High precision 1/2 Vdd voltage generated internally, outputs from this pin. Applied to 8 pin through buffer operational amplifier |
| 16 | ANALOG  Vss | Low potential side power source (GND) for generating 1/2 Vdd voltage of 15 pin |

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**YM3012**

**■ DESCRIPTION OF FUNCTIONS**

1. **Relationship between Digital Input Data and Analog Output Voltage**

To perform one conversion at 16-bit time by YM3012, the first 3-bit data in the 16-bit serial data is treated as invalid data in the DAC. The next 10 bit data (Do through Do) is input into the 10-bit DAC section as the data of MSB to LSB to constitute the manissa section of analog output. The remaining 3-bit data (So through S2) is input into the 2 “ N analog shift section to constitute the exponent section of analog output. For example, when the basic circuit is used, output voltage is as follows.

VOUT\_= 1/2 VDD +J\_/4VDD(- 1 + D? + Ds2 -1 +•••+ Do2-9 + 2~,°) 2-n

N = S222 + S121 + So

S2 = Sj = So = 0: not allowed.

That is, it has the maximum aplitude of 1/2 VDD and the minimum amplitude of 1/2

VDD 2 ~16 with 1 /2 Vdd potential as a center.

1. **Operation in the DAC**

Digital input data is taken into the shift register through the SD pin, synchronized with the clock rise. The latch signal is generated in the timing circuit using the trailing edge of SAMI and SAM2. By this latch signal, the Do through D9 and So through S2 serial data is latched, driving the 10-bit DAC section and the analog shift section, respectively, to start conversion. The analog output is ouptput from the “To BUFF” pin. When this analog output is input to the COM pin through the proper buffer operational amplifier and resistor, it is output from the CHI and CH2 pins for the period during which SAMland SAM2 are When SAMI and SAM2 are “0”, the analog output for each channel is held in a proper electrostatic capacity.

1. **Summary of Operation**

* As shown in Fig. 3, make the trailing edge timing of SAMI and SAM2 coincide with the S2 rear end timing of SD signal.
* The SAMI and SAM2 sampling period can also be set to be other timing than 8-bit I shown in Fig.3.
* When using channel 1 only, set SAM2 to VSS, and make the S2 rear end timing of SD coincide with the SAMI trailing edge timing.
* Conversion cycles with a different bit timing are possible by increasing or decreasing the invalid bit data.

1. **Initial Clear Function**

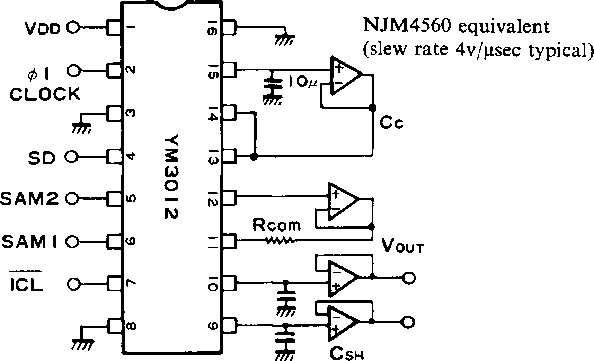
When ICL is made “0”, S2 = Si =0 and So= 1, that is, the mantissa does not change, and output with the exponential section reduced to 2 ~6 is output from each channel output regardless of the digital input data value.

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**YM3012**

■ EXAMPLE OF BASIC CIRCUIT



CSH 1500PF ' .RCOM 270 Q.

Example of External Constant Value

Sample hold capacity: CSH = 560 ~ 33OOPF  
Common resistance: RCOM = 100 ~ 1000 Q

The optimal values within the ranges mentioned above is determined  
by the usage condition (VDD, etc.).

recommended

**■ ELECTRICAL CHARACTERISTICS**

1. Absolute Maximum Rating

|  |  |  |  |
| --- | --- | --- | --- |
| **ITEM** | **RATING** | | **UNIT** |
| Supply voltage | -0.3- | - + 15.0 | V |
| High level input voltage | Vdd | + 0.3 | V |
| Low level input voltage | Vss | -0.3 | V |
| Ambient operating temperature | 0 - | - 70 | °C |
| Storage temperature | -50- | - + 125 | °C |

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**YM3012**

2. Recommended Operation Conditions

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **ITEM** | **SYMBOL** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| Supply voltage | Vdd Vss | + 4.75 0 | 5.0 0 | 10.0 0 | V  V |
| Input signal voltage | CLOCK  SD  SAM 1,2  ICL | 0 | — | Vdd | V |
| Ambient operation temperature | Ta | 0 | — | 70 | °C |

3. D.C. Characteristics

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **ITEM** | **SYMBOL** | **MEASUREMENT CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| High level input voltage | VlH | VDD = 5.0V | 3.3 | — | — | V |
| Low level input voltage | VlL | Vdd = 5.0V | — | — | 1.0 | V |
| Input current | IlN | Vdd = 10.0V | — | — | 10-3 | pA |
| Power current | IDD | Vdd = 5.0 V | — | — | 6 | mA |

4. AC Characteristics

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **ITEM** | **SYMBOL** | **CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| * Clock Frequency   High level time  Rise time  Fall time   * Data Set-up time   Rise time  Fall time | fc |  | 0.65 | 1.6 | 3.2 | MHz |
| tH |  | 100 |  |  | ns |
| tr |  |  |  | 50 | ns |
| tf |  |  |  | 50 | ns |
| Ids | SD SAMI  SAM2 | 100 |  |  | ns |
| tr |  |  | 50 | ns |
| tf |  |  | 50 | ns |

5. Capacity

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **ITEM** | **SYMBOL** | **CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| Input capacity | ClN |  | — | — | 5 | pF |

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**YM3012**

6. DAC Characteristics

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **ITEM** | **SYMBOL** | **CONDITIONS** | **MIN.** | **STD.** | **MAX.** | **UNIT** |
| Max.out put amplitude | VOA |  |  | 1/2VDD |  | V |
| Resolution |  |  |  | 16 |  | Bit |
| Settling time | ts |  |  | 2.5 | 5.0 | **RS** |
| Total harmonic distortion  (Analysis mode) | THD1  THD6 | Vdd = 5 V, 110Hz level 0 dB  -36 dB |  | 0.05 | 0.10  0.15 | % % |
| Noise |  |  |  | — 92 | -80 | dBm |
| Crosstalk |  |  |  | -72 |  | dB |
| Temperature characteristics |  | Output voltage  Total harmonic distor­tion |  | 5 |  | ppm/°C |

7. Timing Diagram

**SD, SAM I ,SAM2**

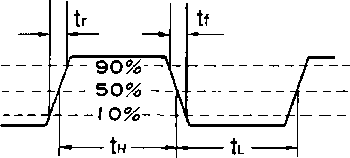


Fig. 1 Data timing

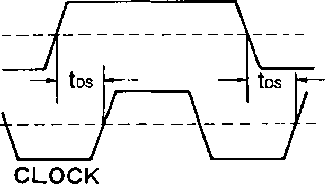


Fig. 2 Input data-clock timing

nnnrouijinnjinnjuijinjino^



**CHI CH2**

**l/l/;/lD!D!DiDlD;DlDlDlDlD;sls;sS/li/i/lD** |d;d|d!d;d|d'd'did'sis;s  
**r //|o]l ]2|3 lajs 16 |7]8 '9 !o| I izj^Zrlo} 1 jz| 3 i4|s|6 dials', o] 1 |z**

**LATCH**

To BUFF

**ANALOG  
OUT**

**SAMPLING**



**CH2**

**j CH2**

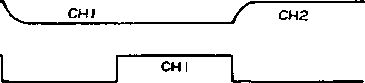


Fig. 3 TIMING

■ 5HM5524 □□□2032 T32 ■

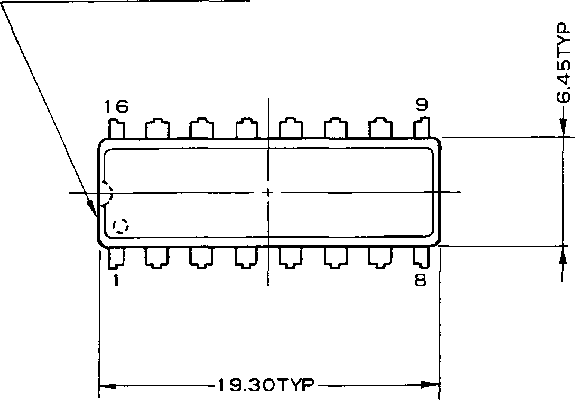
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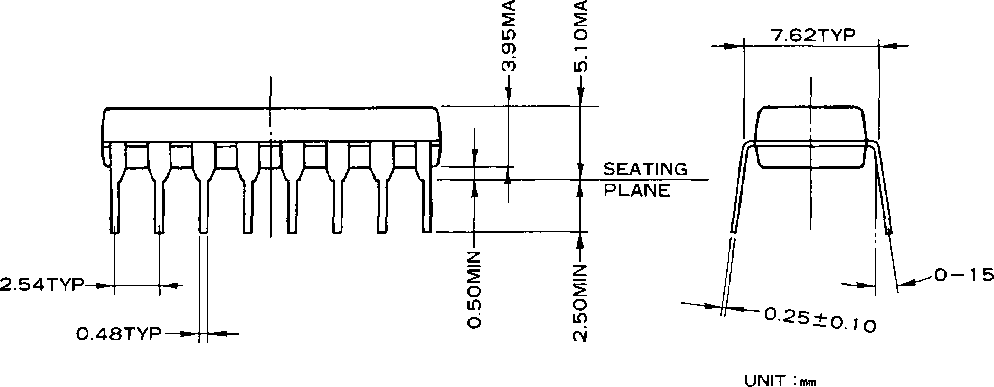
**YM3012**

■ OUTLINE DIMENSIONS

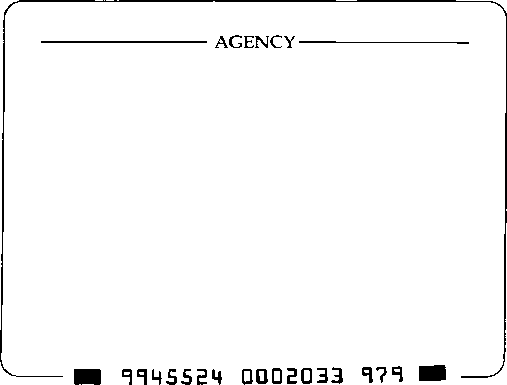
Notch or 1 -pin index mark



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The specifications of this product are subject to improvement changes without prior notice.



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