Design of Voltage Controlled Oscillator

Krishnendu Roy
Department of Electronics and Communication Engineering
National Institute of Technology Rourkela
krishofficial18236@gmail.com

***Abstract*—This paper presents the design and simulation of a Current Starved Voltage Controlled Oscillator (VCO) using CMOS technology. The proposed VCO operates in the GHz frequency range with a tuning span from 0.88 GHz to 2.429 GHz. Implemented and analyzed in the open-source eSim platform, the design emphasizes low power consumption, high frequency stability, and wide tunability. The architecture is based on a ring oscillator with current-starving transistors that regulate the delay and control the oscillation frequency through an applied voltage. Simulation results validate the effectiveness of the design in achieving stable and tunable output frequencies, making it suitable for applications in frequency synthesizers, communication systems, and phase-locked loops (PLLs).**

I. Circuit Details

The Current Starved Voltage Controlled Oscillator (VCO) is implemented using a ring oscillator topology with an odd number of inverter stages connected in a loop. To control the oscillation frequency, each inverter stage is supplied through additional MOSFETs that act as current-limiting devices. By varying the gate voltage of these transistors, the current flow is regulated, which directly affects the propagation delay and hence the oscillation frequency.

In this work, the circuit is designed using CMOS technology. NMOS and PMOS devices are arranged in complementary pairs to form the inverter stages, while current-starving transistors are placed in series with both pull-up and pull-down paths. This configuration enables fine control over the delay of each stage, providing a tunable frequency response.

Simulations in eSim confirm that the proposed design achieves a tuning range from 0.88 GHz to 2.429 GHz, while maintaining low power consumption and good frequency stability, making it suitable for use in communication and PLL applications.

Device Name	Device Type	Aspect Ratio(um/nm)
M2,M5,M9,M13,M17,M21	PMOS	2/180
M6,M10,M14,M18,M22	PMOS	1/180
M3,M7,M11,M15,M19	NMOS	1/180
M1,M4,M8,M12,M16,M20	NMOS	2/180

Aspect ratio of MOSFET

Fig. 1. Circuit output

II. Circuit Diagram

The circuit diagram of the voltage controlled oscillator circuit is as shown in Figure 2.

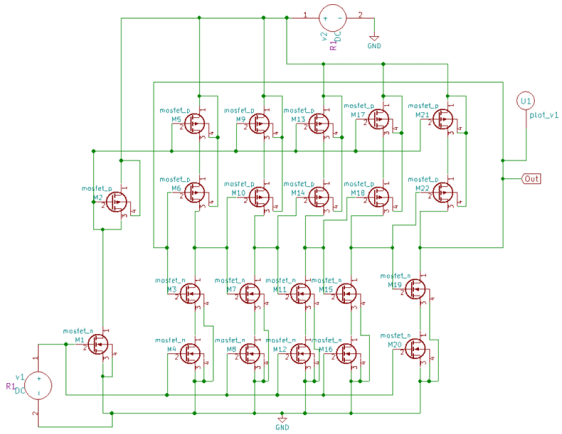

Fig. 2. Circuit Diagram

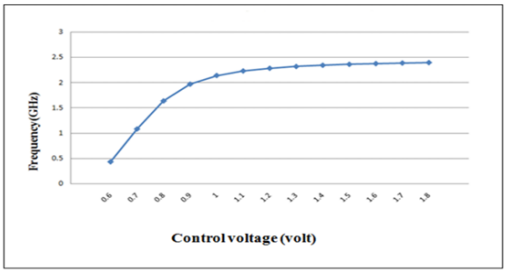

Fig. 3. Graphical Representation of Output Frequency VS Control Voltage

Control Voltage(Volt)	Frequency(Hz)
0.7	0.88 G
0.8	1.479 G
0.9	1.887 G
1	2.107 G
1.1	2.227 G
1.2	2.295 G
1.3	2.338 G
1.4	2.368 G
1.5	2.39 G
1.6	2.406 G
1.7	2.419 G
1.8	2.429 G

Control Voltage vs Frequency

Fig. 4. Control Voltage vs Frequency

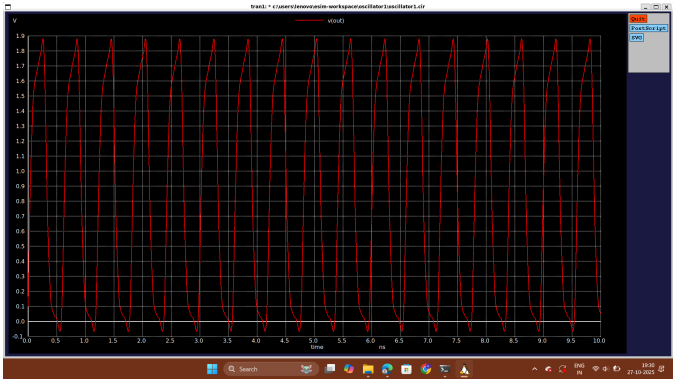

Fig. 5. For 0.7 volt input

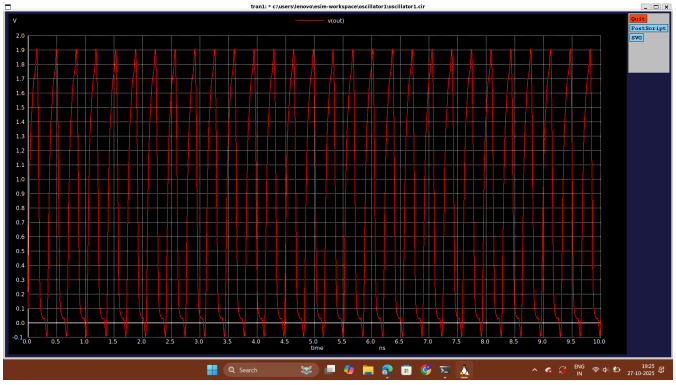

Fig. 6. For 1 volt input

III. Conclusion

In this project, a Current-Starved Voltage Controlled Oscillator (VCO) was successfully designed and simulated using eSim. The output frequency was observed to vary with changes in the input control voltage, confirming the voltage-controlled nature of the circuit. As the control voltage increased, the oscillation frequency also increased due to higher current in the delay stages, resulting in faster charging and discharging of capacitors. The circuit achieved stable oscillations with efficient power consumption from the DC supply. The results

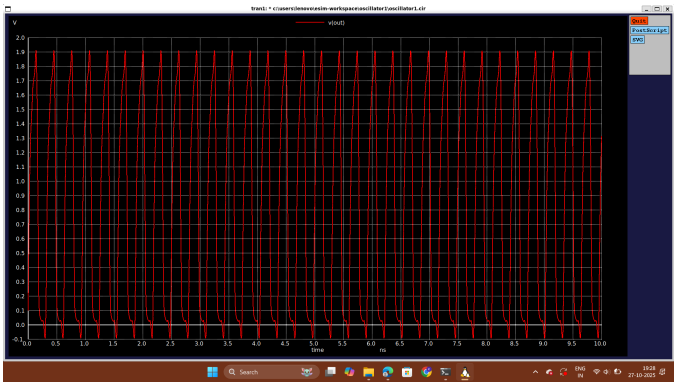

Fig. 7. For 1.5 volt input

demonstrate that the output frequency of the current-starved VCO can be tuned by adjusting the input voltage, making it suitable for applications such as phase-locked loops (PLLs) and frequency synthesizers in communication systems.

IV. GitHub Repository and README

The complete project files, including the schematic, simulation data, and documentation, are available on GitHub at:

- **Repository Link:**
  https://github.com/rkrish00568/CurrentStarvedVCOeSim.git

README Summary: This repository contains the eSim design files, simulation outputs, and report for the project titled *"Design of Current Starved Voltage Controlled Oscillator using eSim"*. The design demonstrates how the output frequency varies with control voltage, suitable for applications in PLLs and RF communication circuits. Instructions for running the simulation and reproducing results are included in the README file.

References

[1] https://www.irjet.net/archives/V5/i3/IRJET-V5I3191.pdf