Alternative Transistor-Based Ramp Generator

Basic Explanation

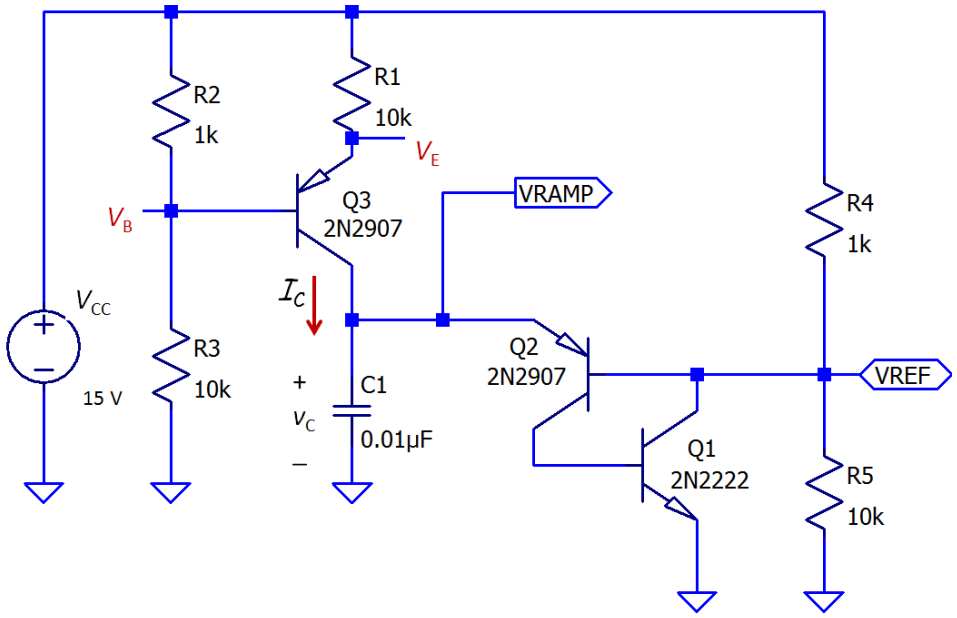
The capacitor is charged via a simulated current source made from PNP transistor Q_3 and associated resistors R_1- R_3. In summary, bias voltage V_B is set by a voltage divider to the (approximate) value $V_{CC}R_3/(R_1 + R_3)$. (Voltage division formula is only approximate because the base current of Q_3 flows into node V_B).

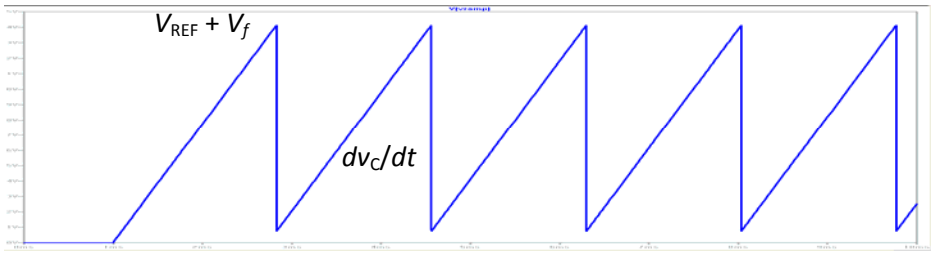
This sets $V_E = V_B + V_f$ where V_f is the forward drop of Q_3's emitter-base junction. The current through R_1, and hence into the capacitor, is a constant $(V_{CC} - V_E)/R_1$.

Meanwhile, a second bias voltage V_{REF} is set by (approximate) voltage division: $V_{CC}\ R_5/(R_4 + R_5)$

The current I_C causes the capacitor voltage to ramp up linearly as $dv_C/dt = I_C/C$. Until v_C becomes high enough to forward bias the emitter-base junction of Q_2, transistor Q_2 will remain off and draws no current from the capacitor or Q_3.

When the capacitor voltage v_C rises to $V_{REF} + V_f$, where V_f is the emitter-base junction voltage of Q_2, PNP transistor Q_2 turns on and sends its collector current into the base of NPN Q_1, turning it on as well. This regenerative action develops essentially instantly and discharges the capacitor to (almost) zero. When the latter occurs, Q_2 and Q_1 turn off again and the cycle is reset.





v_{RAMP} versus time