



D-PLL Design, Layout and Circuit Simulation

Submitted by –

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Phase Frequency Divider

Transistor Level Circuit Schematic –

The PFD is one of the main components of a PLL. The PFD in a PLL will be used to compare the phase difference of the two input signals. The working of the PFD is as follows, when both data and clock are perfectly synchronized with each other and there is no phase difference between the UP DN pulse so we get a clear glitch free output. Similarly, when the data is ahead of clock, then the DN pluses are produced and UP signal are disabled. Whereas, when the data is behind the clock, then the UP pulses are produced and DN is disabled. By utilizing this information, we can forecast, which input between the two input signals is ahead or behind the other.

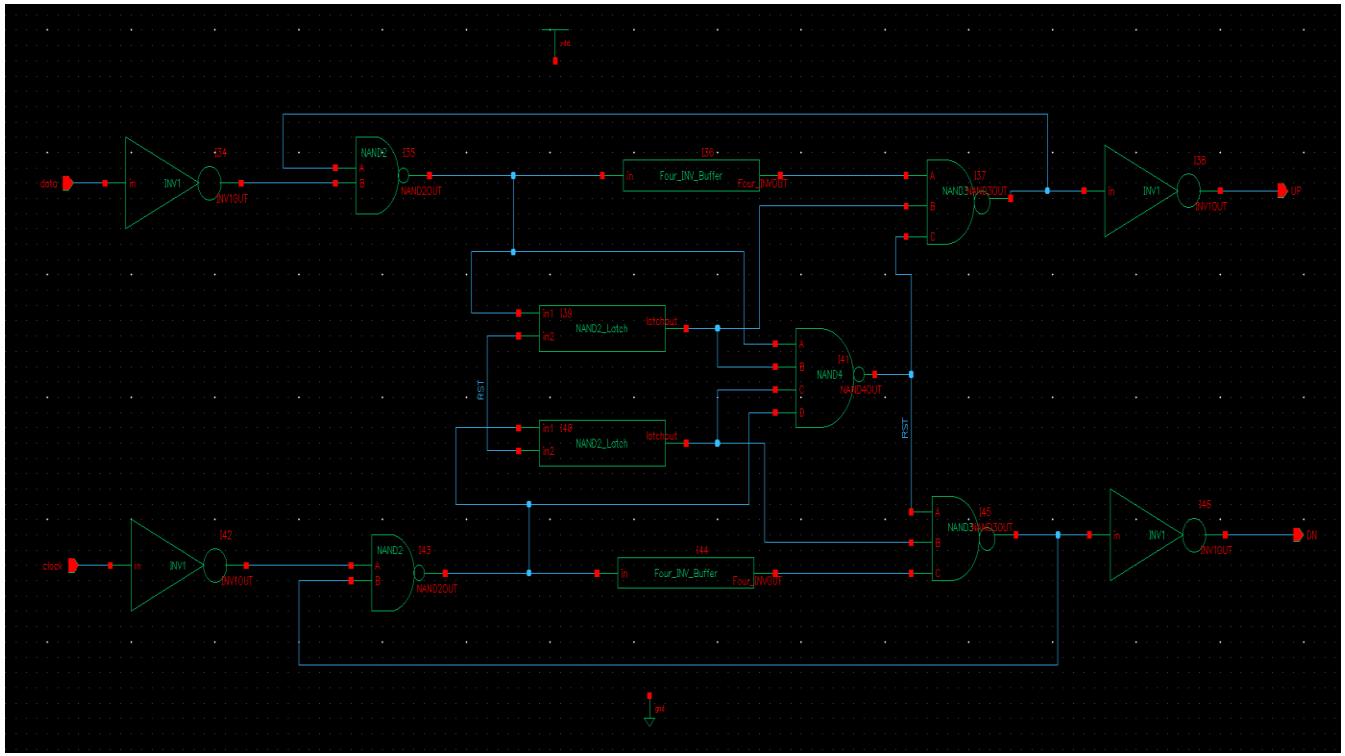


Fig 1: Transistor-level Circuit Schematic

Discussion of circuit -

To implement my NAND Latch in my PFD circuit, I have made a latch and used it as a separate entity to instantiate it for my PFD circuit. This is help me instantiate my Latch design in my PFD circuit, and reduces my load of individually attaching all the components in my main PFD Design.

SR Latch –

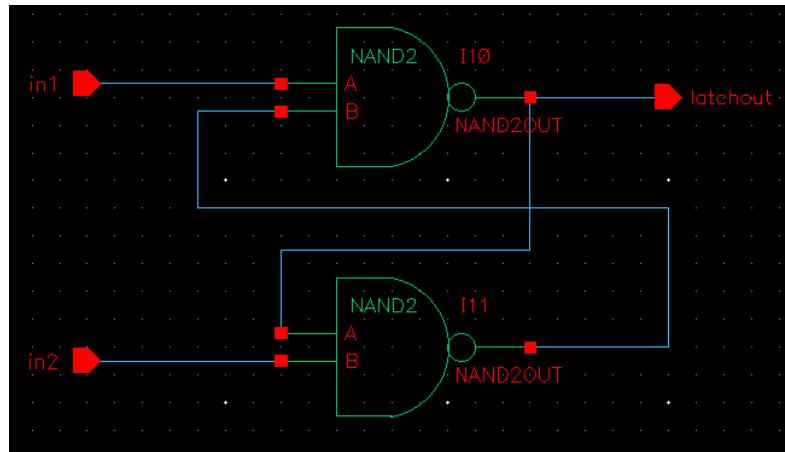


Fig 2: NAND Latch

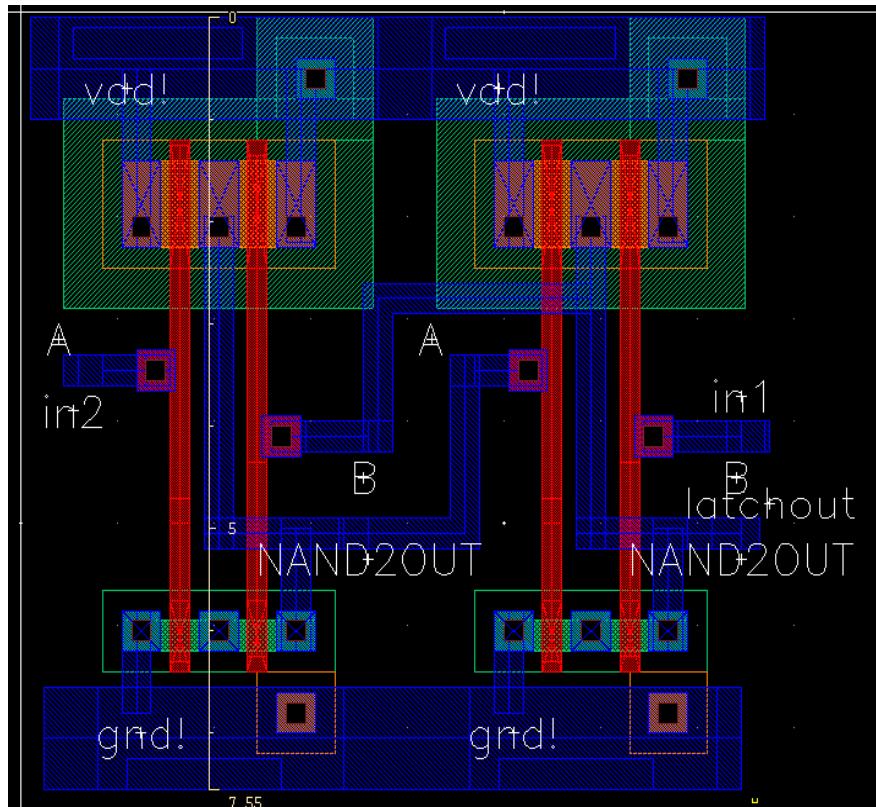


Fig 3: NAND Latch Layout



Fig 4: NAND Latch symbol

4 Input Buffer -

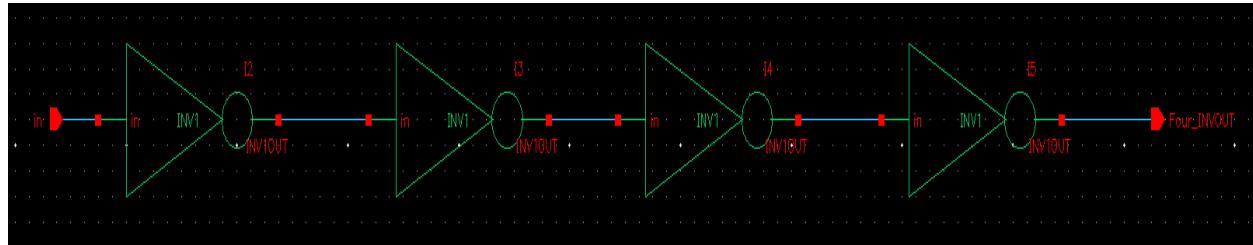


Fig 5: 4 Input Buffer Schematic

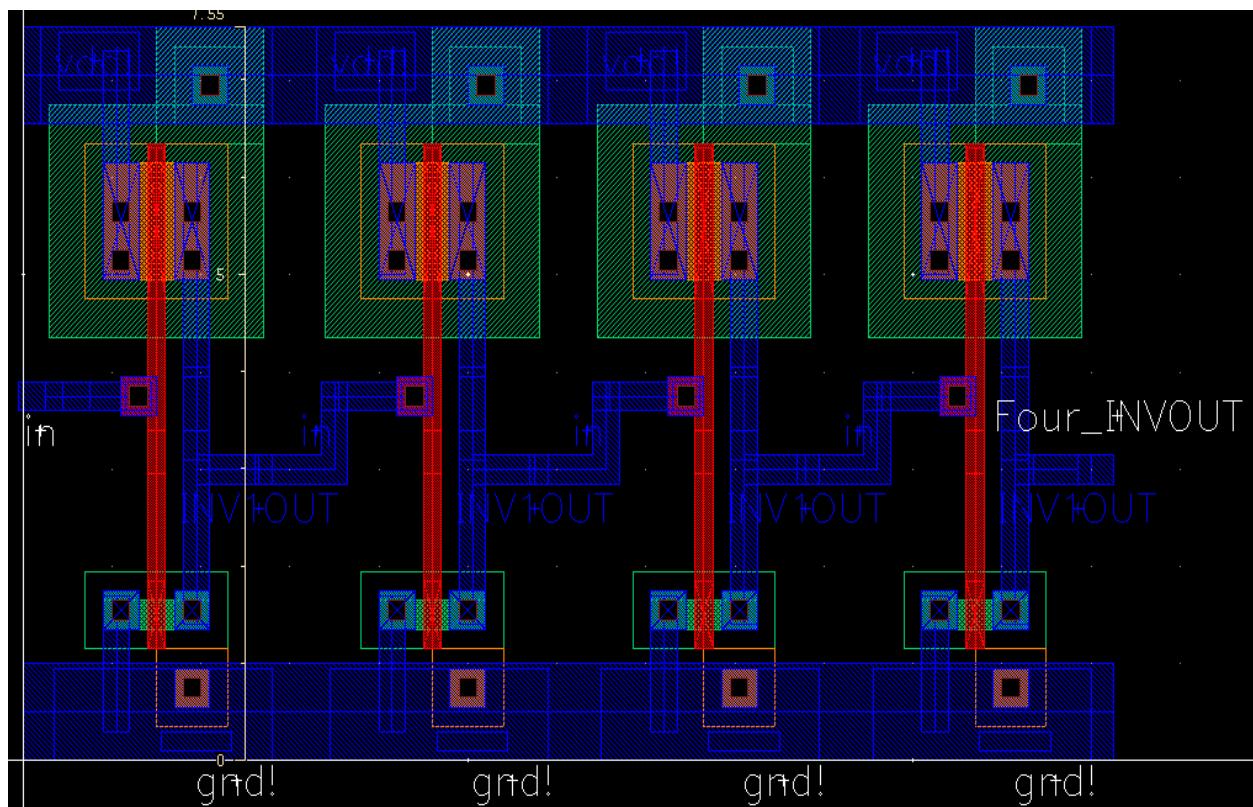


Fig 6: 4 Input Buffer Layout

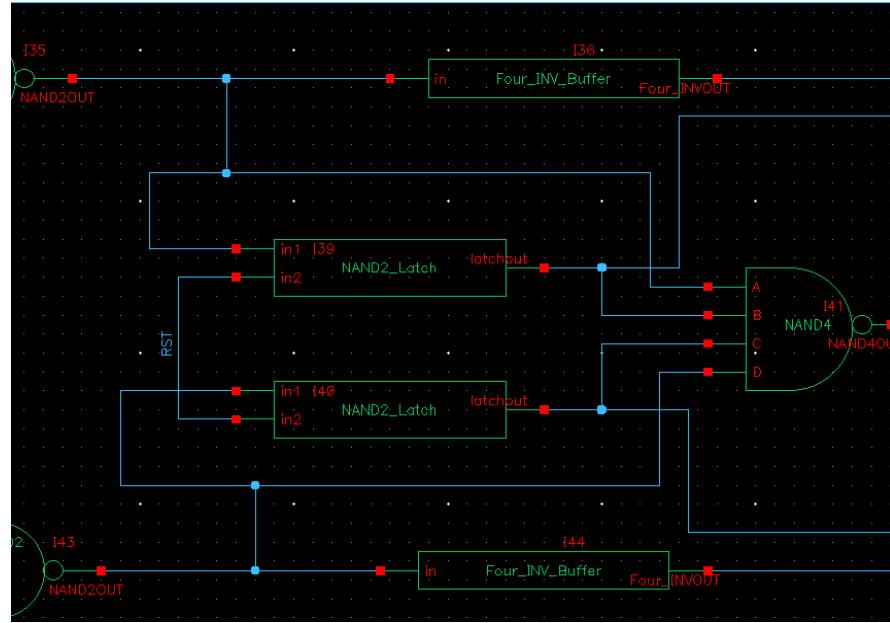


Fig 7: 4 Instantiated Symbols Used

Custom Symbol –

This is the image of the symbol, which I designed for my Phase Frequency Detector, so that I can instantiate it for my further design of PLL.



Fig 8: Layout Phase Frequency Detector with Load LVS match

Cell	Layout Height (μm)	Layout Width (μm)	Layout Area (μm ²)
PFD	6.55	77.1	505

Circuit Level Simulation -

As instructed in the report Instruction, we have taken three inputs for our Phase Frequency Detector, the time period for data 1 input is 20n, for data 2 is 21n, and for data 3 is 19n.

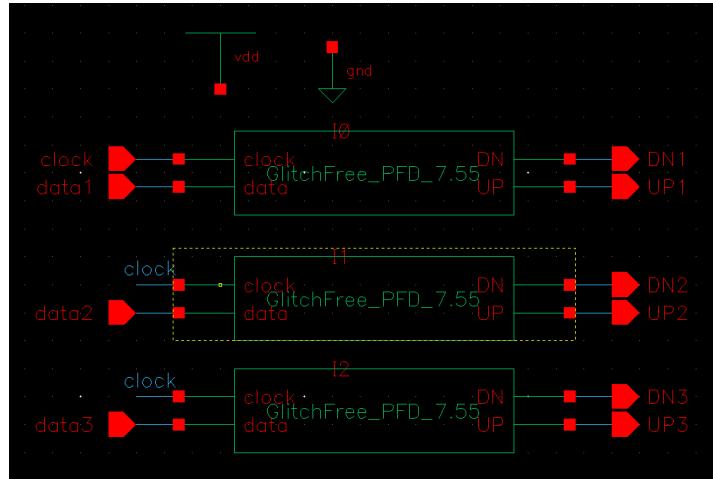


Fig 9: PFD Test Bench Input Model

As it is evident from the waveform below, when both data and clock are perfectly synchronized with each other and there is no phase difference between the UP DN pulse so we get a clear glitch free output. Similarly, when the data is ahead of clock, then the DN pluses are produced and UP signal are disabled. Whereas, when the data is behind the clock, then the UP pulses are produced and DN is disabled.

This demonstrates our PFD is perfectly designed and its layout implementation is properly extracted.

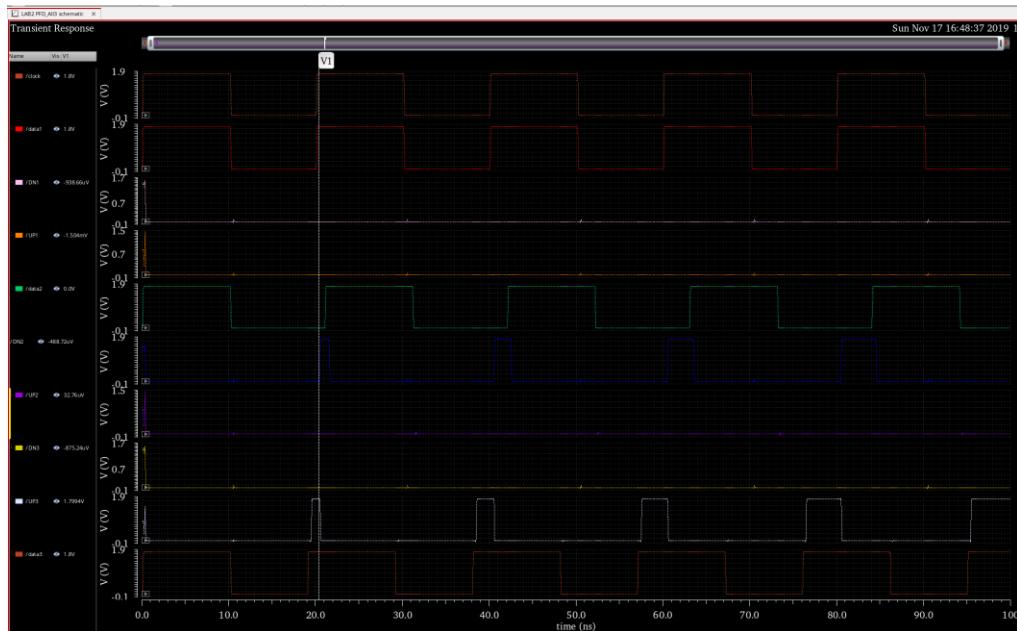


Fig 10: PFD Test Bench Waveform

Physical Layout -

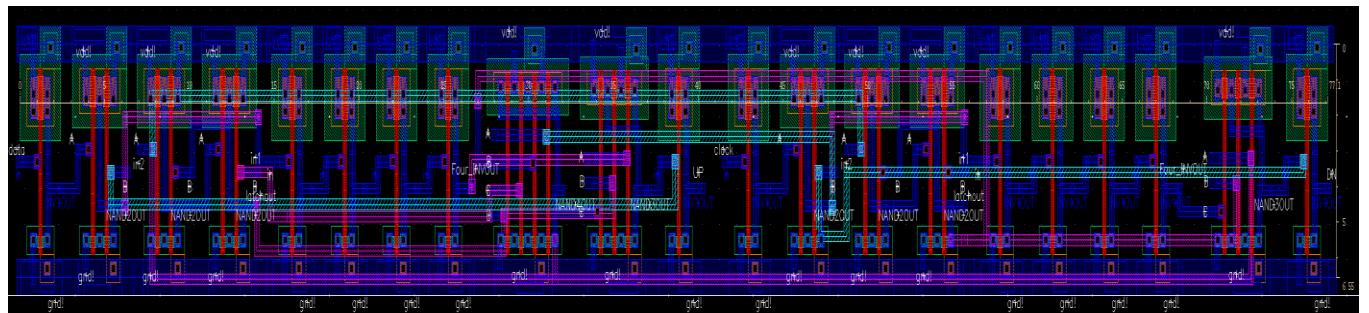
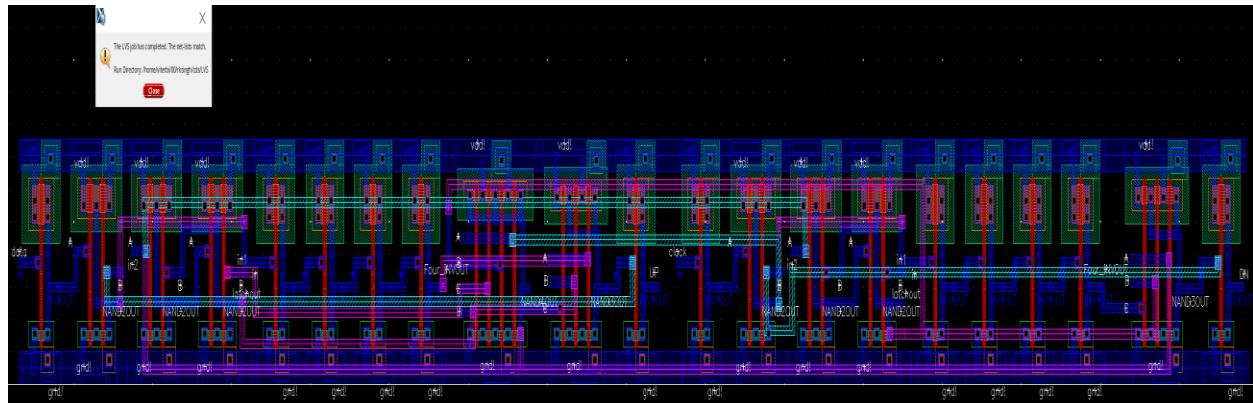


Fig 11: Layout Phase Frequency Detector

Layout vs. Schematics LVS result -



```
Virtuoso® 6.1.7-64b - Log: /home/viterbi/00/rksingh/CDS.log
File Tools Options Help
executing: saveDerived(via5 ("net") cell_view)
Extraction started.....Fri Nov 15 14:51:24 2019
completed ....Fri Nov 15 14:51:25 2019
CPU TIME = 00:00:00 TOTAL TIME = 00:00:01
***** Summary of rule violations for cell "GlitchFree_PFD_7.55 layout" *****
Total errors found: 0
```

Fig 12: Layout Phase Frequency Detector with LVS match

Layout Simulation -

As instructed in the report Instruction, we have taken three inputs for our Phase Frequency Detector, the time period for data 1 input is 20n, for data 2 is 21n, and for data 3 is 19n.

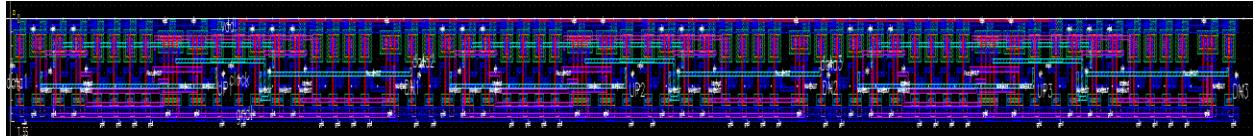


Fig 13: PFD Test Bench Layout Model

As it is evident from the waveform below, when both data and clock are perfectly synchronized with each other and there is no phase difference between the UP DN pulse so we get a clear glitch free output. Similarly, when the data is ahead of clock, then the DN pluses are produced and UP signal are disabled. Whereas, when the data is behind the clock, then the UP pulses are produced and DN is disabled.

This demonstrates our PFD is perfectly designed and its layout implementation is properly extracted.



Fig 14: PFD Test Bench Extracted Waveform

Summary & Result –

We have successfully designed a Phase Frequency Detector using both the combinational logic as well as using D Flip Flops. Though for our assignment we are using the combinational logic design. We have received a glitch free Static Phase Frequency Detector.

Charge Pump

Transistor Level Circuit Schematic –

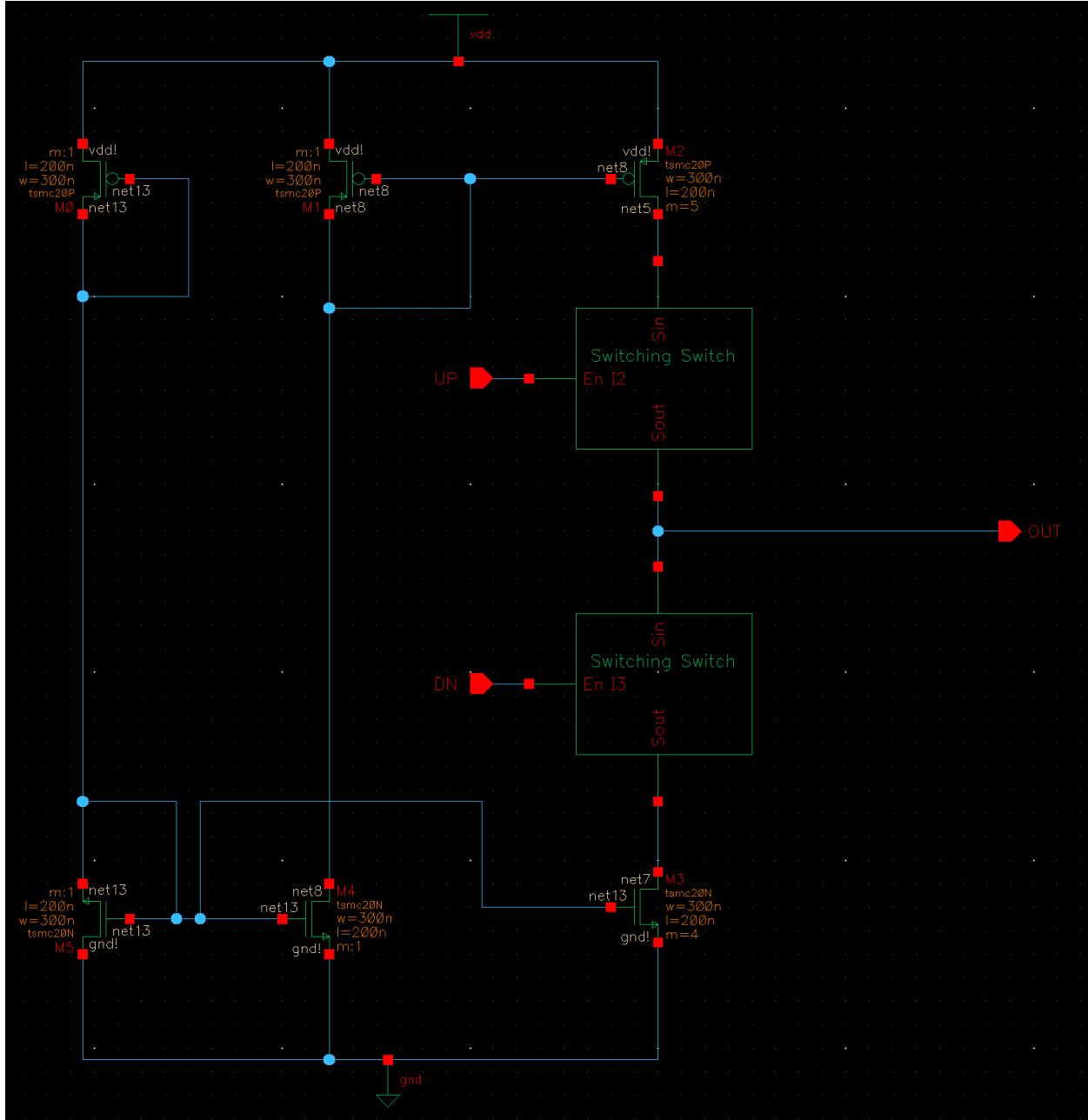


Fig 1: Transistor-level Circuit Schematic

Discussion of circuit -

A Charge Pump consist of an op-amplifier kind of circuit, where we pump and control the flow of the supply voltage across the load, through the use of capacitors. It acts as a bipolar switched current source, so it provides positive and negative current pulses into our loop filter. It consists of two identical source and sink current sources. Whenever the UP signal turns on, the source current source will charge-up the output load capacitor. Additionally, when DN signal turns on, the sink current source will discharge down the output load capacitor. Therefore, the result will be ramp-up and ramp-down spikes at the output. The purpose of the output filter is to filter these spikes making them smooth and create a DC voltage which is the average value. This DC voltage will be the input of the VCO that creates the output frequency

Custom Symbol –

This is the image of the symbol, which I designed for my Charge Pump, so that I can instantiate it for my further design of PLL.

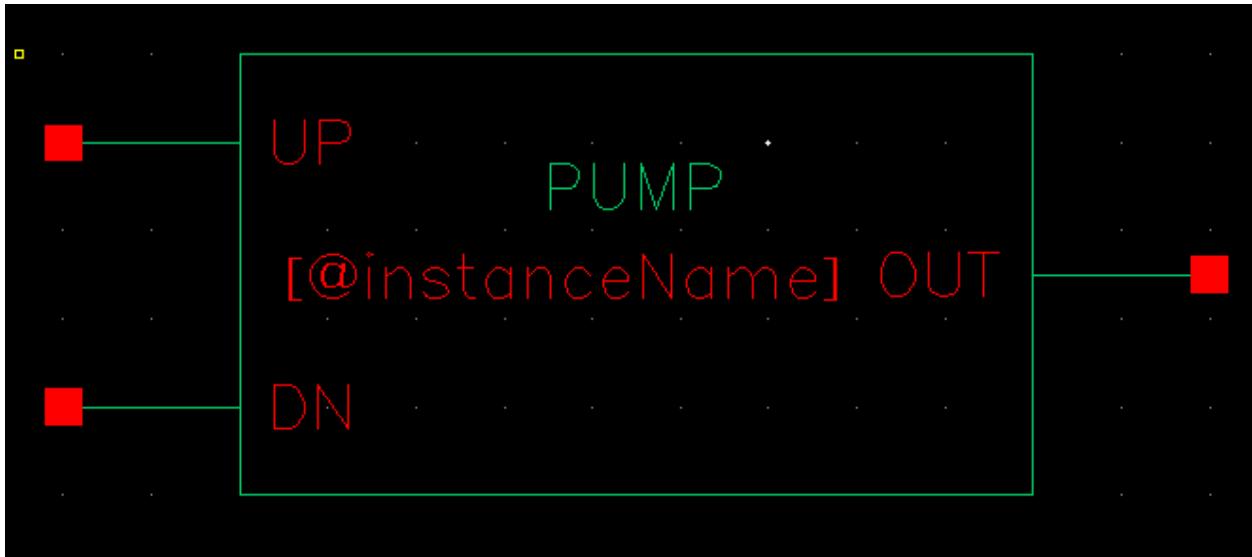


Fig 2: Charge Pump Symbol

Circuit Level Simulation –

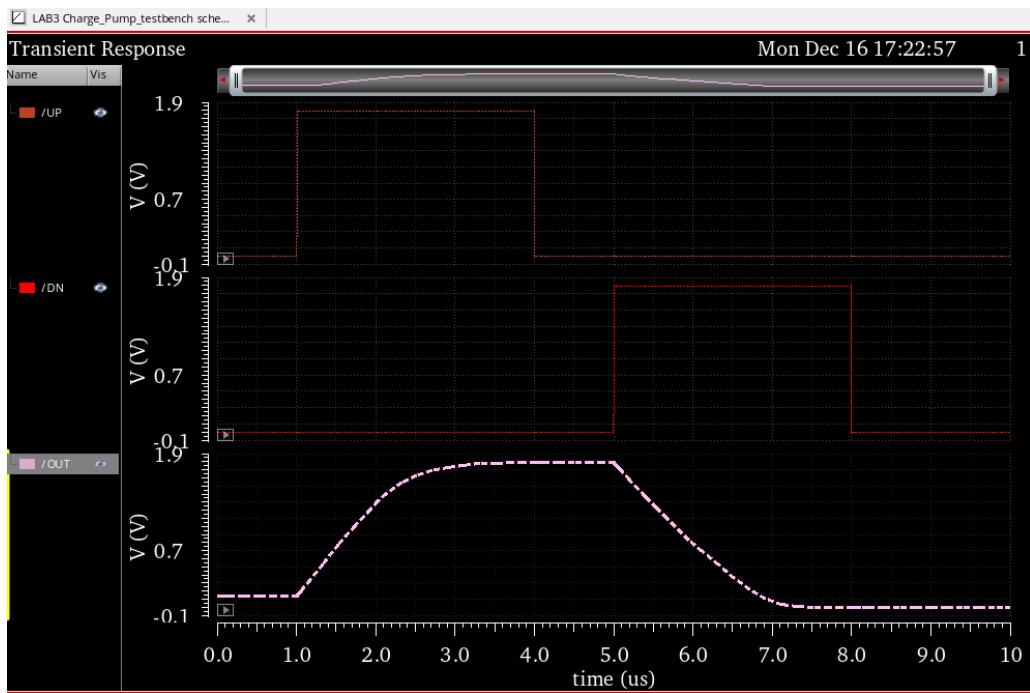


Fig 3: Charge Pump Schematic Simulation

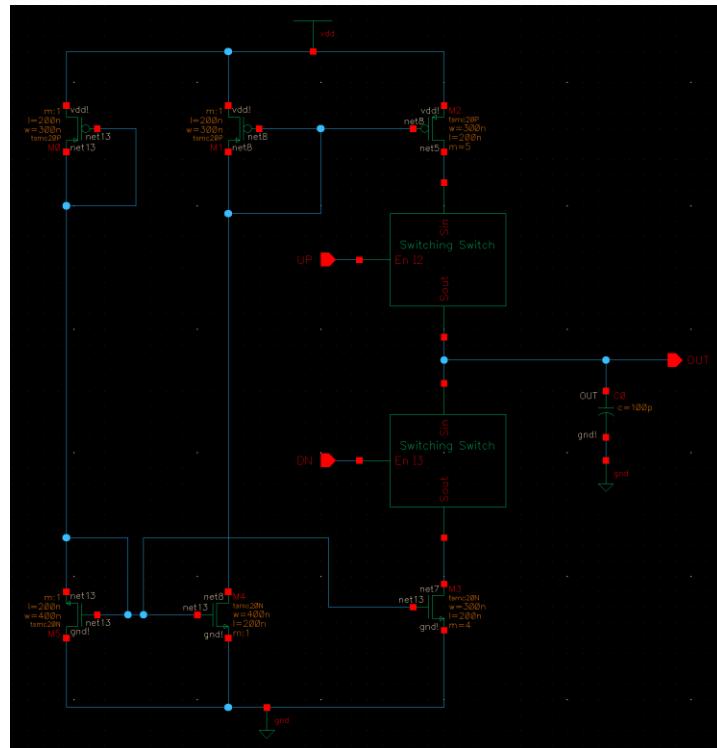


Fig 4: Charge Pump Schematic Simulation

Physical Layout -

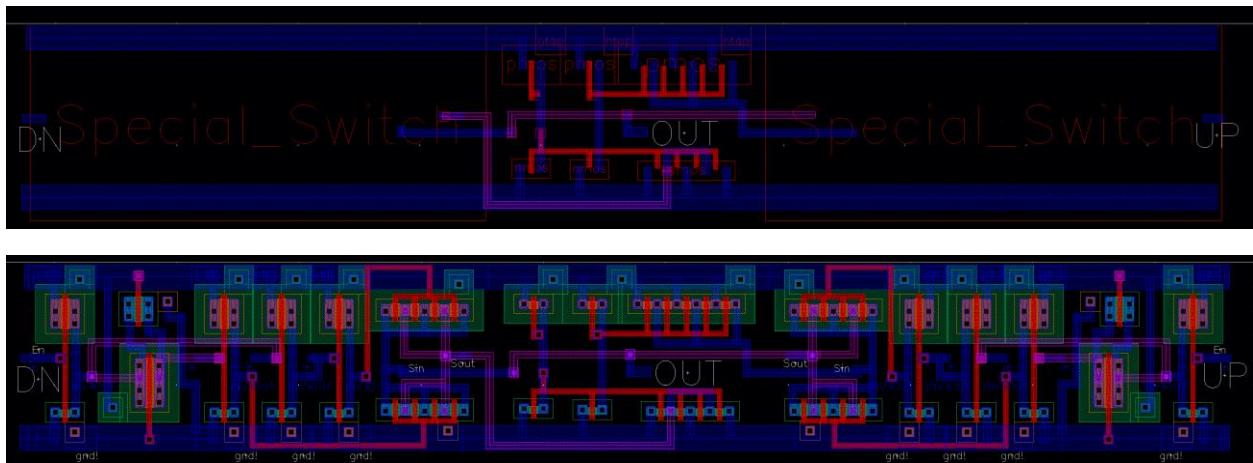


Fig 5: Charge Pump Layout

Layout Simulation -

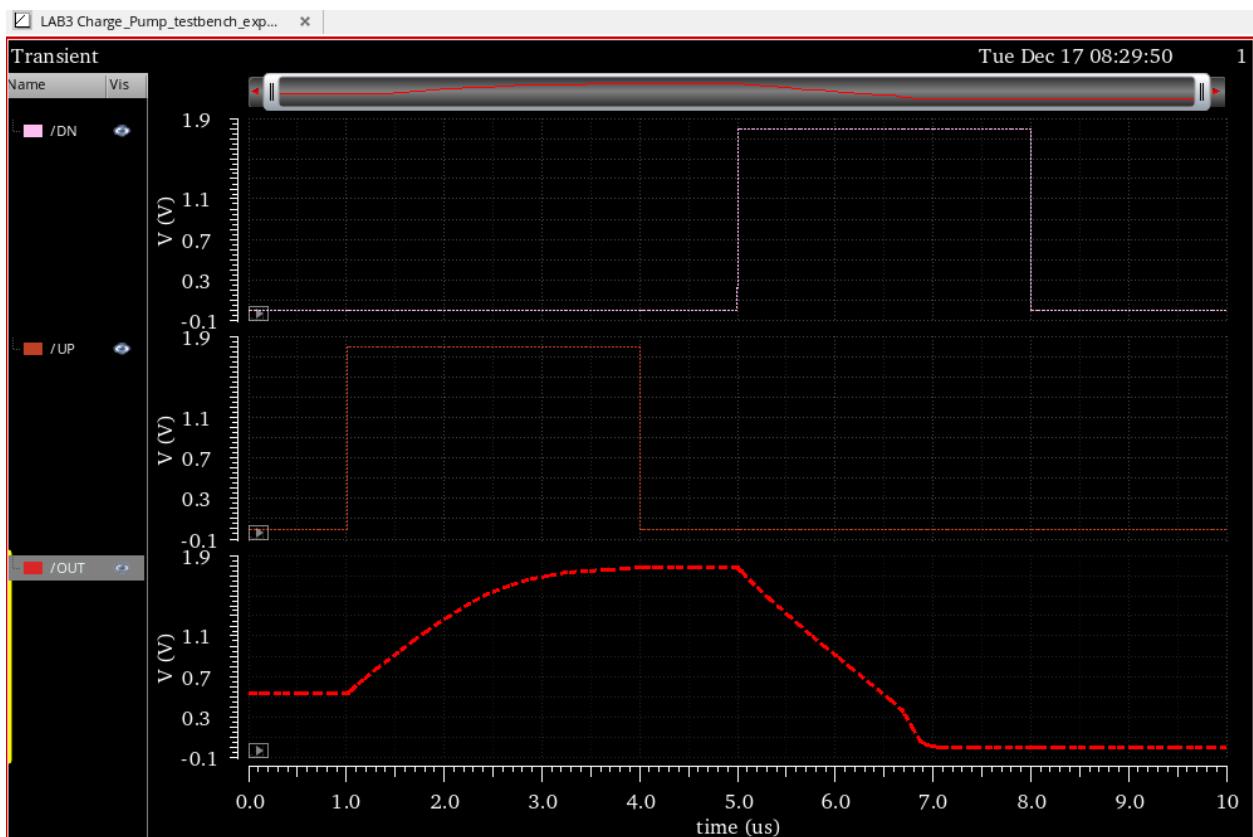


Fig 6: Charge Pump Test Bench Input Model - Layout

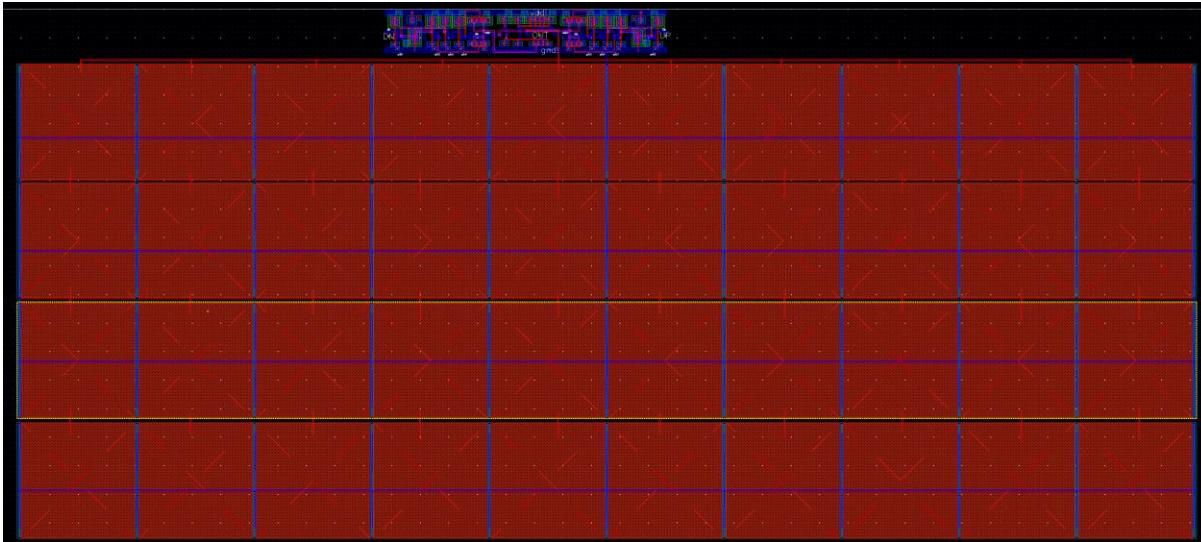


Fig 7: Charge Pump Test Bench Input Model

Layout vs. Schematics LVS result -



Fig 8: Layout Charge Pump with LVS match

Summary & Result –

We have successfully designed a Charge Pump which is providing the desired pulses to my loop circuit. When UP signal turns on, the source current source charges the output load capacitor, discharging it when DN signal turns on.

Voltage Controlled Oscillator

Transistor Level Circuit Schematic –

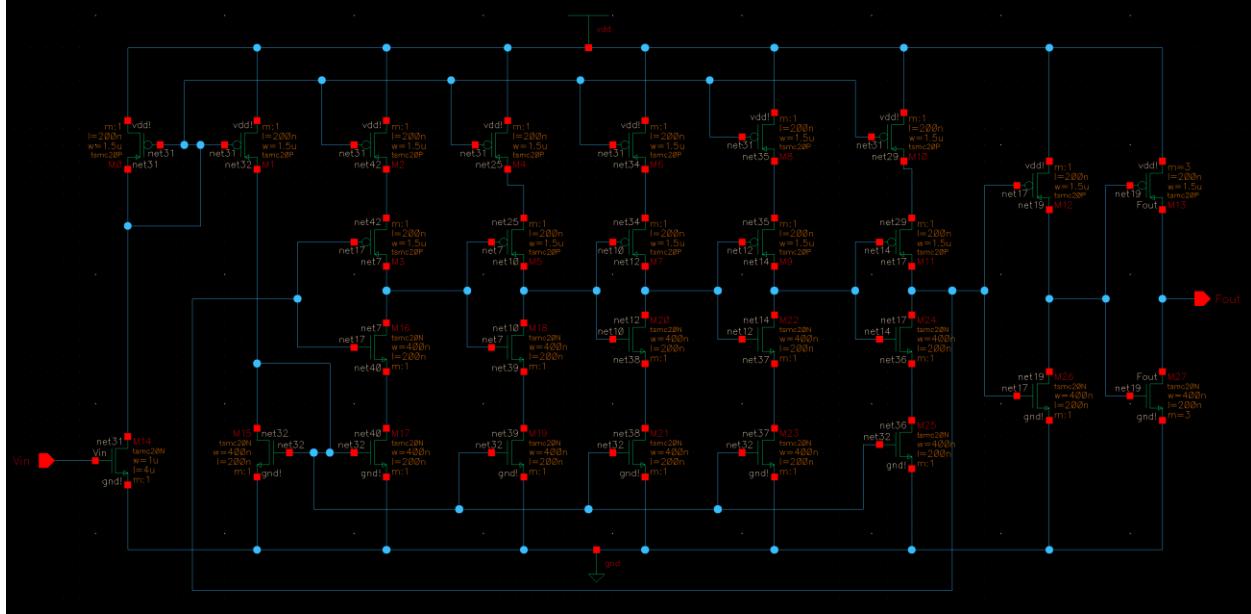


Fig 1: VCO Schematic

Description of circuit –

We have designed a (100MHz) voltage-controlled oscillator. Its oscillation frequency is controlled by current driving circuits which we designed using transistors working in saturation region. The voltage-controlled oscillator can be used for frequency modulation by applying modulating signal to the input current source. We have designed our circuit in order to generate the desired 100Mhz signal

Physical Layout -

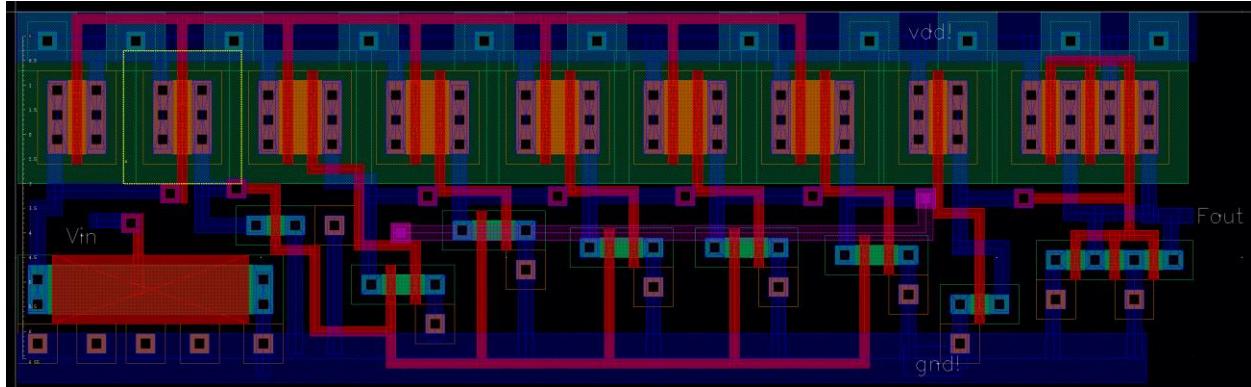


Fig 2: Voltage Controlled Oscillator Layout

Circuit Level Simulation -

Schematic's Waveform –

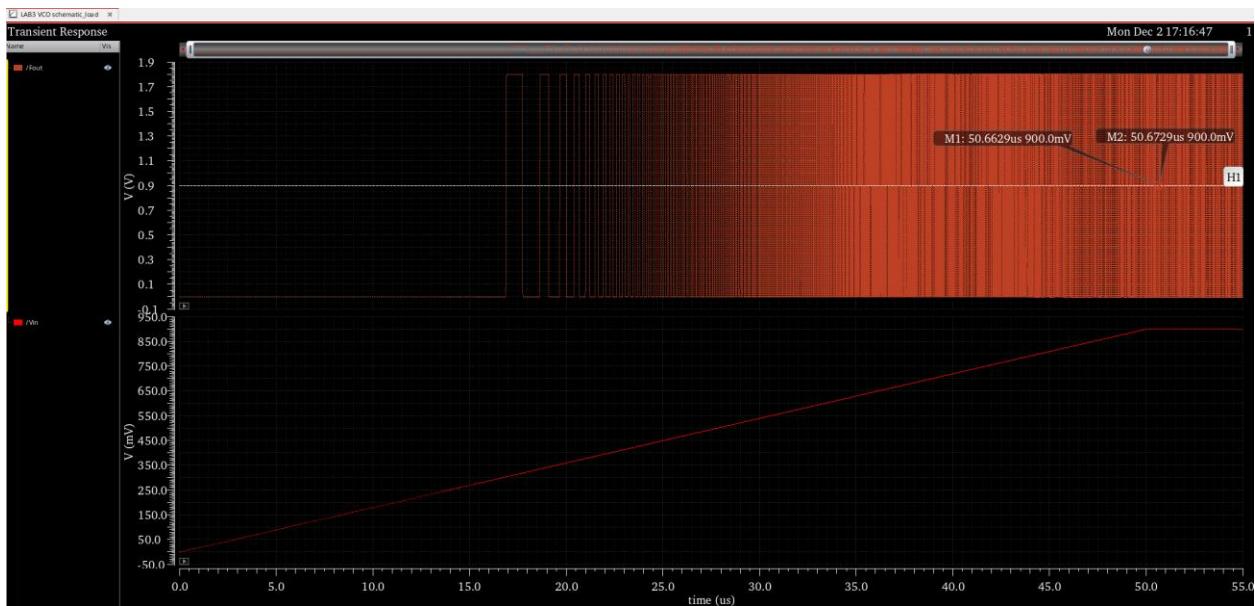


Fig 3: Schematic Waveform

Layout Simulation -

Layout's Waveform –

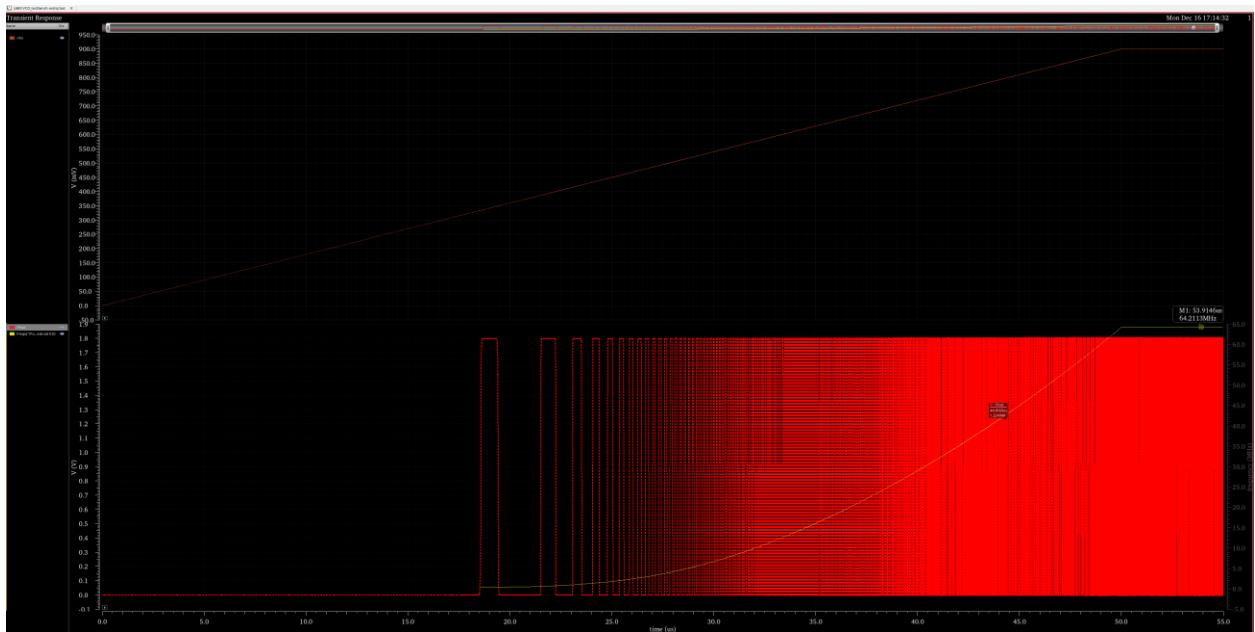


Fig 4: Layout Waveform

Layout vs. Schematic LVS result -

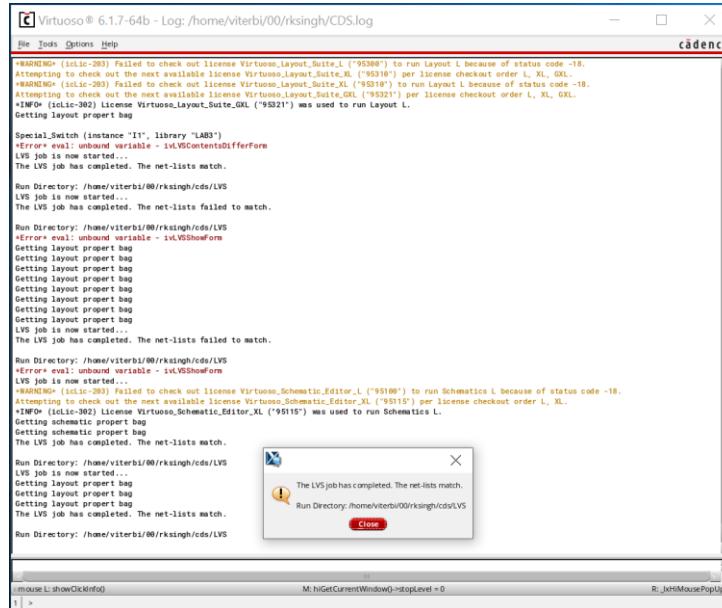


Fig 5: Load LVS match

Summary & Result –

We have successfully designed the (100MHz) voltage-controlled oscillator. VCO is the main block in the PLL that produces the required output clock frequency. VCO takes a DC input voltage and produces the required 50% duty cycle output clock frequency.

Divide by 3

Transistor Level Circuit Schematic –

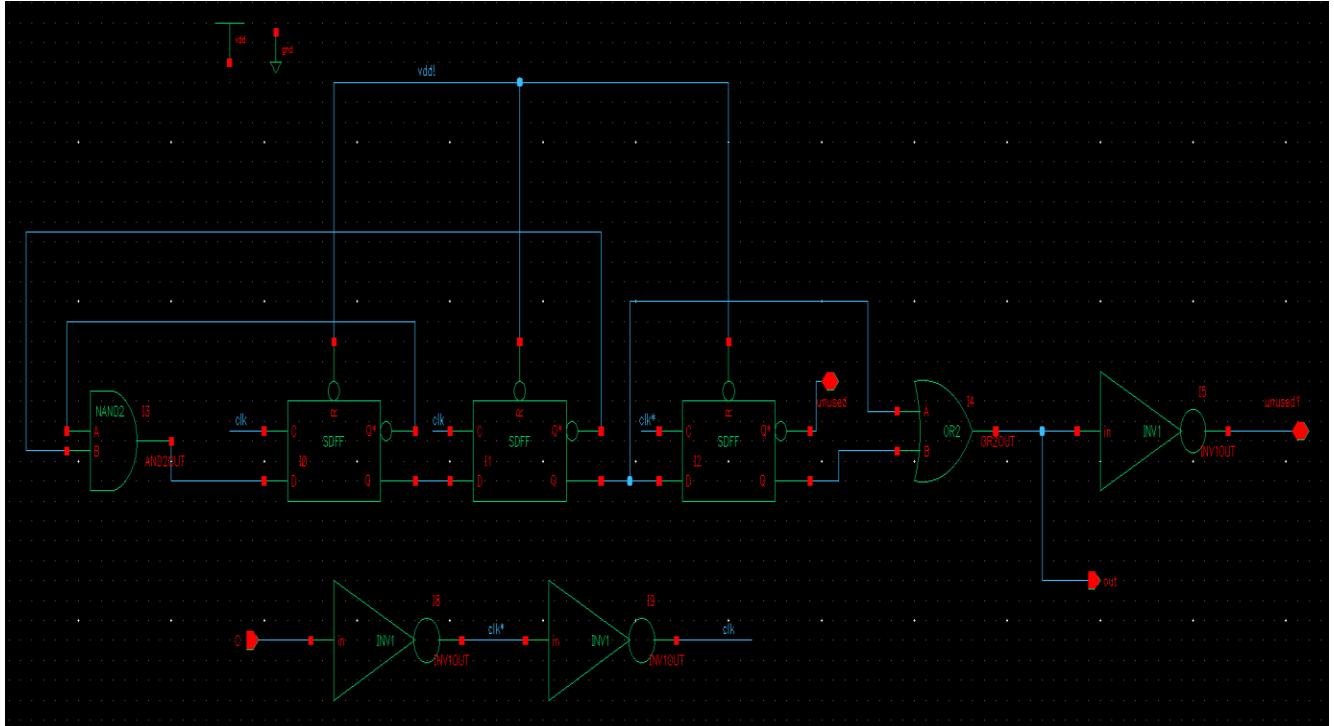


Fig 1: Divide by 3 Schematic

Description of circuit –

A Divide by 3 circuit is used for getting a derived clock which is equal to three times the reference clock, we have provided a 10ns period clock. So, the output clock generated will equal to 30ns. We will calculate the 50% rising edge delay and 50% falling edge delay. I have executed it by taking the voltage equal to 0.9V, which is (50% of 1.8) and calculated the rising clock to Q delay and the falling clock to Q delay.

For calculating the Maximum frequency, we have reduced our clock's time period to that limit when we don't receive the expected frequency divided output. So, our maximum input frequency is the last value of time period for which we are receiving correct output waveform, ie correct divide by three output.

Circuit Level Simulation -

Maximum Input Frequency Calculation –

We have reduced our clock's time period to that limit when we don't receive the expected frequency divided output. So, our maximum input frequency is the last value of time period for which we are receiving correct output waveform, ie correct divide by three output.

Schematic's Waveform –



Fig 2: Schematic Incorrect Output at data time period = 0.68ns

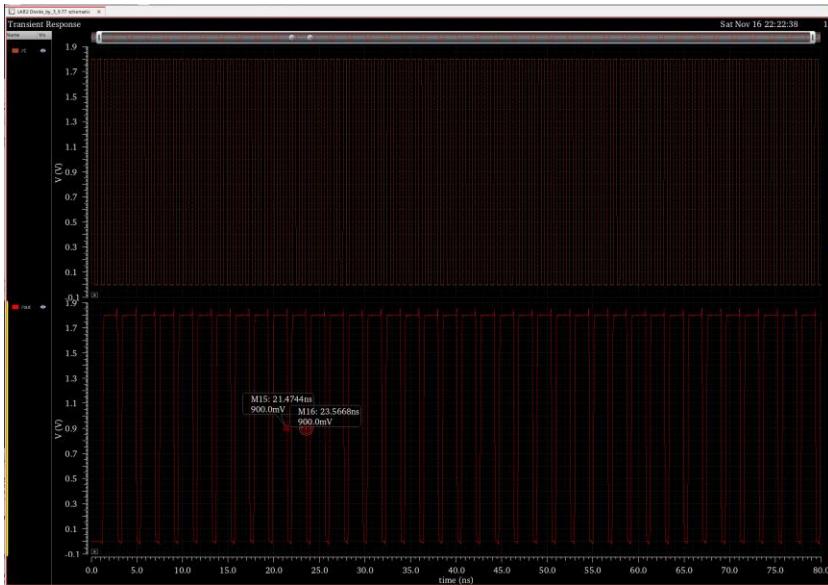


Fig 3: Schematic Correct/ Desired Output received at data time period = 0.69ns

So as per the calculation our schematic's maximum input frequency = $(1/0.69\text{ns})$, which is equal to 1449.27MHz.

50% output Rising and Falling edge delay Calculation –

We have calculated the 50% rising edge delay and 50% falling edge delay by taking the voltage of 0.9V, which is (50% of 1.8) as a reference in the clock signal, after which we have used markers to calculate the difference in the time period between the clock and the output signal. The difference will provide us with the required output.

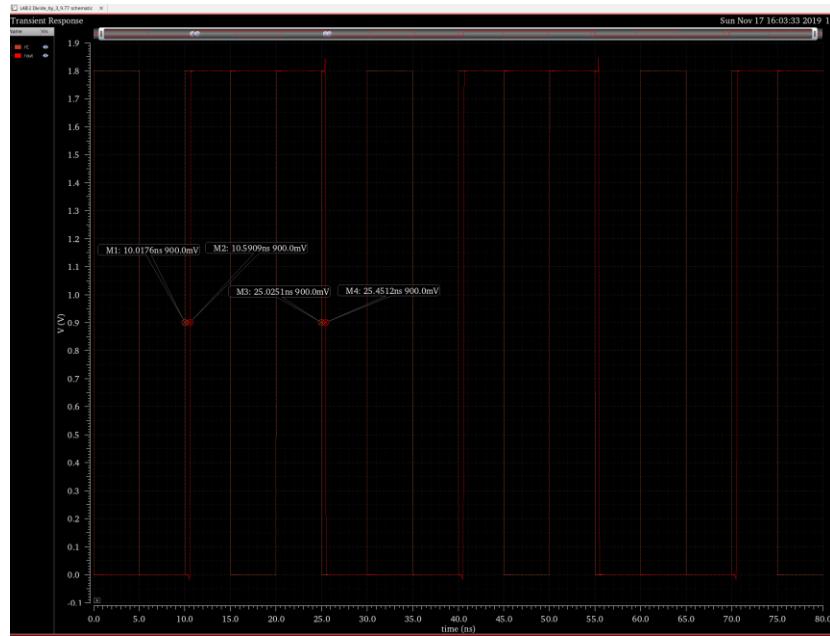


Fig 4: Schematic 50% Rising and Falling edge delay calculation

Physical Layout –

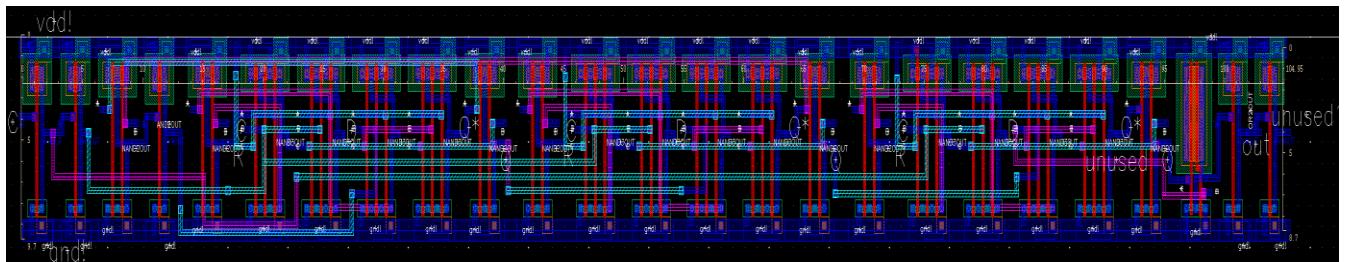


Fig 5: Divide by 3 Layout

Layout Simulation -

Maximum Input Frequency Calculation –

We have reduced our clock's time period to that limit when we don't receive the expected frequency divided output. So, our maximum input frequency is the last value of time period for which we are receiving correct output waveform, ie correct divide by three output.

Layout's Waveform –

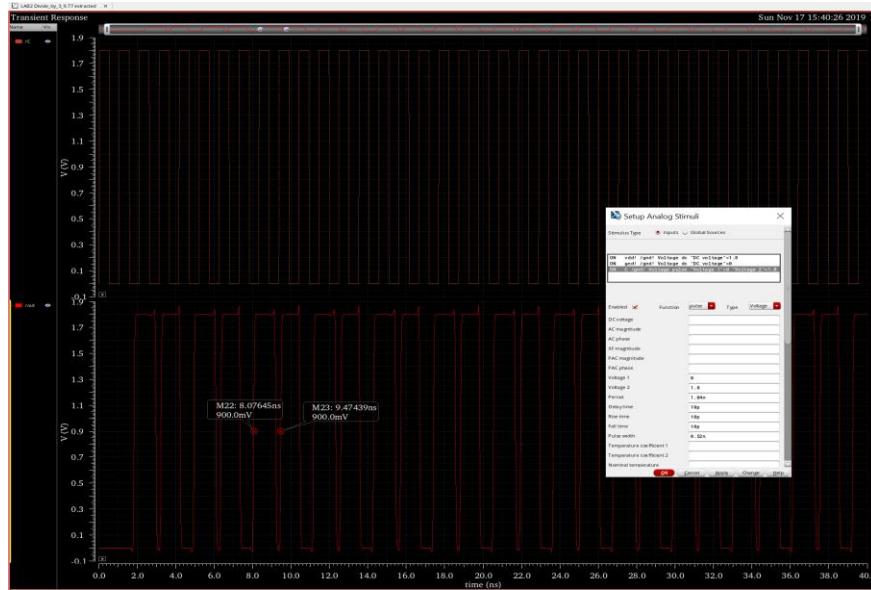


Fig 6: Layout Incorrect Output at data time period = 1.04ns

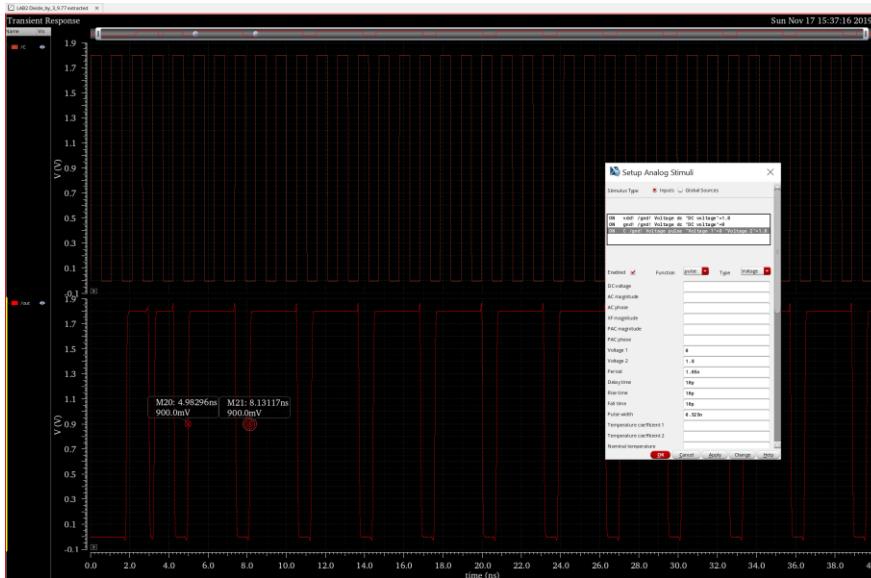


Fig 7: Layout Incorrect Output at data time period = 1.05ns

So as per the calculation our layout's maximum input frequency = $(1/1.05\text{ns})$, which is equal to 952.38 MHz.

50% output Rising and Falling edge delay Calculation –

We have calculated the 50% rising edge delay and 50% falling edge delay by taking the voltage of 0.9V, which is (50% of 1.8) as a reference in the clock signal, after which we have used markers to calculate the difference in the time period between the clock and the output signal. The difference will provide us with the required output.

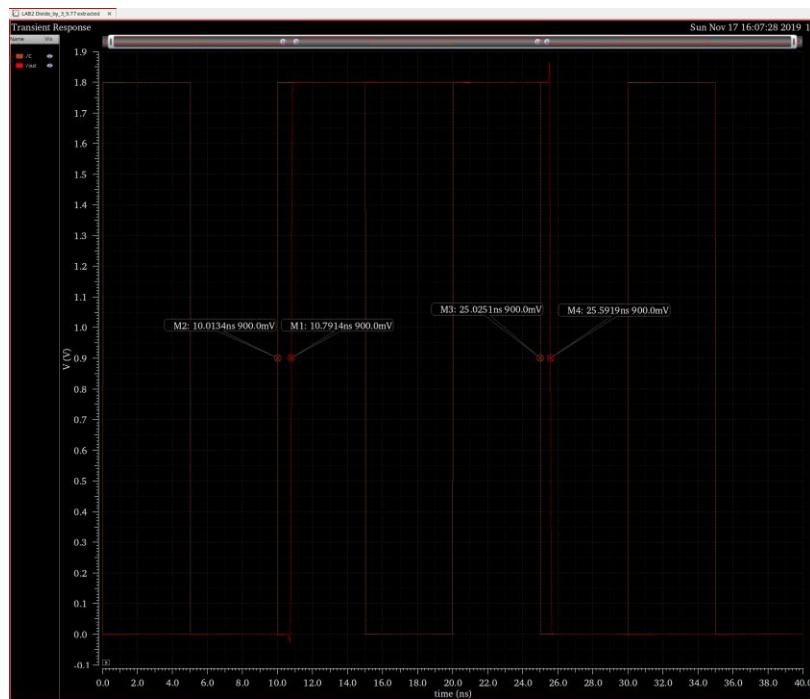


Fig 8: Extracted 50% Rising and Falling edge delay calculation

Layout vs. Schematic LVS result -

The figure shows a screenshot of the Cadence Virtuoso 6.1.7-64b software interface. The title bar reads "Virtuoso® 6.1.7-64b - Log: /home/viterbi/00/rksingh/CDS.log". The menu bar includes File, Tools, Options, Help, and a Cadence logo. The main window displays a log file with the following content:

```
DRC started.....Fri Nov 15 14:57:07 2019
completed ....Fri Nov 15 14:57:07 2019
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "Divide_by_3_9.77 layout" *****
Total errors found: 0
```

The bottom status bar shows mouse coordinates and keyboard shortcuts: "mouse L: showClickInfo()", "M: setDRCForm()", "R: _lxHiMouse PopUp()", "1 | >".

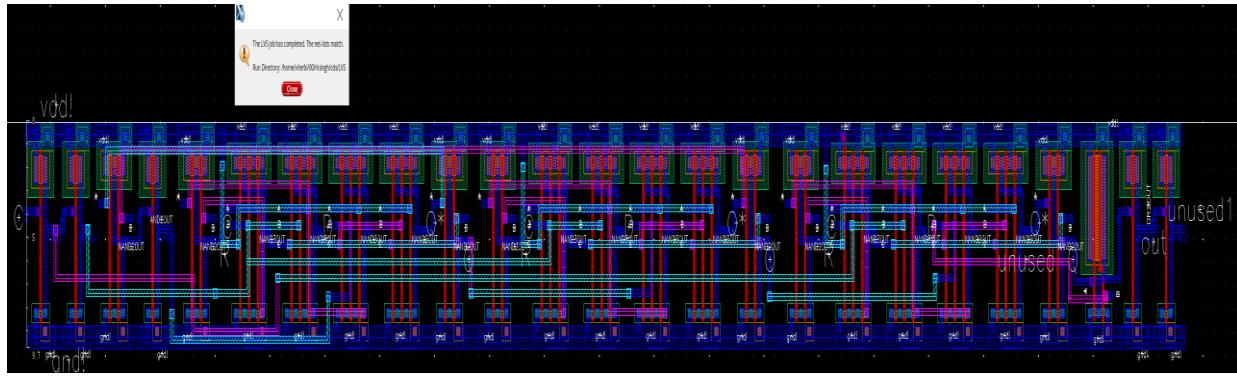


Fig 9: Layout Divide by three with Load LVS match

Cell	Layout Height (μm)	Layout Width (μm)	Layout Area (μm^2)
Divide by 3	8.7	104.95	913.065

Table 3 –

Cell Divided by 3	Maximum input frequency (MHz)	Rising edge 50% delay (ns)	Falling edge 50% delay (ns)
Circuit	1449.27	0.5733	0.4261
Layout	952.38	0.7776	0.5668

Summary & Result –

Comparing the 50% delay of the rising edge and the falling edge of the schematic and layout we can see that the rise time and fall times increase when we extract the waveform from our layout, compared to when we extract it from our schematic. Also, the Maximum Frequency for the schematic is more than that of the layout. The maximum input frequency denotes the maximum frequency for which we receive a correct output, any frequency above the maximum frequency would give us incorrect output, or a glitched output.

Phase Locked Loop

Transistor Level Circuit Schematic –

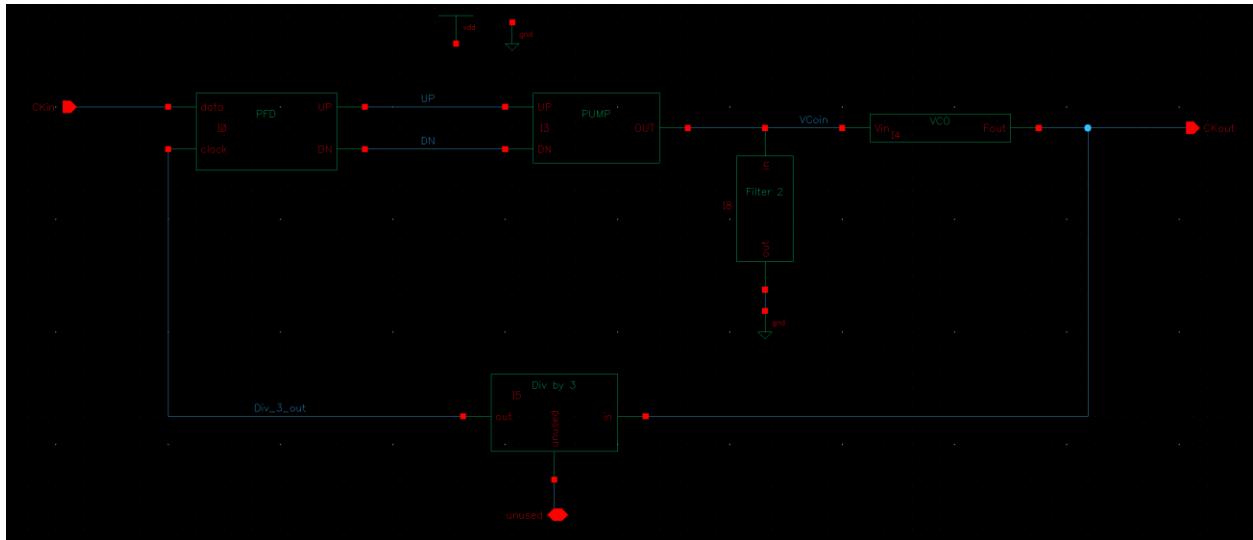


Fig 1: Phase Locked Loop Schematic

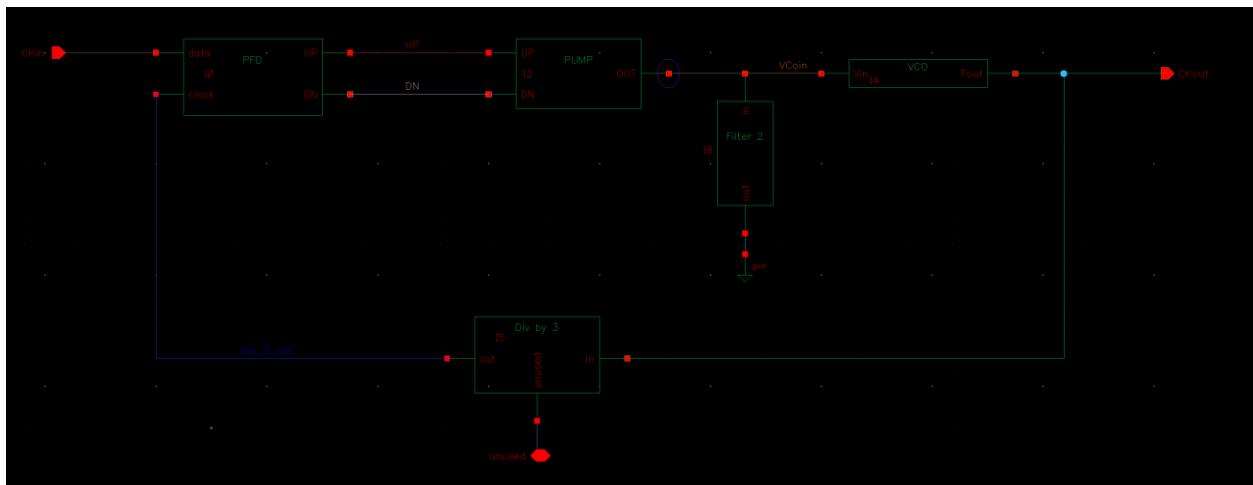
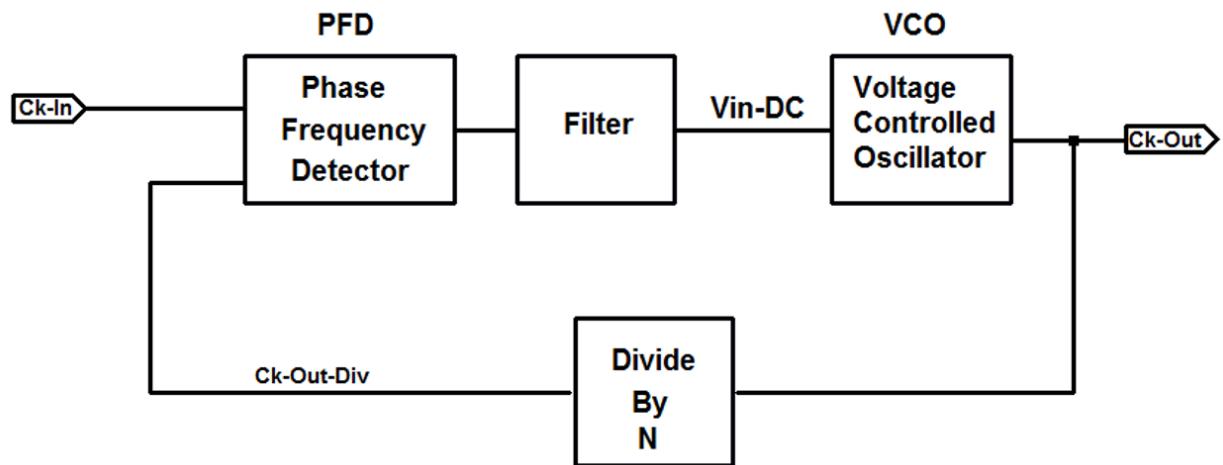
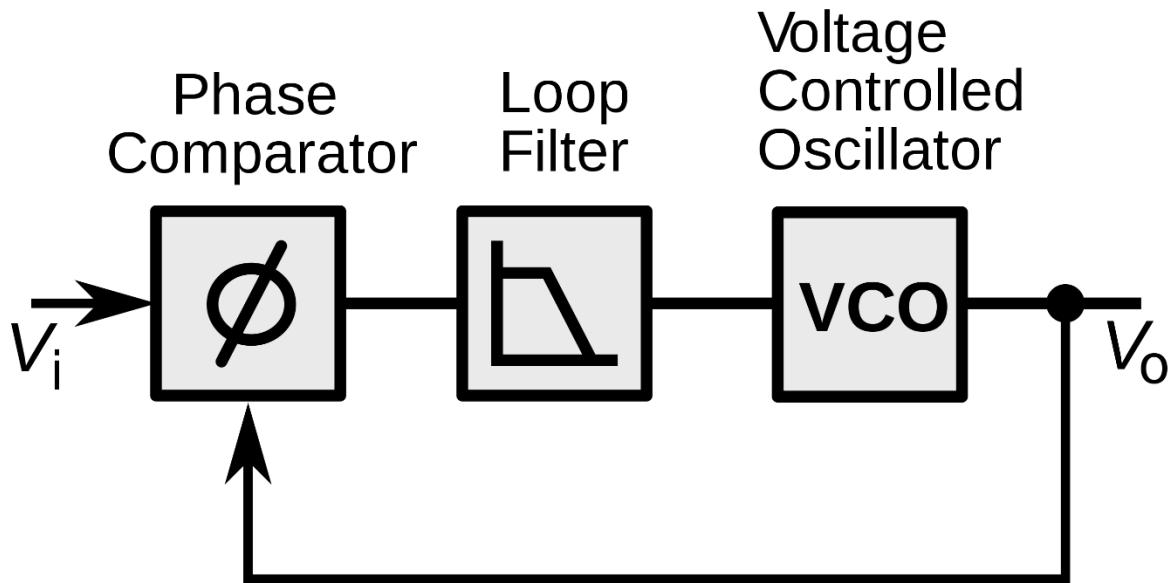


Fig 2: PLL Testbench

Description of circuit –



The Phase locked loop is a feedback loop which accepts an input pulse and generates an output voltage whose phase is related to the phase of an input signal. The phase lock loop compares the phase of the reference signal with the phase of the feedback signal, in our case the feedback signal is 100MHz/3 and the input signal is at a phase of frequency equal to 33.33MHz.

The below are the un-optimized simulations and layout having M=100 for my loop filter, I have further tried different variations and have optimized my circuit to work with M=14 for my loop filter, which will be covered in the optimized section.

Circuit Level Simulation –

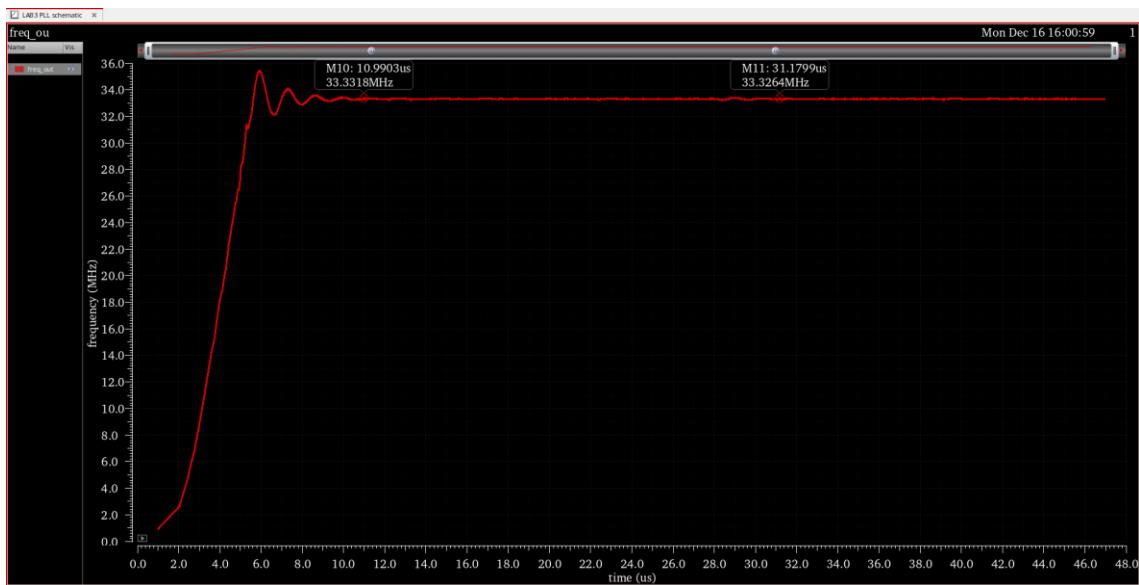


Fig 3: Divide by 3 output Schematic at $m=100$, 25°C

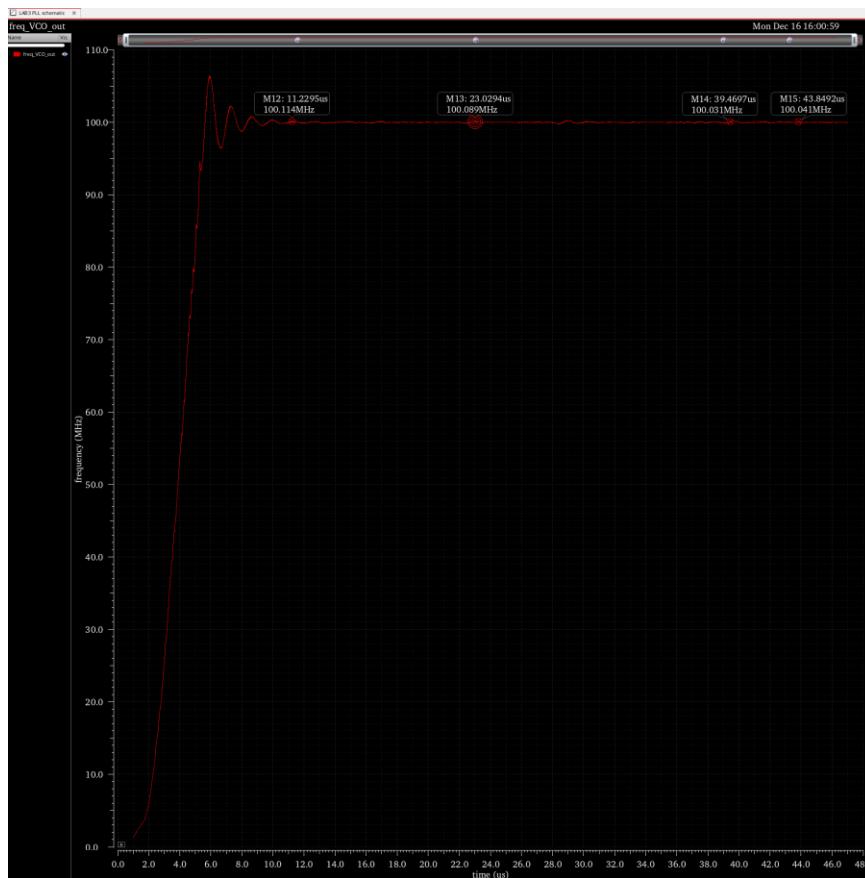


Fig 4: VCO output Schematic at $m=100$, 25°C

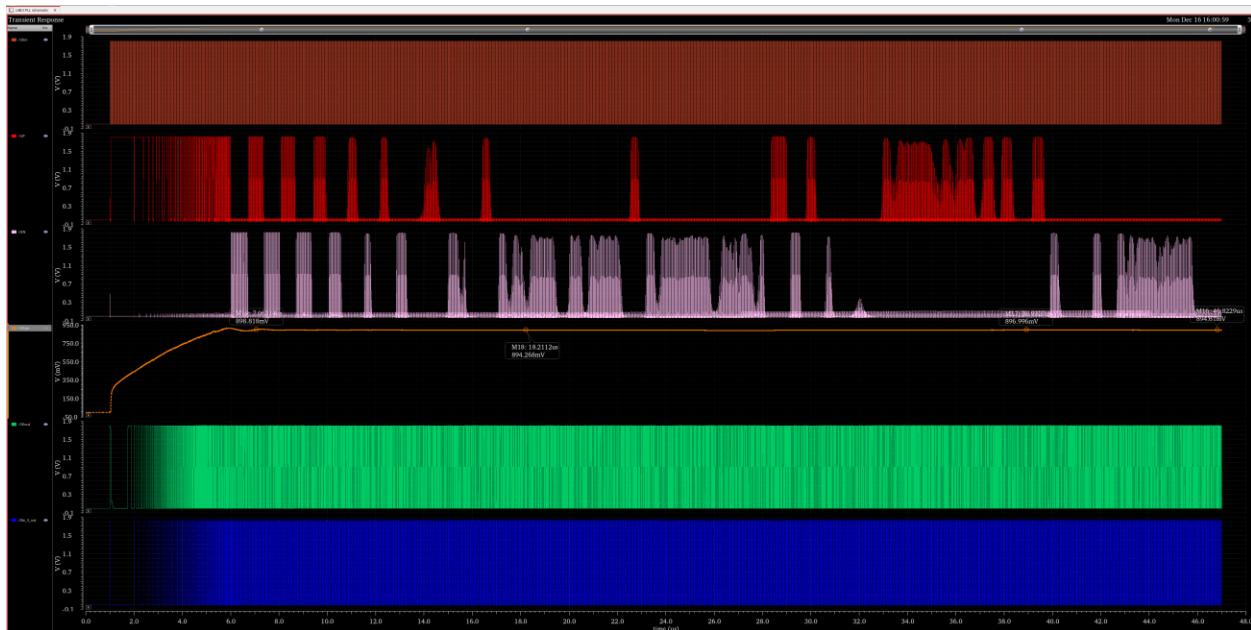


Fig 5: Phase Locked Loop Schematic at $m=100$, 25°C

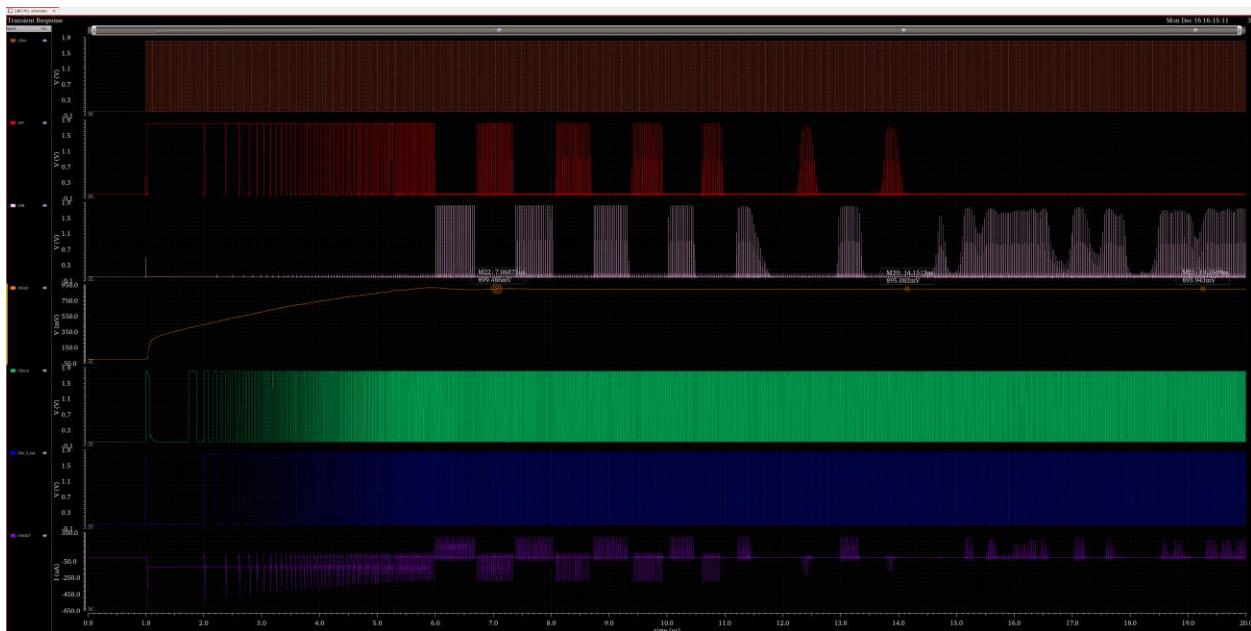


Fig 6: Phase Locked Loop Schematic at $m=100$, 25°C (including Current Calculation)

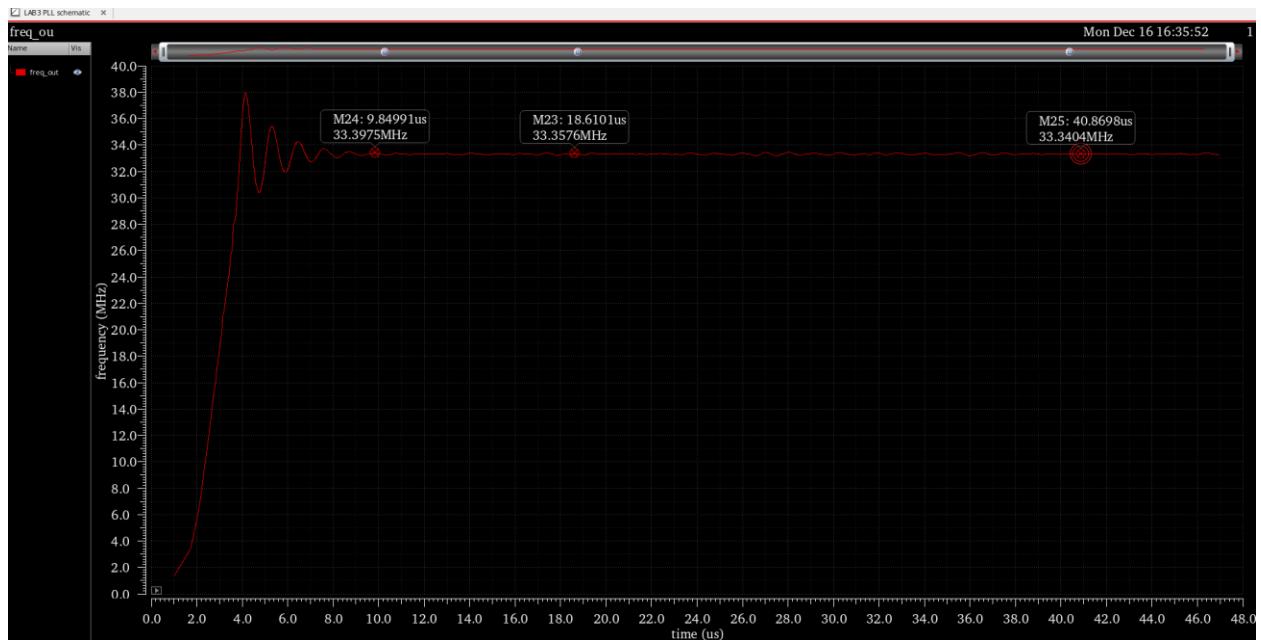


Fig 7: Divide by 3 output Schematic at $m=100$, -25°C

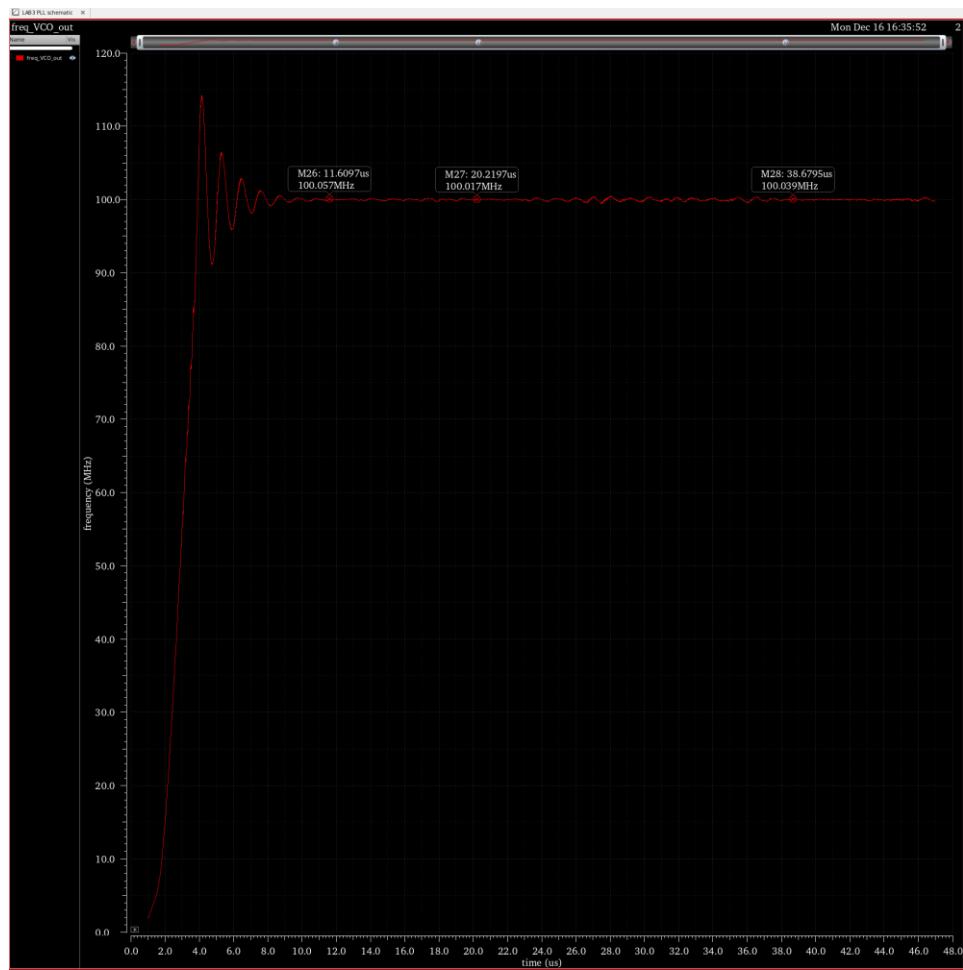


Fig 8: VCO output Schematic at $m=100$, -25°C

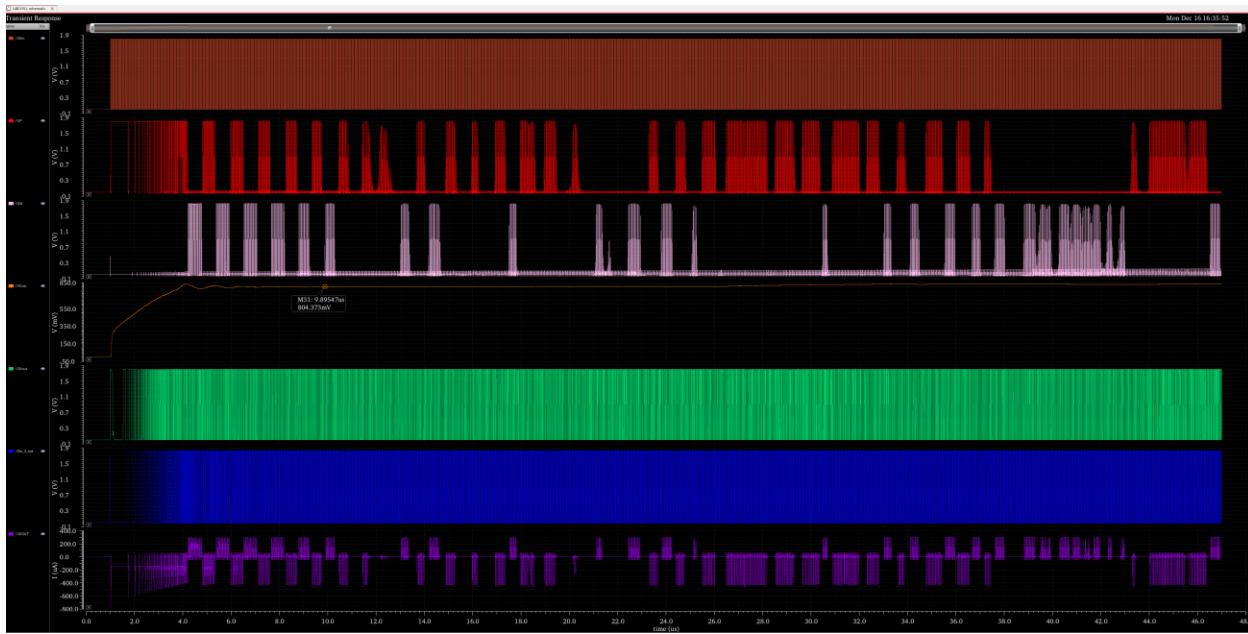


Fig 9: Phase Locked Loop Schematic at $m=100$, -25°C (including current calculation)



Fig 10: Divide by 3 output Schematic at $m=100$, 75°C

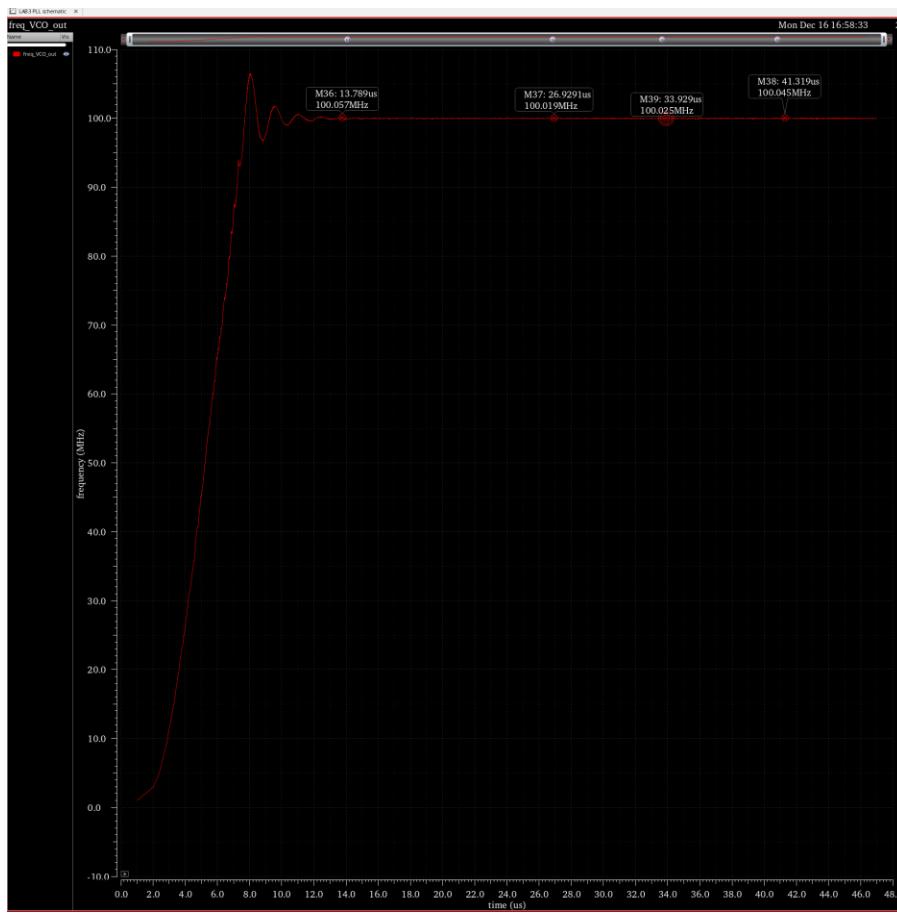


Fig 11: VCO output Schematic at $m=100$, 75°C

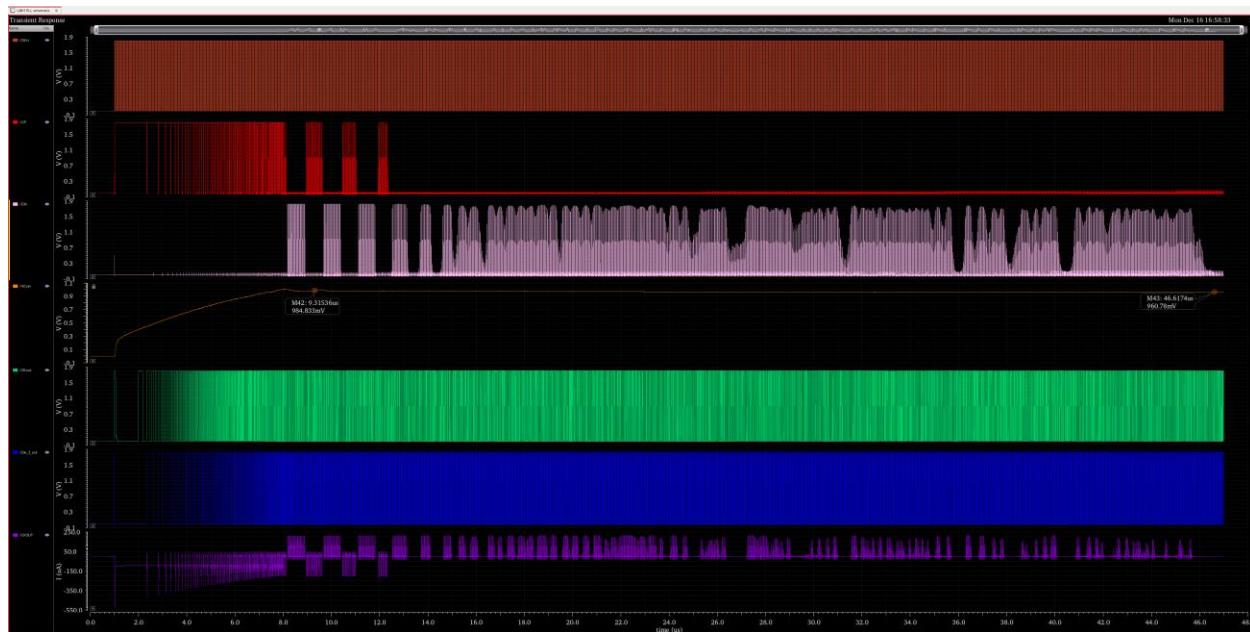


Fig 12: Phase Locked Loop Schematic at $m=100$, 75°C (including current calculation)

Physical Layout -

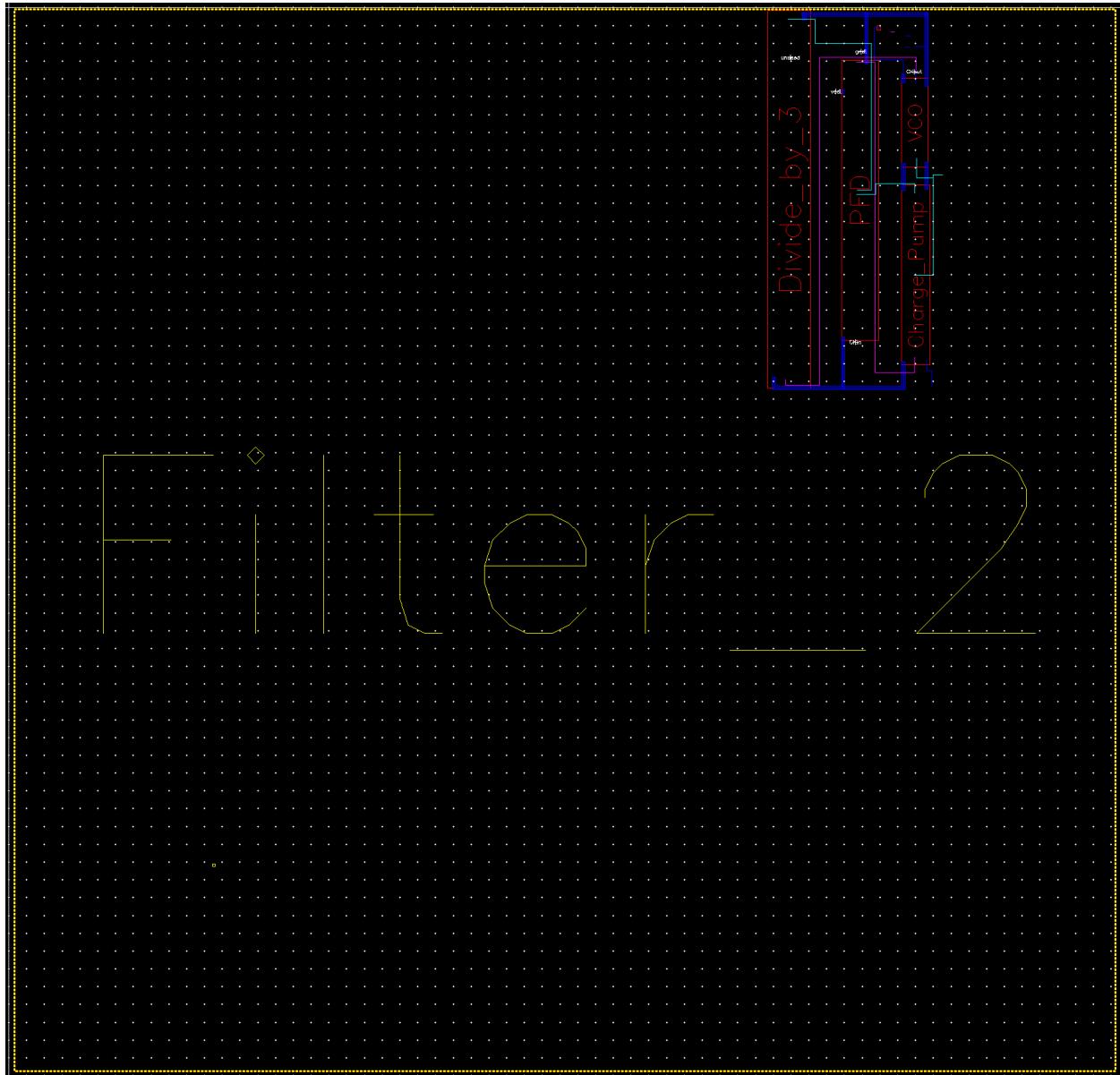


Fig 13: Phase Lock Loop Layout, M=100

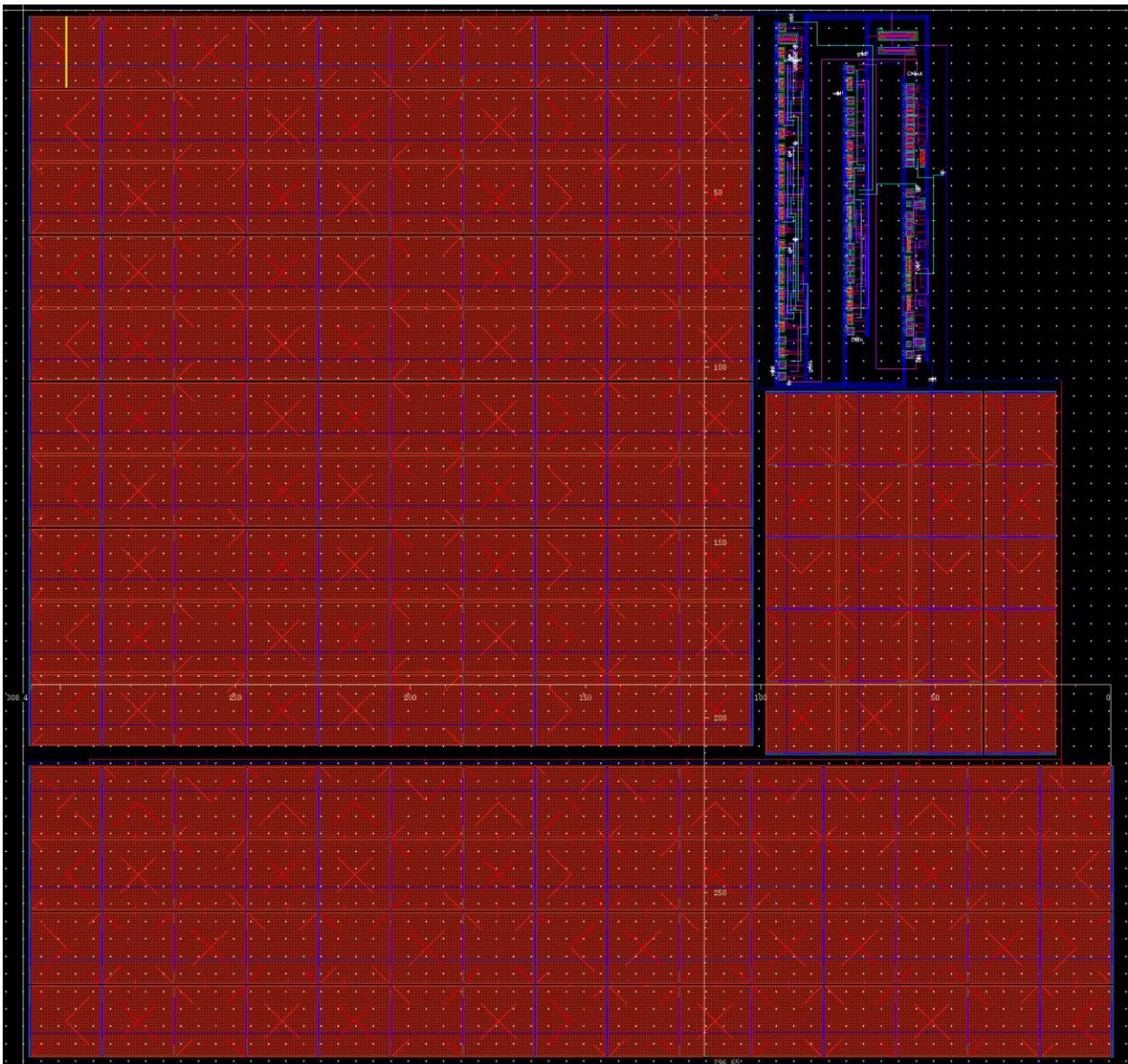


Fig 14: Phase Lock Loop Layout, M=100

If you notice, the layout is designed in such a way that it forms a square – optimum area utilization.

Layout Simulation –

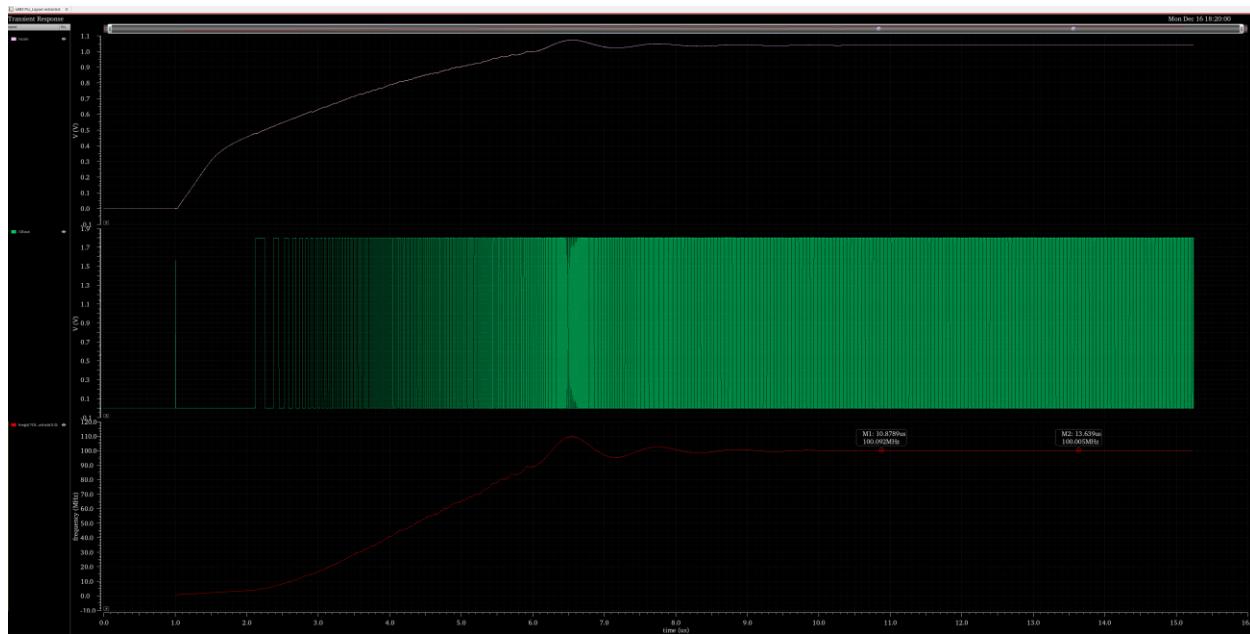


Fig 15: VCO output Layout at $m=100$, 25°C

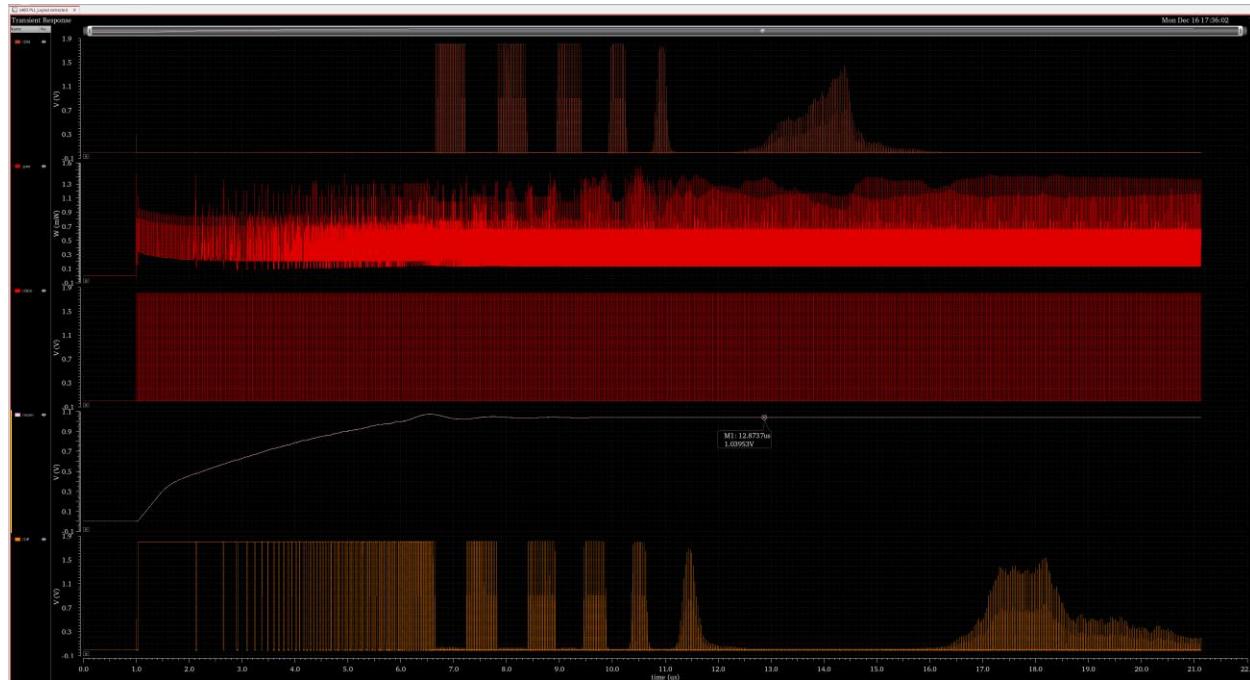


Fig 16: Phase Locked Loop Layout at $m=100$, 25°C

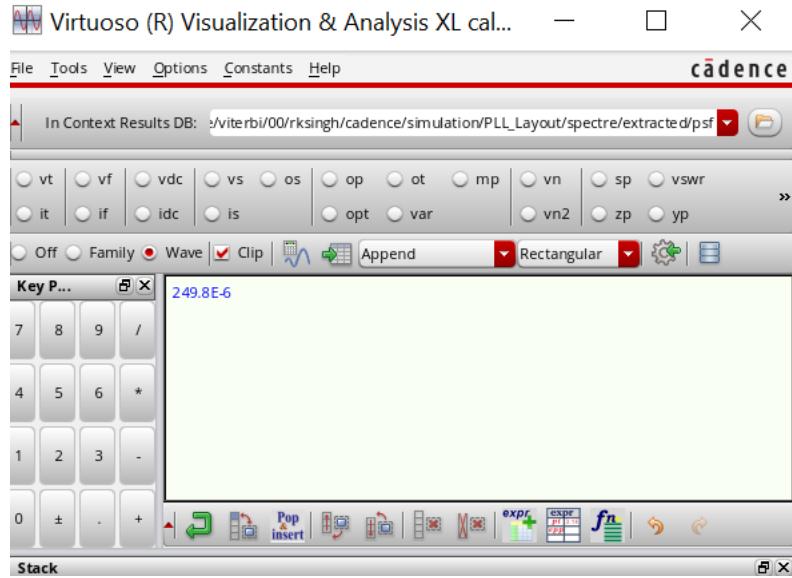


Fig 17: Phase Locked Loop Schematic (average current calculation) at m=100, 25 °C

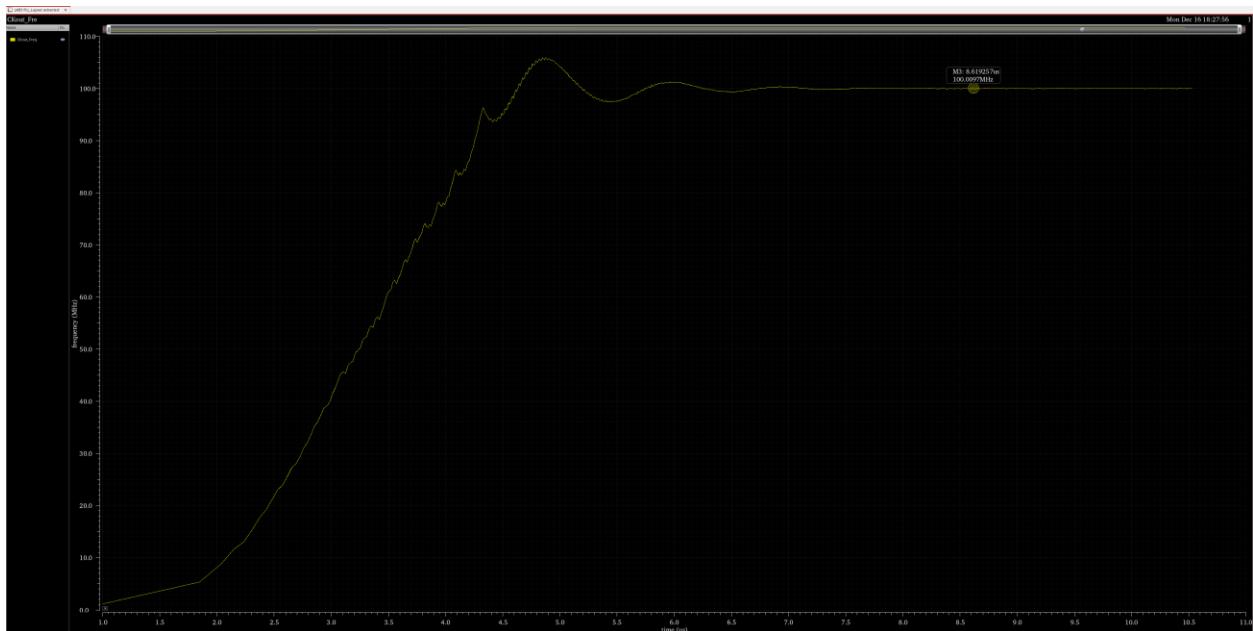


Fig 18: VCO output Layout at m=100, -25 °C

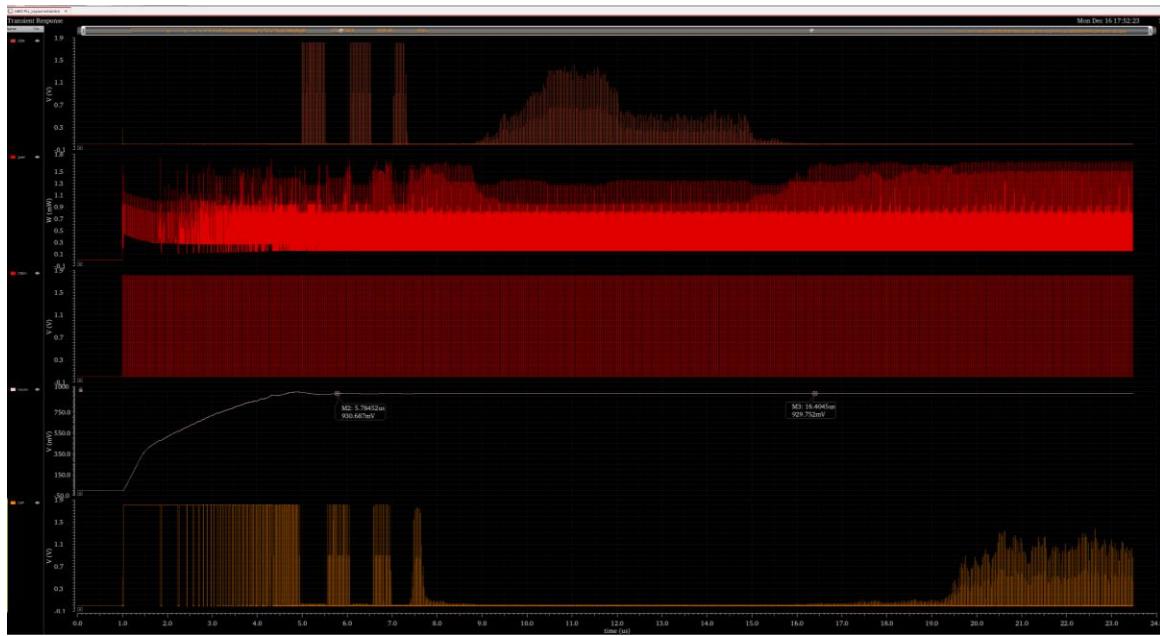


Fig 19: Phase Locked Loop Layout at $m=100$, -25°C

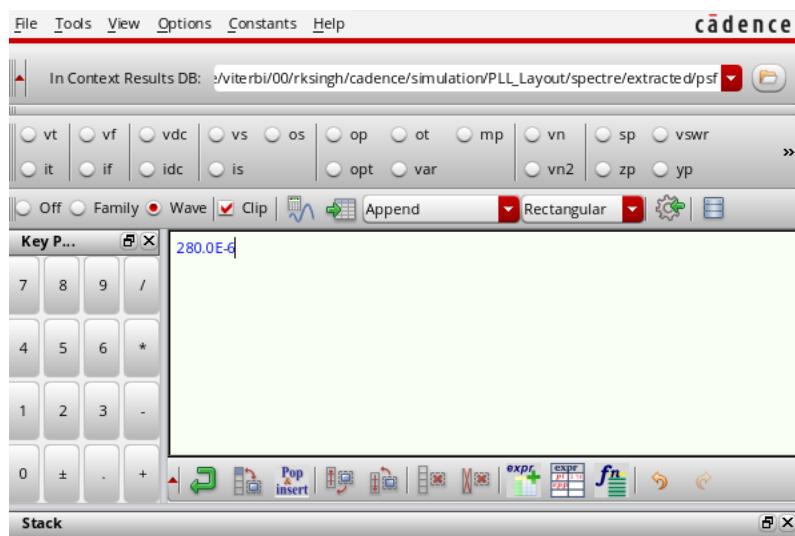


Fig 20: Phase Locked Loop Schematic (average current calculation) at $m=100$, -25°C

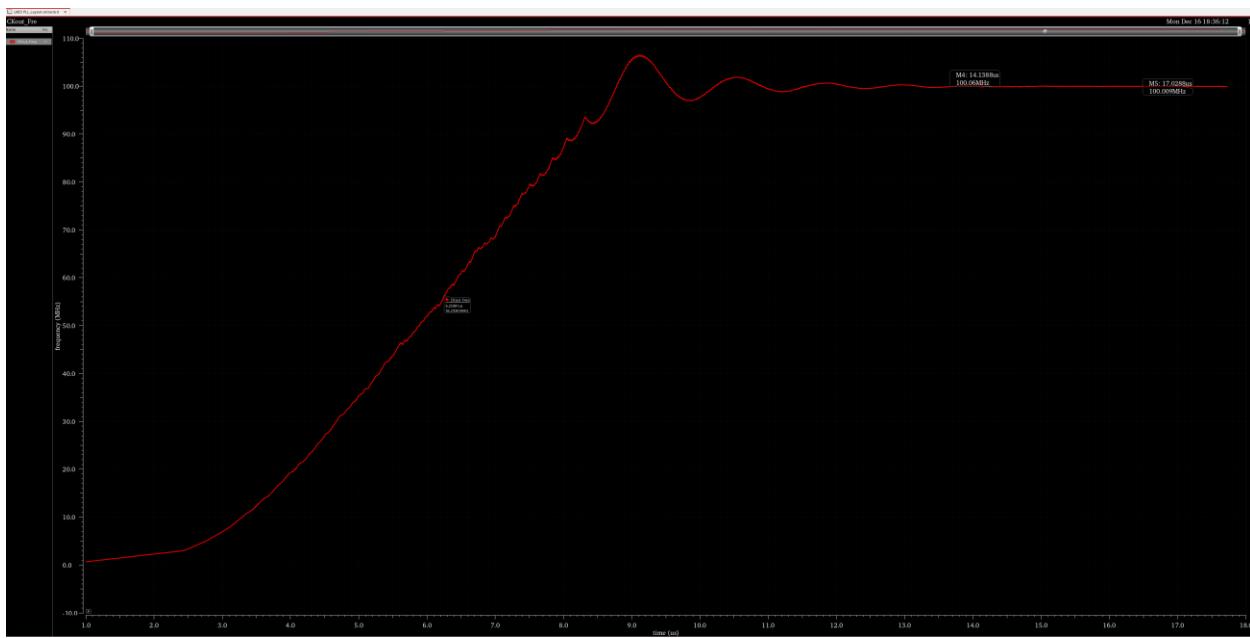


Fig 21: VCO output Layout at $m=100$, 75°C

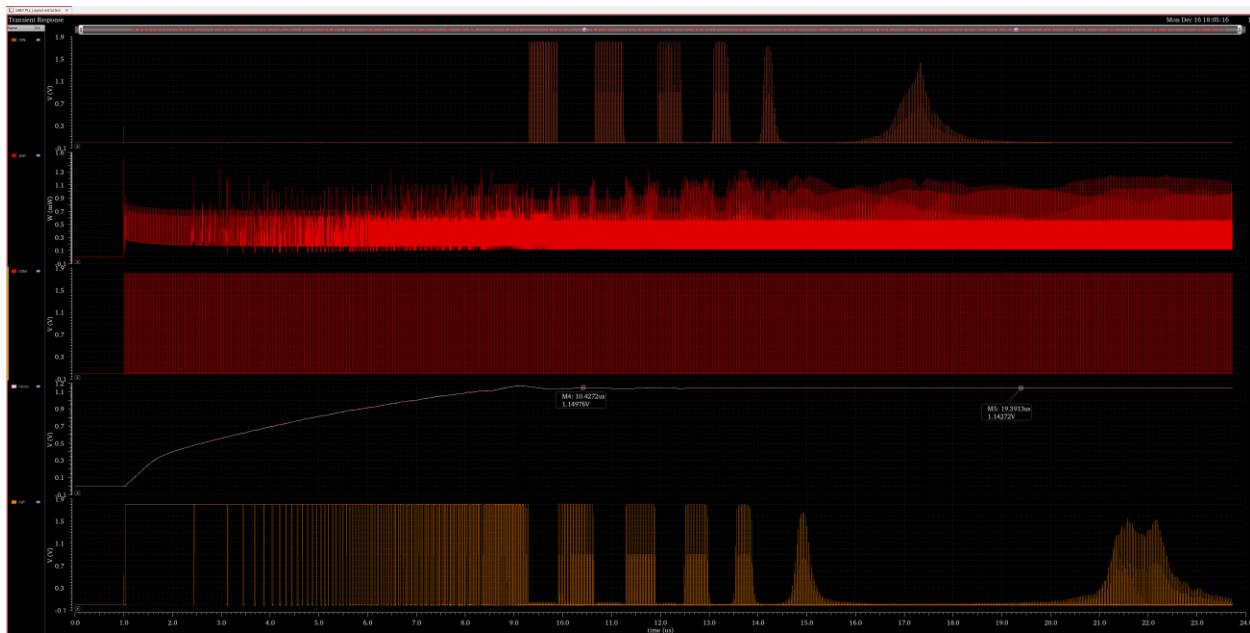


Fig 22: Phase Locked Loop Layout at $m=100$, 75°C

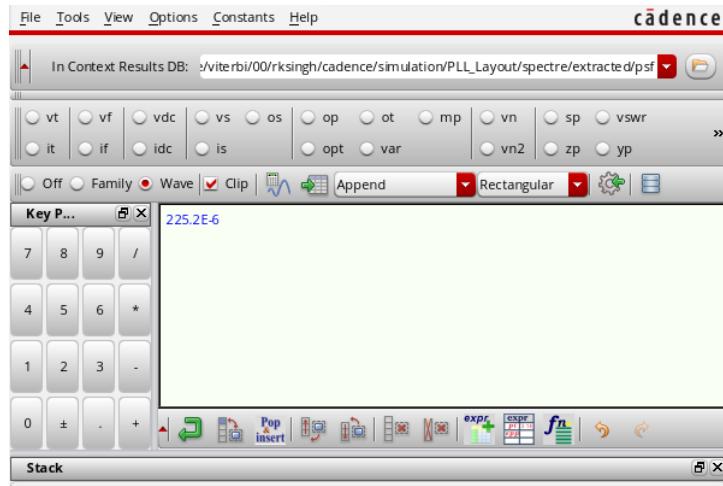


Fig 23: Phase Locked Loop Schematic (average current calculation) at m=100, 75 °C

Layout vs. Schematics LVS result –

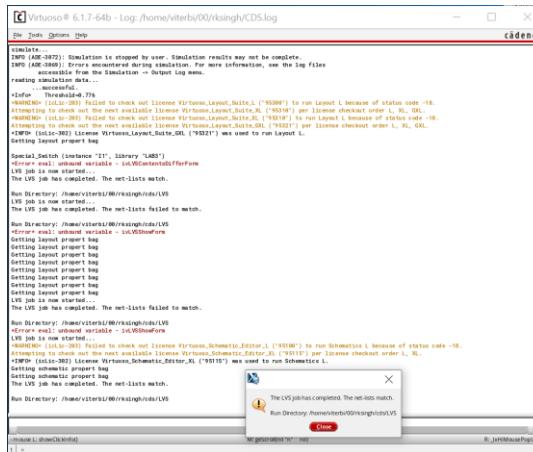


Fig 24: Layout Divide by three with Load LVS match

Optimized Circuit:

In order to optimize my circuit, I have reduced the value of the loop Filter, and significantly reduced the area.

Previously, I was using $m=100$, for my loop filter but right now I am using m as 14.
I have executed the calculations according to the reduced circuit.

As instructed by Professor, I have made sure that my circuit is a square shaped design.

Transistor Level Circuit Schematic –

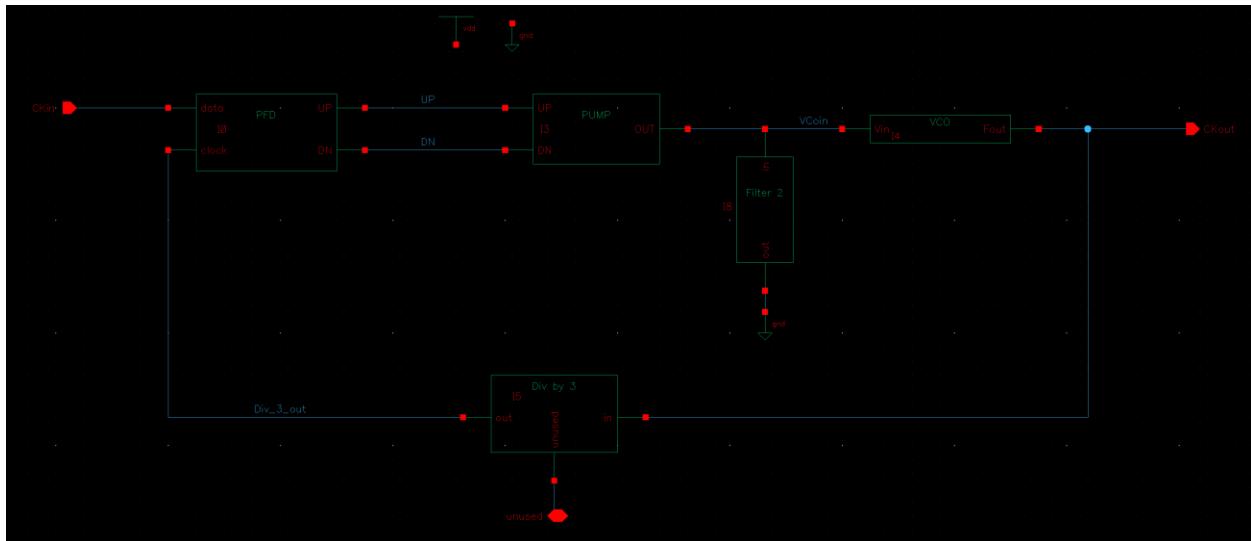


Fig 1: Phase Locked Loop Schematic (average current calculation) at $m=14$

Circuit Level Simulation -

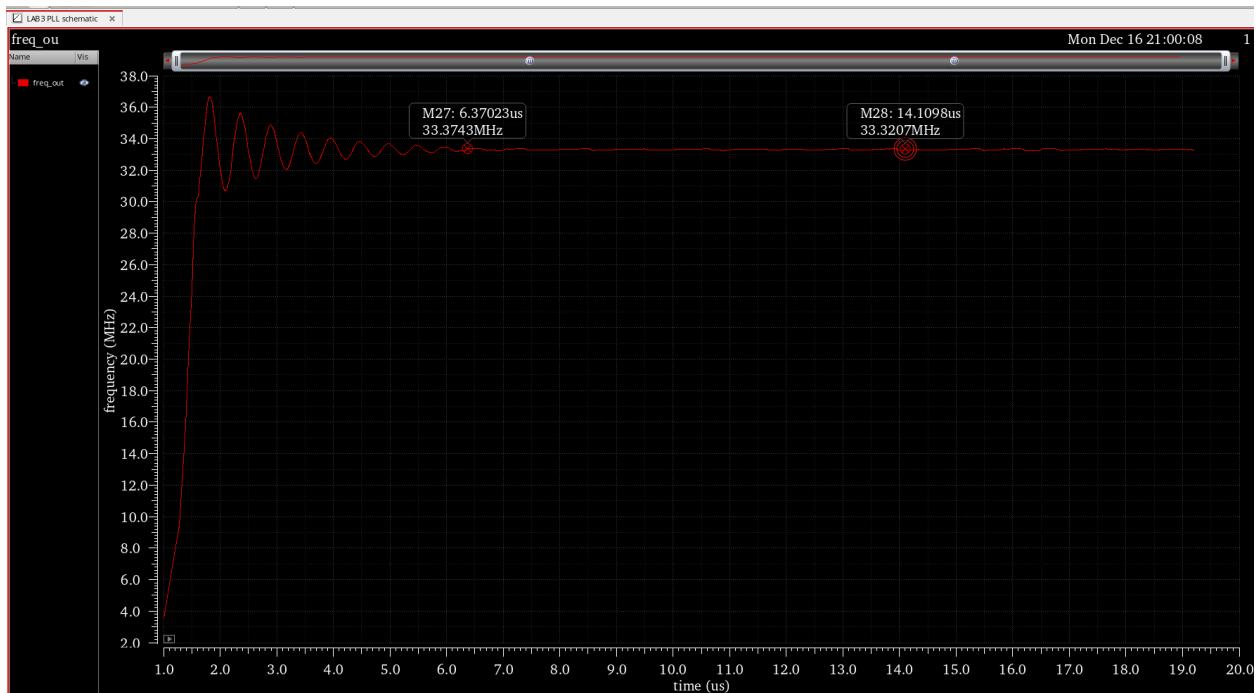


Fig 2: Divide by 3 output Schematic at $m=14$, $T = 25^{\circ}\text{C}$

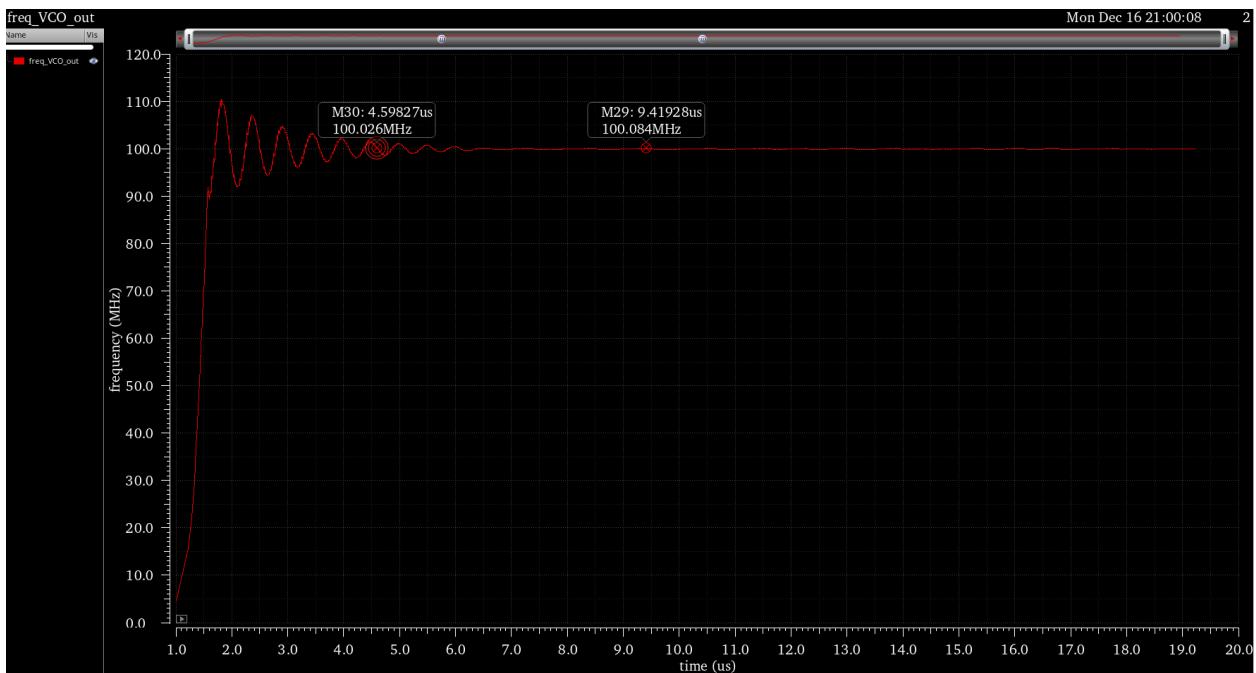


Fig 3: VCO output Schematic at $m=14$, $T = 25^{\circ}\text{C}$

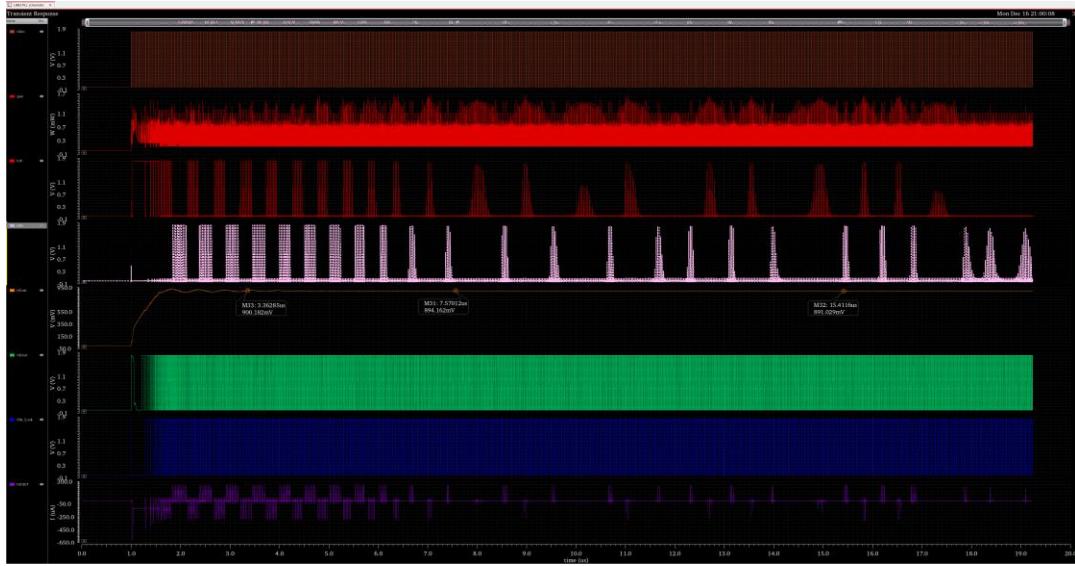


Fig 4: PLL output Schematic at m=14, T =25 °C (including current and power calculation)

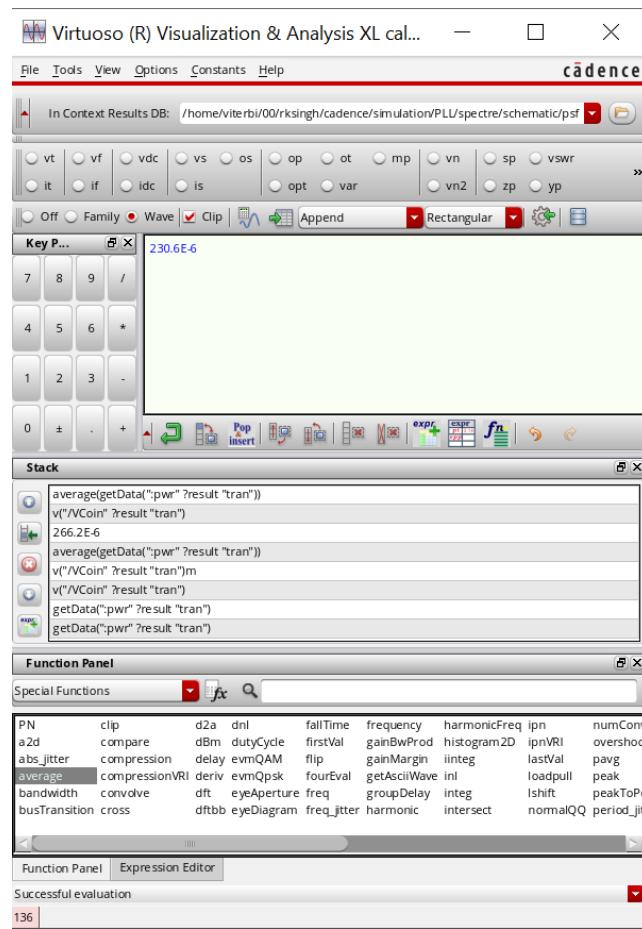


Fig 5: PLL output Schematic at m=14, T =25 °C (including average Power calculation)

Hence the average current calculation is as follows = $230.6 \text{ E-6} / 1.8 = 128.1 \mu\text{A}$

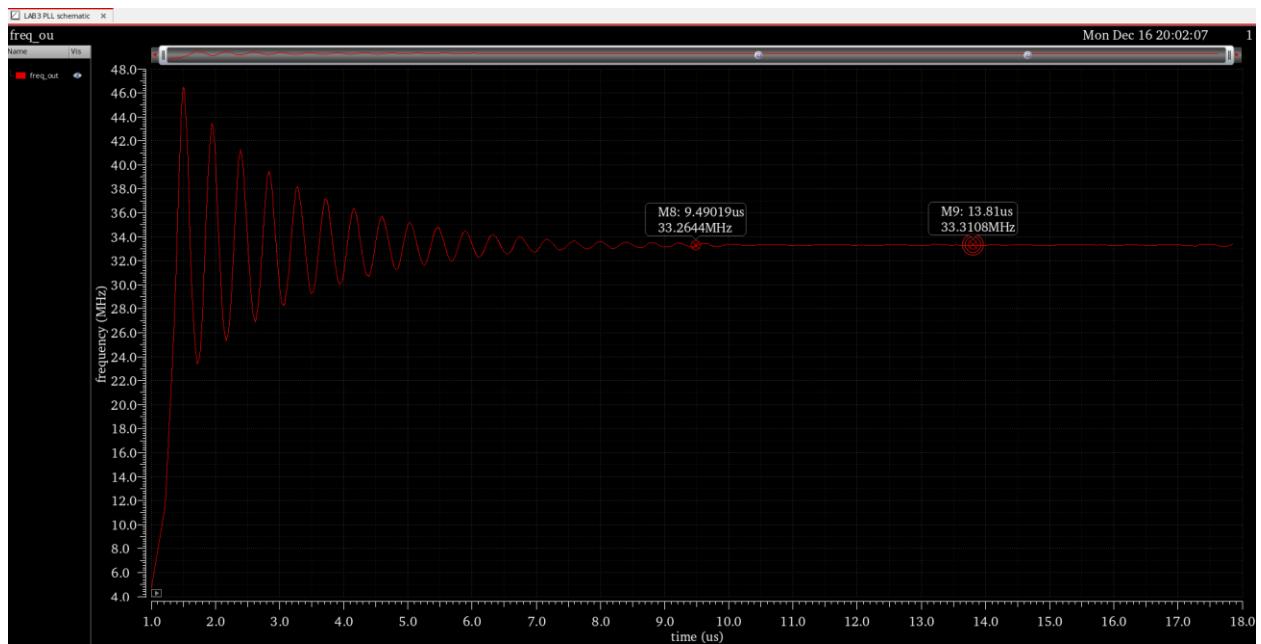


Fig 6: Divide by 3 output Schematic at m=14, T =-25 °C

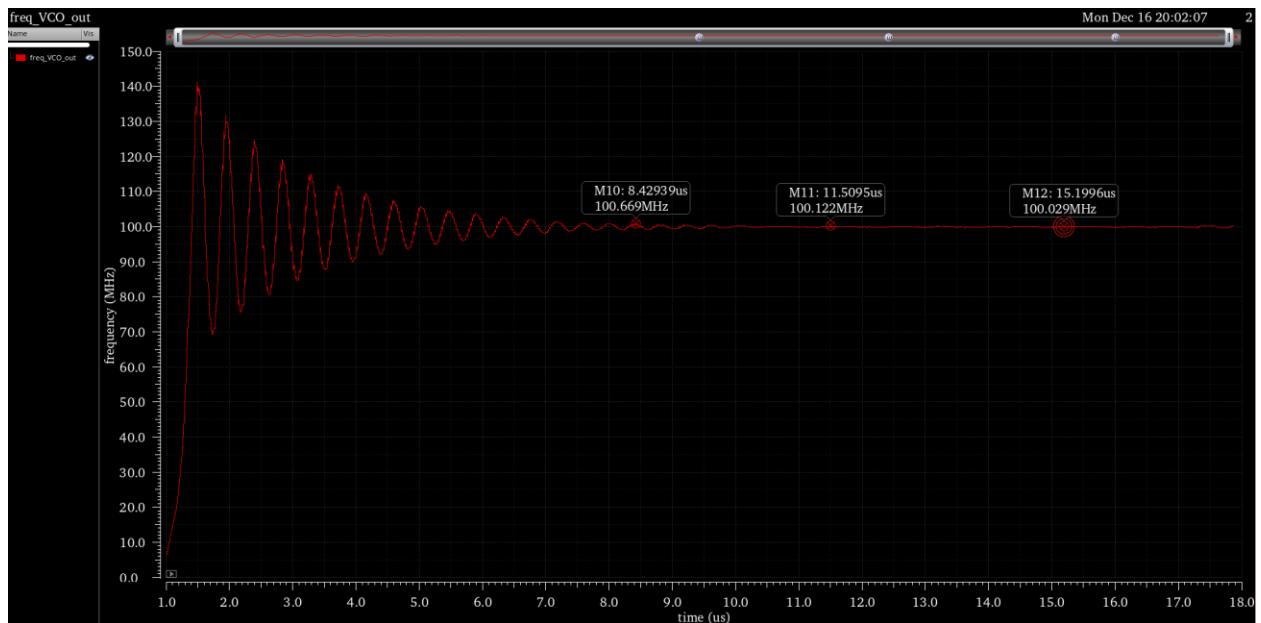


Fig 7: VCO output Schematic at m=14, T =-25 °C

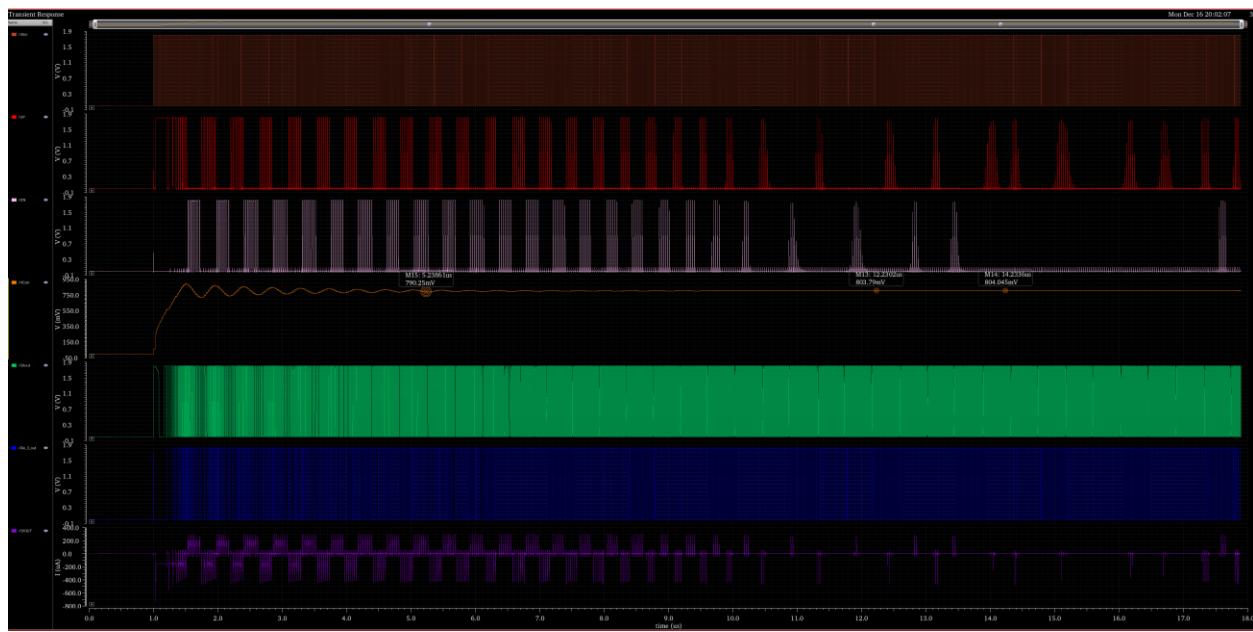


Fig 8: PLL output Schematic at $m=14$, $T = -25^{\circ}\text{C}$

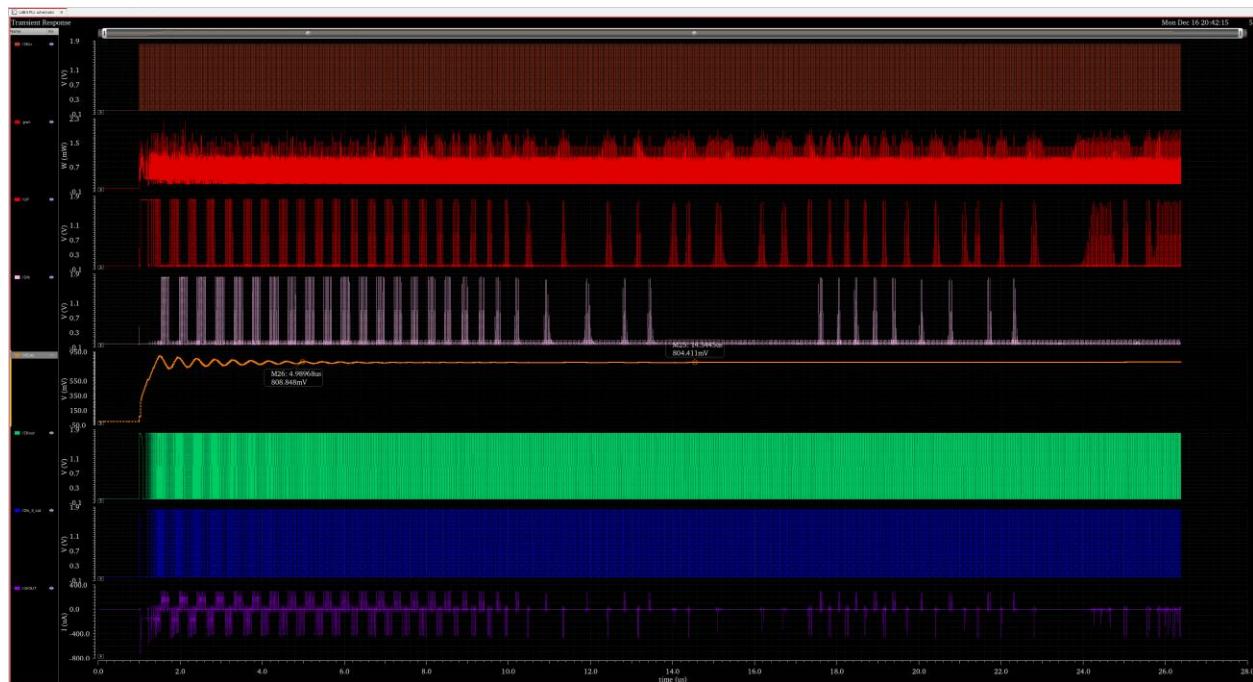


Fig 9: VCO output Schematic at $m=14$, $T = -25^{\circ}\text{C}$ (including current and power calculation)

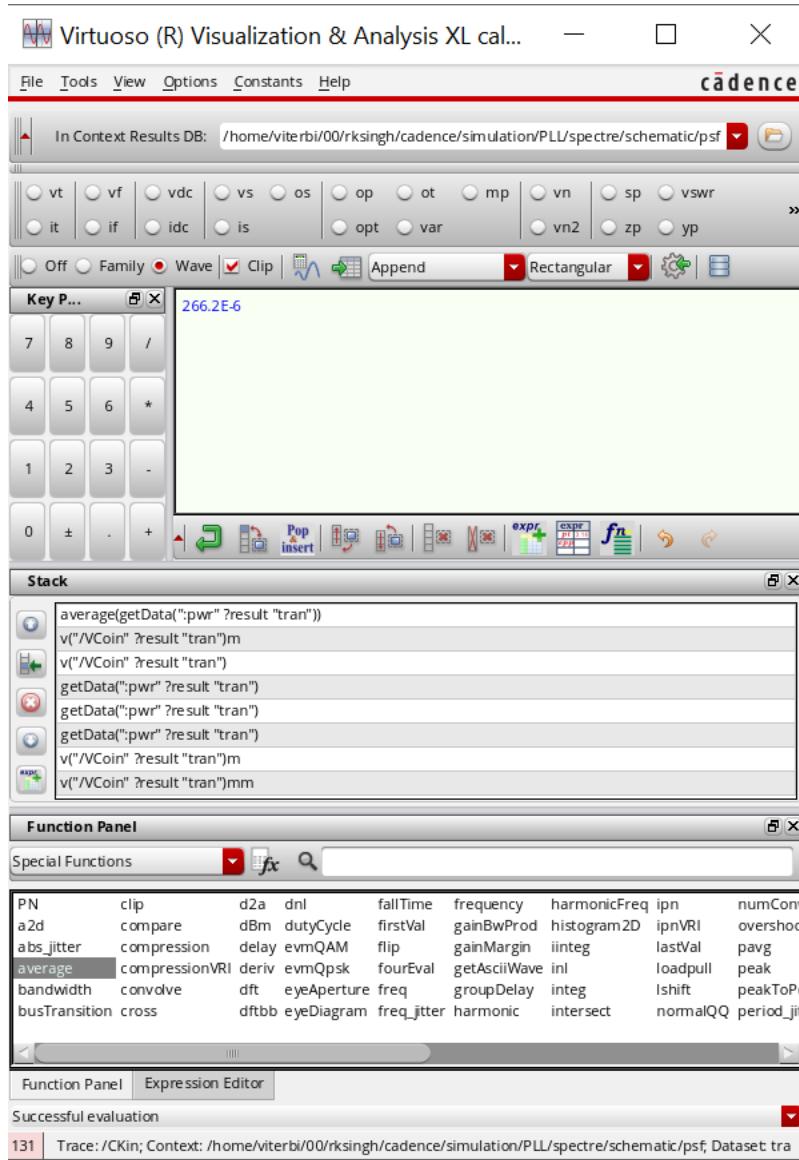


Fig 10: PLL output Schematic at m=14, T =-25 °C (including average current calculation)

Hence the average current calculation is as follows = $266.2 \text{ E-6} / 1.8 = 147.89 \mu\text{A}$

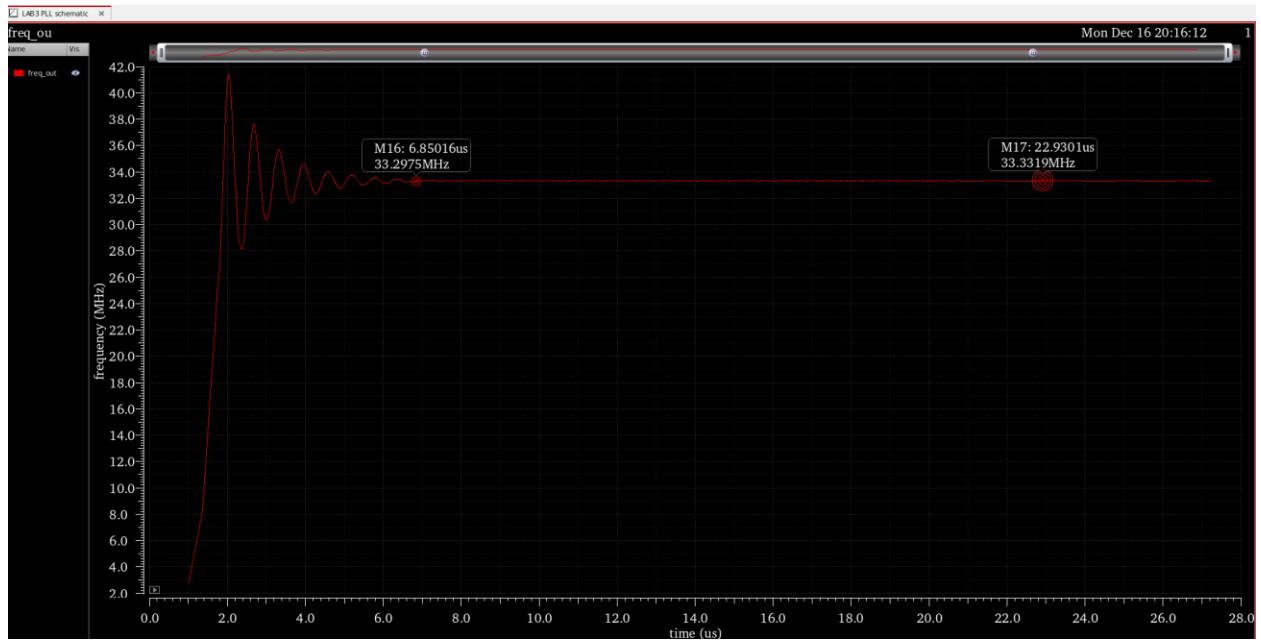


Fig 11:2 Divide by 3 output Schematic at $m=14$, $T = 75^{\circ}\text{C}$

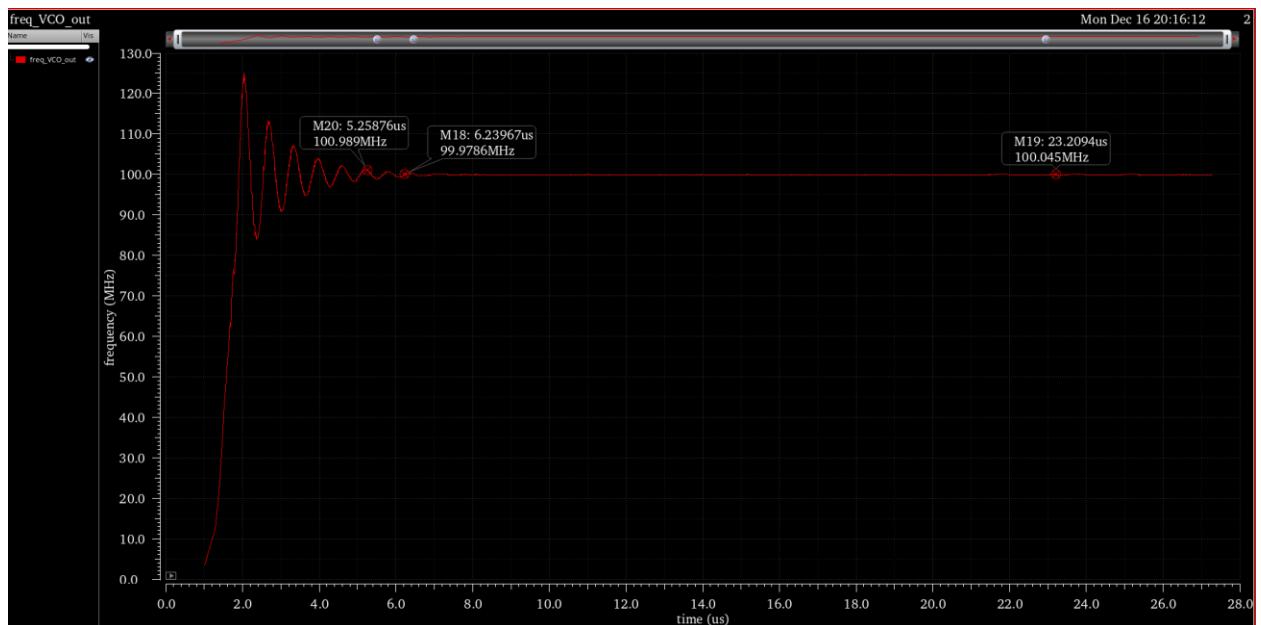


Fig 12: VCO output Schematic at $m=14$, $T = 75^{\circ}\text{C}$

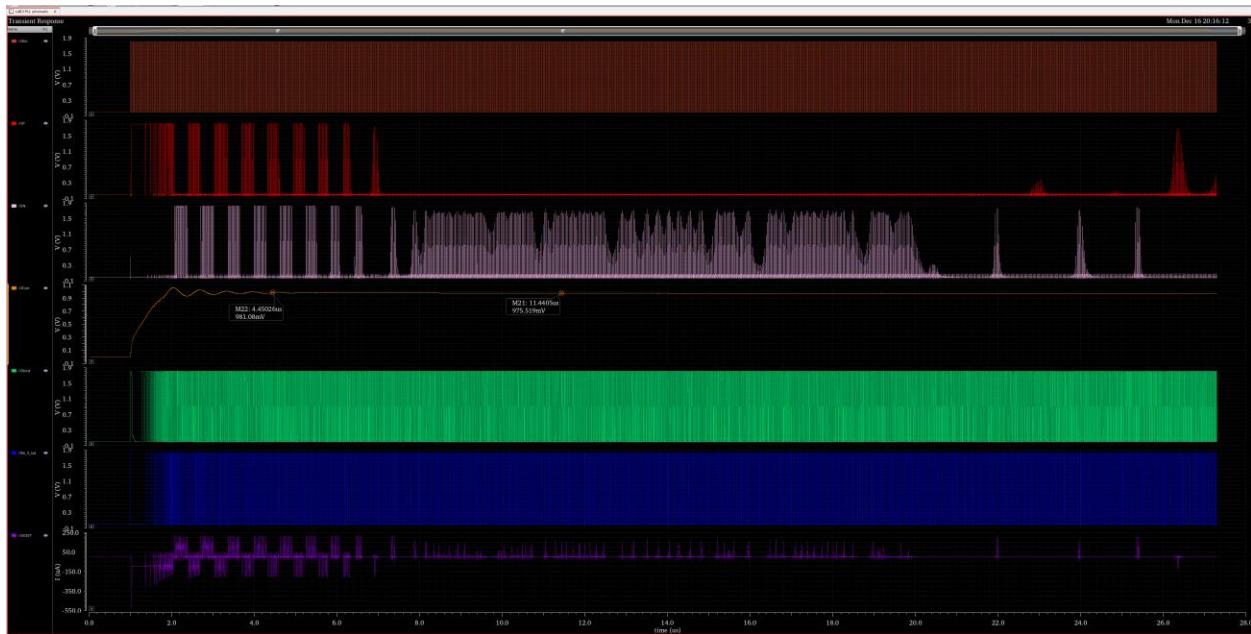


Fig 13: PLL output Schematic at $m=14$, $T = 75^{\circ}\text{C}$

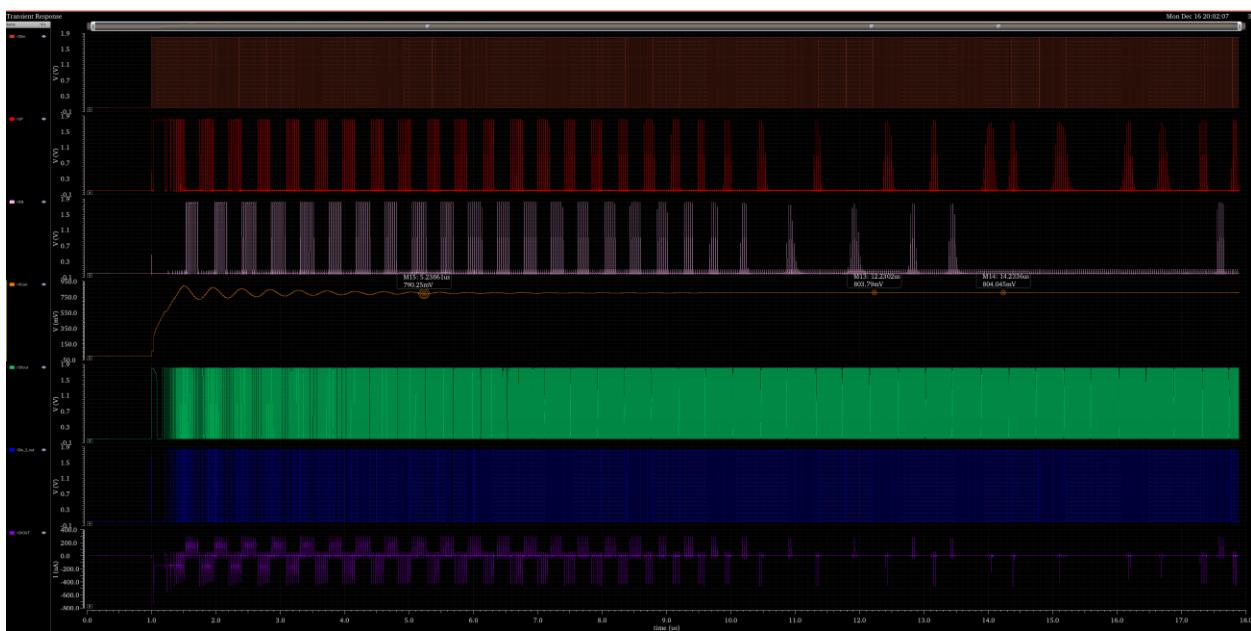


Fig 14: VCO output Schematic at $m=14$, $T = 75^{\circ}\text{C}$ (including current and power calculation)

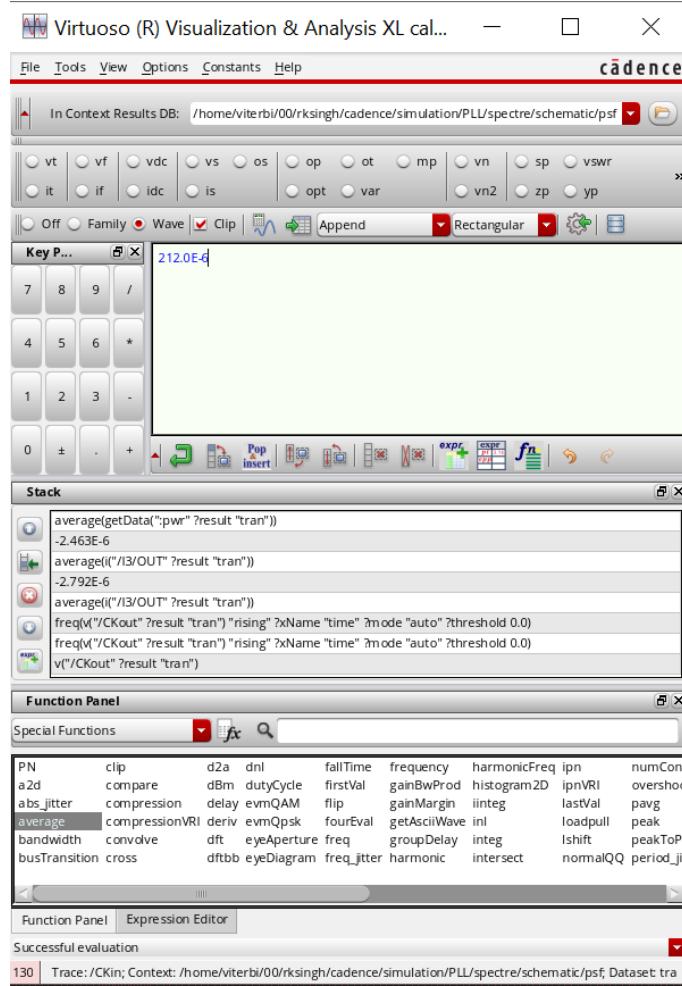


Fig 15: PLL output Schematic at m=14, T = 75 °C (including average current calculation)

Hence the average current calculation is as follows = $212.0 \text{ E-6} / 1.8 = 117.8 \mu\text{A}$

Physical Layout –

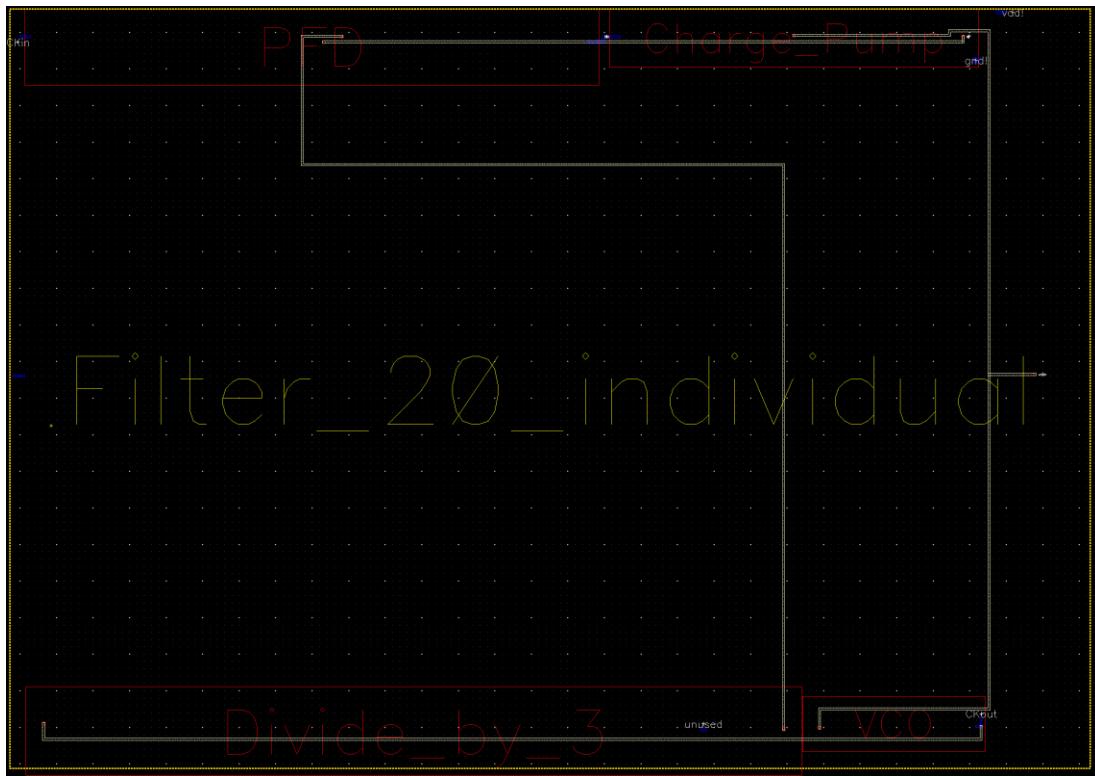


Fig 16: PLL output Layout at m=14

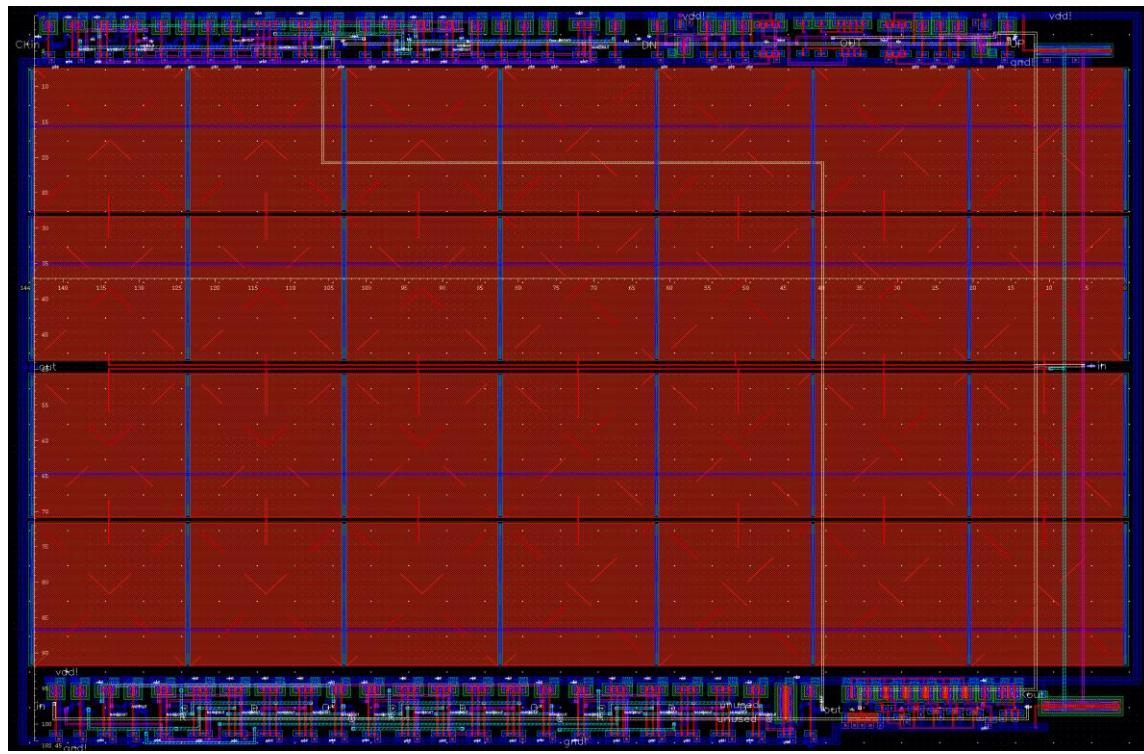


Fig 17: PLL output Layout at m=14

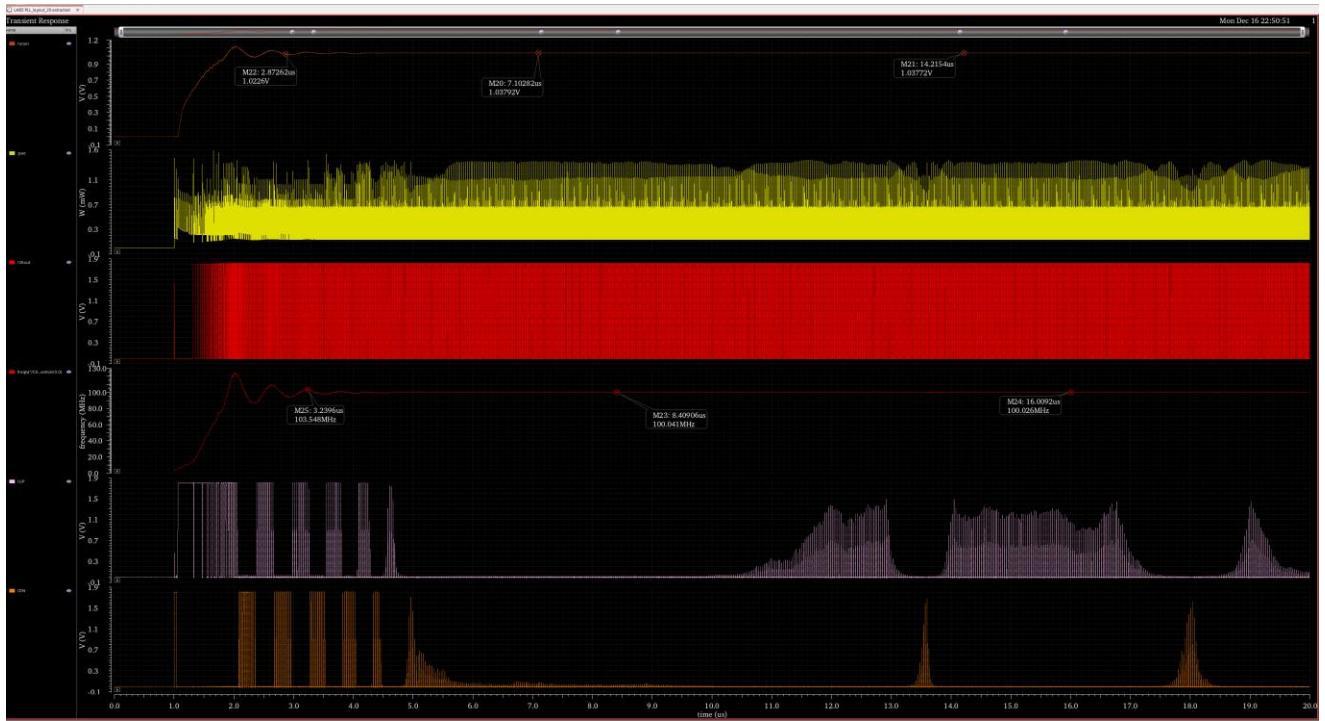


Fig 19: PLL output Schematic at $m=14$, $T = 25^{\circ}\text{C}$ (including current, VCO output and power calculation)

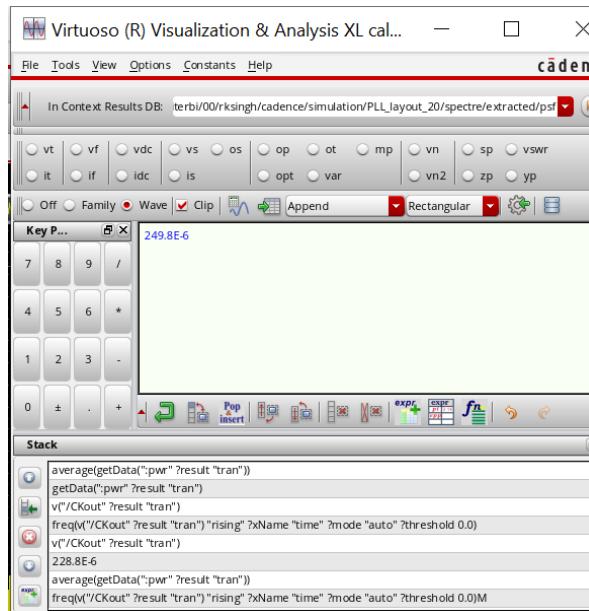


Fig 20: PLL output Layout at $m=14$, $T = 25^{\circ}\text{C}$ (including average current calculation)

Hence the average current calculation is as follows = $249.8 \times 10^{-6} / 1.8 = 138.8 \mu\text{A}$

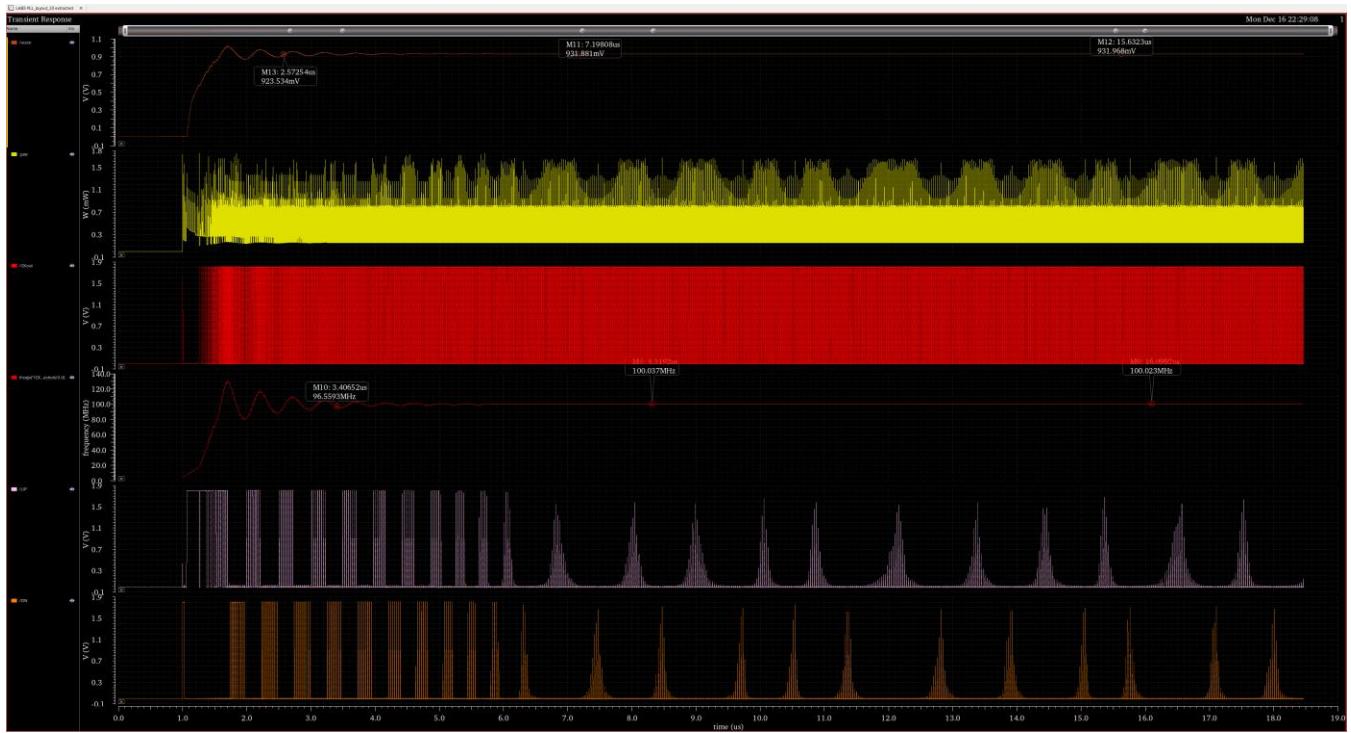


Fig 23: PLL output Layout at $m=14$, $T = -25^{\circ}\text{C}$ (including current, VCO output and power calculation)

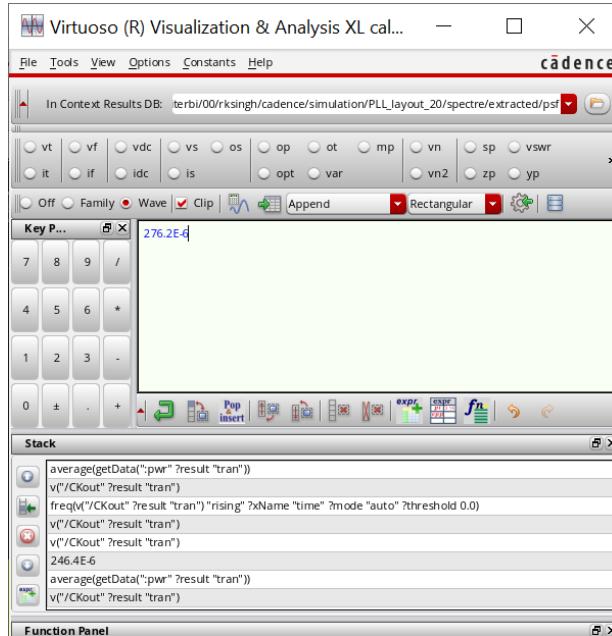


Fig 24: PLL output Layout at $m=14$, $T = -25^{\circ}\text{C}$ (including average current calculation)

Hence the average current calculation is as follows = $276.2 \times 10^{-6} / 1.8 = 153.4 \mu\text{A}$

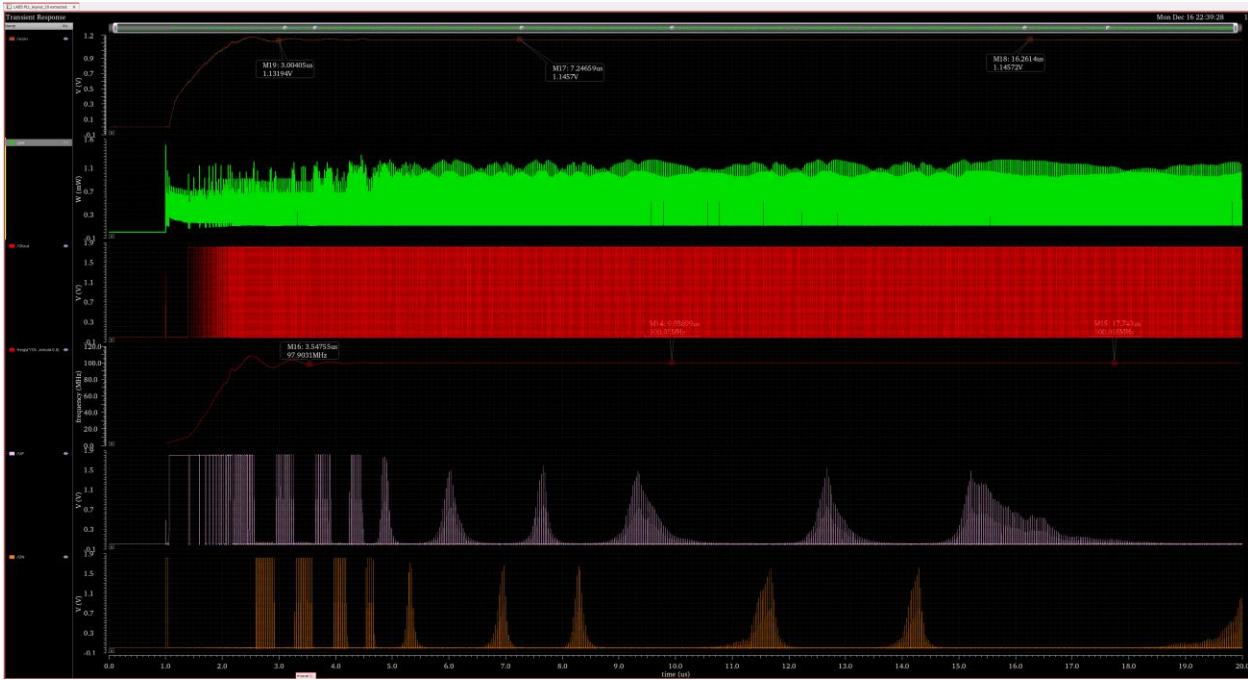


Fig 25: VCO output Layout at $m=14$, $T = 75^{\circ}\text{C}$ (including current, VCO output and power calculation)

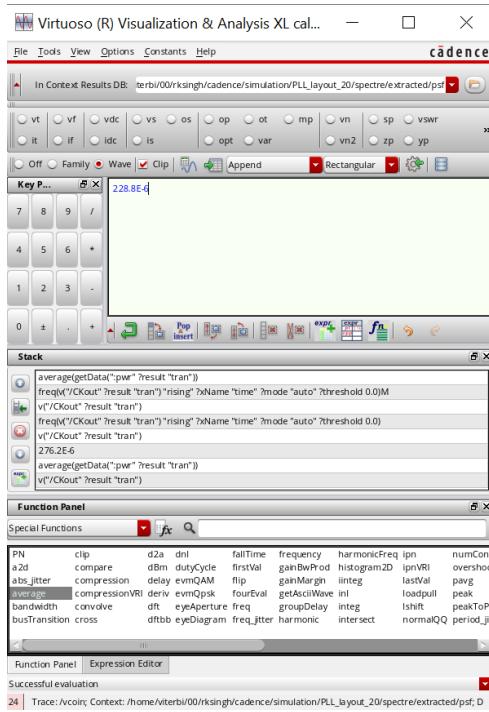


Fig 26: PLL output Layout at $m=14$, $T = 75^{\circ}\text{C}$ (including average current calculation)

Hence the average current calculation is as follows = $228.8 \times 10^{-6} / 1.8 = 127.1 \mu\text{A}$

Layout vs Schematic LVS result -

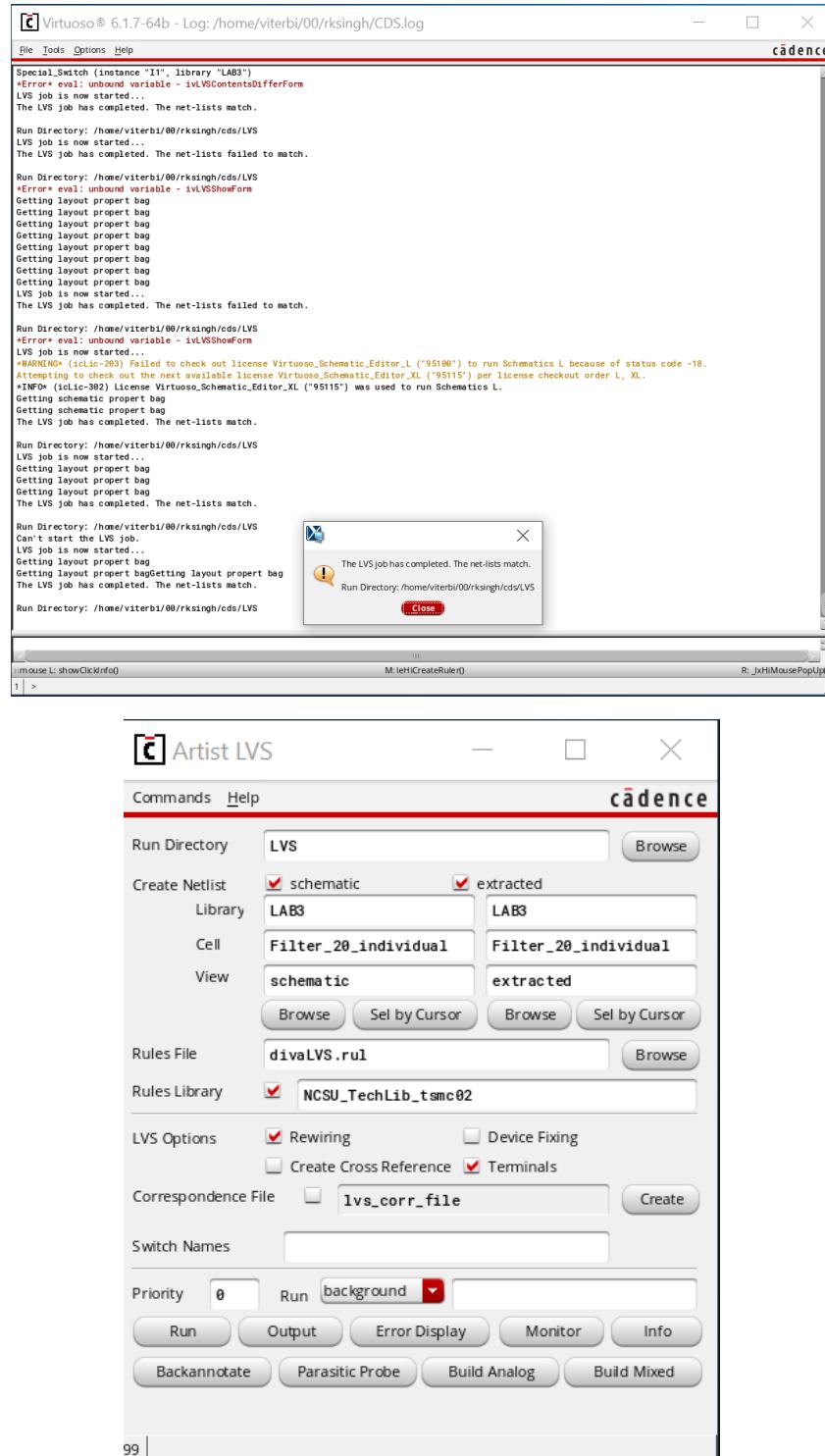


Fig 27: Layout Divide by three with Load LVS match

```

Getting layout property bag
Getting layout property bag
LVS job is now started...
The LVS job has completed. The net-lists failed to match.

Run Directory: /home/viterbi/00/rksingh/cds/LVS
+Error: eval: unbound variable - ivLVSShowForm
LVS job is now started...
+WARNING: (siclic-283) Failed to check out license Virtuoso_Schematic_Editor_L ("95100") to run Schematics L because of status code -18.
Attempting to check out the next available license Virtuoso_Schematic_Editor_XL ("95115") per license checkout order L, XL.
+INFO: (siclic-302) License Virtuoso_Schematic_Editor_XL ("95115") was used to run Schematics L.
Getting schematic property bag
Getting schematic property bag
The LVS job has completed. The net-lists match.

Run Directory: /home/viterbi/00/rksingh/cds/LVS
LVS job is now started...
Getting layout property bag
Getting layout property bag
Getting layout property bag
The LVS job has completed. The net-lists match.

Run Directory: /home/viterbi/00/rksingh/cds/LVS
Can't start the LVS job.
LVS job is now started...
Getting layout property bag
Getting layout property bag
The LVS job has completed. The net-lists match.

Run Directory: /home/viterbi/00/rksingh/cds/LVS
LVS job is now started...
The LVS job has completed. The net-lists match.

Run Directory: /home/viterbi/00/rksingh/cds/LVS

```

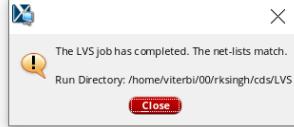



Fig 28: Layout Divide by three with Load LVS match

Summary & Result –

The Phase Lock Loop was designed and executed successfully, it was observed that the lock time and average power calculations changes as per temperature regulations. The lock time and the average current calculation reduces as we increase the temperature from -25 to 75 °C.

FOM Calculation –

Parameters	Temperature	Schematic	Layout	Unit
Layout Area	NA	NA	14,488	µm x µm
Average Current Consumption	-25 °C	147.89	153.4	µA
	25 °C	128.1	138.8	
	75 °C	117.8	127.1	
Lock Time	-25 °C	10.4	7.5	µsec
	25 °C	5.5	4.5	
	75 °C	4.0	3.5	

Figure of Merit (FOM)

Figure of Merit (FOM) = Area x Current x Lock Time

Layout -

$$\text{FOM} (-25 \text{ }^{\circ}\text{C}) = 16.67 \cdot 10^{-18} (\text{Asec m}^2)$$

$$\text{FOM} (25 \text{ }^{\circ}\text{C}) = 9.05 \cdot 10^{-18} (\text{Asec m}^2)$$

$$\text{FOM} (75 \text{ }^{\circ}\text{C}) = 6.45 \cdot 10^{-18} (\text{Asec m}^2)$$

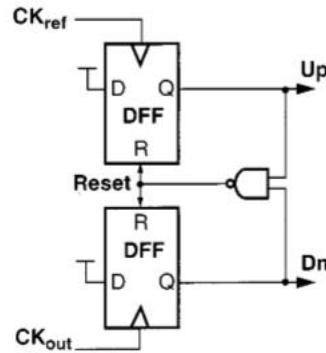
Summary & Result –

The FOM is tabulated and calculated and we have observed that as temperature is increased from -25 to 75 Phase Lock Loop was designed and executed successfully, it was observed that the lock time and average power calculations changes as per temperature regulations. The lock time and the average current calculation reduces as we increase the temperature from -25 to 75 °C.

Also, in order to get the optimum layout area, we should always construct a square layout, in order to achieve as minimum area as possible

Reference –

1. PHASE FREQUENCY DETECTOR OPERATION - A CMOS Phase Frequency Detector for Ctitarge PiiIiip Phase-Locked Loop - G. B. Lee, P. K. Char? and L. Siek
2. Proposed PFD Design - A Novel Phase Frequency Detector for a High Frequency PLL Design, Abdul Majeed K Ka* and Binsu J Kailatha



3. Fast Frequency Acquisition Phase-Frequency Detectors for GSamples/s Phase-Locked Loops, Mozhgan Mansuri, Dean Liu, and Chih-Kong Ken Yan