3-A Step-Down Converter with Hiccup Short Circuit Protection in 2x2 QFN Package

Check for Samples: TPS62085, TPS62086, TPS62087

FEATURES

- **DCS-Control™ Topology**
- **Up to 95% Efficiency**
- **Hiccup Short Circuit Protection**
- **Power Save Mode for Light Load Efficiency**
- **100% Duty Cycle for Lowest Dropout**
- **2.5-V to 6.0-V Input Voltage Range**
- **17-µA Operating Quiescent Current**
- **0.8-V to V_{IN} Adjustable Output Voltage**
- **1.8-V and 3.3-V Fixed Output Voltage**
- **Output Discharge**
- **Power Good Output**
- **Thermal Shutdown Protection**
- **Available in 2-mm x 2-mm QFN Package**

APPLICATIONS

- **Battery Powered Application**
- **Point of Load**
- **Processor Supply**
- **Hard Disk Drives**

DESCRIPTION

The TPS62085, TPS62086, and TPS62087 device family are high frequency synchronous step-down converters optimized for small solution size and high efficiency. With an input voltage range of 2.5 V to 6.0 V, common battery technologies are supported. The devices focus on high efficiency step-down conversion over a wide output current range. At medium to heavy loads, the converter operates in PWM mode and automatically enters Power Save Mode operation at light load to maintain high efficiency over the entire load current range.

To address the requirements of system power rails, the internal compensation circuit allows a large selection of external output capacitor values ranging from 10-µF to 150-µF capacitance. Together with its DCS-Control architecture excellent load transient performance and output voltage regulation accuracy are achieved. The devices are available in a 2-mm x 2-mm QFN package.

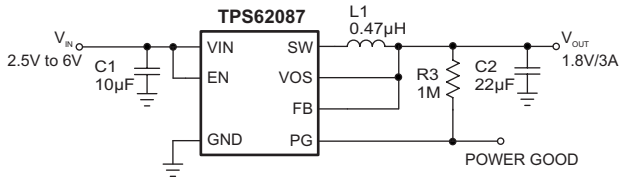


Figure 1. Typical Application

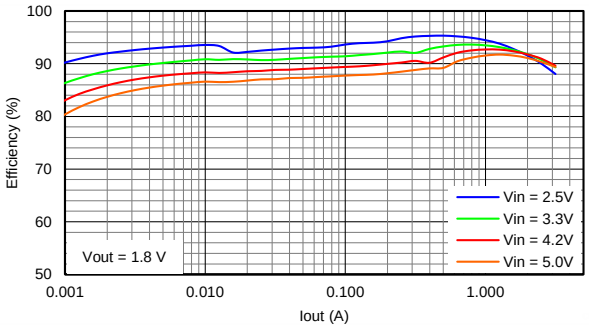


Figure 2. Typical Application Efficiency

ORDERING INFORMATION

PART NUMBER(1)	OUTPUT VOLTAGE	PACKAGE MARKING	PACKAGE
TPS62085RLT	Adjustable	PD5Q	7-Pin QFN
TPS62086RLT	3.3 V	PD4Q	
TPS62087RLT	1.8 V	PD3Q	

(1) For detailed ordering information please check the PACKAGE OPTION ADDENDUM section at the end of this datasheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Voltage Range at Pins(2)	VIN, FB, VOS, EN, PG	–0.3	7	V
	SW	-0.3	V_{IN} + 0.3	
ESD Rating	Human Body Model, HBM		2	kV
	Charged Device Model, CDM		500	V
Temperature Range	Operating Junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS62085/6/7	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	107.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	66.2	
θ_{JB}	Junction-to-board thermal resistance	17.1	
ψ_{JT}	Junction-to-top characterization parameter	2.1	
ψ_{JB}	Junction-to-board characterization parameter	17.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	2.5		6.0	V
I_{SINK_PG}	Sink current at PG pin			1.0	mA
V_{PG}	Pull-up resistor voltage			6.0	V
T_J	Operating junction temperature	-40		125	°C

(1) Refer to the APPLICATION INFORMATION section for further information.

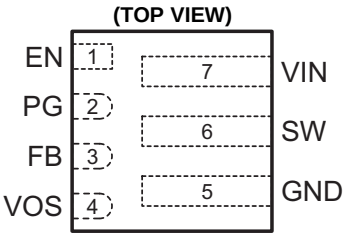
ELECTRICAL CHARACTERISTICS

T_J = -40 °C to 125 °C, and V_{IN} = 3.6 V. Typical values are at T_J = 25 °C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		6.0	V
I_Q	Quiescent current into VIN	No load, device not switching T_J = -40 °C to 85 °C, V_{IN} = 2.5 V to 5.5 V		17	25	µA
I_{SD}	Shutdown current into VIN	EN = Low, T_J = -40 °C to 85 °C, V_{IN} = 2.5 V to 5.5 V		0.7	5	µA
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling	2.1	2.2	2.3	V
	Under voltage lock out hysteresis	V_{IN} rising		200		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE EN						
V_{IH}	High-level input voltage	V_{IN} = 2.5 V to 6.0 V	1.0			V
V_{IL}	Low-level input voltage	V_{IN} = 2.5 V to 6.0 V			0.4	V
$I_{EN,LKG}$	Input leakage current into EN pin	EN = High		0.01	0.16	µA
R_{PD}	Pull-down resistance at EN pin	EN = Low		400		kΩ
SOFT START, POWER GOOD						
t_{SS}	Soft start time	Time from EN high to 95% of V_{OUT} nominal		0.8		ms
V_{PG}	Power good threshold	V_{OUT} rising, referenced to V_{OUT} nominal	93	95	98	%
		V_{OUT} falling, referenced to V_{OUT} nominal	88	90	93	%
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V		0.01	0.16	µA
OUTPUT						
V_{OUT}	Output voltage range, TPS62085		0.8		V_{IN}	V
	Output voltage accuracy, TPS62086, TPS62087(1)	I_{OUT} = 1 A, V_{IN} ≥ V_{OUT} + 1 V, PWM mode	-1.0		1.0	%
		I_{OUT} = 0 A, V_{IN} ≥ V_{OUT} + 1 V, PFM mode	-1.0		2.1	
V_{FB}	Feedback regulation voltage(1)(2)	I_{OUT} = 1A , V_{IN} ≥ V_{OUT} + 1 V, PWM mode	792	800	808	mV
		I_{OUT} = 0 A, V_{IN} ≥ V_{OUT} + 1 V, PFM mode	792	800	817	
$I_{FB,LKG}$	Feedback input leakage current	V_{FB} = 1 V		0.01	0.1	µA
R_{DIS}	Output discharge resistor	EN = LOW, V_{OUT} = 1.8 V		260		Ω
	Line regulation	I_{OUT} = 1 A, V_{IN} = 2.5 V to 6.0 V		0.02		%/V
	Load regulation	I_{OUT} = 0.5 A to 3 A		0.16		%/A
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance	I_{SW} = 500 mA		31	56	mΩ
	Low-side FET on-resistance	I_{SW} = 500 mA		23	45	mΩ
I_{LIM}	High-side FET switch current limit		3.7	4.6	5.5	A
f_{SW}	PWM switching frequency	I_{OUT} = 1 A		2.4		MHz

(1) For more information, see POWER SAVE MODE section.
(2) Conditions: L = 0.47 µH, C_{OUT} = 22 µF

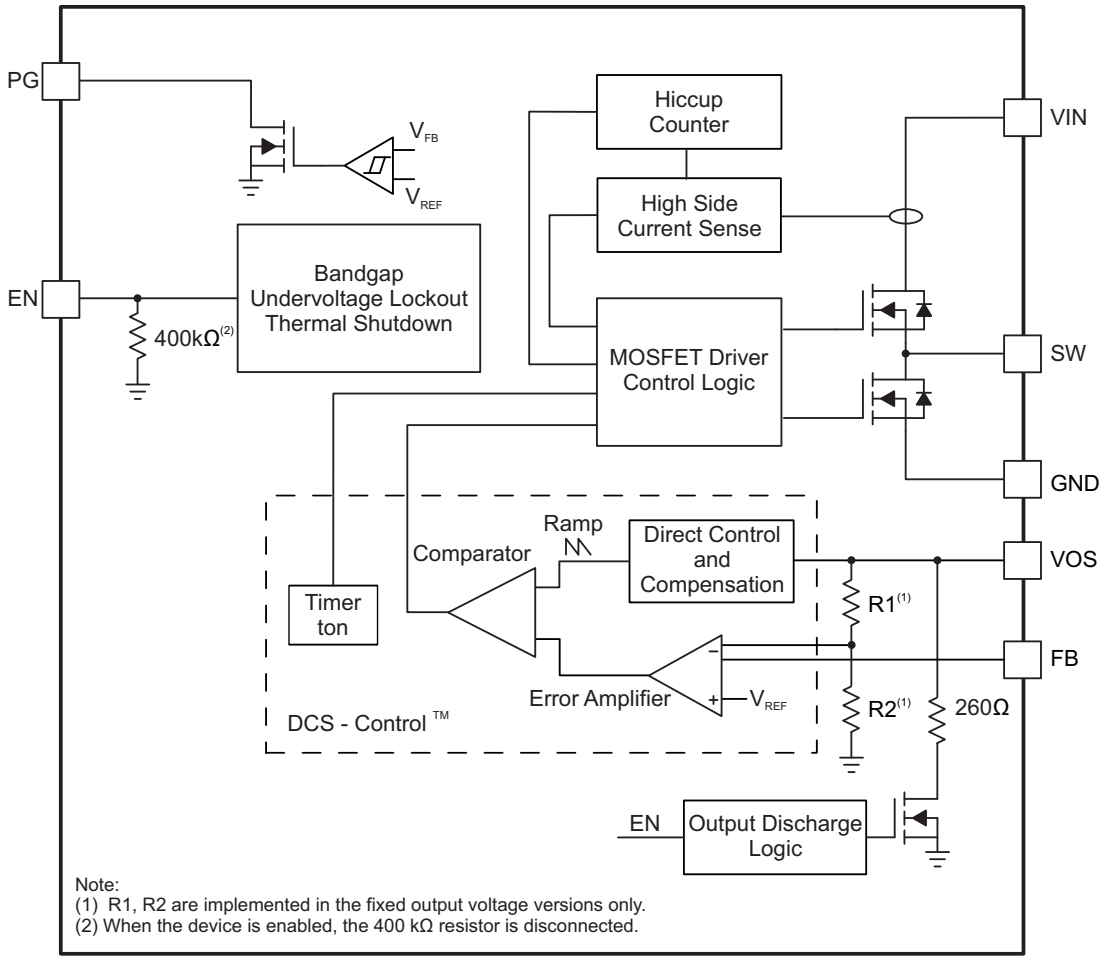
DEVICE INFORMATION



PIN FUNCTIONS

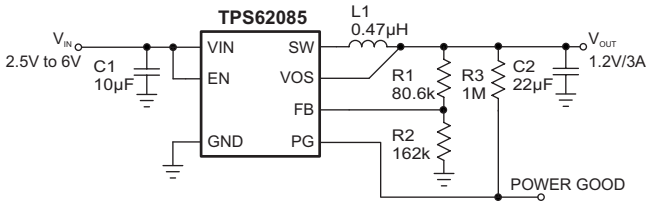
PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	IN	Device enable pin. To enable the device this pin needs to be pulled high. Pulling this pin low disables the device. This pin has an pull-down resistor of typically 400 kΩ when the device is disabled.
PG	2	OUT	Power good open drain output pin. The pull-up resistor can not be connected to any voltage higher than 6 V.
FB	3	IN	Feedback pin. For the fixed output voltage versions this pin must be connected to the output.
VOS	4	IN	Output voltage sense pin. This pin must be directly connected to the output.
GND	5		Ground pin.
SW	6	PWR	Switch pin of the power stage.
VIN	7	PWR	Input voltage pin.

FUNCTIONAL BLOCK DIAGRAM



Note:
(1) R1, R2 are implemented in the fixed output voltage versions only.
(2) When the device is enabled, the 400 kΩ resistor is disconnected.

TYPICAL CHARACTERISTICS



Measurement Application Circuit

List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 µF, Ceramic Capacitor, 6.3 V, X7R, size 0805, GRM21BR71A106ME51L	Murata
C2	22 µF, Ceramic Capacitor, 6.3 V, X5R, size 0805, GRM21BR60J226ME39L	Murata
L1	0.47 µH, Power Inductor, size 4x4x1.5 mm, XFL4015-471ME	Coilcraft
R1	Depending on the output voltage, 1%, size 0603; 0 Ω for TPS62086, TPS62087	Std
R2	162 kΩ, Chip Resistor, 1/16 W, 1%, size 0603; open for TPS62086, TPS62087	Std
R3	1 MΩ, Chip Resistor, 1/16 W, 1%, size 0603	Std

Table of Graphs

V_{IN} = 3.6 V, V_{OUT} = 1.2 V, T_A = 25 °C, unless otherwise noted		Figure
Efficiency	TPS62085, V_{OUT} = 0.95 V	Figure 3
	TPS62085, V_{OUT} = 1.2 V	Figure 4
	TPS62086, V_{OUT} = 3.3 V	Figure 5
	TPS62087, V_{OUT} = 1.8 V	Figure 6
Line Regulation	TPS62085	Figure 7
Load Regulation	TPS62085	Figure 8
Switching Frequency	TPS62085	Figure 9
Waveforms	TPS62085, PWM Operation (Load = 3 A)	Figure 10
	TPS62085, PFM Operation (Load = 100 mA)	Figure 11
	TPS62085, Load Sweep (Load = Open to 3 A)	Figure 12
	TPS62085, Startup (Load = 0.47 Ω)	Figure 13
	TPS62085, Startup (Load = Open)	Figure 14
	TPS62085, Shutdown (Load = 0.47 Ω)	Figure 15
	TPS62085, Shutdown (Load = Open)	Figure 16
	TPS62085, Load Transient (Load = 0.5 A to 3 A)	Figure 17
	TPS62085, Load Transient (Load = 50 mA to 3 A)	Figure 18
	TPS62085, Output Short Circuit Protection (Load = 0.47 Ω, Entry)	Figure 19
	TPS62085, Output Short Circuit Protection (Load = 0.47 Ω, Recovery)	Figure 20
	TPS62085, Output Short Circuit Protection (Load = 0.47 Ω, HICCUP Zoom In)	Figure 21

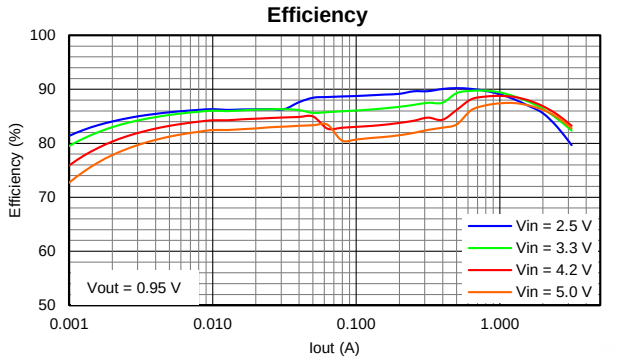


Figure 3.

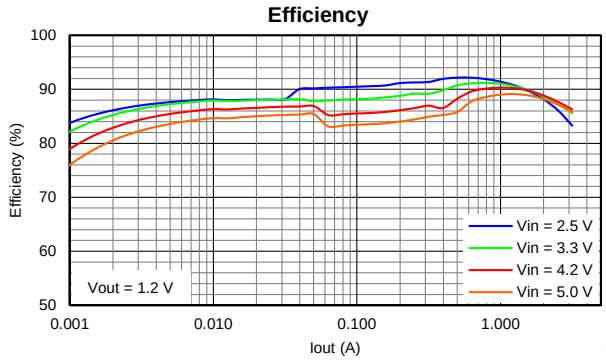


Figure 4.

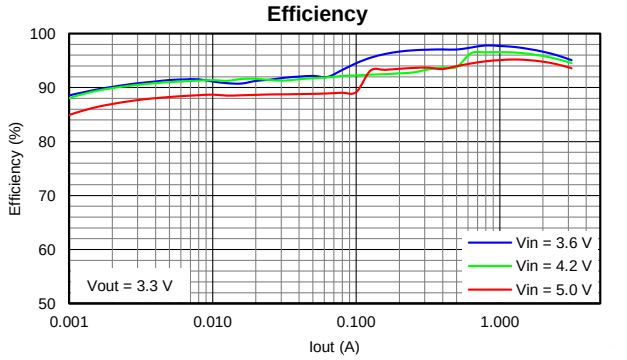


Figure 5.

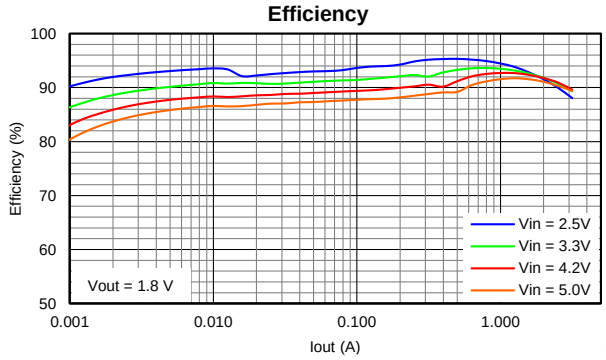


Figure 6.

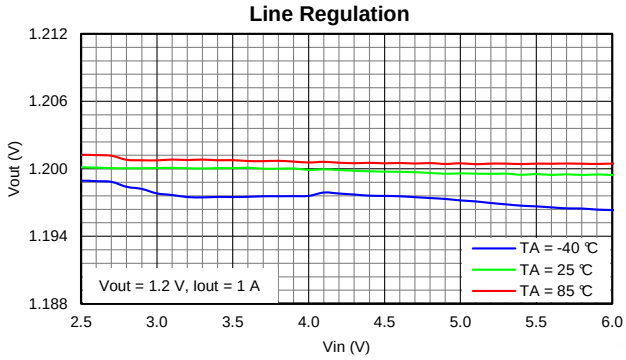


Figure 7.

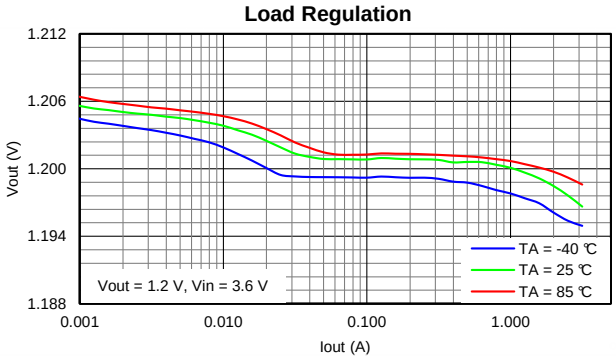


Figure 8.

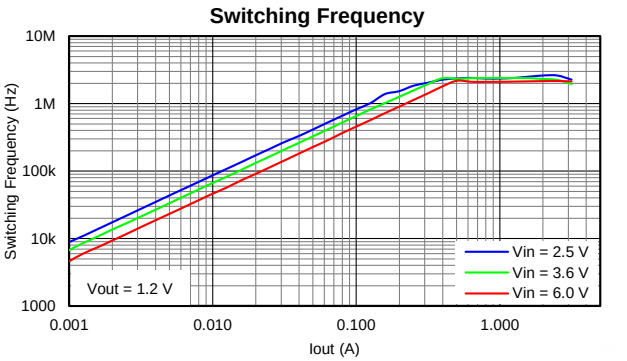


Figure 9.

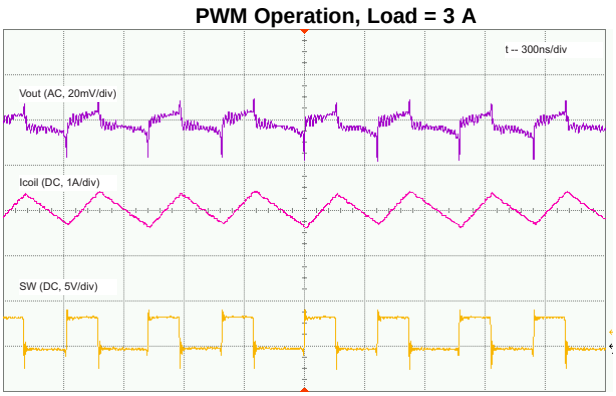


Figure 10.

PFM Operation, Load = 100 mA

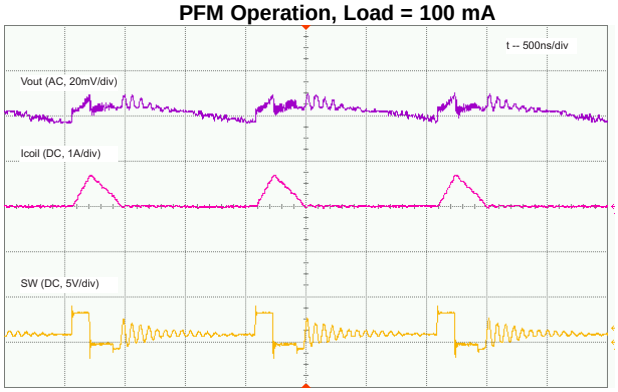


Figure 11.

Load Sweep, Load = Open to 3 A

Figure 12.

Startup, Load = 0.47 Ω

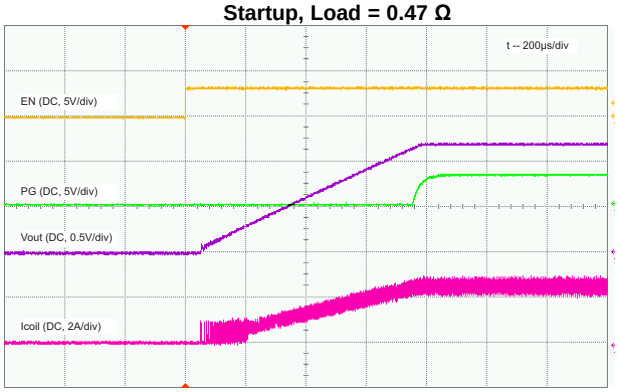


Figure 13.

Startup, Load = Open

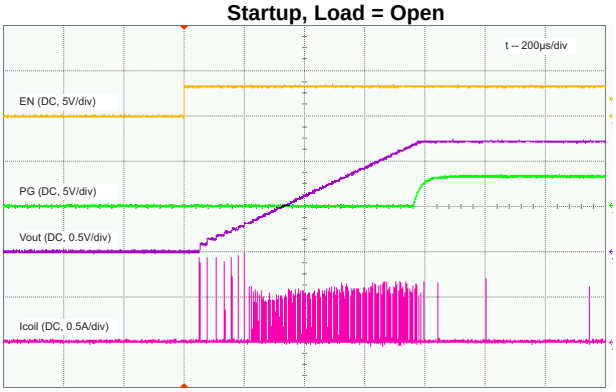


Figure 14.

Shutdown, Load = 0.47 Ω

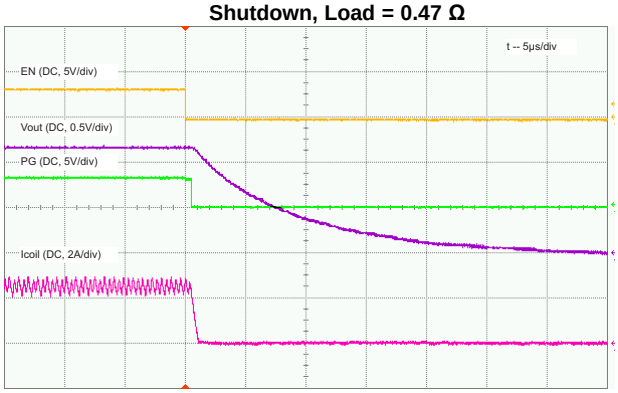


Figure 15.

Shutdown, Load = Open

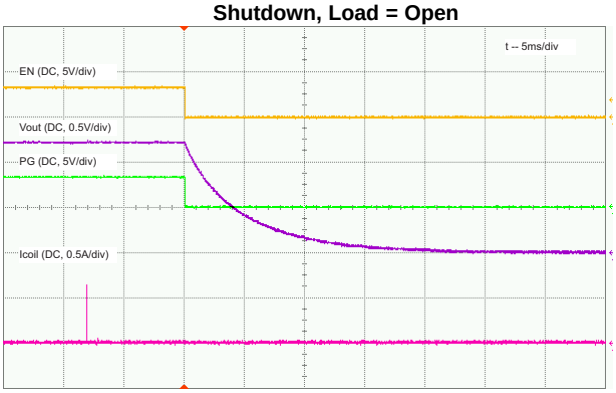


Figure 16.

Load Transient, Load = 0.5 A to 3 A

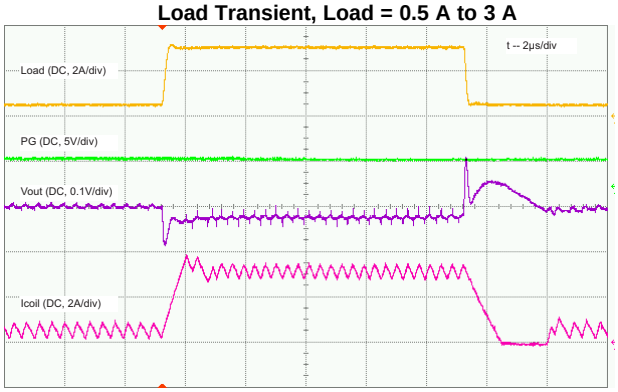


Figure 17.

Load Transient, Load = 50 mA to 3 A

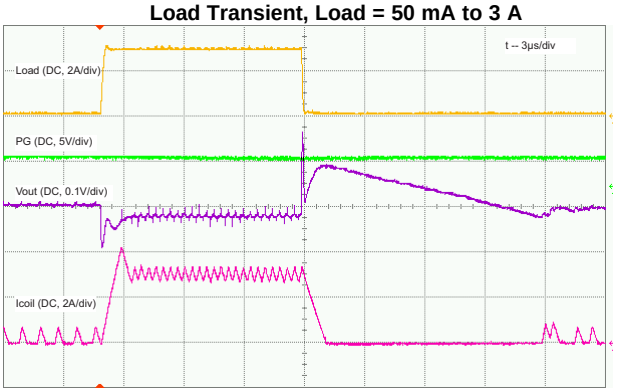


Figure 18.

Output Short Circuit Protection, Load = 0.47 Ω, Entry

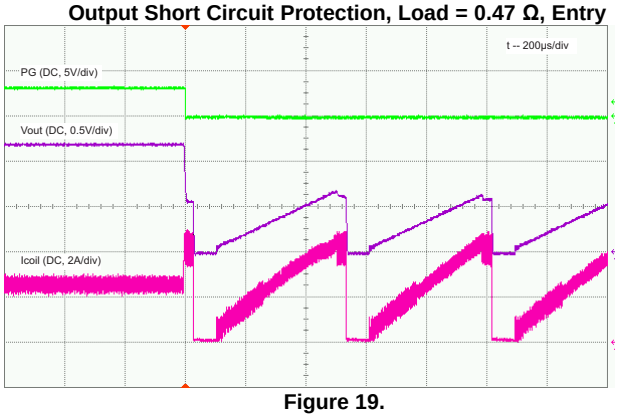


Figure 19.

Output Short Circuit Protection, Load = 0.47 Ω, Recovery

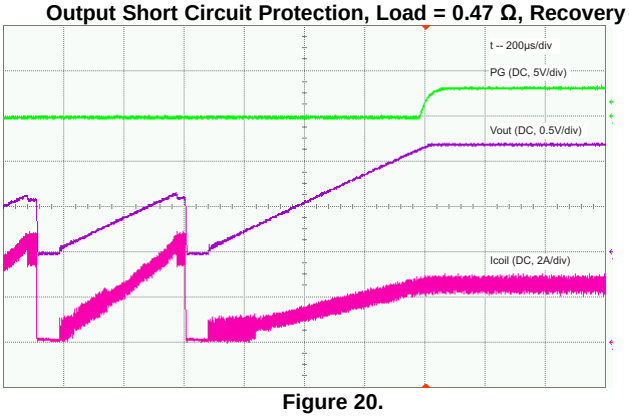


Figure 20.

Output Short Circuit Protection, Load = 0.47 Ω, HICCUP Zoom In

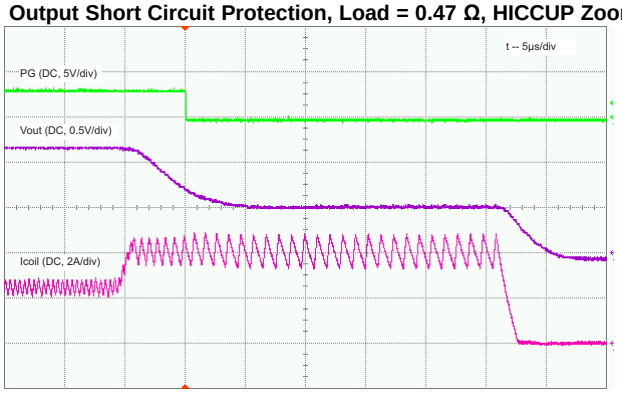


Figure 21.

DETAILED DESCRIPTION

DEVICE OPERATION

The TPS62085, TPS62086, and TPS62087 synchronous step-down converters are based on the DCS-Control (Direct Control with Seamless transition into Power Save Mode) topology. This is an advanced regulation topology that combines the advantages of hysteretic, voltage, and current mode control schemes.

The DCS-Control topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 2.4 MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. Since DCS-Control supports both operation modes (PWM and PFM) within a single building block, the transition from PWM mode to Power Save Mode is seamless and without effects on the output voltage. Fixed output voltage version provides smallest solution size combined with lowest quiescent current. The devices offer both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

POWER SAVE MODE

As the load current decreases, the TPS62085, TPS62086, and TPS62087 enter Power Save Mode operation. During Power Save Mode, the converter operates with reduced switching frequency and with a minimum quiescent current maintaining high efficiency. The power save mode occurs when the inductor current becomes discontinuous. It is based on a fixed on-time architecture, following Equation 1. The switching frequency over the whole load current range is also shown in Figure 9 for a typical application.

$$t_{ON} = 420ns \times \frac{V_{OUT}}{V_{IN}}$$

$$f_{PFM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \quad (1)$$

In Power Save Mode, the output voltage rises slightly above the nominal output voltage, as shown in Figure 8. This effect is minimized by increasing the output capacitor or inductor value. The output voltage accuracy in PFM operation is reflected in the electrical specification table and given for a 22-µF output capacitor.

100% DUTY CYCLE LOW DROPOUT OPERATION

The devices offer low input to output voltage difference by entering 100% duty cycle mode. In this mode the high side MOSFET switch is constantly turned on and the low side MOSFET is switched off. This is particularly useful in battery powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain output regulation, depending on the load current and output voltage can be calculated as:

$$V_{IN,MIN} = V_{OUT} + I_{OUT,MAX} \times (R_{DS(on)} + R_L) \quad (2)$$

With:

$V_{IN,MIN}$ = Minimum input voltage to maintain an output voltage
$I_{OUT,MAX}$ = Maximum Output current
$R_{DS(on)}$ = High side FET on-resistance
R_L = Inductor ohmic resistance (DCR)

ENABLE / DISABLE

The devices are enabled by setting the EN pin to a logic HIGH. Accordingly, shutdown mode is forced if the EN pin is pulled LOW with a shutdown current of typically 0.7 µA.

In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal resistor of 260 Ω discharges the output via the VOS pin smoothly. The output discharge function also works when thermal shutdown, undervoltage lockout or short circuit protection are triggered.

An internal pull-down resistor of 400 kΩ is connected to the EN pin when the EN pin is LOW. The pull-down resistor is disconnected when the EN pin is High.

SOFT START

The TPS62085, TPS62086, and TPS62087 have an internal soft start circuitry which monotonically ramps up the output voltage and reaches the nominal output voltage during a soft start time of typical 0.8 ms. This avoids excessive inrush current and creates a smooth output voltage slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance. The device is able to start into a pre-biased output capacitor. The device starts with the applied bias voltage and ramps the output voltage to its nominal value.

SWITCH CURRENT LIMIT AND HICCUP SHORT CIRCUIT PROTECTION

The switch current limit prevents the devices from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted/saturated inductor or a heavy load/shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. Once this switch current limits is triggered 32 times, the devices stop switching and enables the output discharge. The devices then automatically start a new startup after a typical delay time of 66 µs has passed. This is named HICCUP short circuit protection. The devices repeat this mode until the high load condition disappears.

POWER GOOD

The TPS62085, TPS62086, and TPS62087 have a power good output. The power good goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 6 V. The power good goes low when the devices are disabled or in thermal shutdown. When the devices are in UVLO, the PG pin is high impedance.

The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

UNDER VOLTAGE LOCKOUT

To avoid mis-operation of the device at low input voltages, an under voltage lockout is implemented, which shuts down the devices at voltages lower than V_{UVLO} with a hysteresis of 200 mV.

THERMAL SHUTDOWN

The device goes into thermal shutdown and stops switching once the junction temperature exceeds T_{JSD}. Once the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

APPLICATION INFORMATION

Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify the selection process, Table 1 outlines possible inductor and capacitor value combinations for most applications.

Table 1. Matrix of Output Capacitor / Inductor Combinations

NOMINAL L [µH](1)	NOMINAL C_{OUT} [µF](2)				
	10	22	47	100	150
0.47		+(3)	+	+	+
1	+	+	+	+	+
2.2					

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and -50%.
(3) Typical application configuration. Other '+' mark indicates recommended filter combinations.

Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, Equation 3 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (3)$$

Where:

$I_{OUT,MAX}$ = Maximum output current
ΔI_L = Inductor current ripple
f_{SW} = Switching frequency
L = Inductor value

It is recommended to choose the saturation current for the inductor 20% to 30% higher than the $I_{L,MAX}$, out of Equation 3. A higher inductor value is also useful to lower ripple current but increases the transient response time as well. The following inductors are recommended to be used in designs.

Table 2. List of Recommended Inductors

INDUCTANCE [µH]	CURRENT RATING [A]	DIMENSIONS L x W x H [mm^3]	DC RESISTANCE [mΩ typ]	PART NUMBER
0.47	6.6	4x4x1.5	7.6	Coilcraft XFL4015-471
0.47	4.7	3.2x2.5x1.2	21	TOKO DFE322512-R47N
1	5.1	4x4x2	10.8	Coilcraft XFL4020-102

Capacitor Selection

The input capacitor is the low impedance energy source for the converters which helps to provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between VIN and GND as close as possible to those pins. For most applications 10 µF is sufficient, though a larger value reduces input current ripple.

The architecture of the TPS62085, TPS62086, and TPS62087 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectrics. The recommended typical output capacitor value is 22 µF and can vary over a wide range as outline in the output filter selection table.

Setting the Output Voltage

The output voltage is set by an external resistor divider according to the following equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8V \times \left(1 + \frac{R1}{R2}\right) \quad (4)$$

R2 should not be higher than 180 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. Lowest operating quiescent current and best output voltage accuracy are achieved with the fixed output voltage versions. For the fixed output voltage versions, the FB pin must be connected to the output.

PCB Layout Recommendation

The PCB layout is an important step to maintain the high performance of the TPS62085, TPS62086, and TPS62087 devices.

The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the traces short. Routing these traces direct and wide results in low trace resistance and low parasitic inductance. The low side of the input and output capacitors must be connected directly to the GND pin to avoid a ground potential shift. The sense traces connected to FB and VOS pins are signal traces. Special care should be taken to avoid noise being induced. By a direct routing, parasitic inductance can be kept small. GND layers might be used for shielding. Keep these traces away from SW nodes. See Figure 22 for the recommended PCB layout.

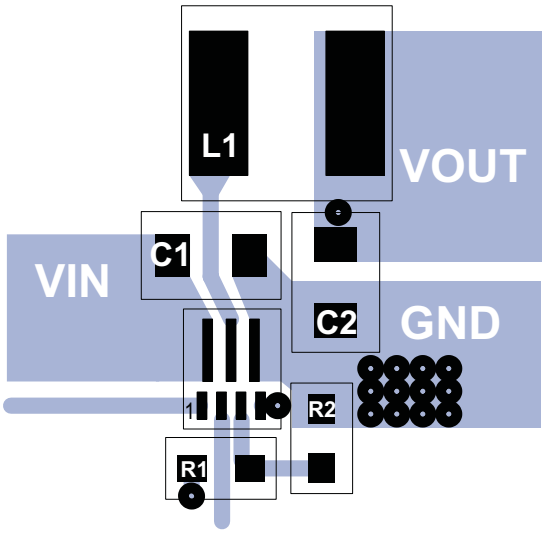


Figure 22. PCB Layout Recommendation

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

The Thermal Data section in the TPS62085EVM-169 Evaluation Module User's Guide SLVU809 provides the thermal metric of the device on the EVM after considering the PCB design of real applications. The big copper planes connecting to the pads of the IC on the PCB board improve the thermal performance of the device. For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Notes SZZA017 and SPRA953.

APPLICATION EXAMPLES

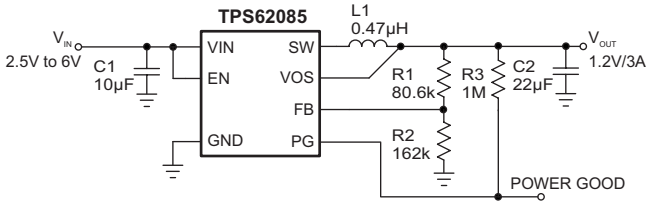


Figure 23. 1.2V Output Voltage Application

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62085RLTR	ACTIVE	VSON	RLT	7	3000	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD5Q	Samples
TPS62085RLTT	ACTIVE	VSON	RLT	7	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD5Q	Samples
TPS62086RLTR	ACTIVE	VSON	RLT	7	3000	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD4Q	Samples
TPS62086RLTT	ACTIVE	VSON	RLT	7	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD4Q	Samples
TPS62087RLTR	ACTIVE	VSON	RLT	7	3000	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD3Q	Samples
TPS62087RLTT	ACTIVE	VSON	RLT	7	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD3Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

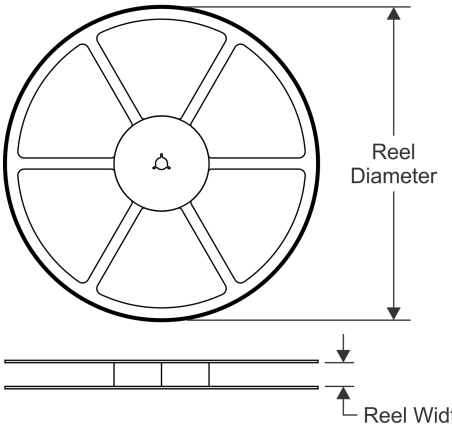
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

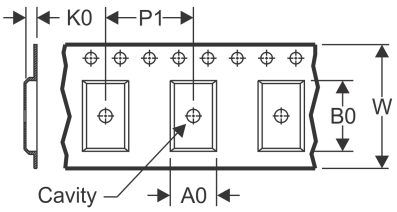
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

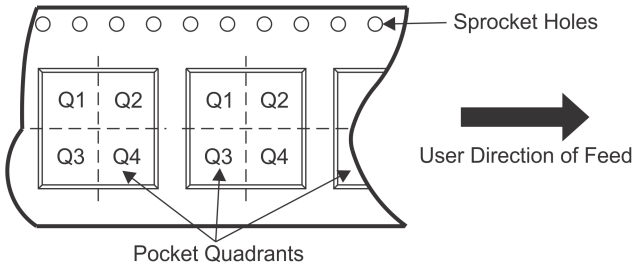


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

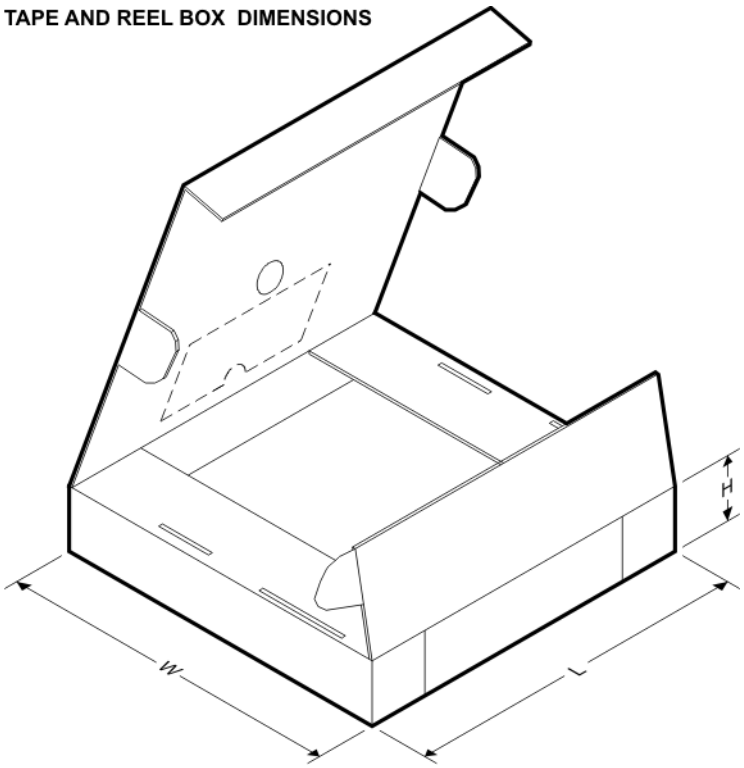
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62085RLTR	VSON	RLT	7	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62085RLTT	VSON	RLT	7	250	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62086RLTR	VSON	RLT	7	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62086RLTT	VSON	RLT	7	250	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62087RLTR	VSON	RLT	7	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62087RLTT	VSON	RLT	7	250	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

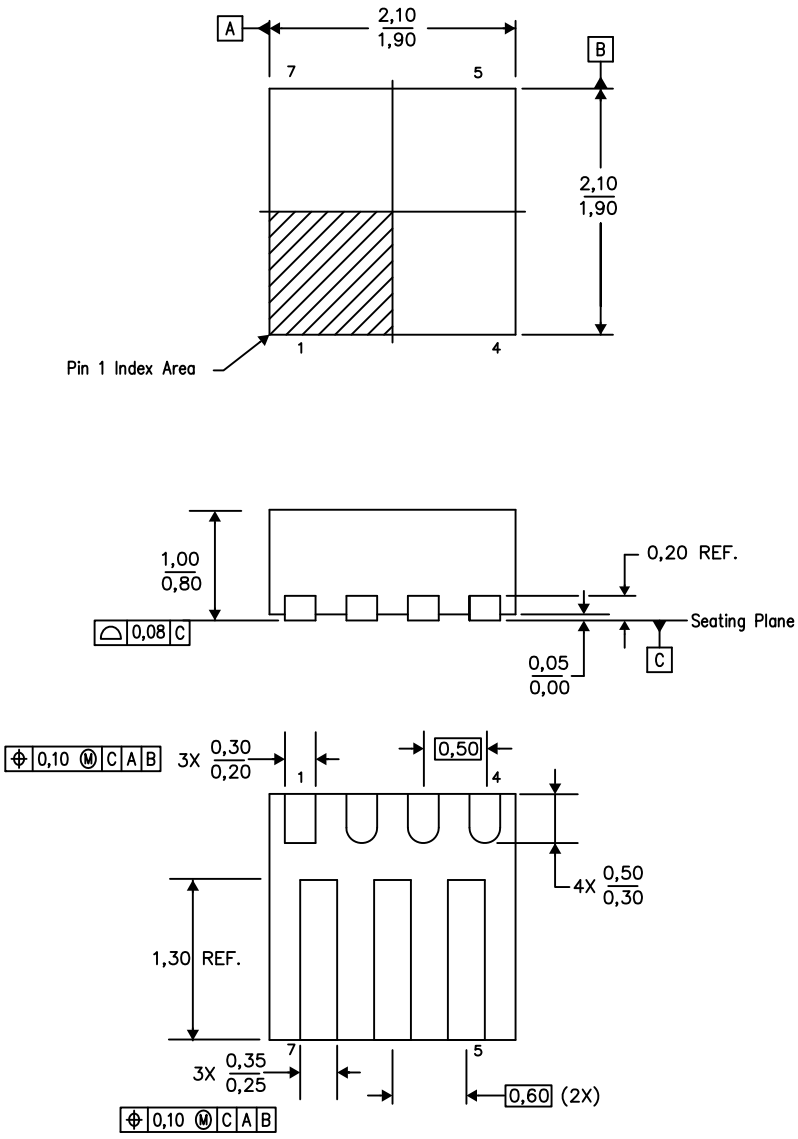
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62085RLTR	VSON	RLT	7	3000	203.0	203.0	35.0
TPS62085RLTT	VSON	RLT	7	250	203.0	203.0	35.0
TPS62086RLTR	VSON	RLT	7	3000	203.0	203.0	35.0
TPS62086RLTT	VSON	RLT	7	250	203.0	203.0	35.0
TPS62087RLTR	VSON	RLT	7	3000	203.0	203.0	35.0
TPS62087RLTT	VSON	RLT	7	250	203.0	203.0	35.0

RLT (S–PVQFN–N7) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.

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