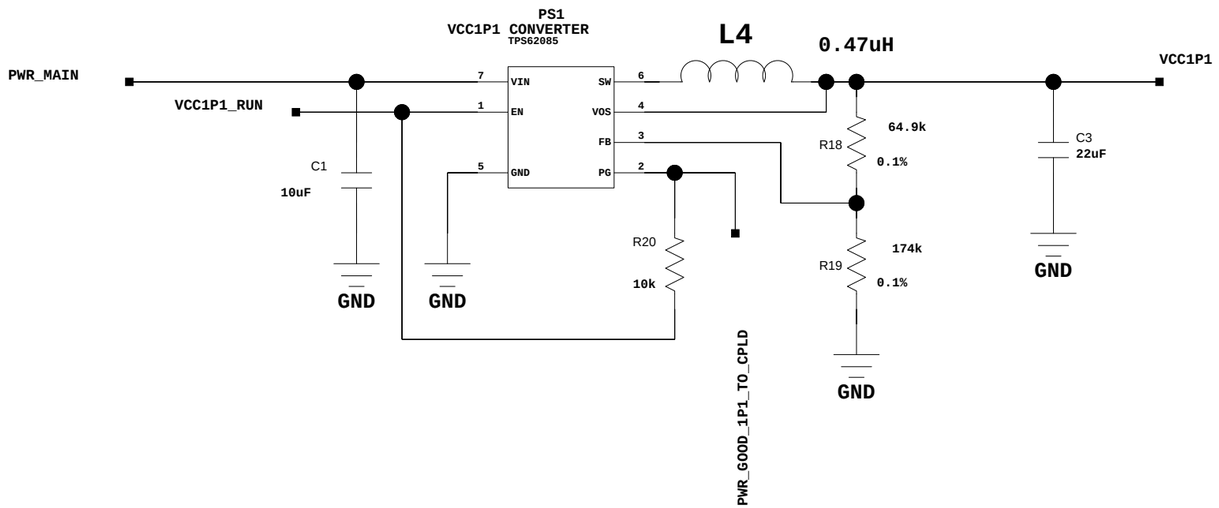
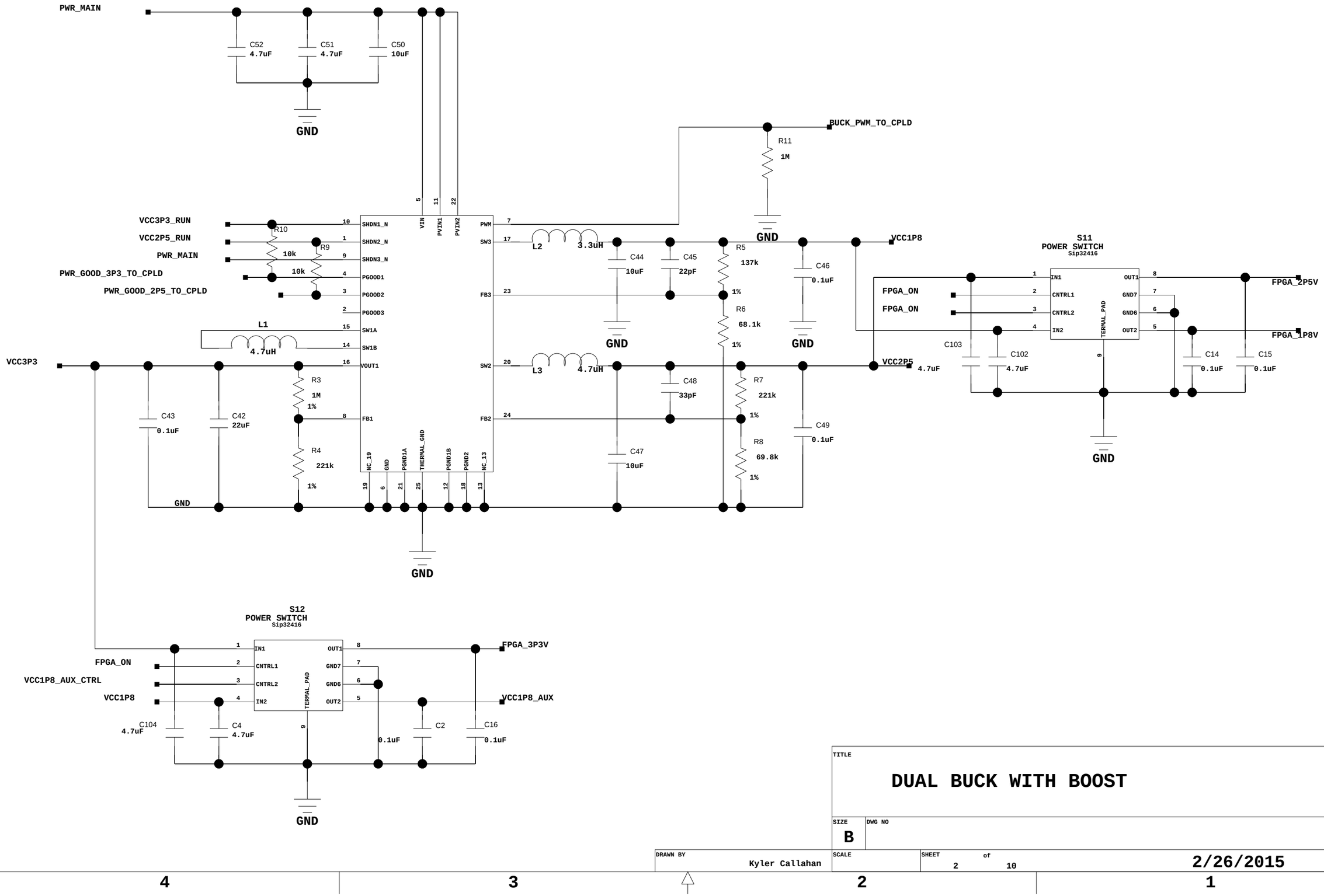
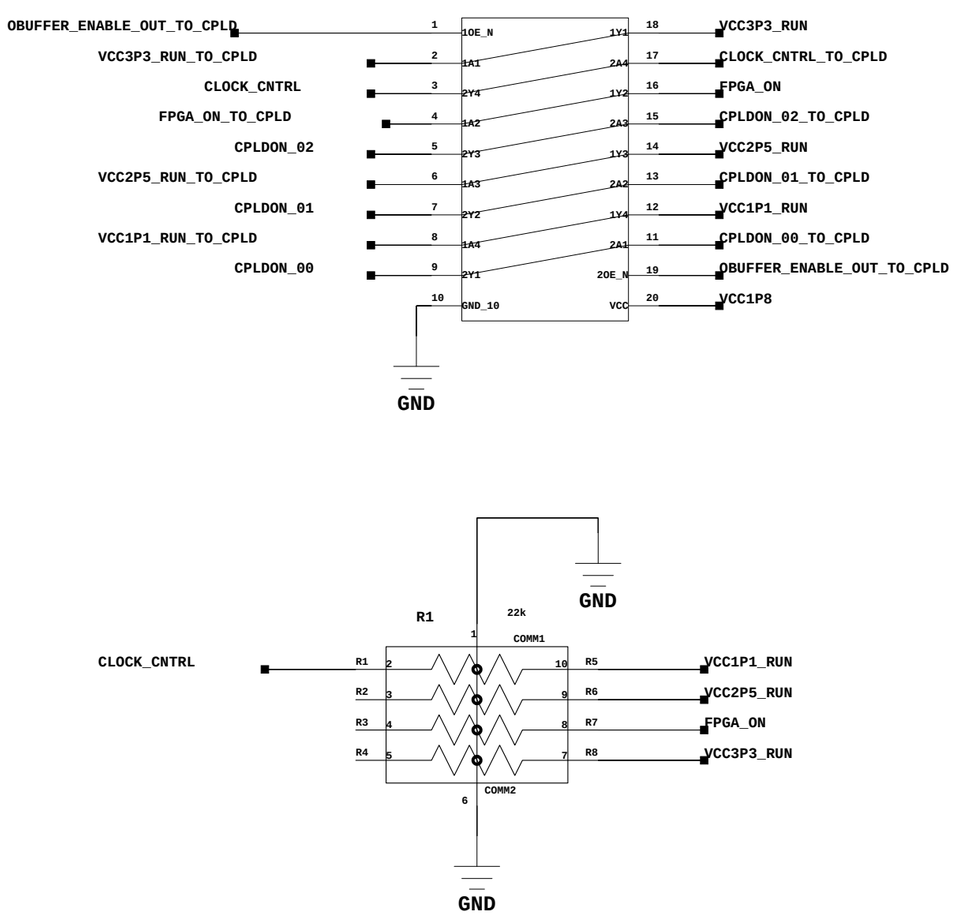


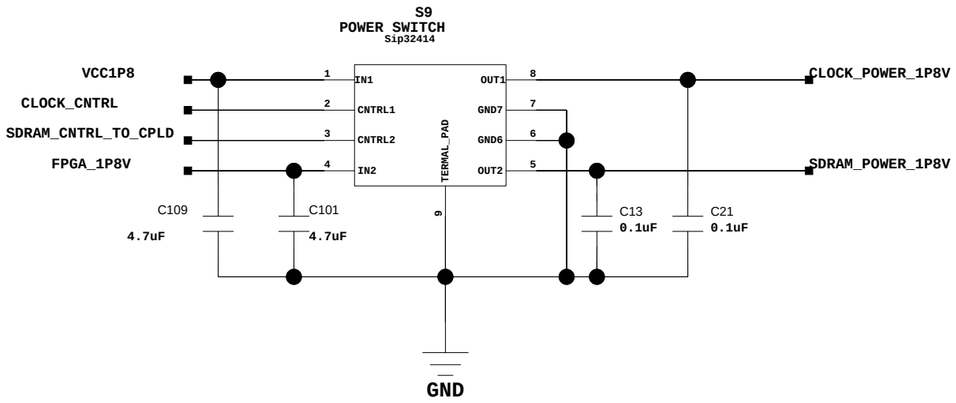
TITLE	1P1V CONVERTER		
SIZE B	DWG NO		REV 2
DRAWN BY Kyler Callahan	SCALE	SHEET 1 of 10	2/26/2015

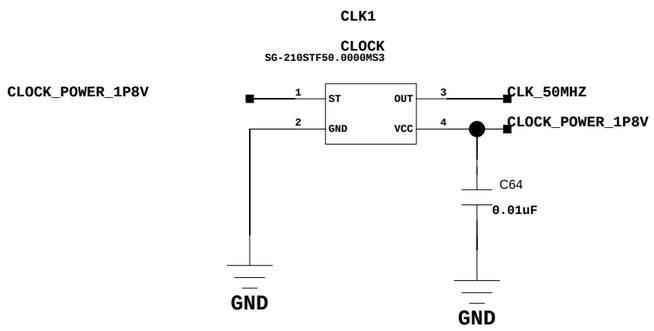


TITLE	DUAL BUCK WITH BOOST		
SIZE B	DWG NO		REV 2
DRAWN BY Kyler Callahan	SCALE	SHEET 2 of 10	2/26/2015

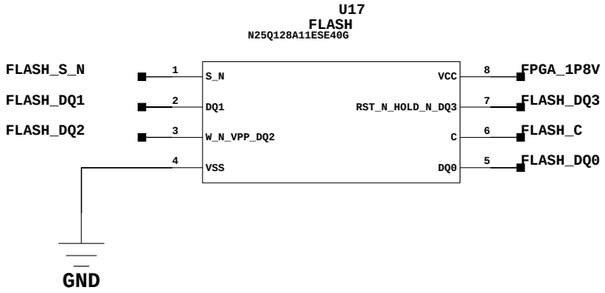


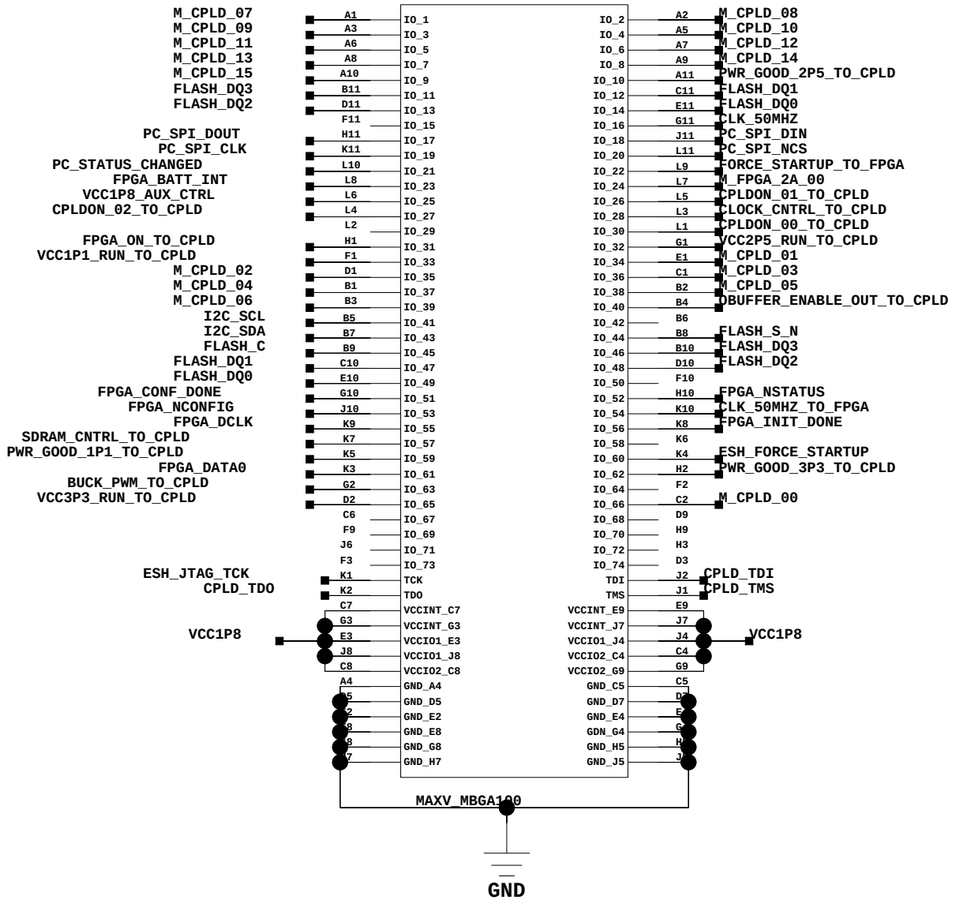
TITLE	OCTAL BUFFER		
SIZE B	DWG NO		REV 2
DRAWN BY Kyler Callahan	SCALE	SHEET 3 of 10	3/22/15

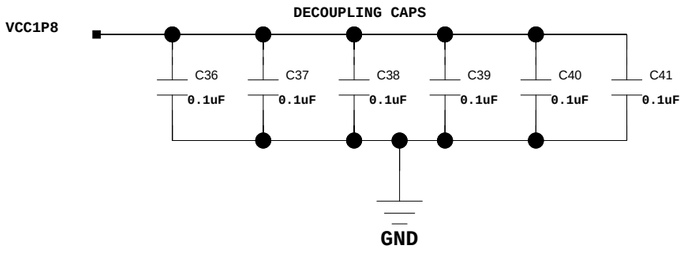




TITLE: CLOCK			
SIZE: B	DWG NO		REV: 2
DRAWN BY: Kyler Callahan	SCALE	SHEET: 4 of 10	2/26/2015



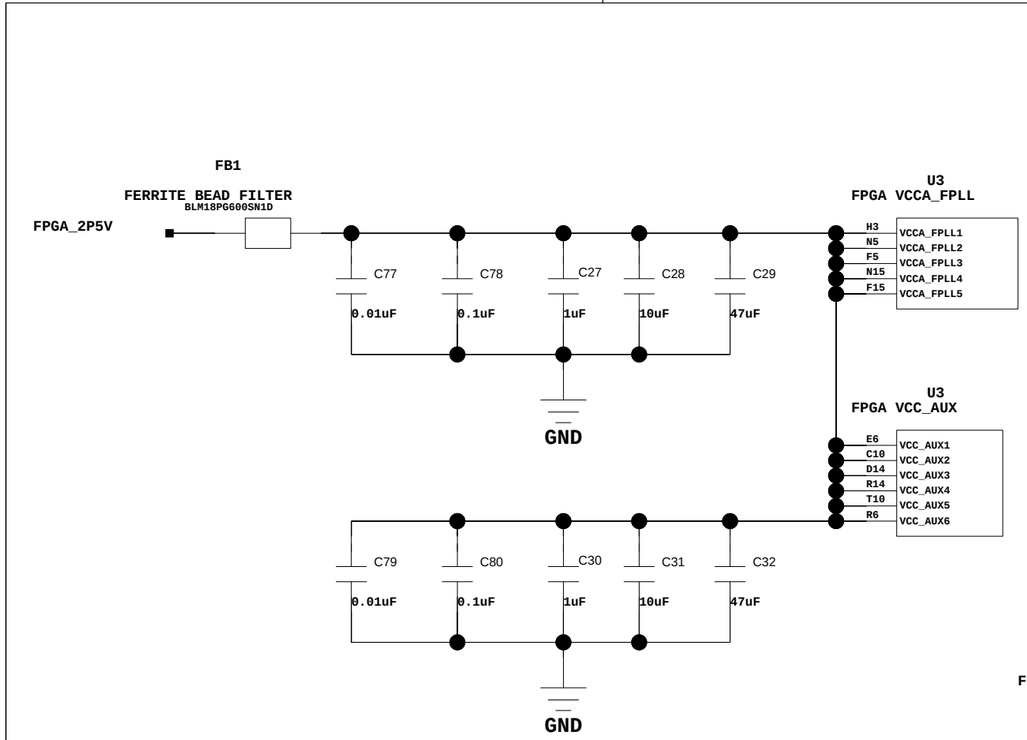


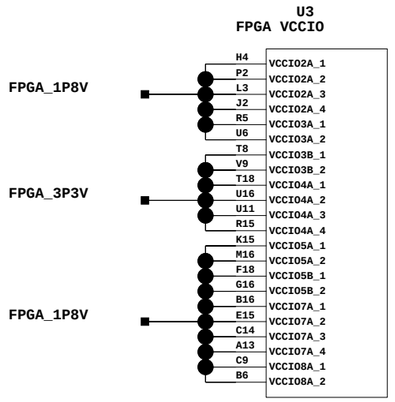


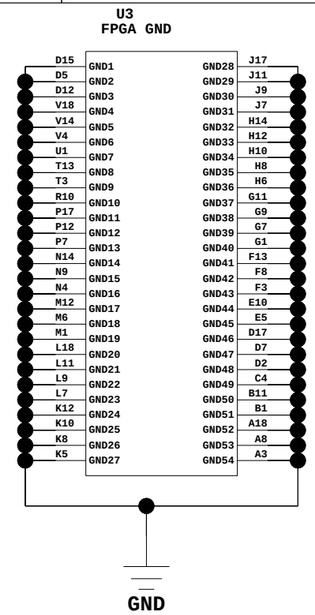
TITLE: CPLD AND FLASH

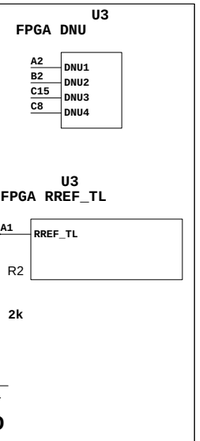
SIZE	DWG NO	REV
B		2

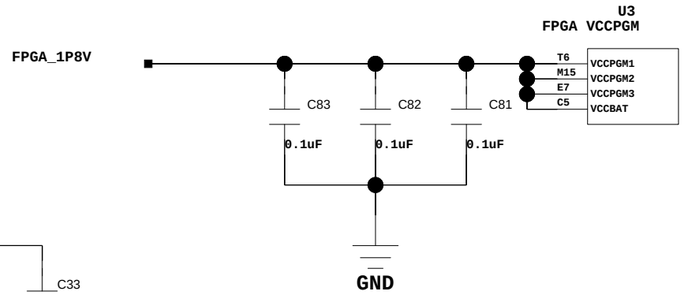
DRAWN BY	SCALE	SHEET	
Kyler Callahan		5 of 10	3/23/15

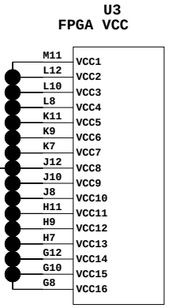


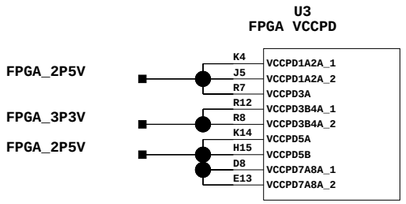


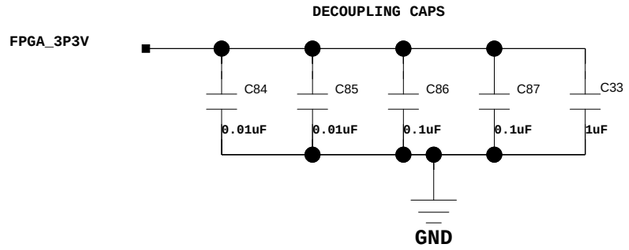


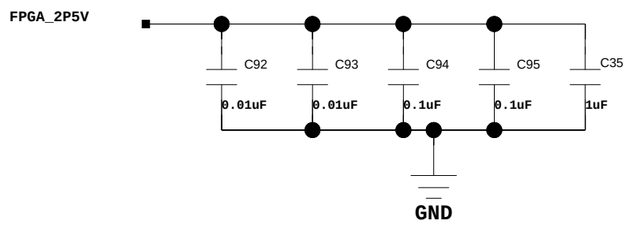


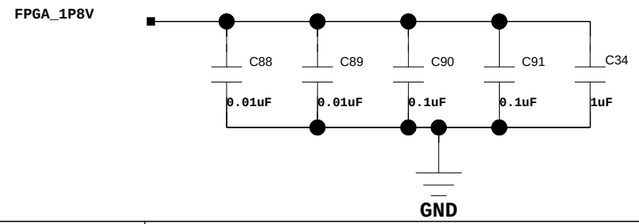


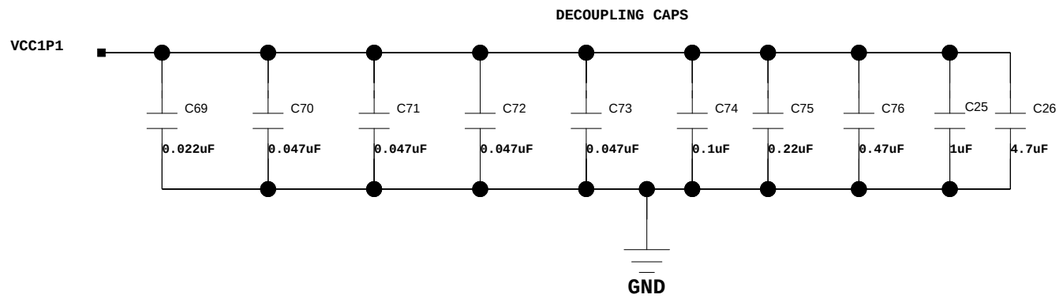




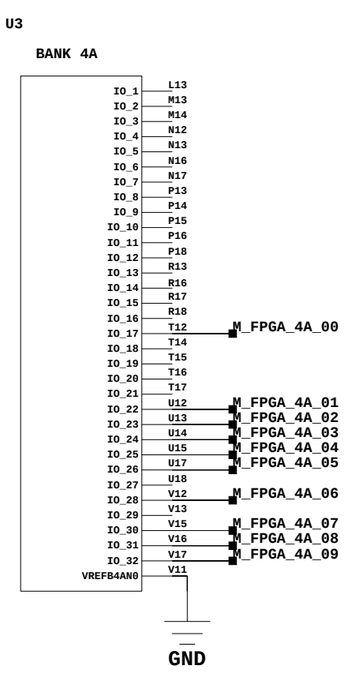


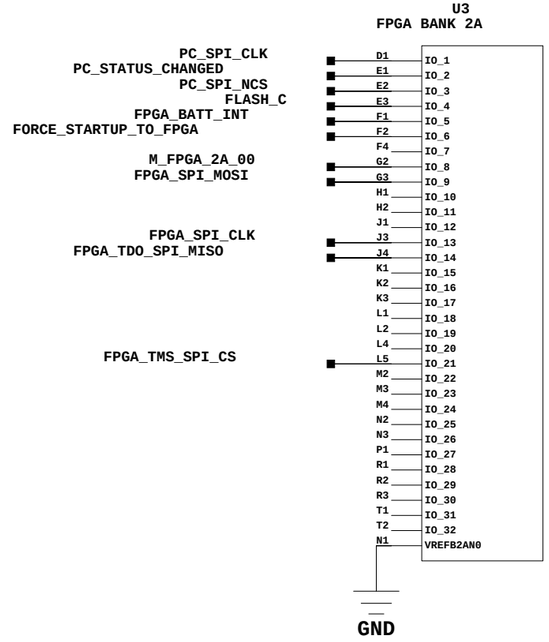


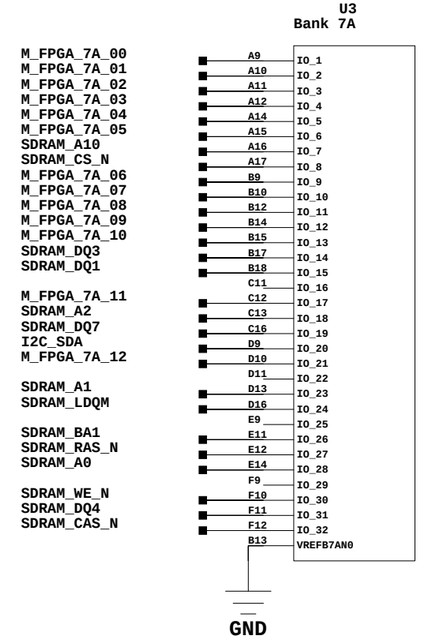


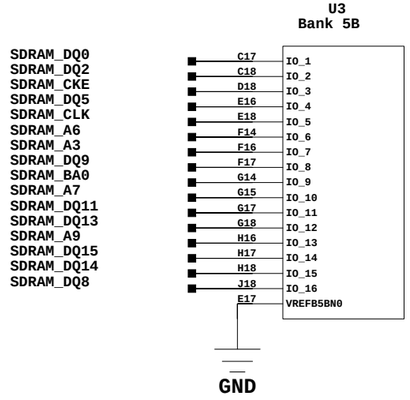


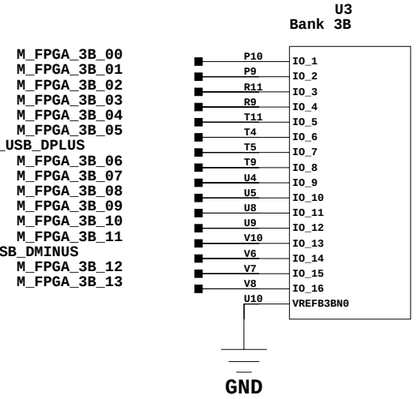
TITLE	FPGA POWER		
SIZE B	DWG NO		REV 2
DRAWN BY Kyler Callahan	SCALE	SHEET 6 of 10	2/26/2015

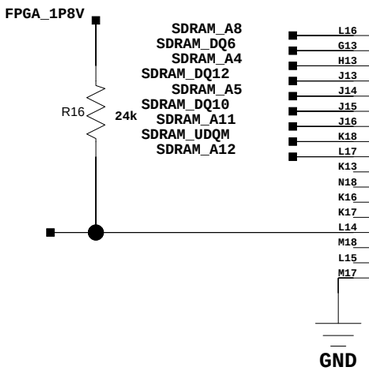


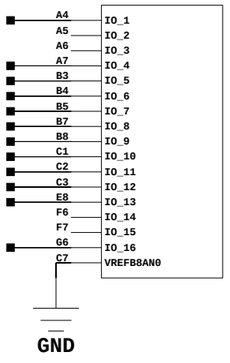


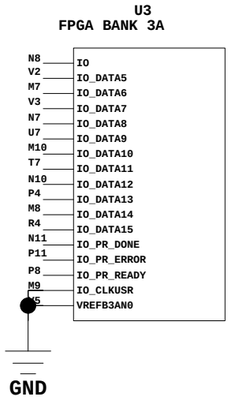


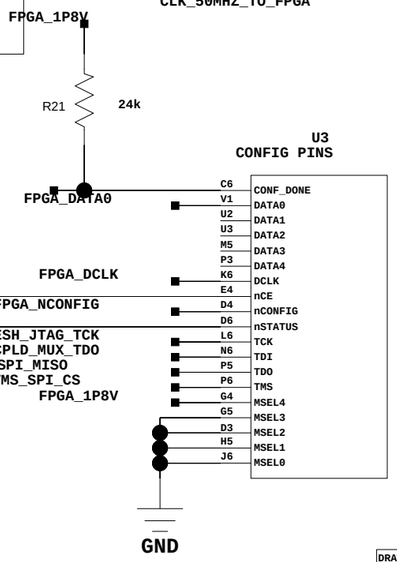










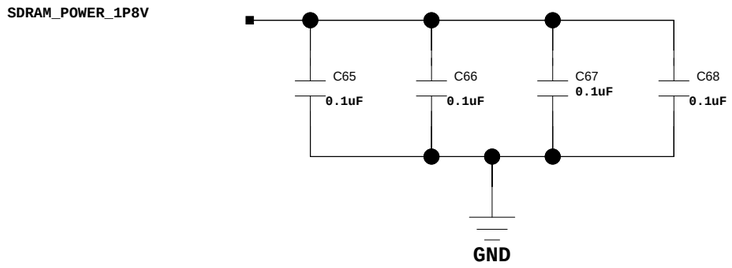


TITLE	FPGA IO		
SIZE B	DWG NO		REV 2
DRAWN BY Kyler Callahan	SCALE	SHEET 7 of 10	3/23/2015

B

A

DECOUPLING CAPS



U9
SD RAM
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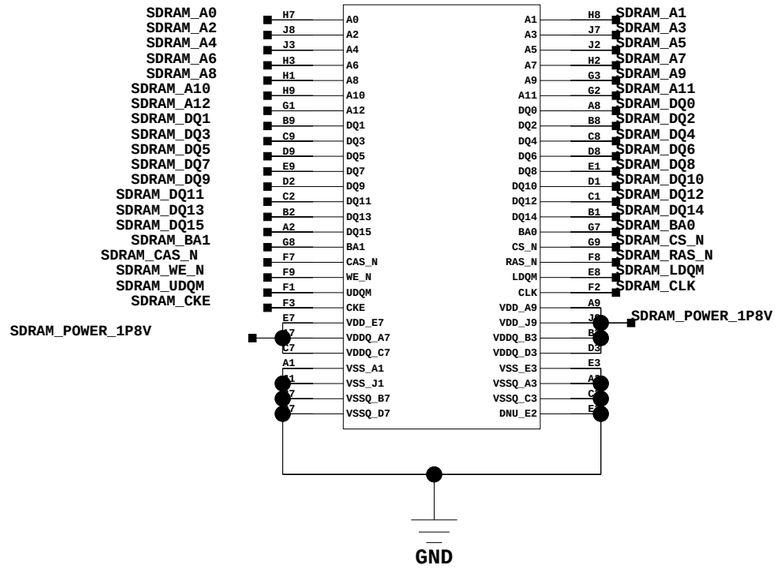
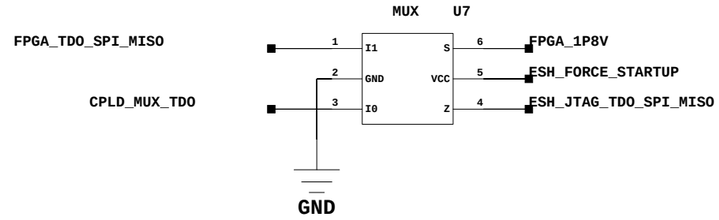
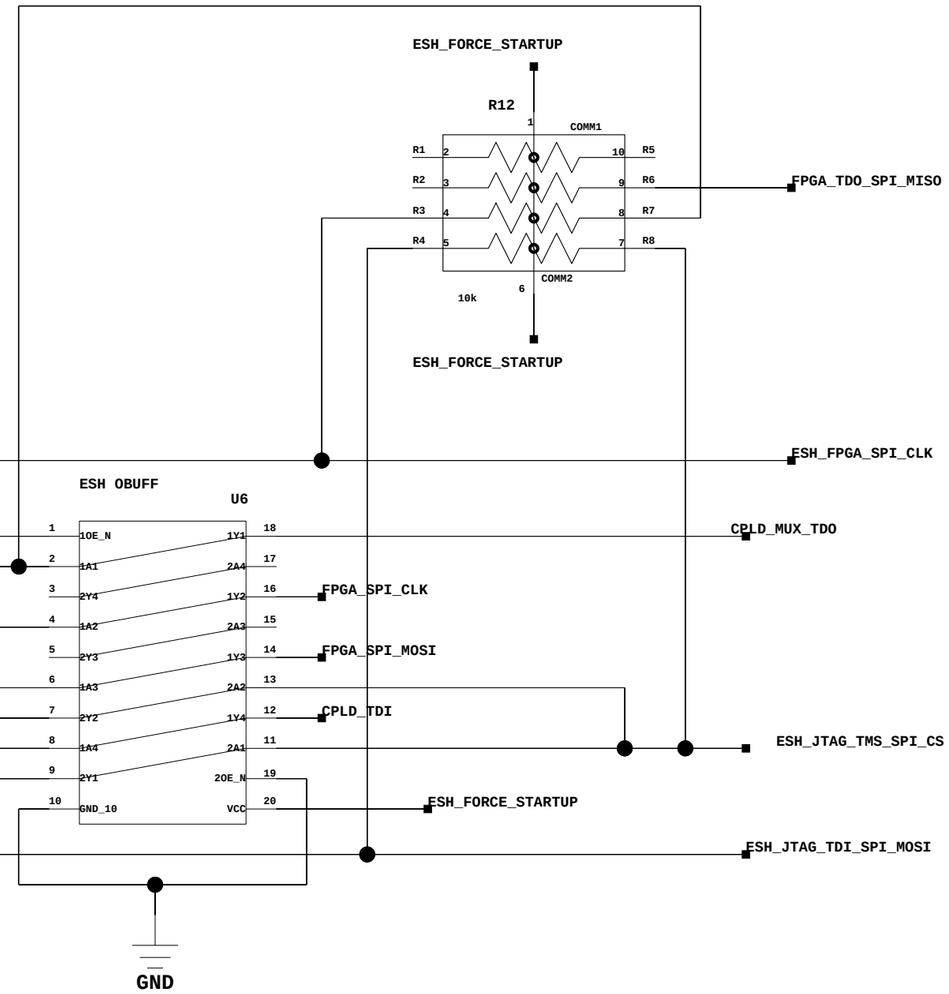
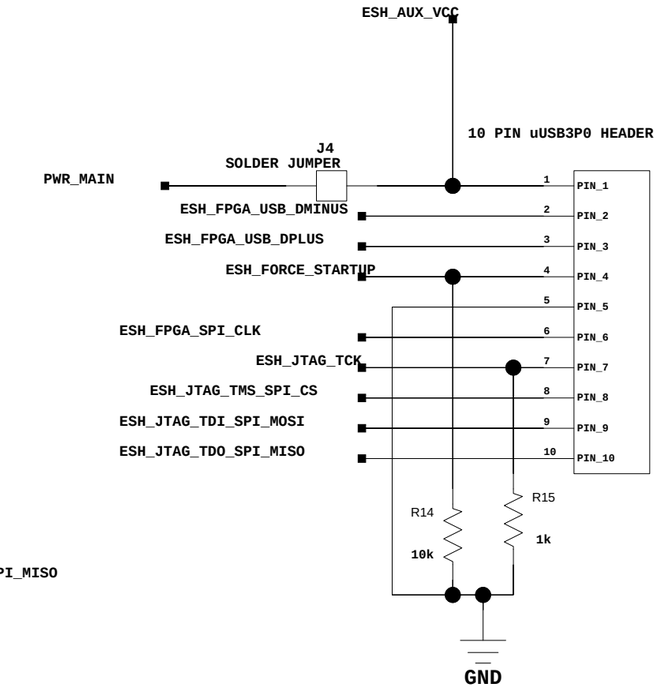
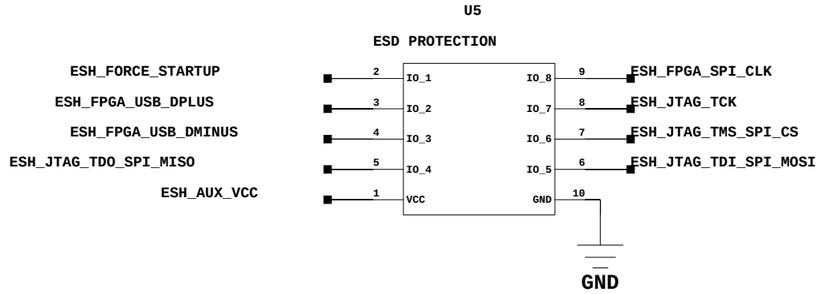


TITLE: SDRAM			
SIZE: B	DWG NO		REV: 2
DRAWN BY: Kyler Callahan	SCALE	SHEET: 8 of 10	2/26/2015

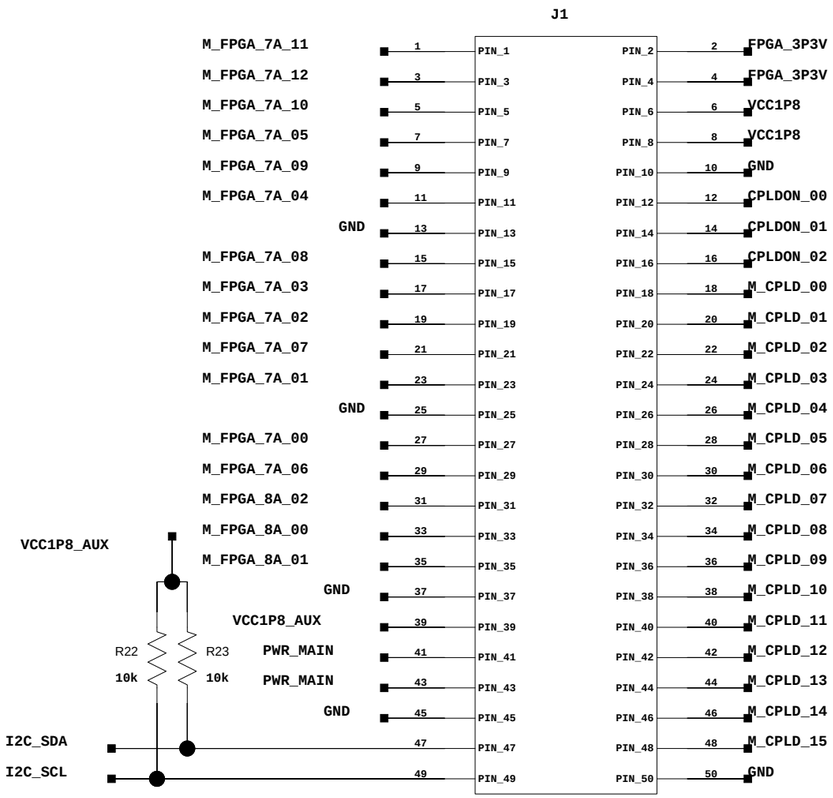


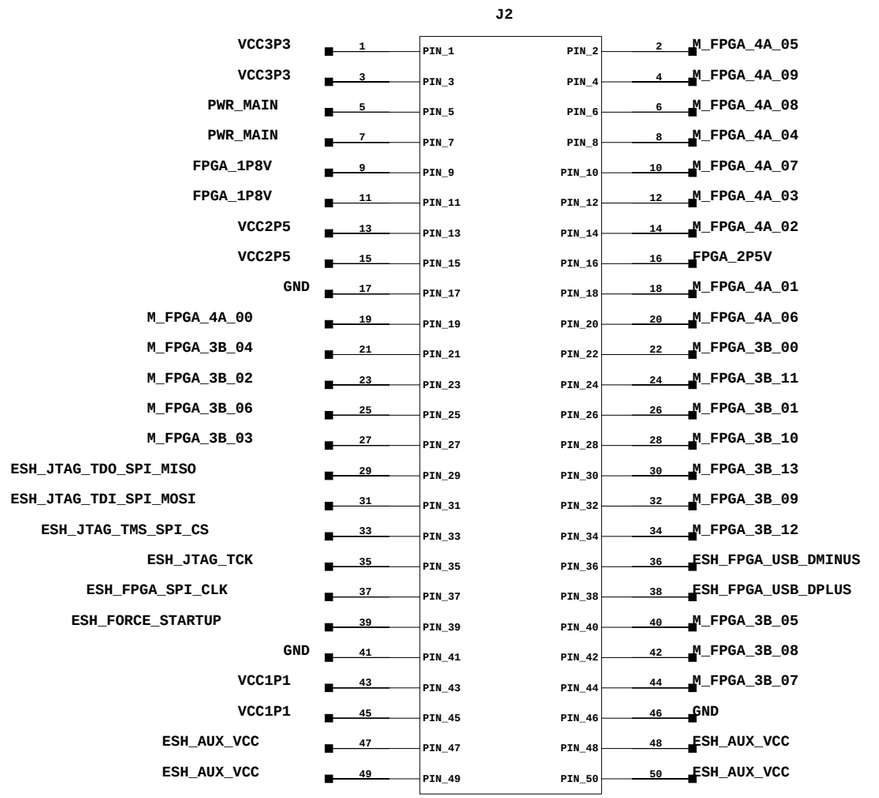






TITLE: 10 PIN EXTERNAL HEADER			
SIZE: B	DWG NO		REV
DRAWN BY: Kyler Callahan	SCALE	SHEET 9 of 10	3/19/15





TITLE	BOARD CONNECTORS		
SIZE B	DWG NO		REV 2
DRAWN BY Kyler Callahan	SCALE	SHEET 10 of 10	3/23/15