Use of SD Level Translator and Implications on System Power

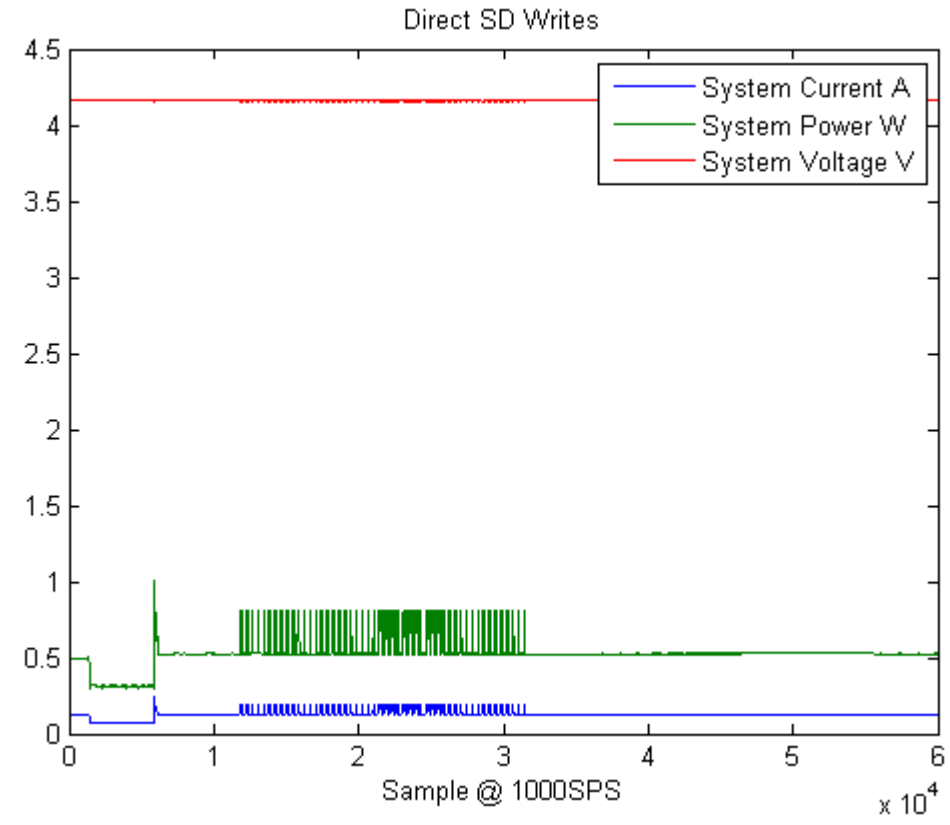
Does using the level translator scheme for writing to the SD card save total system power over a 50mB write test occurring at a clocking speed of 40Mhz? The results show that non substantial amounts of power are saved and in fact the total system power on average per 1mB write is 20mW greater for the level translated system.

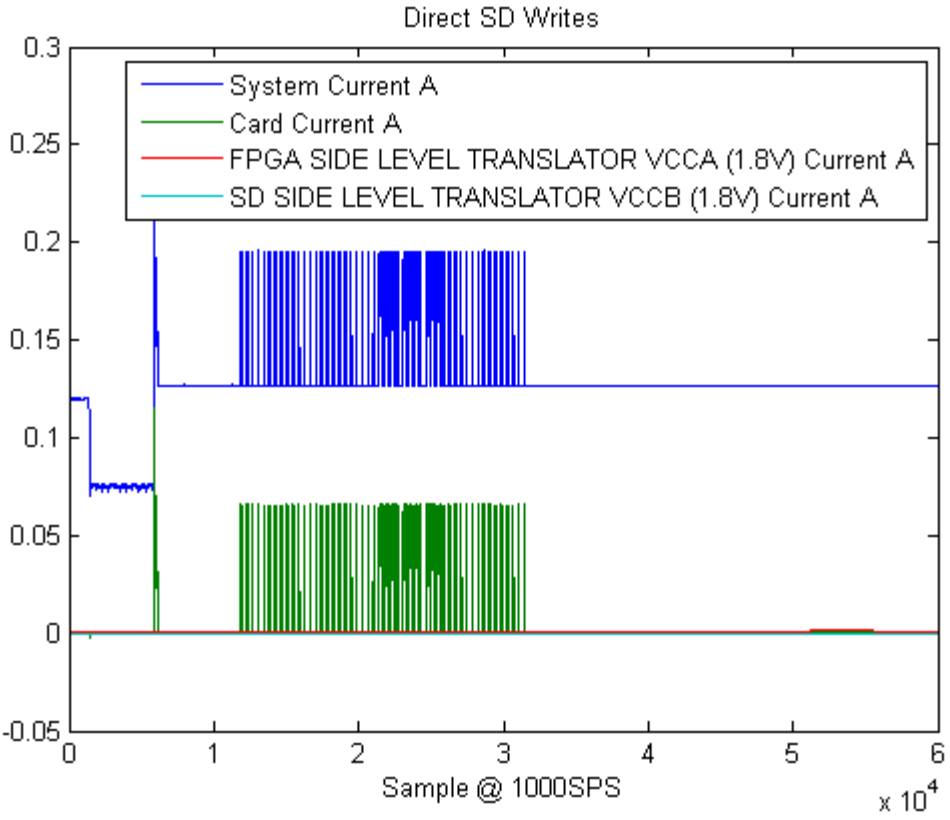
The two FPGA images used to test system power are nearly identical. The differences in the level shifted scheme are turning on the level translator and shifting data through it from the FPGAs 1.8V bank versus the 3.3V bank in the direct writing instance.

Initialization differences are taken out of the equation as only pure data operations are considered in this report. The level shifted initialization of the sd card takes somewhat longer and involves more command response to and from the FPGA. However only data which occurs post initialization are considered. Between the two data sets, the exact same data is sent to the sd card involving the same sequence of commands.

Both images utilized a 40mHz PLL output for sd clocking. Thus overall system power usage will most likely be greater than in a non PLL scheme, however the level translator's max data rate appears to be 40mHz in the current configuration. Thus a 40Mhz PLL clock was used.

Below we see system characteristics during a 50mB test write to the sd card without the use of the level translator. All signaling occurs at 3.3V and a 3.3V bank of the FPGA is utilized. The pulses indicate sending exactly 1mB of data to the sd card. A total of 50 1mB pulses are sent. Important things to notice here are the current usage of the level translator during this test. It is not drawing any current.


Direct SD Writes
System Current A
System Power W
System Voltage V
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
0
1
2
3
4
5
6
Sample @ 1000SPS
x 10^4

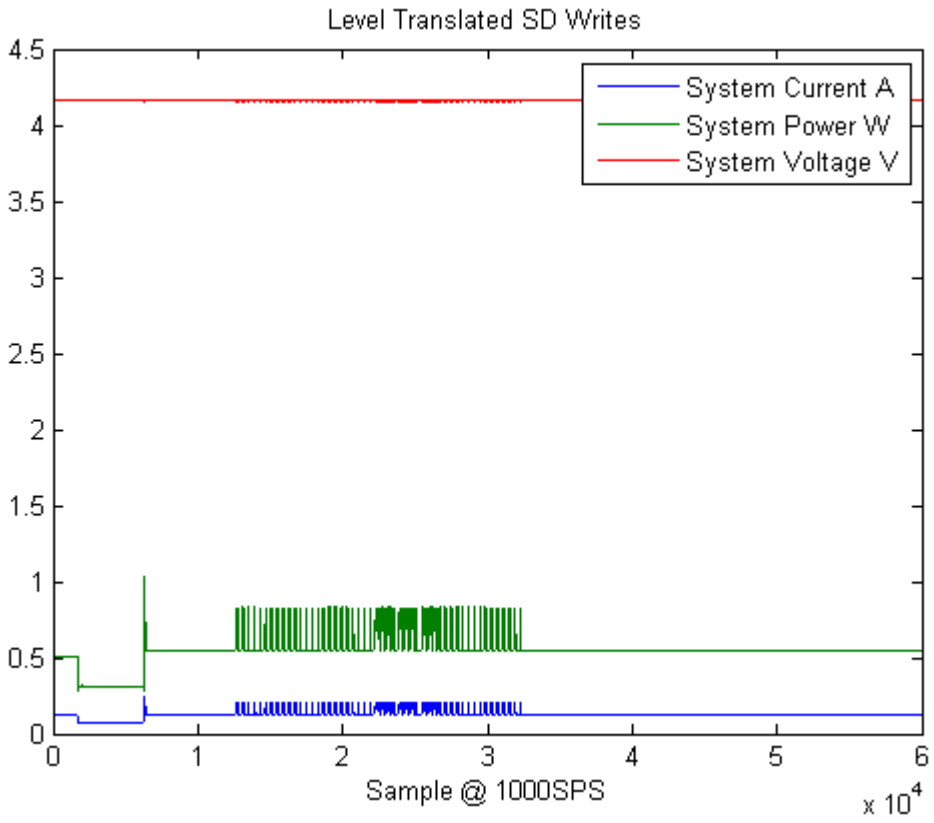

Direct SD Writes
System Current A
Card Current A
FPGA SIDE LEVEL TRANSLATOR VCCA (1.8V) Current A
SD SIDE LEVEL TRANSLATOR VCCB (1.8V) Current A
0.3
0.25
0.2
0.15
0.1
0.05
0
-0.05
0
1
2
3
4
5
6
Sample @ 1000SPS
x 10^4

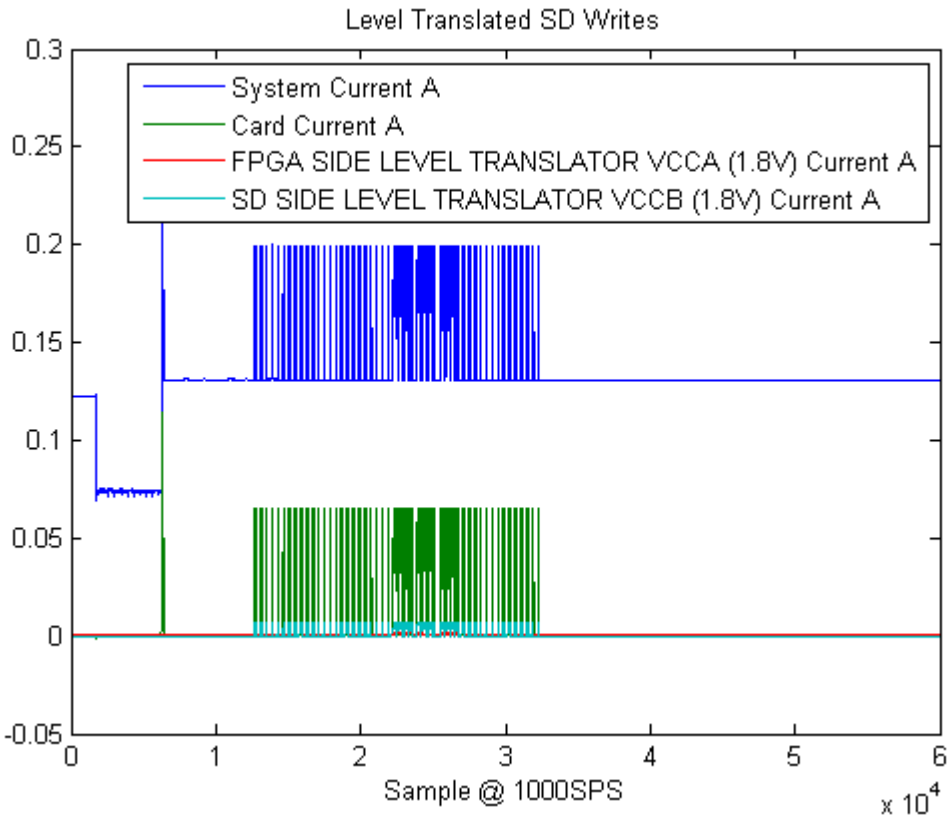
If the system power peaks are extracted and the average system power is taken but only when the card is actively engaged writing (during the pulse) the following results are found. These results are for the DIRECT WRITE mode.

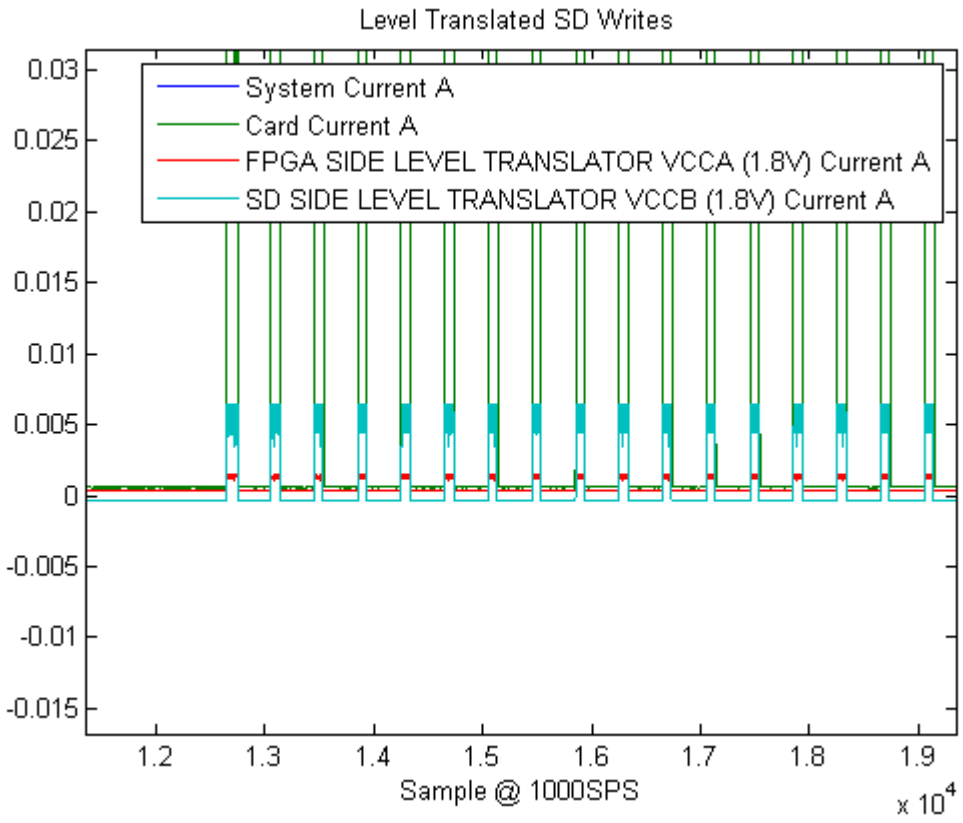
Speed (Mhz)	Width	Signalling	Data Amount (1mB)	Multi block	Sampling_Rate	Total_Time (Samples)	Data_Time(s)	Speed (MB/s)	Total_System_Power_While_Active_Mean mW
40	4	3.3	1	128	1000	87	0.087	11.49425287	755.296996
40	4	3.3	1	128	1000	85	0.085	11.76470588	755.8259132
40	4	3.3	1	128	1000	87	0.087	11.49425287	755.9650404
40	4	3.3	1	128	1000	88	0.088	11.36363636	753.9285424
							AVG	AVG	AVG
							0.12402	9.897577889	752.9780723

Thus the average system power to write 1MB of data to sd flash directly is 752mW in this instance. The first 47 data points are cut from the above table, only the last 3 and averages are shown.

The same analysis can be done on a level shifted 50mB write test. In this case, the level translator is actively engaged. In this case, the level translator only handles 1.8V -> 3.3V signaling conversion during the first portion of sd card initialization. After the voltage switch of sd card initialization, the level translator is effectively doing a 1.8V -> 1.8V signaling conversion. Thus all data pulses are a 1.8V -> 1.8V signaling conversion.


Level Translated SD Writes
System Current A
System Power W
System Voltage V
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
0
1
2
3
4
5
6
Sample @ 1000SPS
x 10^4


Level Translated SD Writes
System Current A
Card Current A
FPGA SIDE LEVEL TRANSLATOR VCCA (1.8V) Current A
SD SIDE LEVEL TRANSLATOR VCCB (1.8V) Current A
0.3
0.25
0.2
0.15
0.1
0.05
0
-0.05
0
1
2
3
4
5
6
Sample @ 1000SPS
x 10^4



The system characteristics look similar but it can be seen above that that unlike the direct write mode, the level translator here is engaged and actively consuming current on both its reference voltage ports during the writing activity. These pulses again are occurring at a 1.8V -> 1.8V signaling conversion, that is both VCCA and VCCB of the TI TXB0106 are at 1.8V.

The 1mB pulse currents can also be averaged for the VCCA current and the VCCB current. When the peaks are extracted with a function and all the individual 1mB averages are again averaged across all 50mB, the following numbers are arrived at.

On average the VCCA port is drawing 1.33mA additional current while writing data to the sd card. On average the VCCB port is drawing 5.3mA additional current while writing data to the sd card.

Speed (Mhz)	Width	Signalling	Data Amount (1mB)	Multiblock	Sampling_Rate	Total_Time (Samples)	Data_Time(s)	Speed (MB/s)	Total_System_Power_While_Active_Mean mW
40	4	1.8	1	128	1000	88	0.088	11.36363636	772.7683892
40	4	1.8	1	128	1000	87	0.087	11.49425287	773.9158221
40	4	1.8	1	128	1000	85	0.085	11.76470588	774.6536672
40	4	1.8	1	128	1000	87	0.087	11.49425287	774.8100368
40	4	1.8	1	128	1000	88	0.088	11.36363636	772.4130477
							AVG	AVG	AVG
							0.12428	9.891012157	771.5832851

Here we see that total average system power for a 1mB write to the level shifted card is ~20mW greater than in the direct write mode instance.

This is a direct system comparison. The only difference between the data above for the direct write instance and the level translated instance is the route of the data to the sd card from a 3.3V bank directly to the card or from a 1.8V FPGA bank, through the TXB0106, and then to the card. Powering the reference voltage ports of the TXB0106 is necessary and visible in the level translated instance.

3 previous data sets were also analyzed but had not integrated power measurement yet and only looked at current measurement of the main power rail. However in all three comparison instances, the total system current was always greater in the level translated case.

Current utilization of the sd card itself appears to be .6mA greater in the level translated configuration.

Conclusion

Use of a sd level translation scheme to save total system power is not recommended. The use of two FPGA banks (1.8V and 3.3V) with controllable buffers is most likely the next step for speeds greater than 50Mhz.