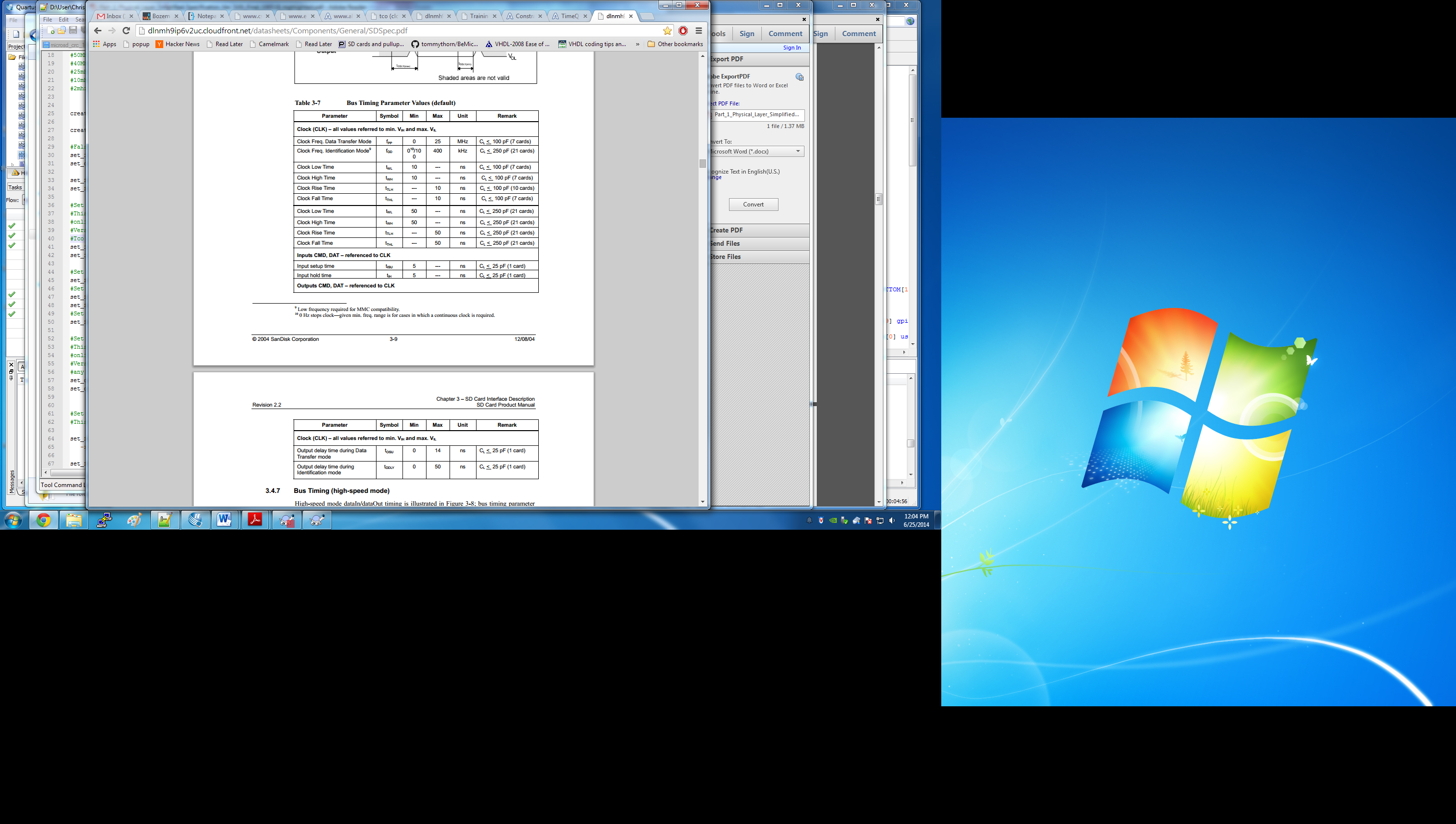
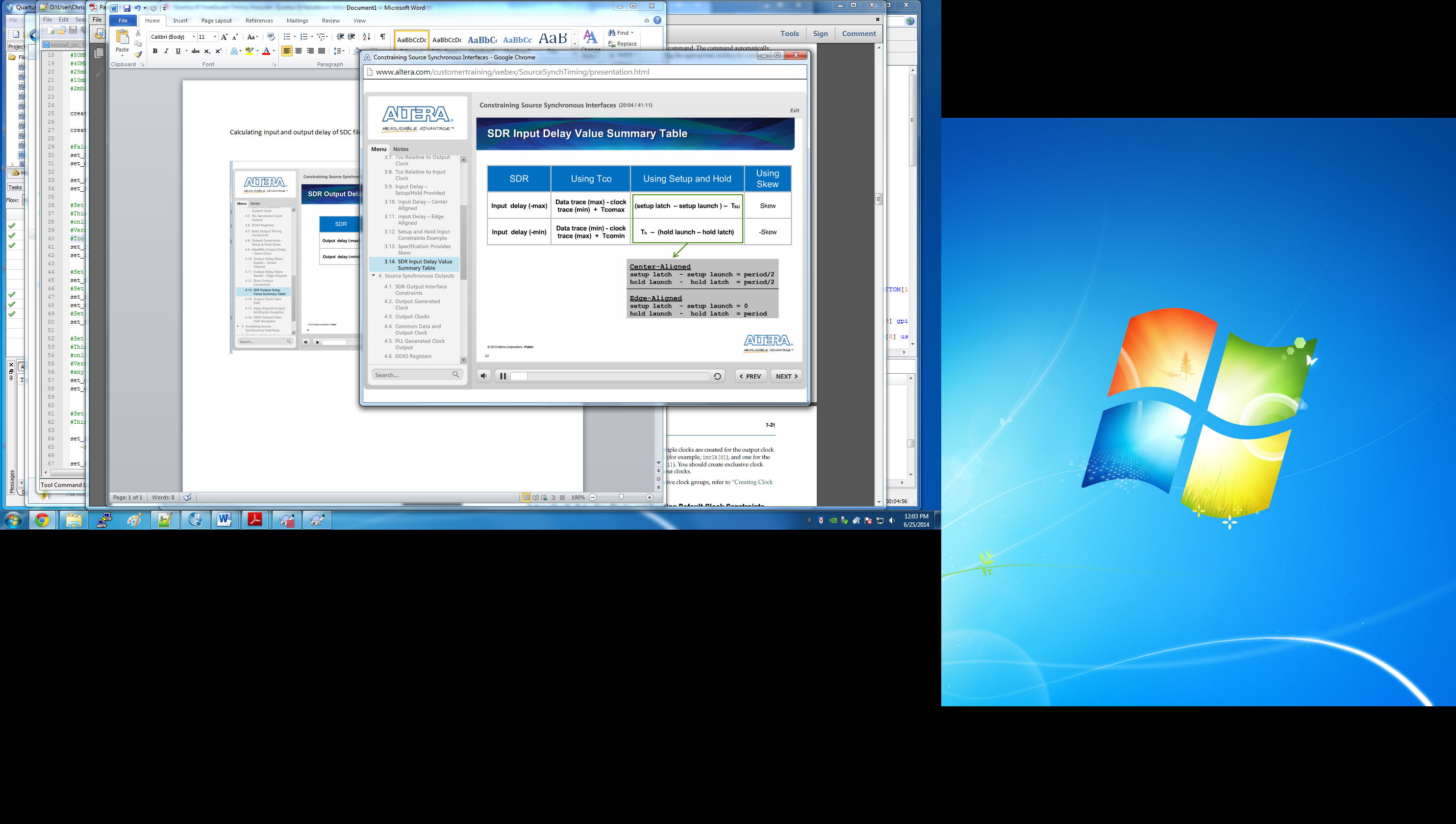
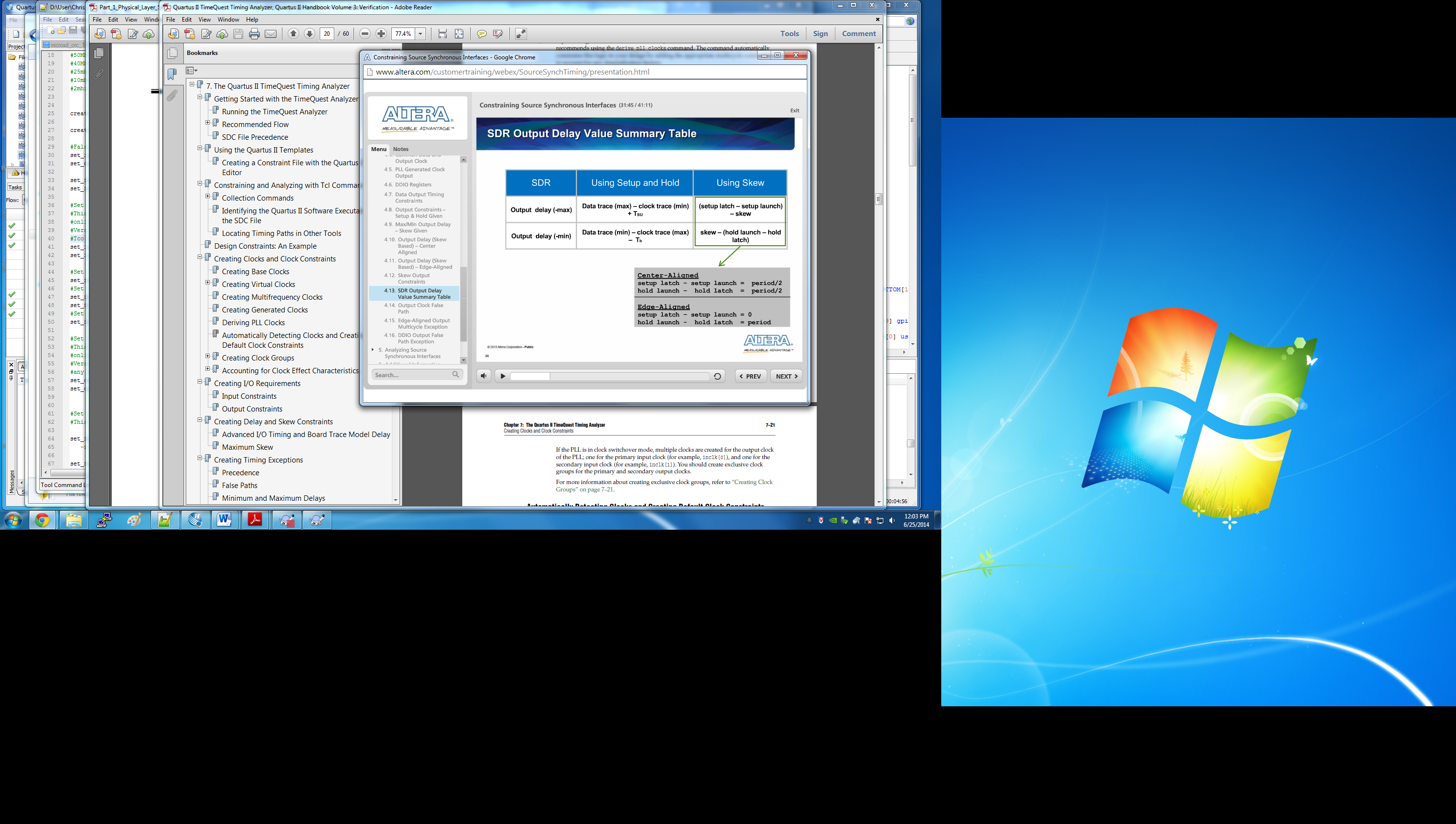
Calculating input and output delay of SDC file for a source synchronous interface.



Tco of Altera speak taken to be Tosu of the SD manual. No clock or data trace delay was added to the sdc file calculations. Below are the formulas for the SDR timings.





Altera speak on Tco

|  |  |  |
| --- | --- | --- |
|  |  |  |
| [**[gloss.gif](http://quartushelp.altera.com/12.1/mergedProjects/quartus/gl_quartus_welcome.htm)**](http://quartushelp.altera.com/12.1/mergedProjects/quartus/gl_quartus_welcome.htm) | **tCO (clock to output delay)** |  |

The maximum time required to obtain a valid output at an output pin after a clock transition at an input clock pin, directly or through a register.