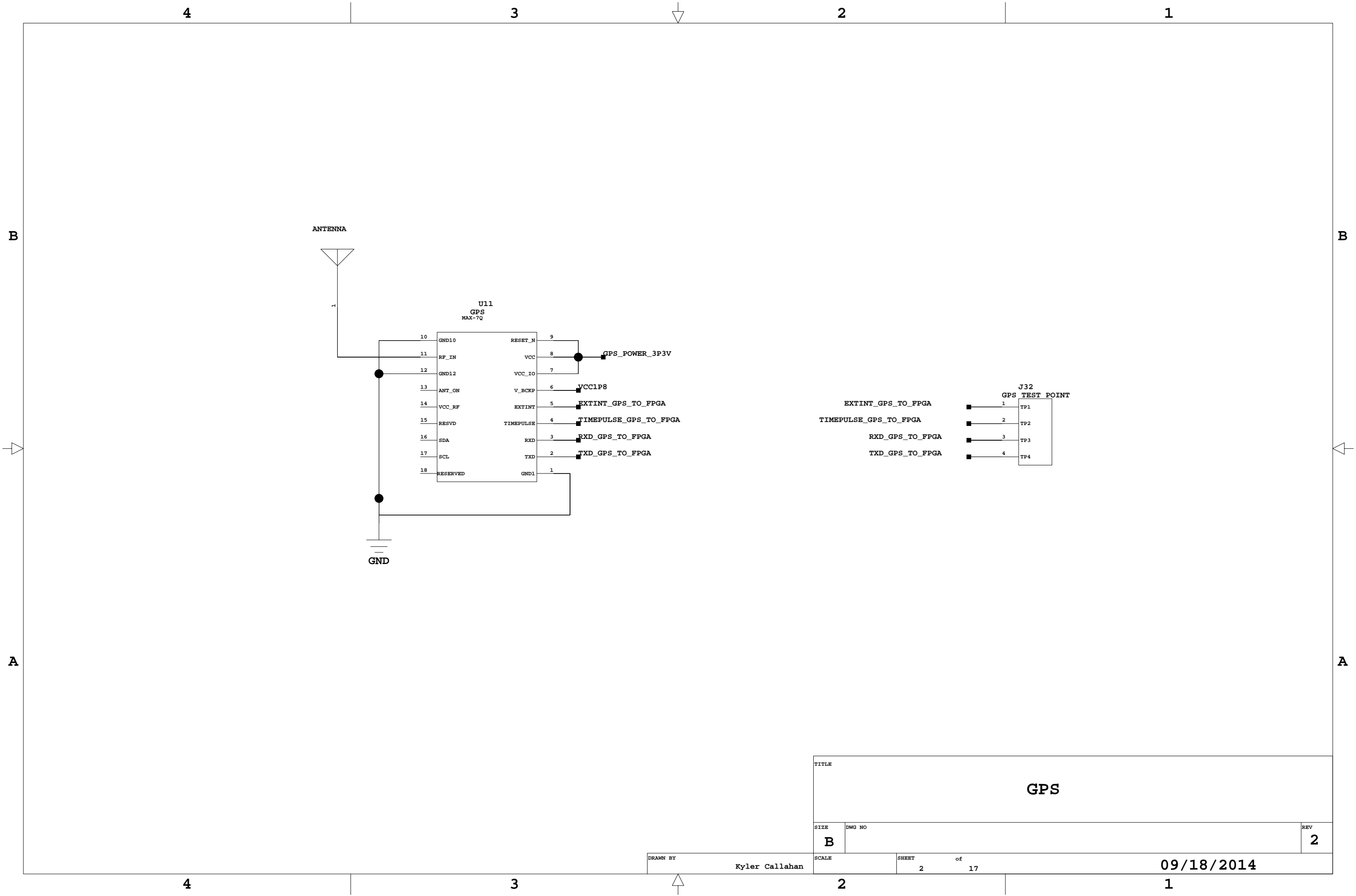
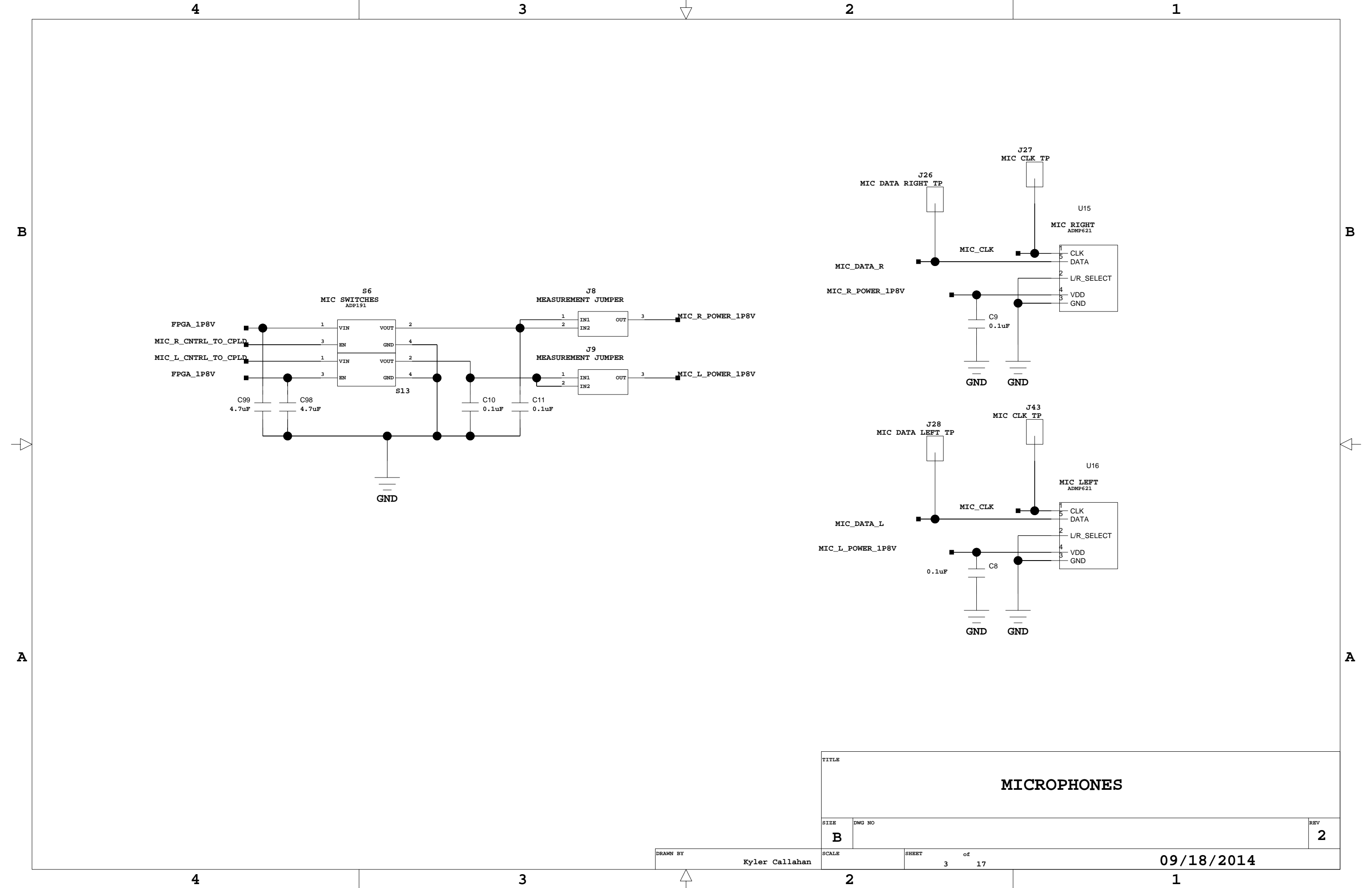
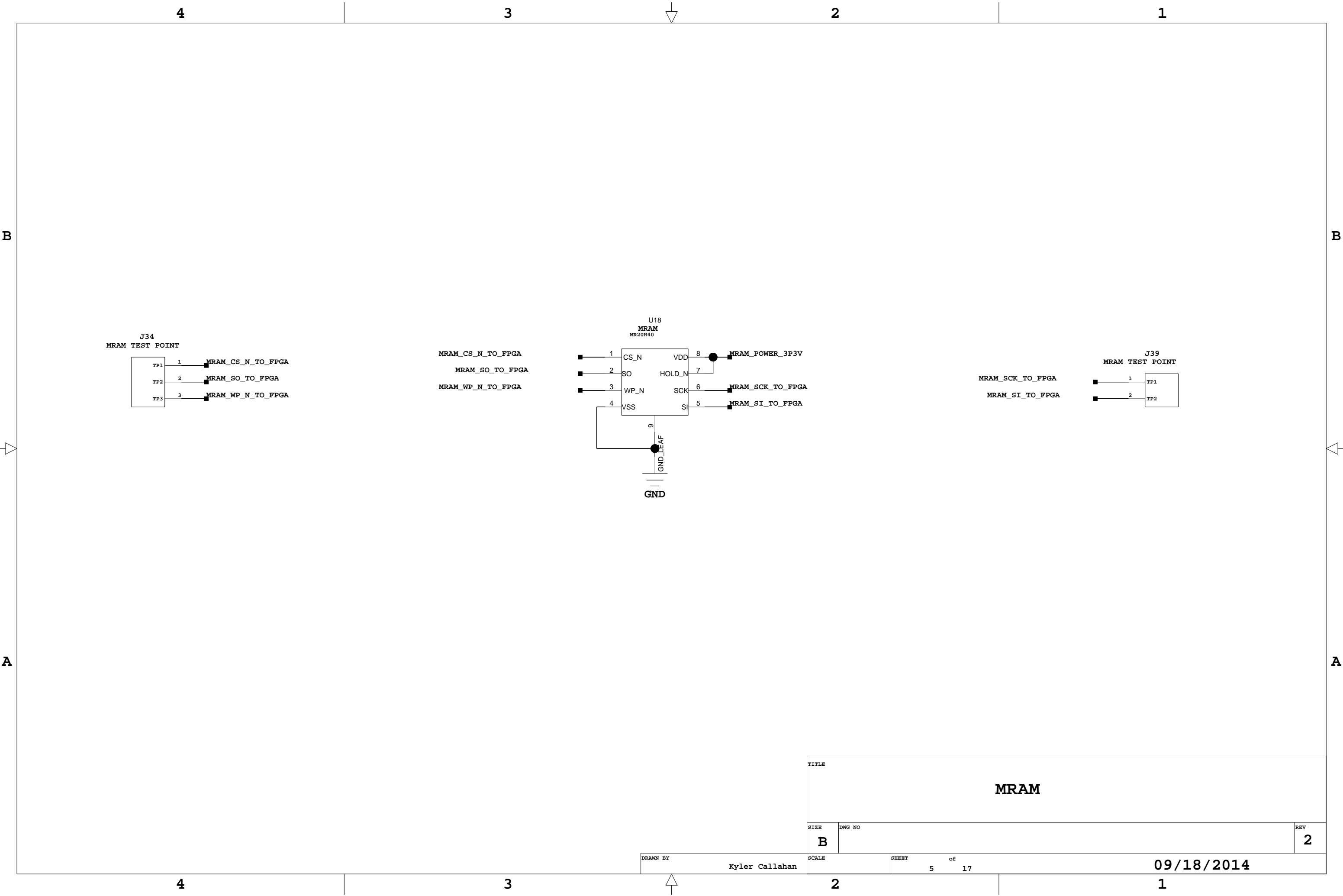


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INERTIAL MODULE			
SIZE	DWG NO	REV	
B		2	
SCALE	SHEET	of	REV
	1	17	09/18/2014



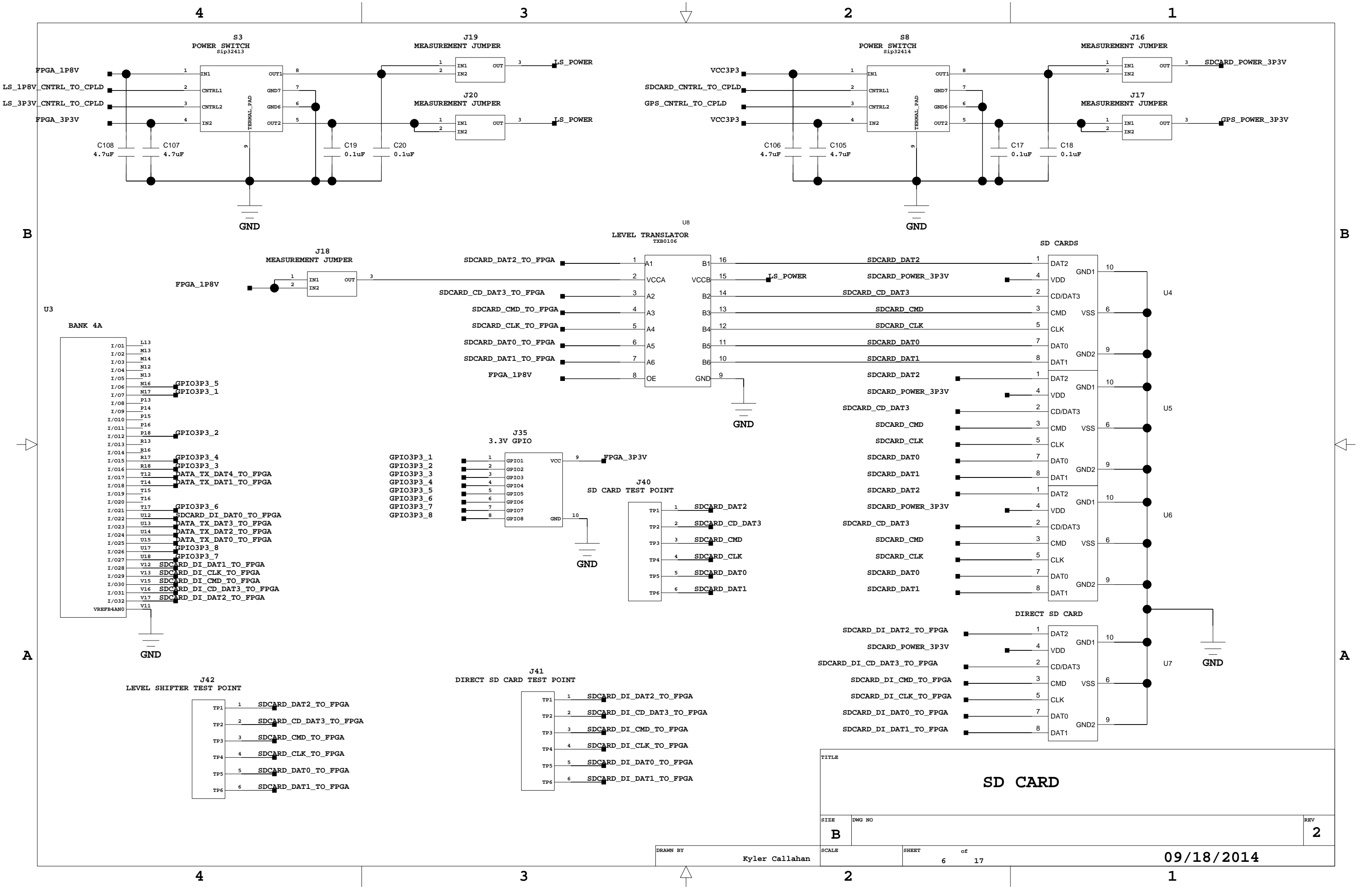
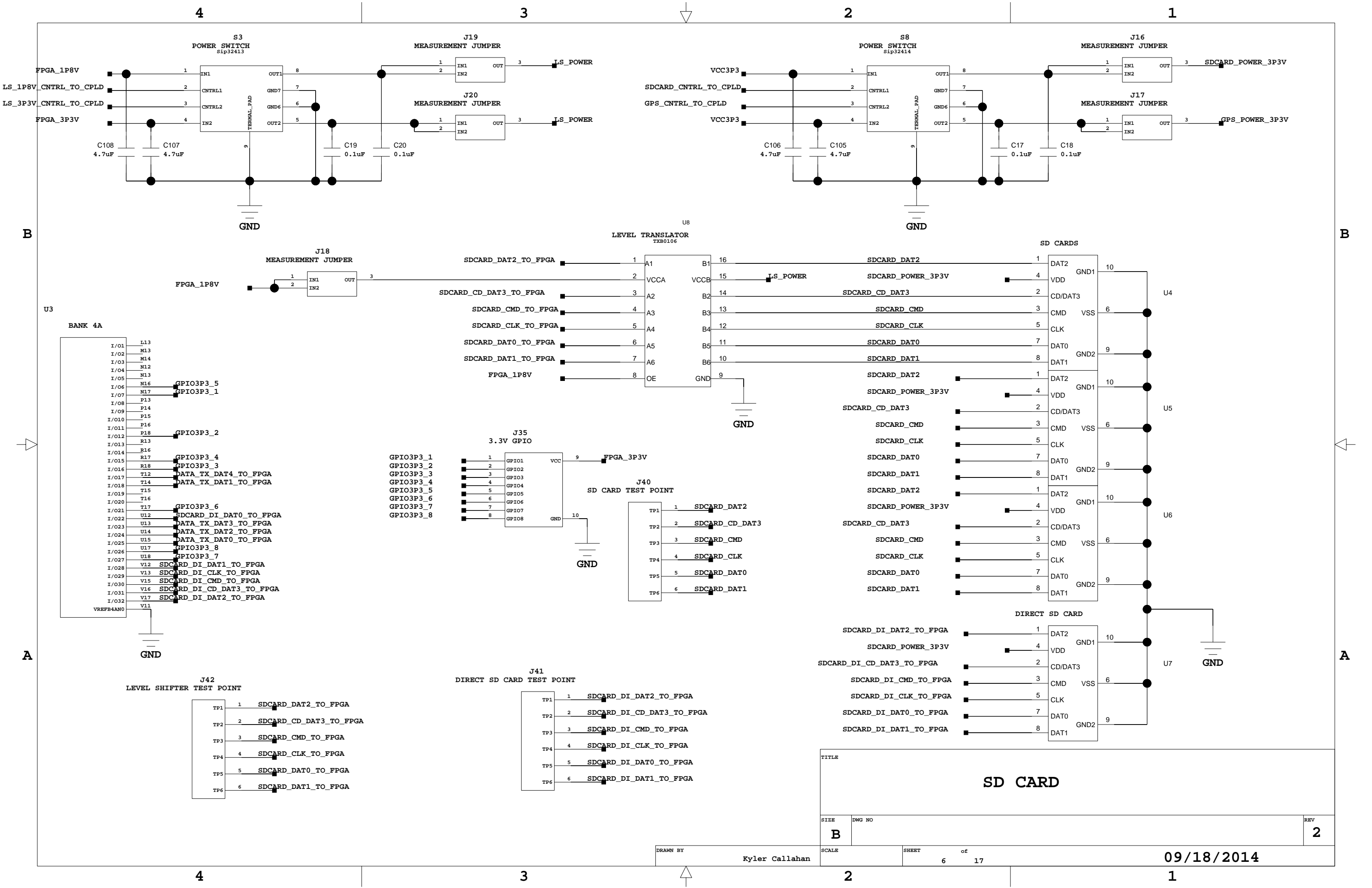
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B							
SCALE	SHEET		of	09/18/2014			
	2		17				

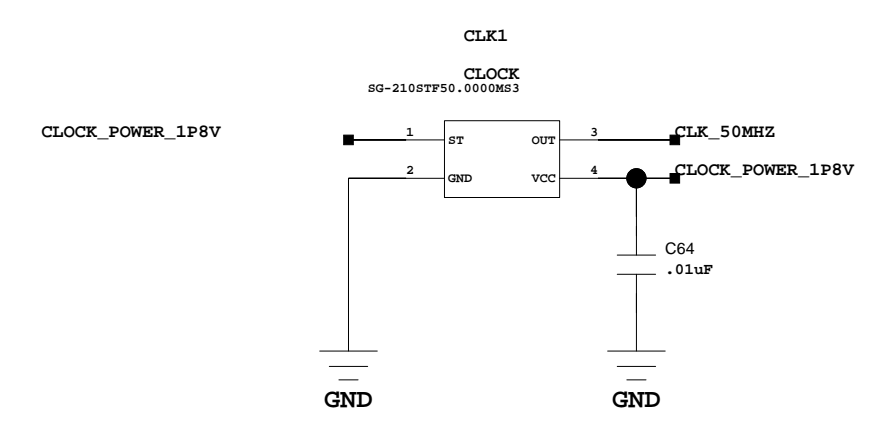
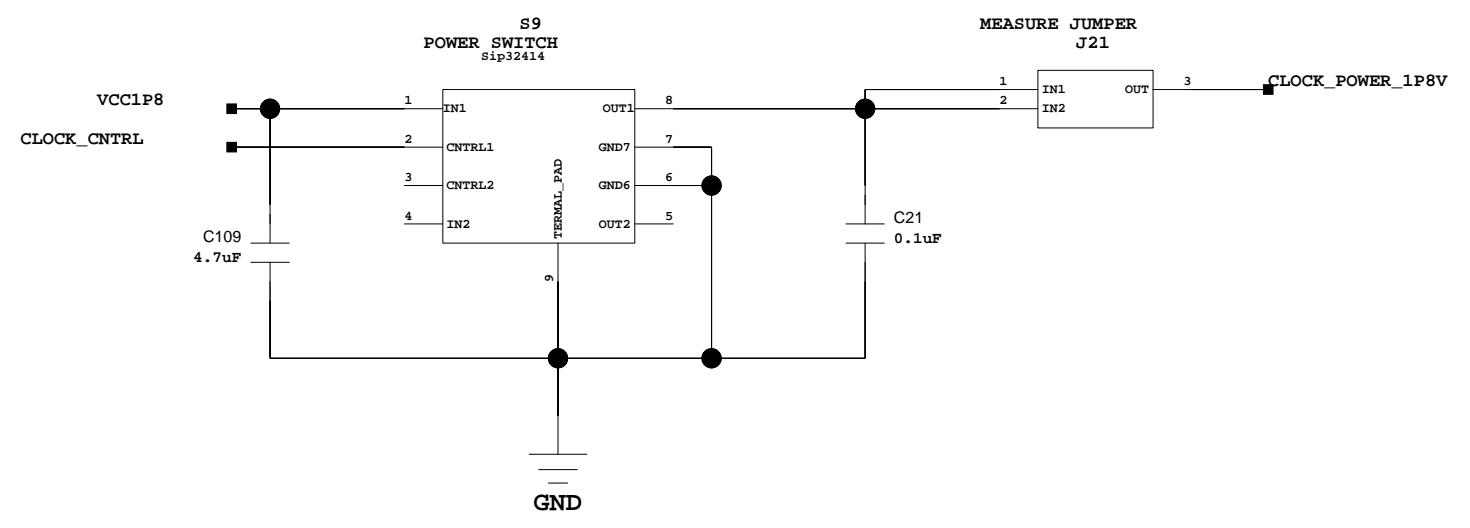




TITLE				MRAM			
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SCALE			SHEET	5	of	17	09/18/2014

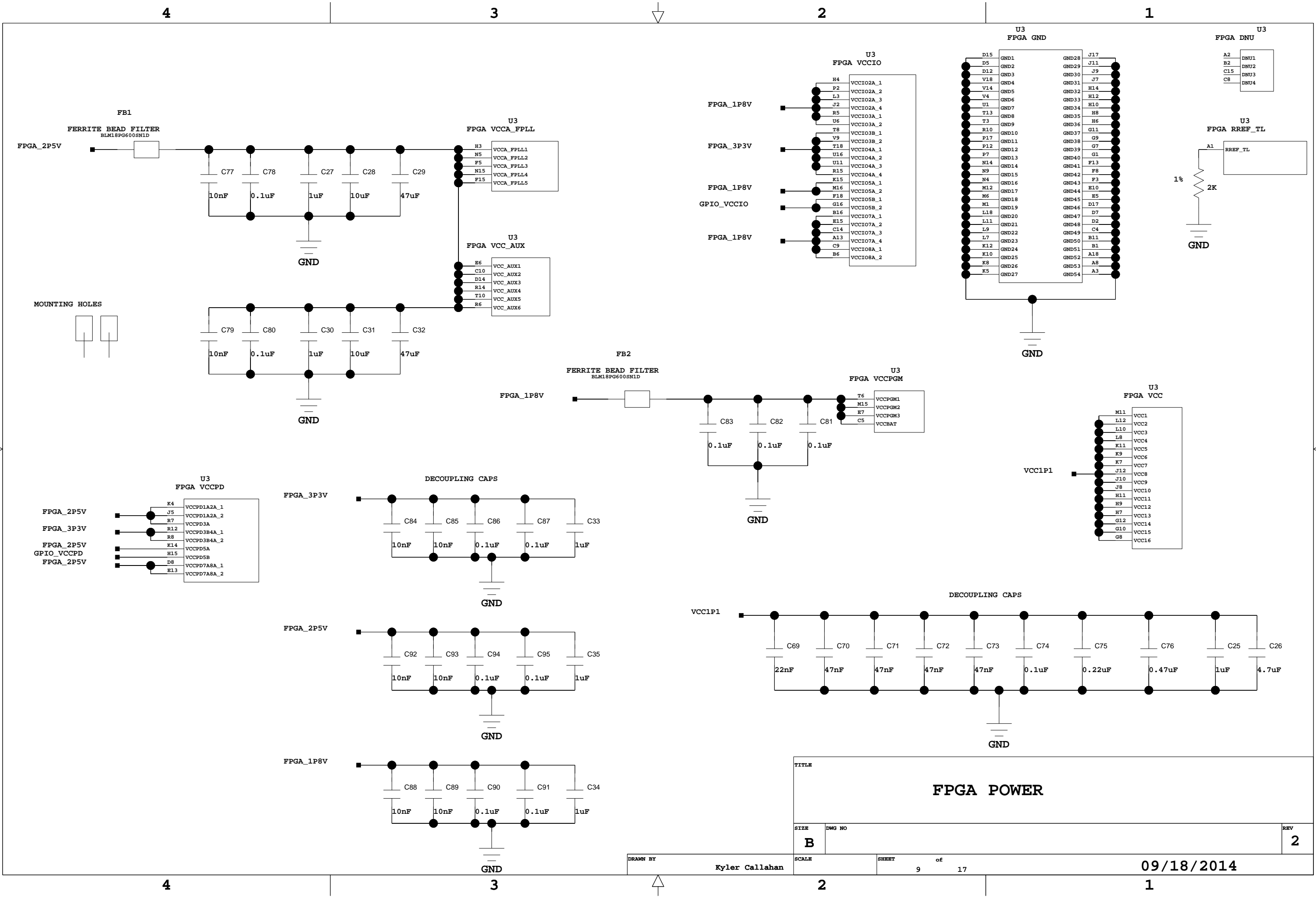
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TITLE			
CLOCK			
SIZE	DWG NO	REV	
B		2	
SCALE	SHEET	of	09/18/2014
	7	17	

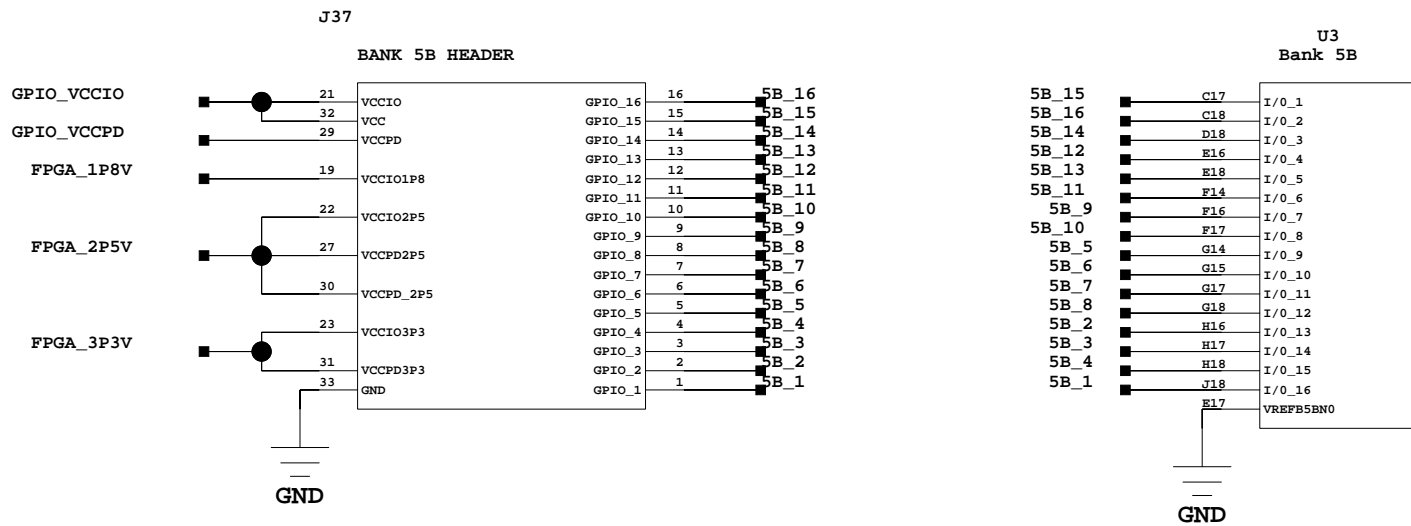
DRAWN BY
Kyler Callahan



TITLE				
FPGA POWER				
SIZE	DWG NO	SCALE	SHEET	REV
B			9 of 17	2
09/18/2014				

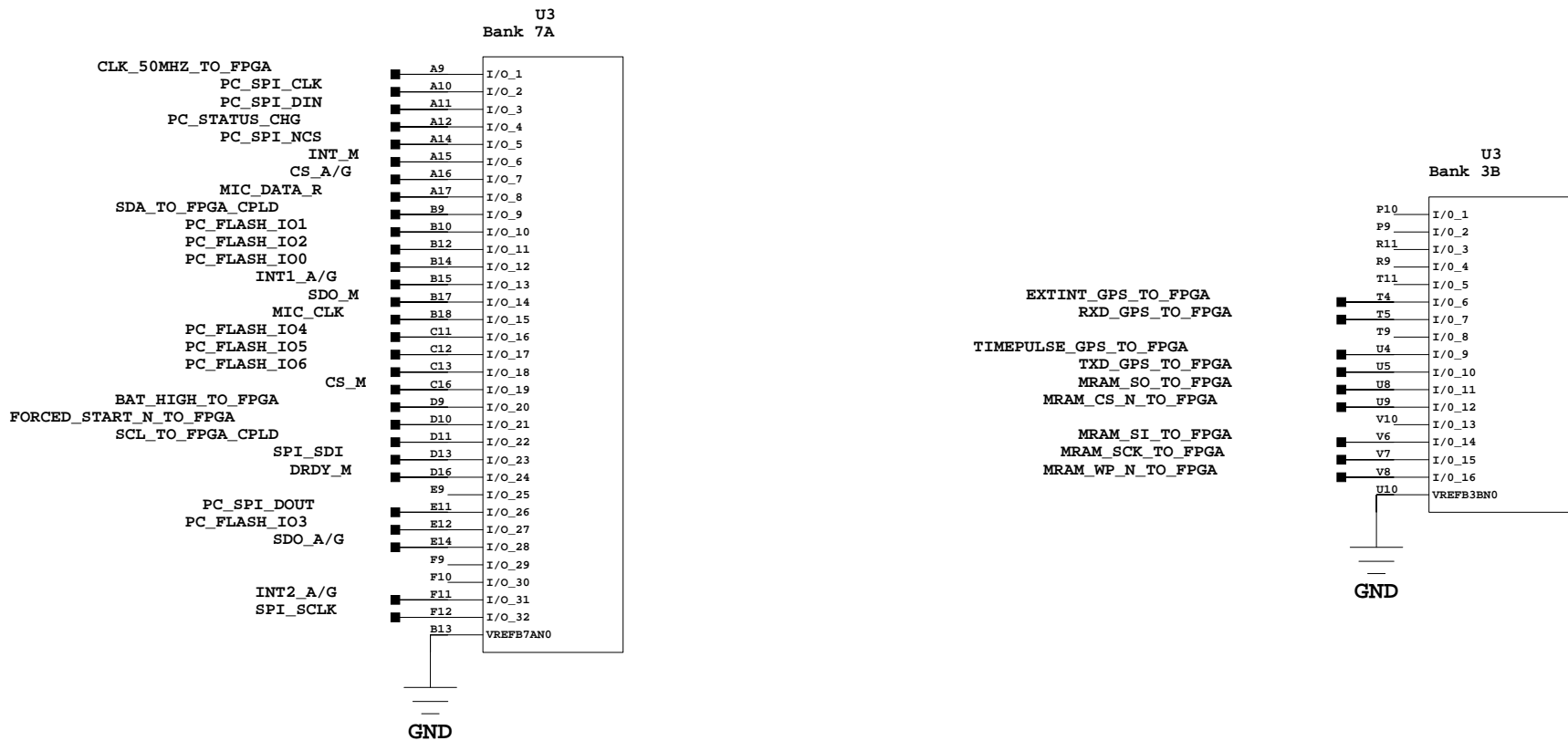
B

B



A

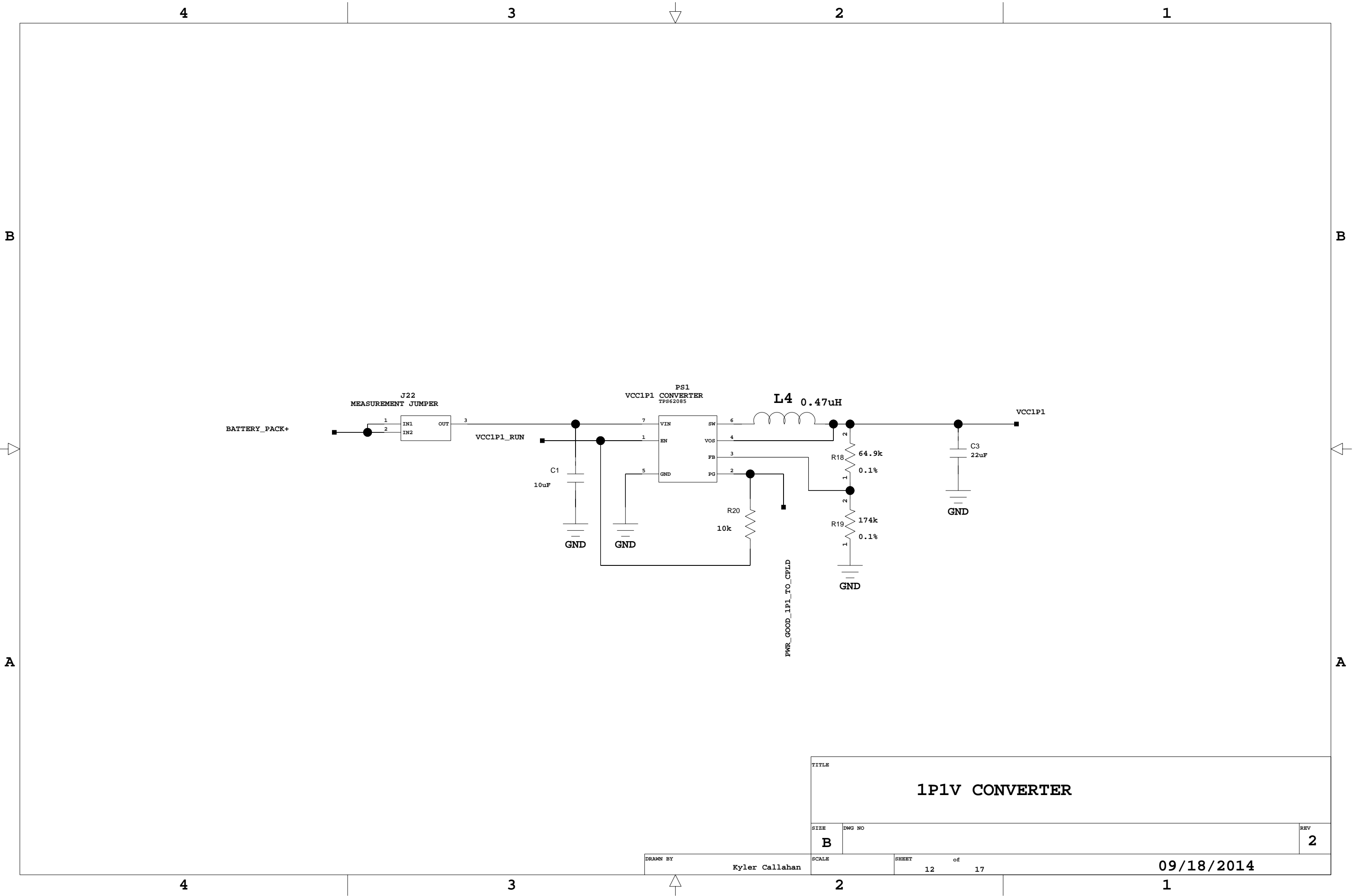
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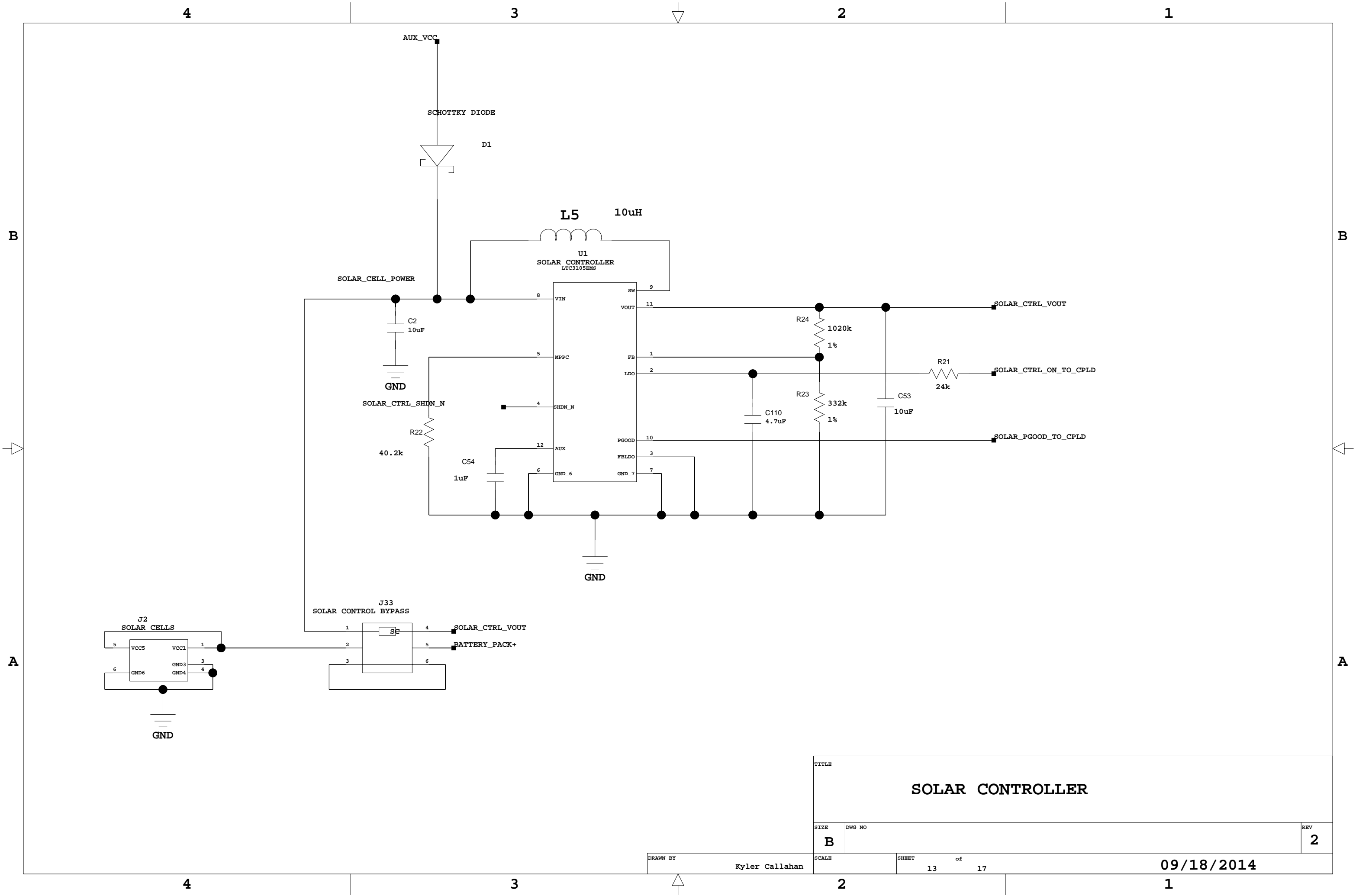


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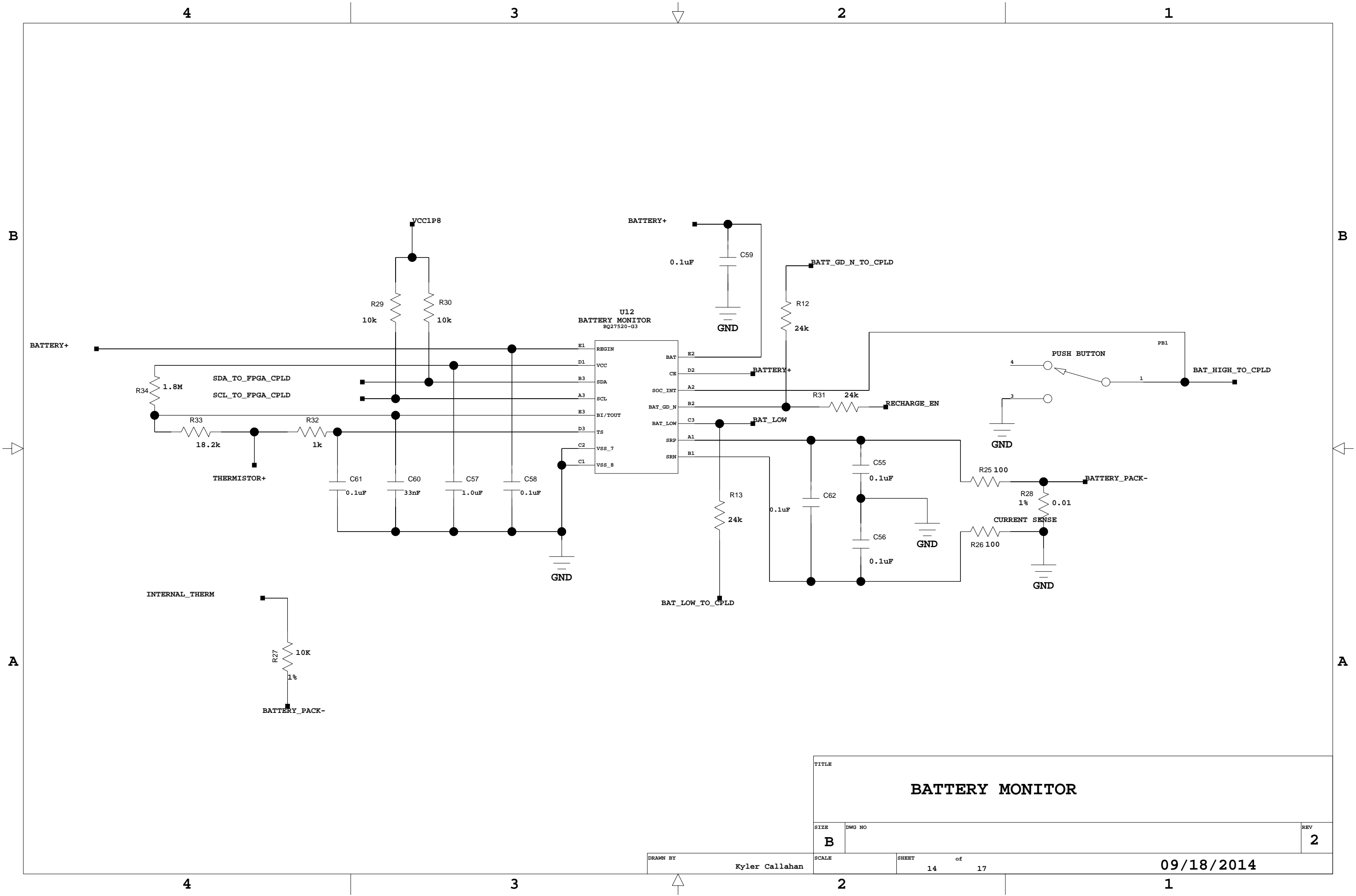
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TITLE			
FPGA I/O			
SIZE	DWG NO		REV
B			2
SCALE	SHEET	of	09/18/2014
	10	17	



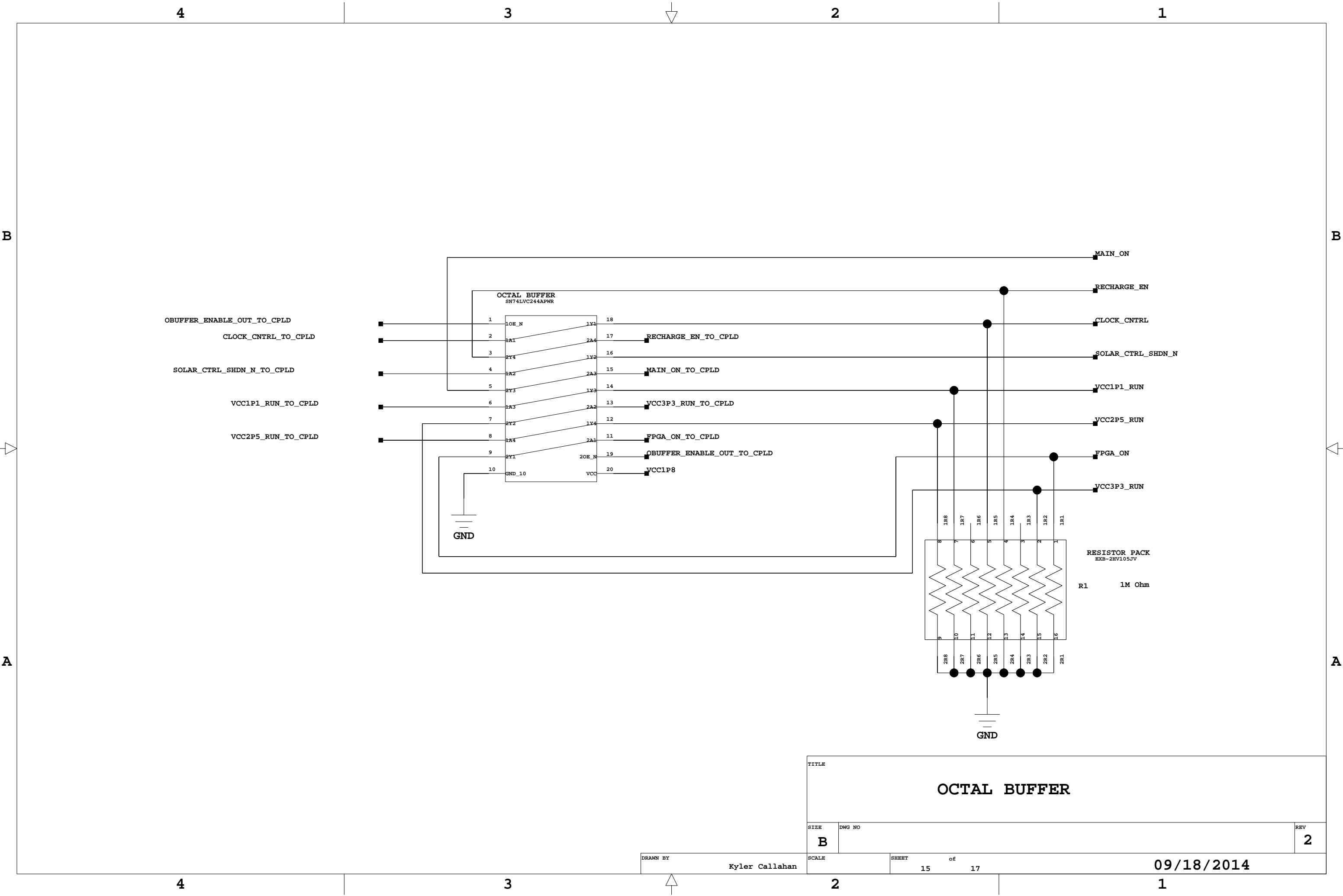


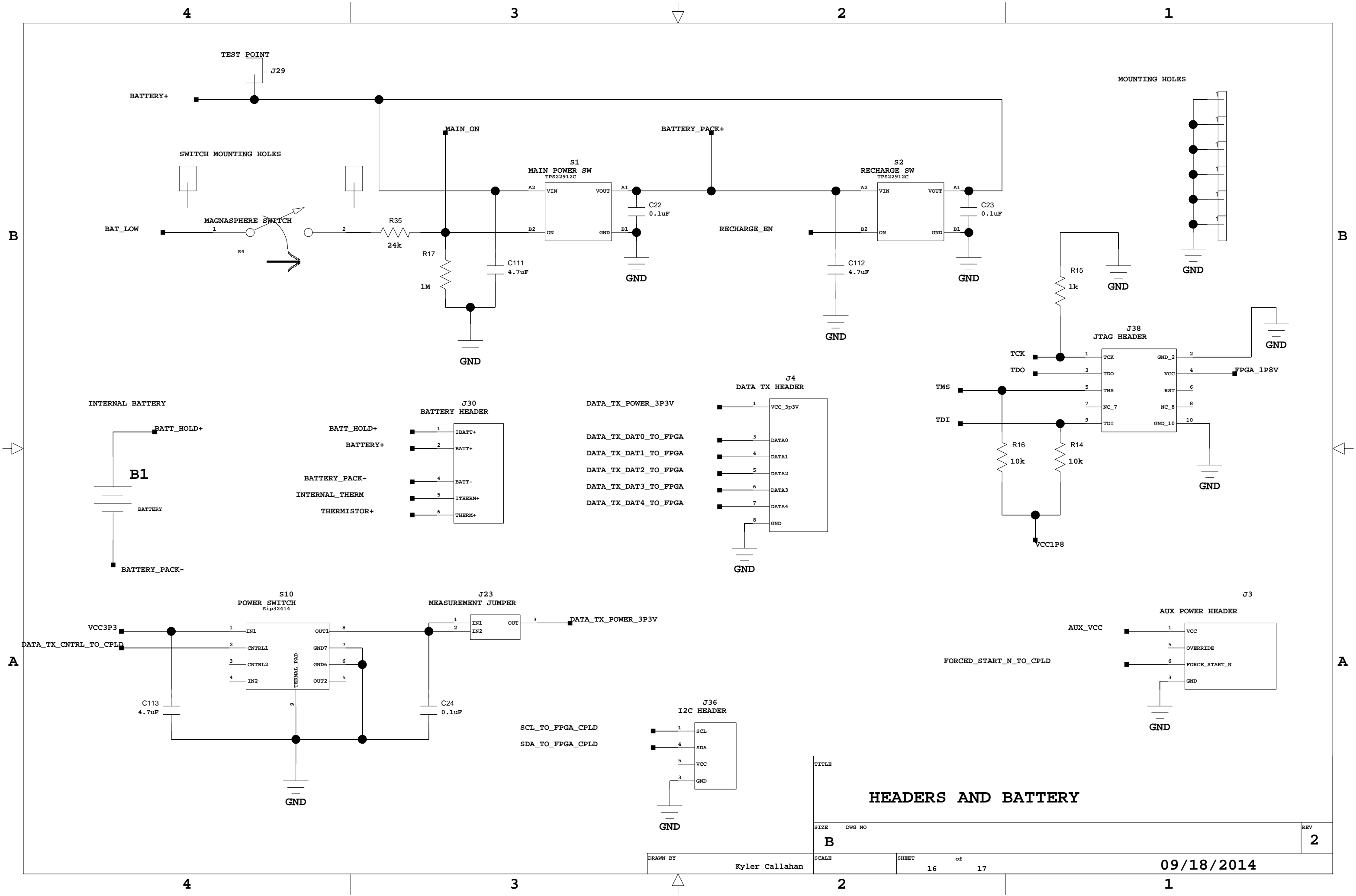
TITLE				
SOLAR CONTROLLER				
SIZE	DWG NO	SHEET		REV
B		13	of 17	2
DRAWN BY		09/18/2014		
Kyler Callahan				



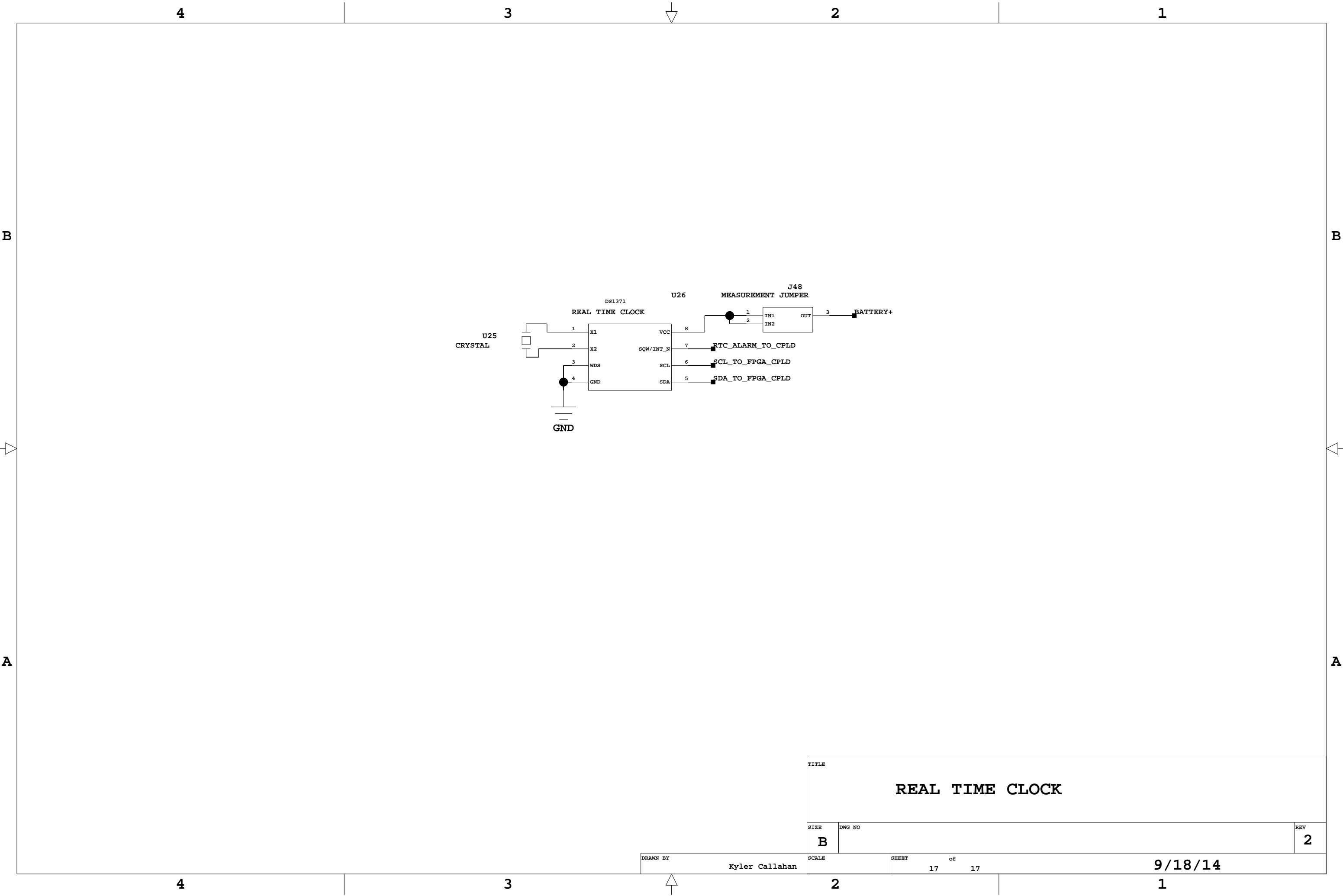
TITLE				
BATTERY MONITOR				
SIZE	DWG NO	REV		
B		2		
SCALE	SHEET	of	DATE	
	14	17	09/18/2014	

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TITLE				
HEADERS AND BATTERY				
SIZE	DWG NO			REV
B				2
SCALE		SHEET	of	
		16	17	09/18/2014



TITLE			
REAL TIME CLOCK			
SIZE	DWG NO	REV	
B		2	
SCALE	SHEET	of	9/18/14
	17	17	

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