

## MAX<sup>®</sup> V Device Family Pin Connection Guidelines

### Preliminary PCG-01012-1.0

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Create a Quartus® II design, enter your device I/O assignments and compile the design. The Quartus II software will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

MAX V Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
<b>Supply and Reference Pins</b>			
VCCINT	Power	Voltage supply pins for the device.	All VCCINT pins must be connected to 1.8 V supply.
VCCIO[1:4](2)	Power	I/O supply voltage pins for banks 1 through 4 respectively. Each VCCIO bank supports a different voltage level with the VCCIO pins providing power for the input and output buffers within that particular I/O bank.	Connect these pins to 1.2 V, 1.5 V, 1.8 V, 2.5 V or 3.3 V supplies, depending on the I/O standard assigned to the I/O bank.
GND(3)	Ground	Device ground pins.	All GND pins should be connected to the board ground plane.
NC	No Connect	No Connect.	Do not connect these pins to any signal. These pins must be left unconnected.
<b>Clock and PLL Pins</b>			
CLK[0:3]	I/O, Clock	Dual-purpose clock pins that connect to the global clock network.	This pin can be used as a regular I/O if it is not used to drive the global clock network.
<b>Configuration/JTAG Pins</b>			
TCK	Input	Dedicated JTAG test clock input pin.	Connect this pin to a 1-kΩ pull-down resistor to GND. To disable the JTAG circuitry connect TCK to GND.
TMS	Input	Dedicated JTAG test mode select input pin.	Connect this pin to a 10-kΩ pull-up resistor to VCCIO1. To disable the JTAG circuitry connect TMS to VCCIO1 via a 1-kΩ resistor.
TDI	Input	Dedicated JTAG test data input pin.	Connect this pin to a 10-kΩ pull-up resistor to VCCIO1. To disable the JTAG circuitry connect TDI to VCCIO1 via a 1-kΩ resistor.
TDO	Output	Dedicated JTAG test data output pin.	If the TDO pin is not used, leave this pin unconnected.
DEV_CLRn	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.	When the dedicated input DEV_CLRn is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground.
DEV_OE	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all output pins are tri-stated; when this pin is driven high, all output pins behave as defined in the design.	When the dedicated input DEV_OE is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground.
<b>Differential I/O Pins</b>			
DIFFIO_[B,L,R,T][##][p,n]	I/O, Output	These are emulated LVDS output channels. It can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with a "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in Quartus II software.

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

**Notes:**

- (1) This pin connection guideline is created based on the MAX V device family.
- (2) VCCIO1 does not support 1.2 V.
- (3) GND pins in the 5M1270Z and 5M2210Z devices consist of GNDIO and GNDINT pins.
- (4) To determine the current requirements for the power supplies, use the MAX V Early Power Estimator.
- (5) Unused I/O pins need to be tied high, tri-stated, or tied low to match your Quartus II design.

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Revision History

Revision	Description of Changes	Date
1.0	Initial release.	12/3/2010

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