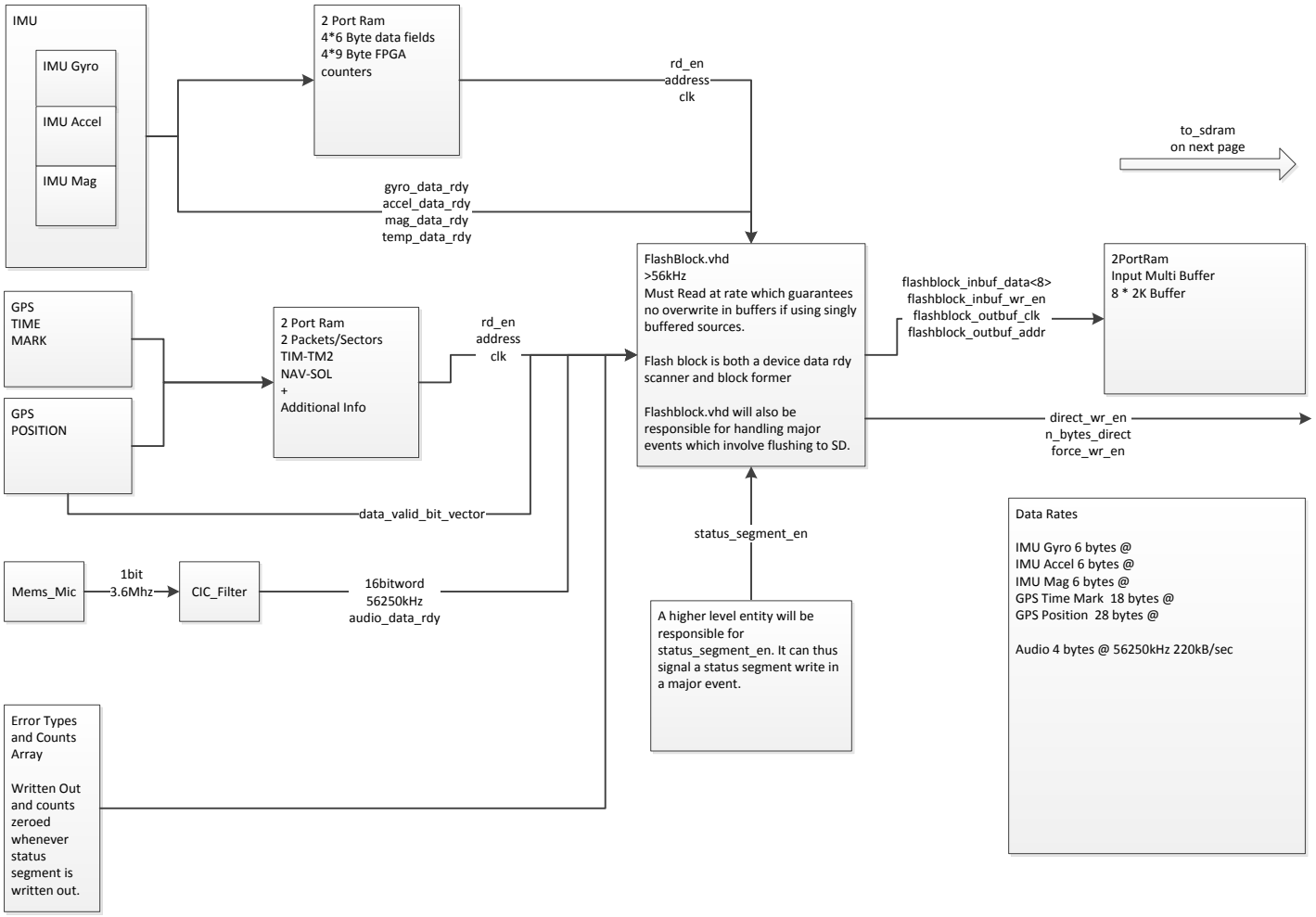
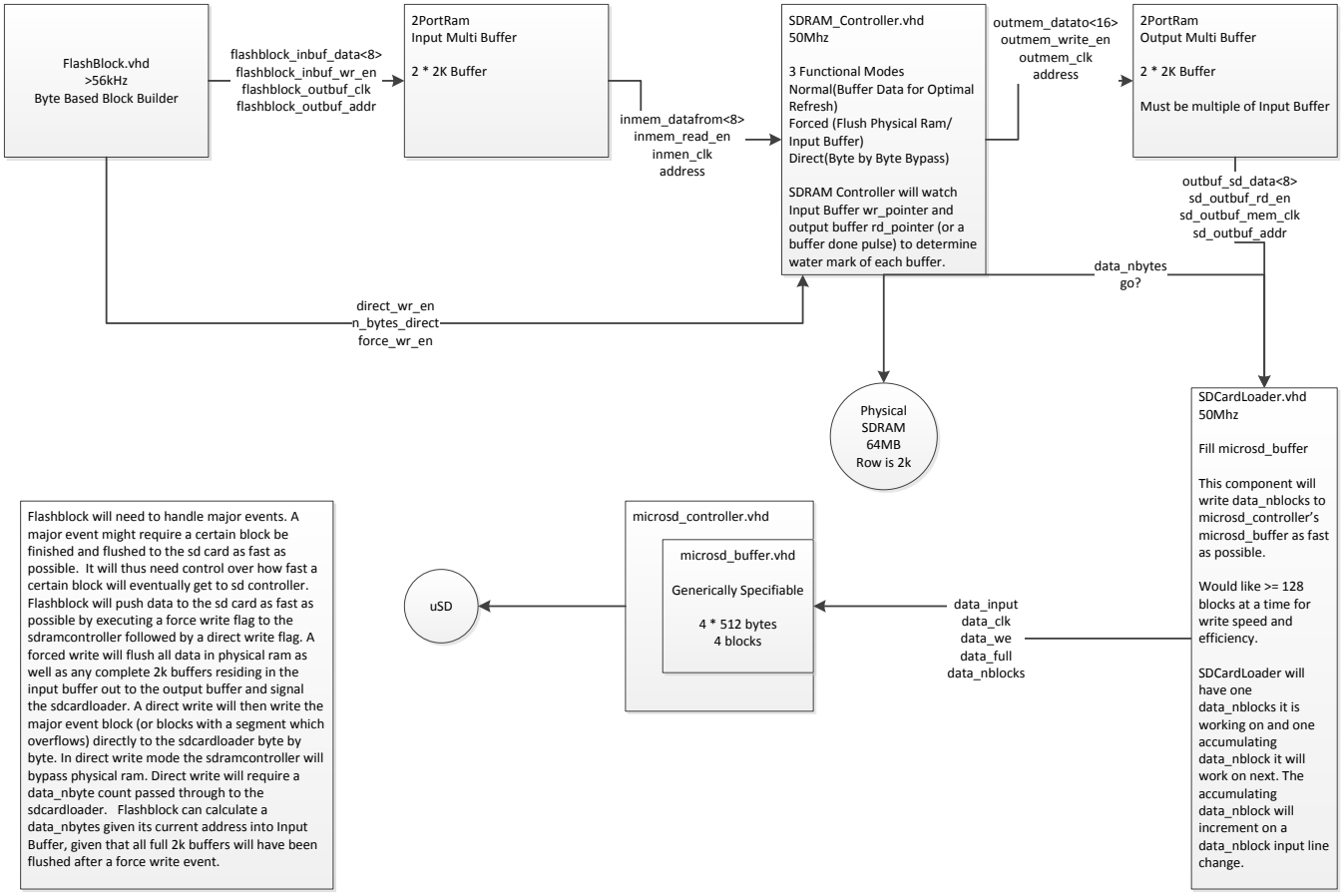
## Data Assembly and Memory Flow






## Buffer Addressing

IMU BUFFER
2 Port Ram
4*6 Byte data fields
4*9 Byte FPGA counters

SIZE : 64 BYTES

Byte Addressing

Byte Address:Data

0-5 Accelerometer Word
6-14 Accelerometer Sample FPGA Time
15-20 Gyroscope Word
21-29 Gyroscope Sample FPGA Time
30-35 Magnetometer Word
36-44 Magnetometer Sample FPGA Time
45-50 Temperature Word
51-59 Temperature Sample FPGA Time

2PortRam
Input Multi Buffer

2 * 2K Buffer
4096 Bytes

Address : std_logic_vector(11 downto 0);

BYTE_ADDR_LEN :natural := 9;
BUFFER_ADDR_LEN :natural := 3

This will allow simply incrementing address and watching high order bit for 2k boundry.

2 Port Ram
2 Packets/Sectors
TIM-TM2
NAV-SOL
+
Additional Info

2PortRam
Output Multi Buffer

2 * 2K Buffer

Must be multiple of Input Buffer

Address : std_logic_vector(11 downto 0);

BYTE_ADDR_LEN :natural := 9;
BUFFER_ADDR_LEN :natural := 3

No buffering for CIC Filter 16 bit word.
Simply a ready pulse 3.6Mhz wide and an associated 16 bit word.