Microsd\_Controller  
Specification

Author: Christopher Casebeer

Christopher.casebee1@msu.montana.edu

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Revision History

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| --- | --- | --- | --- |
| 1.0 | 06/13/2014 | [Casebeer] | Initial Release |

Introduction

*[This section contains the introduction to the core, describing its use and features.]*

Microsd\_controller and its sub entities are a system to write serial amounts of data to a microSDXC card. The controller is written in VHDL for use on an FGPA and has been developed with the Altera toolchain on a Cyclone V development board.

Through use of this component the user can dump blocks of data to the SD card beginning at a desired SD card address. The SD card uses blocks (512 bytes) as the minimum amount of addressable data. Thus the user of the component sends data to the card in 512 byte chunks. The user will notify the card how many blocks (data\_nblocks) the host will send to the SD card. An internal buffer stores a generically specified amount of data for the sd card to write. The component is also capable of notifying the user through a flag and address that a previous block has been received successfully. This could be used for logging purposes.

The component operates in 4 bit mode and at 1.8V signaling levels by default. The 1.8V signaling level required external circuitry detailed later.

The component does not have any utility to function with or operate on a filesystem. The component strictly dumps data onto the attached SD card in a linear fashion from a presented start address. Data presented to the component will show up on the card.

Architecture



Figure 1 microsd\_controller top

Microsd\_controller

This top component instantiates microsd\_controller\_inner. It also tri-states the cmd and data lines depending on the state of write enable signals coming from either sd\_init or sd\_data. This level also handles the sd\_data core control in relation to the data buffer. For example, if the buffer has data ready to be written, this component engages sd\_data to write that data.

Microsd\_controller\_inner

This inner component has two jobs. One is to create the 400k initialization clock through a clock divider. The other is to instantiate the two lower components sd\_data and sd\_init and multiplex cmd and data lines that come out of them.

Sd\_init

This core is responsible for issuing all commands related to SD card initialization. This component is responsible for all commands up through issuing CMD3 to the SD card. The SD card physical specification contains diagrams partitioning what falls into initialization. The sd\_init core also makes decisions on initialization steps based on the desired operating modes. During initialization is when 1.8V signaling switch occurs.

Sd\_crc\_7

This component contains the logic required for generating the crc7 checksum that is associated with all commands issued to the SD card over the command line. The code herein is a vhdl port of Kay Gorontzi’s online crc generator and LGPL code.

Sd\_data

This component is responsible for all writing to the sd card. The core is currently capable of exercising a CMD25 multiblock write to steam continuous 512 byte blocks to the card. The number of blocks in any multiblock stream has been coded to be 128 blocks or less depending on the data\_nblocks top I/O. Other requirements of writing data such as switching into 4 bit mode and tracking data crc16 appends is handled here. The core also contains partial read and erase functionality.

Sd\_crc\_16

All data blocks sent to and received from the card over the data lines are protected by crc16 checksum. This engine has the logic to generate these checksums attached to blocks of data sent to the card. The code herein is a vhdl port of Kay Gorontzi’s online crc generator and LGPL code.

Data\_buffer

This component is a data buffer where data is buffered by the host while the card is busy writing other data in the buffer. The host will buffer data here quicker than the card can write the data. The sd\_data core takes its data from this component. This buffer is expandable in size via top level generic. The Altera 2 port ram is used here. Level marks keep track of available data in the buffer. The number of data\_nblocks that have streamed through the buffer already is also kept track of.

Data\_buffer uses an Altera 2 port ram megafunction. Users of other tools chains should substitute this 2 port ram with one from their own vendor. This is the only Altera specific code in this project.

Operation

*[This section describes the operation of the core. Specific sequences, such as startup sequences, as well as the modes and states of the block should be described.]*

Flow:

* Clock the design with a 400kHz to 50Mhz clock on clk IO
* Set data\_sd\_start\_address and data\_nblocks inputs to appropriate values
* Begin clocking data on data\_input on the rising edge of data\_we
* Halt data\_we and data\_input on data\_full high flag
* Repeat previous steps for another data series upon having sent data\_nblocks and data\_full returning low.

Figure 1 describes the top level abstraction of the design. The user should clock the design with a 400kHz to 50Mhz to get the design into its initialization procedure. The user should then present the card with the number of blocks (512 bytes) to be written,data\_nblocks, and the start address on the card where the blocks will begin to be written,data\_sd\_start\_address.

The user can then clock in data bytes on data\_input on the rising edge of data\_we. Data\_full flag will go high when the internal buffer is full and the component can no longer accept data. The user should stop presenting data immediately and gate the data\_we. Upon receiving the number of blocks data\_nblocks, the component will keep the data\_full line high until all data is flushed from buffer and written to the card. The component relies on the idea that data\_nblocks worth of data will come from the host. The component will then reset the buffer and wait for another set of inputs and first rising edge of data\_we. The component samples data\_sd\_start\_address and data\_nblocks near the first rising edge of data\_we after a previously successful transfer.

Clk should be 400kHz to 50Mhz. This will be the rate at which internal logic is clocked and the rate at which data is transferred to the card. Enable low will gate clk upon completion of writing the current CMD25 stream. Reset will cause the card to reinitialize and wait for another set of data\_input ,data\_nblocks, and data\_sd\_start\_address.

The microSD card uses 6 lines to communicate with the host, in this case an FPGA. The lines are Clock, Command, and Data 0 through 3. The IO are labeled sd\_clk,sd\_cmd and sd\_dat respectively. The microSD card also requires power (3.3V) and ground. The appropriate data, clock, and command lines are tri-stated internally in this component since these lines are bidirectional. The user of this component must take these inout lines and tie them to bidirectional pins at the top of their design. The pins must then be connected to the equivalent pins of the SD card through a bidirectional voltage level translator. This is discussed later.

The component was tested from 400kHz to 50Mhz successfully. An example synopsis design constraint file (.sdc) is included that was used to constrain the timing of the design successfully. Timing constraint is critically important when using this component on an FPGA. In particular is input and output port constraint correctness.

Two test and verification files have been included. A 2048 block (1MB) write and 128x16 blocks write test framework is presented.

The component writes via CMD25 of the SD Card command set. CMD25 is a streaming write command. It is called the multi block write. It was found that write speed and efficiency went up dramatically as the number of blocks streamed after any CMD25 increased. This was tested up to 128 blocks which resulted in the greatest write speed of ~11MB/s. Thus if the user specifies greater than 128 blocks to write to the card, the data will be sent in 128 block sets. The component will decrease the blocks sent in the CMD25 stream if the number of blocks is less than 128. However, this will result in a slower write time.

The component makes use of an internal buffer. The buffer allows temporary storage of the data to be written before it is written to the sd card. The buffer size can be specified. The buffer makes use of Altera specific 2-port ram.

Three generics exist for microsd\_controller. BUFSIZE specifies the size of the internal buffer. It must be a multiple of 512 bytes. HS\_SDR25\_MODE is a single bit which should correspond to the frequency of the input clk. The generic should be set 1 when operating above 25Mhz. This bit changes the initialization process of the card via CMD6, setting the card into a higher speed mode. CLK\_DIVIDE specifies a divide by value used to divide the clk down to ~400kHz. In the case of a 50Mhz clk, a 128 CLK\_DIVIDE is used.

The sd card has several other functional parameters. One of these is the signaling level of the data, cmd and clk lines. The signaling level can be either 1.8V or 3.3V. This component in its default state is set to switch into 1.8V communication. This will require a level translator IC and voltage switches to accomplish. This is necessary as the sd card always begins communication at 3.3V. 1.8V is also required for communication above 50Mhz.

The components used for the 1.8V switch were as follows:

TPS22966 Dual-Channel, Ultra-Low Resistance Load Switch

<http://www.ti.com/lit/ds/symlink/tps22966.pdf>

TXB0106 6-Bit Bidirectional Voltage-Level Translator

<http://www.ti.com/lit/ds/symlink/txb0106.pdf>

The microsd top level component provides 1.8V and 3.3V OnOff output signals. These are for ultimately controlling the Vcca voltage of the level translator. Vcca in this configuration controls the voltage levels between the level translator and sd card. In this implementation, Vcca of the level translator was tied to both outputs of the dual switch This switch was then used to enable either 1.8V or 3.3V to the Vcca port of the level translator, effectively switch from 3.3V signaling to 1.8V signaling to the sd card. The FPGA output pins stayed 3.3V throughout. The following diagram describes the setup used.



Figure 2 Level Translation Setup

The sd card can also communicate with 1 data line or all 4 data lines. By default the 4 bit mode is used by default for increased throughput.

This component was developed on a SanDisk Ultra microSDXC UHS-1 64GB card.

Registers

*[This section specifies all internal registers. It should completely cover the interface between the core and the host as seen from the software view.]*

This design has no addressable registers. Data which is presented to the card will be written to the card. A software or bus interfacing register set is not part of the design.

Clocks

*[This section specifies all the clocks. All clocks, clock domain passes and the clock relations should be described.]*

| **Name** | **Source** | **Rates (MHz)** | | **Description** |
| --- | --- | --- | --- | --- |
| **Max** | **Min** |
| clk | Input | 50 | .4 | Data system and data transmit clock |
| clk\_400k\_signal | Divide on clk | ~.4 | ~.4 | Init system clock |

Table 1: List of clocks

IO Ports

*[This section specifies the core IO ports.]*

| **Port** | **Width** | **Direction** | **Description** |
| --- | --- | --- | --- |
| Clk | 1 | Input | Clock Input |
| Reset\_n | 1 | Input | Reset Input |
| Clock\_enable | 1 | Input | Clock Enable |
| Data\_input | 8 | Input | Byte to be written to sd card |
| Data\_we | 1 | Input | Data\_input write enable |
| data\_sd\_start\_address | 32 | Input | Starting address on sd card for data write |
| data\_nblocks | 32 | Input | Number of blocks(512bytes) to be written and will be presented |
| data\_current\_block\_written | 32 | Output | Address of last block successfully written |
| sd\_block\_written\_flag | 1 | Output | Data\_current\_block\_written is valid |
| sd\_clk | 1 | Output | Sd card clock |
| sd\_cmd | 1 | InOut | Sd card command line |
| sd\_dat | 4 | InOut | Sd card data lines |
| V\_3\_3\_ON\_OFF | 1 | Output | 3.3 V On/Off control to level shifter |
| V\_1\_8\_ON\_OFF | 1 | Output | 1.8 V On/Off control to level shifter |
| init\_start | 1 | Input | Debug: Init on button press |
| user\_led\_n\_out | 4 | Output | Debug: FSM states to leds |

Table 2: List of IO ports

Verification

[This section may be added to outline different specifications.]

The verification process uses a top level vhdl file to exercise microsd\_controller. Two verification vhdl files are included with the design. One file writes 2048 blocks to the card in one large data\_nblock. The other writes 128\*16 nblocks through repeated interaction with microsd\_controller. The test uses a 512 byte ram initialized with random hex values. The mif file used to initialize this ram was created with Matlab. This Matlab script generates both a mif file for use with Quartus and a bin file for use with the unix compare function for verification. The top level test files write a total of 1MB of data to the SD card. The bin file for use with cmp is also 1MB in size.

The data written to the card was checked by using the dd command inside of a virtual machine running Debian linux. The command “dd if=/dev/sdb of=/home/chrisc/desktop/sd\_test count= 2048”, was used to dump the first 2048 blocks for examination. The command “cmp sd\_test 512bytecount\_rand.bin” returns no result if the two files are the same and the write was successful.

To Do

The CMD25 multiblock write pathway is the major focus of the development so far. The CMD25 4 bit pathway is the only portion of the design currently utilized. However a framework and partial design exists for reading from the card and erasing the card. The single block read, single block write and erase have all been implemented and tested working previously. The FSM paths and associated processes for these functions need maintenance to bring them back to working order. Multiblock read however has never been implemented and would need more work than the others.

To Do:

* Erase
* Single Block and Multiblock Read
* Single Block Write

References

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SandDisk Corporation. *SanDisk SD Card Product Manual Version 2.2 Document No. 80-13-00169 November 2004*

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