Reese Kuper

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Objective: Summer of 2022 internship in computer architecture, digital hardware design, or hardware verification

Education

Masters: University of Illinois at Urbana-Champaign **Starts Fall 2021**
Department of Electrical and Computer Engineering
Focus: Computer Architecture
Advisor: Nam Sung Kim

Bachelors: University of Wisconsin-Madison (3.88/4.00) **2017 - Present**
Degrees in Computer Engineering and Computer Science

Related College Coursework

- Parallel Computer Architecture
- Parallel and Throughput-Optimized Programming
- Artificial Intelligence
- Circuits and Circuits Analysis
- Computer Architecture
- Operating Systems
- Circuits and Circuits Analysis
- Microprocessor Systems
- Digital System Design & Synthesis
- Algorithms
- Microprocessor Systems

Skills

Programming Languages: C/C++, Python
Hardware Description Languages: System Verilog
Software: ModelSim, Icarus, Quartus, Vim, Git
Operating Systems: Linux, MacOS, Windows
Databases: MySQL

Work Experience

Arm – Austin, TX **Summer 2020**
Hardware Engineering Internship – Systems Interconnect Verification Team

- Developed internal Python tool to analyze the use of all plusargs within the UVM testbenches
- Fixed UVM register definition auto-generation for more flexible RAL models
- Programmed module for modeling transactions between a master device to interconnect return nodes in SystemC
- Formally verified round robin and LSB priority arbiters using System Verilog assertions

Qualcomm – San Diego, CA **Summer 2019**
Software Engineering Internship – Linux Kernel Memory Team

- Improved kernel ION allocation memory speeds by ~10%
- Analyzed the efficiency of IOVA's use of caching and compared it with MMAP's gap searching RBTree
- Created internal Python tool for parsing Linux RAM dump binaries
- Worked towards shifting mmap allocations to use the mempool API

Projects

Research Projects **2020 - 2021**
Research-based projects from either graduate coursework or in a research group

- [Current work] GPU architecture research in Professor Matthew Sinclair's HAL group
- Predicted performance for coherence decoupled systems (directory-based MESI protocol) using a 2-level predictor for *improved* accuracy, and estimated rollback costs for *complete* accuracy using the gem5 architecture simulator

Computer Science and Engineering Projects **2018 - 2020**
Projects created through computer science and engineering courses

- Self-balancing Segway written in Verilog for a DE0-Nano FPGA board
- Synthesized 5-stage pipelined CPU with separate, 2-way set associative Instruction and Data Caches (using an LRU replacement policy) written in Verilog

Hackathons (HackNYU and HackMobile) **2018 - 2019**
48- and 24-hour coding project competitions

- Developed a mobile iOS application for animal photo recognition using Microsoft's Custom Vision API
- Wrote an Android app that sends dense packets of information to proactively track lost people (connection-free)