VERISILICON
Micro LED Chip Specification

Rev 0.8

2020/11/20

VeriSilicon Microelectronics (Shanghai) Co., Ltd.

Checked by: _____

Approved by: _____

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VeriSilicon Microelectronics (Shanghai) Co., Ltd.

20A, No.560, Songtao Road, Zhangjiang Center, Zhangjiang Hi-Tech Park,
Pudong New Area, Shanghai 201203, P. R. China

Tel : +86-21-5131-1118

Fax : +86-21-5131-1119

Web : http://www.verisilicon.com

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0.8	Updated the pin name and some information	2020-11-20

Contents

1. General Description

1.1. Overview

This is a driver chip designed specifically for the application of LED full-color display panels. The driver chip is partitioned to 24*24 driving blocks. Each driving block drives 8*8 pixels. It supports 192*192 LED pixels totally.

It is a low-power LED driver. The maximum output current is up to 400uA. The maximum LED driver current can be adjusted by the external resistors with different resistances. Each driving block also has a 6 bit current gain control to adjust its driver current.

It has a built-in 12-bit gray scale control pulse width modulation function for each driving block. It makes each output shows a 12-bit (4096 gray scale) color change. In addition, It can be used to compensate gamma correction or LED deviation through 12-bit image data Information to adjust the brightness of each LED.

It integrates four LVDS receivers. Each LVDS receive is designed to support Single Link transmission and supports up to 805Mbps data rate.

It has two driver modes, Serial Mode and Parallel Mode. The maximum frame refresh rate reaches 200Kfps.

1.2. Main Features

- 6-bit programmable output current gain
- 12-bit gray color depth PWM control
- 3.3V supply voltage
- Data clock frequency:250Mhz/800Mhz
- Die size: 4725um*10422um (include seal ring, after shrink)
- Minimum data update frequency:60kfps
- Maximum data update frequency:200kfps
- Constant output current range:1~400uA
- Drive mode: sparse drive by block, up to drive 8 pixel point at the same time in one block.
- Drive 64 pixel points per block, 24*24 blocks totally.
- Drive 192*192 pixel points totally
- Pixel pitch:24.3um
- Internal PLL
- Internal temperature detector(TSHUT)
- Three working mode: Serial mode, Parallel mode, Narrow parallel mode

1.3. Block Diagram

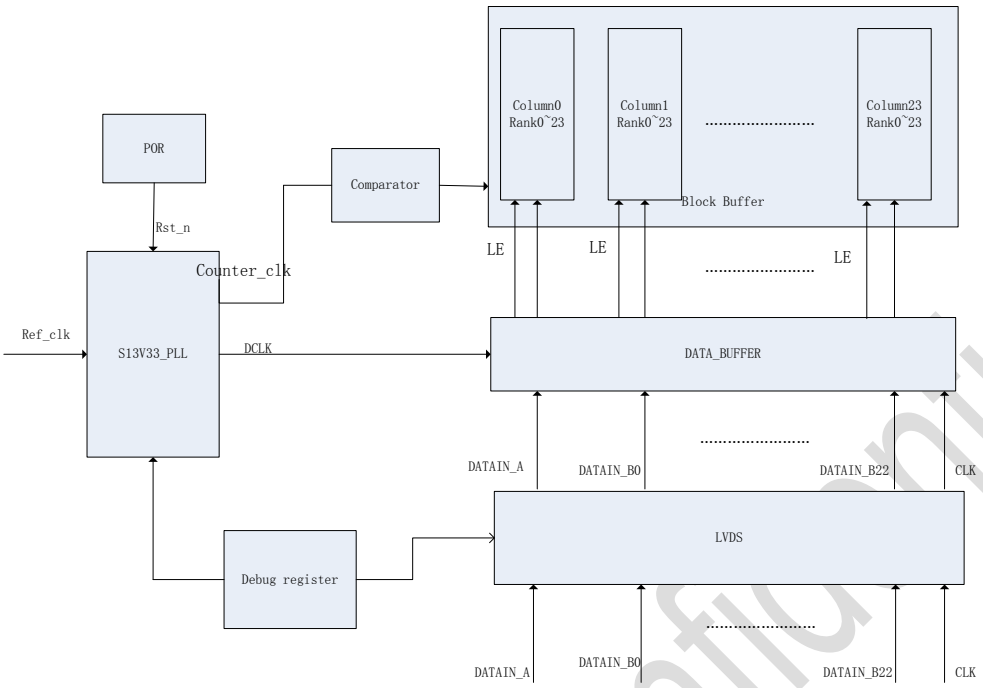


Fig. 1 Micro LED Block Diagram

2. Pin Description

Table. 1 Pin Description

PIN NAME	PIN TYPE	DESCRIPTION
Digital Part		
DVDD12	PV	Digital power supply. 1.2V Typ.
DGND	PG	Digital Power ground.
RST_N	Digital input	System Reset.
CRC_ENABLE	Digital input	1:crc check enable; 0:crc check disable.(Default:1'b0)
CX	Digital input	0:Serial mode,1:Parallel mode.(Default:1'b1)
ERROR	Digital output	CRC check error output
LVDS_NARROW	Digital input	For LVDS to select narrow mode. (Default:1'b0)
PLL_CONFIG[1:0]	Digital input	PLL Configure input pin.(Default: 2'b0)
TEST_MODE	Digital input	0: Normal mode; 1: Test mode.(Default: 1'b0)
LVDS Receiver Part		
DATAIN_A_P	Analog input	Serial-data positive input to the shift buffer for column0 in serial mode and parallel mode
DATAIN_A_N	Analog input	Serial-data negative input to the shift buffer for column0 in serial mode and parallel mode
DATAIN_B0_P	Analog input	Serial-data positive input to the shift buffer for

~ DATAIN_B22_P		column1~23 in parallel mode
DATAIN_B0_N ~ DATAIN_B22_N	Analog input	Serial-data negative input to the shift buffer for column1~23 in parallel mode
DATAIN_CLK0_P ~ DATAIN_CLK3_P	Analog input	Positive CLK input for DATAIN_A and DATAIN_Bx
DATAIN_CLK0_N ~ DATAIN_CLK3_N	Analog input	Negative CLK input for DATAIN_A and DATAIN_Bx
VCCRX0~3	PV	3.3V Power for LVDS Receiver
GNDRX0~3	PG	Ground for LVDS Receiver
VCCBUF0~3	PV	3.3V Power for LVDS Buffer and DFF
GNDBUF0~3	PG	Ground for LVDS Buffer and DFF
LED Driver Part		
DVDD33	PV	Digital power supply. 3.3V Typ.
AVDD33	PV	Analog Power supply. 3.3V Typ.
AGND33	PG	Analog Ground.
LED_PV	PV	Power Supply for LED driver output. 3.3V Typ.
LED_PG		Power Ground for LED. -3V Typ.
VREF	Analog Input	Voltage reference input pin. An external 1.2V voltage reference should be Connected to this pin.
VNW	Analog output	Analog output for internal voltage bias. An external 0.1uF decoupling cap should be connected.
R_EXT	Analog input	An external resistor is connected between R_EXT and analog ground to adjust full-scale current of DAC.
LOUT_XnYm<63:0>	Analog output	LED current output for each LED pixel. Totally 36864 LED pixel anode outputs. XnYm denotes row/column address of driver block. Valid numbers of n/m are 0 to 23.
PLL Part		
REF_CLK	Digital input	Reference CLK input. This input (4~200MHz) is used as the reference source for PLL.
AVDD12	PV	PLL Analog Power Supply. 1.2V Typ.
AGND12	PG	PLL Analog Ground.
AVDD2	PV	Power supply for PLL Internal Digital block. 1.2V Typ.
AGND2	PG	Power supply for PLL Internal Digital block.

3. Main Function Description

3.1. Column Unit Block

3.1.1. Overview

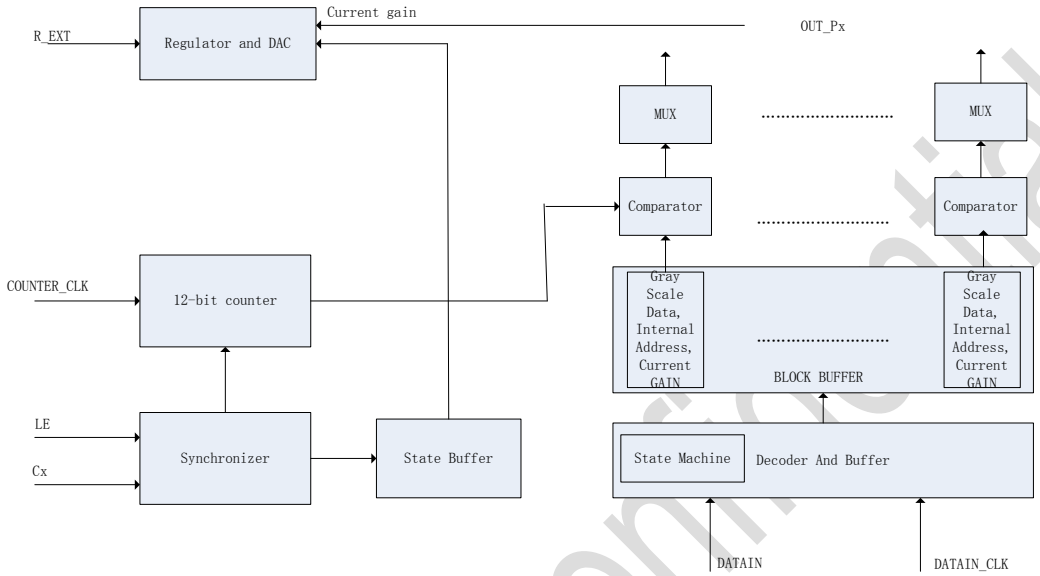


Fig. 2 Column Unit Block Diagram

3.1.2. Data Format

The frame consists of frame sync header, block num, block address, reserve bit, start bit, constant current bits, pixel num, internal address, and grayscale data. It contains m(m<=103) blocks and each block has n(n<=8) pixel points. The frame has 4096 bits at most.

Table. 2 Frame Data Format

Frame sync	Block num	Reserve(sync control)	Block Address	Data hold Control bit	constant current bits	pixel num	Internal address	gray scale data	CRC Data (optional)
35:0	43:36	44	53+m*18n:45+m*18n	54+m*18n	60+m*18n:55+m*18n	63+m*18n:61+m*18n	63+m*(5+18n):63+m*(18n)	63+m*(17+18n):63+m*(6+18n)	15+64+m*18n:64+m*18n

(m>1,8>n>=0)

Sync header:

[0:3]	[4:31]	[32:35]
1010	0	1011

Data hold control bit:
If data hold control bit was 1, the whole frame should be saved in block buffer. The frame be saved will be cleared when a new frame's data hold bit is 0 or the store data in block buffer will be cleared when a new frame's data have same block address. Block address:
The block address [9:5] is used for column index and block address [4:0] is used for row index.

Reserved bit:
The reserved bit is used as sync control bit in narrow parallel mode. If it is 1'b1,the chip will send data after one frame was received. If it is 1'b0, the chip will send data after four frames was received.

Block num:
The block num should not be zero.

3.1.3. Control Command

Table. Control Command

Command Name	The action after receiving a command
Data Latch	Serial data are transferred to the buffers
FLUSH	The data in buffer will be send out
Clear	Clear all buffer

Data latch:
Please see table 2.
FLUSH command:

Frame sync header	Block num	Clear bit	CRC Data (optional)
35:0	43:36	44	60:45

The block num should be 0 and the clear bit should be 0.
CLEAR command:

Frame sync header	Block num	Clear bit	CRC Data (optional)
35:0	43:36	44	60:45

The block num should be 0 and the clear bit should be 1.

3.1.4. Data Latch State Machine

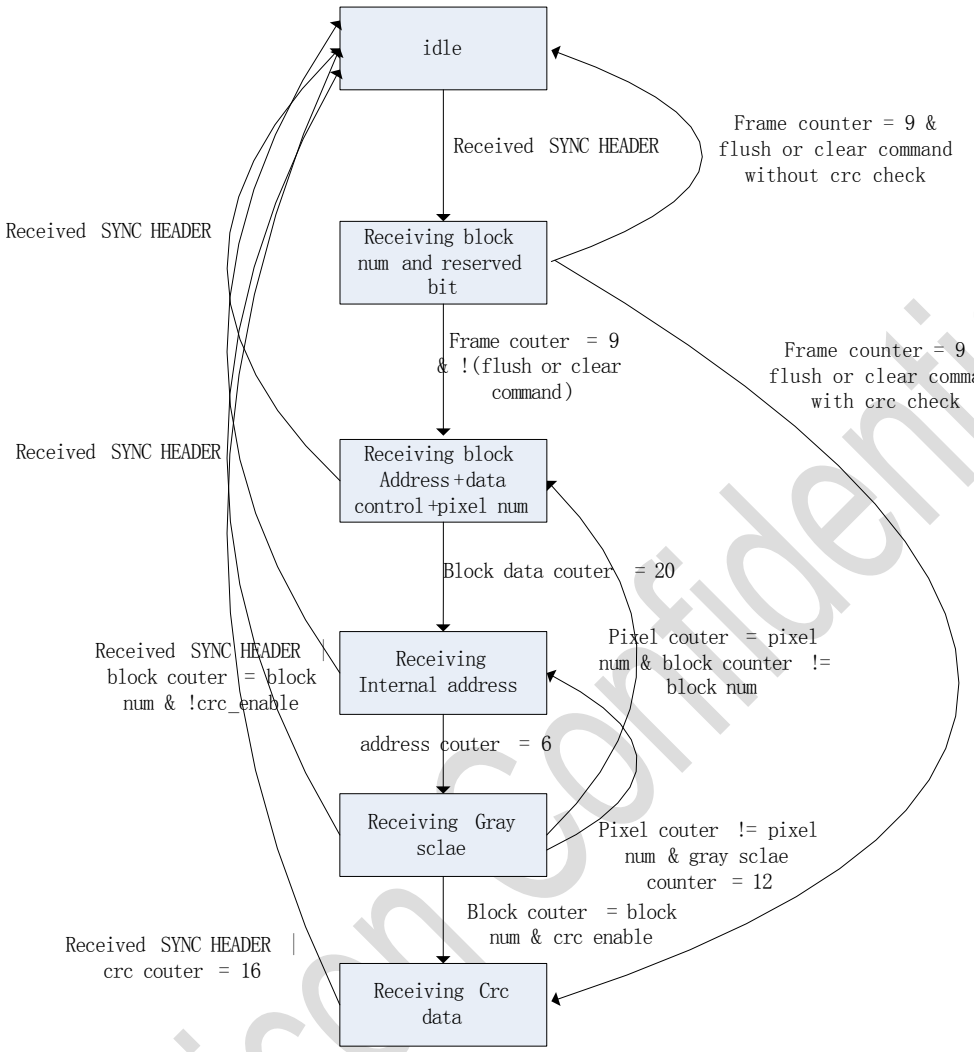


Fig. 3 Data Receiving State Machine

3.1.5. Error Check

3.1.5.1. CRC Check

If CRC_ENABLE is 1, the CHIP should perform CRC16 checking. If a error occurs, the CHIP should set CRC_ERROR bit in register and set the error pin to 1.The whole fame should be discarded.The CRC_ERROR bit will be cleared when the CRC16 checking in next frame is right.

3.2. Configuration Register

3.2.1. Definition of Configuration Register

Table. 3 PLL Control Register Address:4'b0001

bit	Attribute	Definition	Default Value	Function
18	RW	PLL_PD	Normal:1'b0 Test:1;b0	
17	RW	PLL_RESETN	Normal:1'b1 Test:1;b1	
16	RW	PLL_BYPASS	Normal:1'b1 Test:1;b1	
15:10	RW	PLL_DM	6'h0	Normal: 7 倍频： 6'b000011 7/4 倍频：6'b000011 40 倍频： 6'b0 Test:6'b0
9:3	RW	PLL_DN	7'h1	Normal: 7 倍频： 7'b0011011 7/4 倍频：7'b0011011 40 倍频： 7'b0100111 Test:7'b0
2:0	RW	PLL_DP	3'h1	Normal: 7 倍频： 3'b000 7/4 倍频：3'b011 40 倍频： 3'b000 Test:3'b0

Table. 4 LVDS 0 Control Register1 Address:4'b0011

bit	Attribute	Definition	Default Value	Function
31	RW	RXEN0	Normal:1'b1 Test:1'b1	
30	RW	RXEN15	Normal:1'b1 **Test:1'b1**	
29	RW	LVDSINEN	Normal:1'b1 **Test:1'b0**	
28	RW	TESTEN	Normal:1'b0 **Test:1'b1**	
27:25	RW	CH0_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
24:22	RW	CH1_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
21:19	RW	CH2_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
18:16	RW	CH3_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	

15:13	RW	CH4_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
12:10	RW	CH5_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
9:7	RW	CLK_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
6	RW	IUP	Normal:1'b0 **Test:1'b0**	
5	RW	IDN	Normal:1'b0 **Test:1'b0**	
4	RW	ISW	Normal:1'b0 **Test:1'b0**	
3:2	RW	CM_AMPL[1:0]	Normal:2'b0 **Test:2'b11**	
1:0	RW	DIFF_AMPL[1:0]	Normal:2'b0 Test:2'b11	

Table. 5 LVDS0 Control Register2 Address:4'b0100

bit	Attribute	Definition	Default Value	Function
18	RW	ERR_INJECT	Normal:1'b0 **Test:1'b0**	
17:16	RW	PATCFG[1:0]	Normal:2'b0 **Test:2'b0**	
15:2	RW	PATUDF[13:0]	Normal:14'b0 **Test:14'b0**	
1	RW	PATGENEN	Normal:1'b0 **Test:1'b1**	
0	RW	PATCHKEN	Normal:1'b0 Test:1'b1	

Table. 6 LVDS1 Control Register1 Address:4'b0101

bit	Attribute	Definition	Default Value	Function
31	RW	RXEN0	Normal:1'b1 Test:1'b1	
30	RW	RXEN15	Normal:1'b1 **Test:1'b1**	
29	RW	LVDSINEN	Normal:1'b1 **Test:1'b0**	
28	RW	TESTEN	Normal:1'b0 **Test:1'b1**	
27:25	RW	CH0_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	

24:22	RW	CH1_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
21:19	RW	CH2_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
18:16	RW	CH3_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
15:13	RW	CH4_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
12:10	RW	CH5_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
9:7	RW	CLK_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
6	RW	IUP	Normal:1'b0 **Test:1'b0**	
5	RW	IDN	Normal:1'b0 **Test:1'b0**	
4	RW	ISW	Normal:1'b0 **Test:1'b0**	
3:2	RW	CM_AMPL[1:0]	Normal:2'b0 **Test:2'b11**	
1:0	RW	DIFF_AMPL[1:0]	Normal:2'b0 Test:2'b11	

Table. 7 LVDS1 Control Register2 Address:4'b0111

bit	Attribute	Definition	Default Value	Function
18	RW	ERR_INJECT	Normal:1'b0 **Test:1'b0**	
17:16	RW	PATCFG[1:0]	Normal:2'b0 **Test:2'b0**	
15:2	RW	PATUDF[13:0]	Normal:14'b0 **Test:14'b0**	
1	RW	PATGENEN	Normal:1'b0 **Test:1'b1**	
0	RW	PATCHKEN	Normal:1'b0 Test:1'b1	

Table. 8 LVDS2 Control Register1 Address:4'b1000

bit	Attribute	Definition	Default Value	Function
31	RW	RXEN0	Normal:1'b1 Test:1'b1	
30	RW	RXEN15	Normal:1'b1 **Test:1'b1**	

29	RW	LVDSINEN	Normal:1'b1 **Test:1'b0**	
28	RW	TESTEN	Normal:1'b0 **Test:1'b1**	
27:25	RW	CH0_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
24:22	RW	CH1_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
21:19	RW	CH2_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
18:16	RW	CH3_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
15:13	RW	CH4_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
12:10	RW	CH5_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
9:7	RW	CLK_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
6	RW	IUP	Normal:1'b0 **Test:1'b0**	
5	RW	IDN	Normal:1'b0 **Test:1'b0**	
4	RW	ISW	Normal:1'b0 **Test:1'b0**	
3:2	RW	CM_AMPL[1:0]	Normal:2'b0 **Test:2'b11**	
1:0	RW	DIFF_AMPL[1:0]	Normal:2'b0 Test:2'b11	

Table. 9 LVDS2 Control Register2 Address:4'b1001

bit	Attribute	Definition	Default Value	Function
18	RW	ERR_INJECT	Normal:1'b0 **Test:1'b0**	
17:16	RW	PATCFG[1:0]	Normal:2'b0 **Test:2'b0**	
15:2	RW	PATUDF[13:0]	Normal:14'b0 **Test:14'b0**	
1	RW	PATGENEN	Normal:1'b0 **Test:1'b1**	
0	RW	PATCHKEN	Normal:1'b0 Test:1'b1	

Table 1LVDS3 control register1 Address:4'b1010

bit	Attribute	Definition	Default Value	Function
31	RW	RXEN0	Normal:1'b1 Test:1'b1	
30	RW	RXEN15	Normal:1'b1 **Test:1'b1**	
29	RW	LVDSINEN	Normal:1'b1 **Test:1'b0**	
28	RW	TESTEN	Normal:1'b0 **Test:1'b1**	
27:25	RW	CH0_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
24:22	RW	CH1_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
21:19	RW	CH2_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
18:16	RW	CH3_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
15:13	RW	CH4_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
12:10	RW	CH5_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
9:7	RW	CLK_DLYCFG[2:0]	Normal:3'b0 **Test:3'b0**	
6	RW	IUP	Normal:1'b0 **Test:1'b0**	
5	RW	IDN	Normal:1'b0 **Test:1'b0**	
4	RW	ISW	Normal:1'b0 **Test:1'b0**	
3:2	RW	CM_AMPL[1:0]	Normal:2'b0 **Test:2'b11**	
1:0	RW	DIFF_AMPL[1:0]	Normal:2'b0 Test:2'b11	

Table. 10 LVDS3&TEST Control Register2 Address:4'b1011

bit	Attribute	Definition	Default Value	Function
23:22	RW	TEST_MODE	2'b0	
21	RW	CRC_ENABLE	1'b1	
20	RW	CX	1'b1	
19	RW	LVDS_NARROW	1'b0	
18	RW	ERR_INJECT	Normal:1'b0	

			Test:1'b0	
17:16	RW	PATCFG[1:0]	Normal:2'b0 **Test:2'b0**	
15:2	RW	PATUDF[13:0]	Normal:14'b0 **Test:14'b0**	
1	RW	PATGENEN	Normal:1'b0 **Test:1'b1**	
0	RW	PATCHKEN	Normal:1'b0 Test:1'b1	

Table. 11 Chip Status1 Register Address:4'b1100

bit	Attribute	Definition	Default Value	Function
29	RO	CRC_ERROR	**1'b0**	Crc check error status
28	RO	FRAME_ERR	**1'b0**	Sync header errors status
27	RO	LVDS1_PATLOCK0		
26	RO	LVDS1_PATLOCK1		
25	RO	LVDS1_PATLOCK2		
24	RO	LVDS1_PATLOCK3		
23	RO	LVDS1_PATLOCK4		
22	RO	LVDS1_PATLOCK5		
21:14	RO	LVDS1_ERROR_COUNT[7:0]		
13	RO	LVDS0_PATLOCK0		
12	RO	LVDS0_PATLOCK1		
11	RO	LVDS0_PATLOCK2		
10	RO	LVDS0_PATLOCK3		
9	RO	LVDS0_PATLOCK4		
8	RO	LVDS0_PATLOCK5		
7:0	RO	LVDS0_ERROR_COUNT[7:0]		

Table. 12 Chip Status2 Register Address:4'b1101

bit	Attribute	Definition	Default Value	Function
27	RO	LVDS3_PATLOCK0		
26	RO	LVDS3_PATLOCK1		
25	RO	LVDS3_PATLOCK2		
24	RO	LVDS3_PATLOCK3		
23	RO	LVDS3_PATLOCK4		
22	RO	LVDS3_PATLOCK5		
21:14	RO	LVDS3_ERROR_COUNT[7:0]		
13	RO	LVDS2_PATLOCK0		
12	RO	LVDS2_PATLOCK1		

11	RO	LVDS2_PATLOCK2		
10	RO	LVDS2_PATLOCK3		
9	RO	LVDS2_PATLOCK4		
8	RO	LVDS2_PATLOCK5		
7:0	RO	LVDS2_ERROR_COUNT[7:0]		

3.3. Working Mode

3.3.1. Serial Mode

If the CX is 0, the CHIP should run at serial mode. In the serial mode, the data come from the DATAIN_A, and the data is sent into the chip serially. The data from DATAIN_A will be sent to column 0~23.After the whole frame was saved, the CHIP will sent the pixel's data to corresponding block buffer according to the block address. The CHIP will send block buffer's data to the block when it received next sync header. In this mode, the LVDS1~3 and the lane1~5 will be disabled.

3.3.2. Parallel Mode

If the CX is 1, the CHIP should run at parallel mode. In the parallel mode, the data come from the DATAIN_A and DATAIN_B0~22, the data is sent into the chip serially. The data from DATAIN_A will be sent to column 0 and the data from DATAIN_B0~22 will be sent to column 1~23. After the whole frame was saved, the CHIP will send the pixel's data to corresponding block buffer according to the block address. The CHIP will send all block buffers' data to the block when it received next sync header from DATAIN_A.

3.3.3. Narrow Mode

If the LVDS_NARROW was 1, the CHIP should run at the narrow mode. In this mode, the LVDS model is running in lower bandwidth. The data come from the DATAIN_A and DATAIN_B0~4. If the sync control bit is 1, the chip will send data after one frame was received. If it is 1'b0, the chip will send data after four frames was received. The CHIP will send the pixel's data to corresponding lead driver according to the block address. By the way, the counter_clk is different with dclk in this mode. In this mode, the LVDS1~3 will be disabled.

3.4. PIN MUX

Some digital pins have different usage in test mode and normal model.

Table. 13 Pin MUX

Normal Mode	Test Mode0	Test Mode1	Test Mode2
CRC_ENABLE	JTG_TCK	JTG_TCK	JTG_TCK
CX	JTAG_TDI	JTAG_TDI	JTAG_TDI
LVDS_NARROW	JTAG_TMS	JTAG_TMS	JTAG_TMS
ERROR	JTAG_TDO	JTAG_TDO	JTAG_TDO

PLL_CONFIG[1]	PLL_CLK0	TE	TD_OV
PLL_CONFIG[0]	PLL_CLK	TOUT	COUT

3.5. PLL

The Chip has a programmable Analog PLL. It is suitable for high speed clock generation. The high speed VCO of this PLL can run up to 1000MHz.

3.5.1. Features

- Supply voltage: 1.4V~1.5V~1.6V, 3V~3.3V~3.6V
- Current: ~8mA
- Operating junction temperature: - 40°C ~ +25°C ~ +125°C
- Two outputs:
  - PLL_CLKO: standard output from the output divider
  - PLL_CLK: output from VCO directly

3.5.2. Electrical Specifications

Table. 14 PLL Electrical Characteristics

Characteristics	Min	Typ	Max	Unit	Conditions
Analog power supply(PLL_AV33)	3.0	3.3	3.6	V	
Digital power supply(PLL_DV15)	1.4	1.5	1.6	V	
Digital power supply(PLL_AVDD2)	1.4	1.5	1.6	V	
Temperature range	-40	25	125	℃	
Lock time			0.2	ms	
Supply current (Locked Mode)			8	mA	
Leakage current (PWDN Mode)			0.1	uA	No input clock and at room temperature (simulation result)
			1	uA	No input clock, FF corner, 125℃, 1.6v power (simulation result)
VCO frequency range	300		1000	MHz	
PLL_REFIN					
PLL_REFIN frequency range	10		200	MHz	Programmable
Duty cycle requirement	20		80	%	
Period jitter(p-p)			100	ps	It is recommended for better output clock jitter.
PLL_CLK, PLL_CLKO					
PLL_CLK frequency range	300		1000	MHz	Programmable

PLL_CLKO frequency range	37.5		1000	MHz	Programmable
Duty cycle	40		60	%	
Period jitter(rms)		5		ps	Application dependent and PLL_REFIN is clean.
PLL_BAKD2O					
PLL_BAKD2O frequency range	2		40	MHz	
Duty cycle of PLL_BAKD2O	45		55	%	

3.5.3. PLL Configure

The CHIP uses PLL configure pin to control the PLL. The pin is defined as follow table:

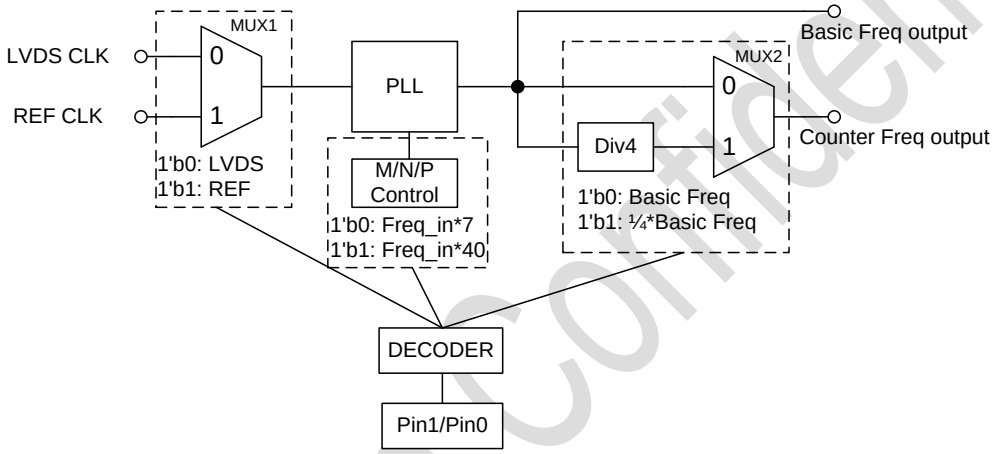


Fig. 4 PLL Configure Diagram

Table. 15 PLL ConfigureTable

PLL_CONFIG[1:0]							
PLL_ CONFIG[1]	PLL_ CONFIG[0]	MUX1	M/N/P control	MUX2	CLK MODE	Basic Freq	Counter Freq
0	0	1'b0	1'b0	1'b0	LVDS CLK	Freq_in*7	Freq_in*7
0	1	1'b1	1'b1	1'b0	REF CLK	Freq_in*40	Freq_in*40
1	0	1'b0	1'b0	1'b1	LVDS CLK	Freq_in*7	1/4*Basic Freq
1	1	1'b1	1'b1	1'b1	REF CLK	Freq_in*40	1/4*Basic Freq

3.6. LVDS Receiver

The Chip has four LVDS Receivers. Each LVDS Receive is designed to support Single Link transmission. The LVDS Receiver converts the LVDS data stream back into 42 bits of CMOS data with a variety of LCD panel controllers.

The receiver LVDS clock operates at rates from 25 MHz to 115 MHz, At an incoming clock rate of 115MHz, each LVDS input line is running at a bit rate of 805Mbps.

3.6.1. Feature

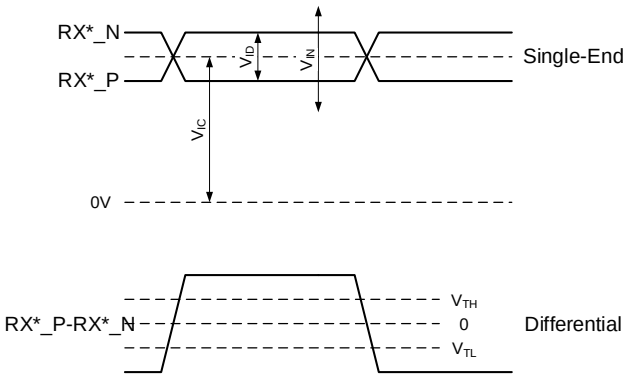
- Function compatible with the National DS90CF386
- Converts 6-pair LVDS data stream into parallel 42 bits of CMOS data
- Supports up to 805Mbps data rate
- On-chip DLL requires no external component
- Low-power CMOS design
- Power-down control function
- Compatible with the TIA/EIA-644 LVDS standards
- Full industrial operating junction temperature range: -40°C ~ +85 °C
- On chip 100Ω termination resistor.
- Negative clock edge for data output

3.6.2. Electronic Characteristic

Table. 16 LVDS Electronic Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction temperature	**Tj**	-40	25	85	°C
1.2 V Supply voltage	DVDD	1.08	1.2	0.32	V
3.3 V Supply voltage	VCCRX	2.97	3.3	3.63	V
3.3 V Supply voltage VCCBUF	VCCBUF	2.97	3.3	3.63	V
LVDS Input Analog Signals					
Single Link Bit Rate		175		805	Mbps
Input common mode voltage	V_{IC}	0.1		2.5	V
Input differential voltage threshold	V_{ID}	100			mV
Receiver input range	V_{IN}	0		2.5	V
Low-level differential input voltage threshold	V_{TL}	-100			mV
High-level differential input voltage threshold	V_{TH}			100	mV
LVDS Input Clock					
LVDS input clock range	f_{clk}	25		115	MHz
Digital Inputs/Outputs					
Logic Family		CMOS 1.2V			
Timing Characteristics					
RX data Sample window	t_{SW}	350			ps
Data setup skew requirements	t_{SKEW1}			0.5UI-t_{SW}	ps
Data hold skew requirements	t_{SKEW2}			0.5UI-t_{SW}	ps
RX input data skew margins(setup)	R_{SM}	0.5UI-t_{SW}-t_{SKEW1}			ps
RX input data skew margins(hold)	R_{HM}	0.5UI-t_{SW}-t_{SKEW2}			ps
Power Current Consumption*					
Current consumption of 3.3V	$I_{3.3}$		65		mA
Power-down leakage of 3.3V	I_{PD}		0.06		uA

Note*: The typical current consumption is at the condition of 805Mbps PRBS7 pattern.



***Note:** V_{IC}=0.1V~2.5V, V_{TH}=100mV, V_{TL}=-100mV

Fig. 5 Definition of DC Parameters of Differential Input

3.7. LED Matrix Driver

The Matrix Driver is used to driver LED for Micro LED ASIC. It integrates 24*24 LED matrix cells and internal current generation.

Each matrix cell contains 64 output channels; it is implemented by the 8*8 array in the back-end. Only 8 constant current sources were integrated in each matrix cell.

Each matrix cell shares a 6 bit current gain control to adjust the output current. The maximum output current is up to 400uA. It also supports the PWM grayscale brightness control.

3.7.1. Feature

- Supply voltage: DVDD:1.2V±10%
  AVDD33/DVDD33: 3.3V±10%
  LED_PV: 3.3V±10%
- Support 24*24*64 LED Channels
- 6 bits Current Gain control
- Maximum 400uA output current for LED
- Operating junction temperature: -40^{0}C ~125^{0}C
- Support PWM grayscale brightness control
- Matrix Cell Size: 194.4um*194.4um(after shrink)

3.7.2. Electronic Characteristic

(TA= +25°C, AVDD33/DVDD33/LED_PV = 3.3 V, DVDD=1.2V. The unless otherwise noted)

Table. 17 LED Matrix Driver Electronic Characteristic

PARAMETER	MIN	TYP	MAX	UNIT
Operating Temperature Range	-40	25	125	℃
LED_PV Power Supply		3.3	3.63	V

LED_PG Power Supply			-3		V
3.3V Analog Power Supply(AVDD33)		2.97	3.3	3.63	V
3.3V Digital Power Supply(AVDD33)		2.97	3.3	3.63	V
1.2V Digital Power Supply(DVDD12)		1.08	1.2	1.32	V
Maximum output current of LED driver(I_{OUT})				400	uA
Voltage drop for LED output channel(V_{DROP})	I_{OUT}=400uA	1.75			V
	I_{OUT}=200uA	1.22			
Threshold Voltage of LED Pixel(V_{THLED}@400uA)				4.2	V
Output Current Precision Channel to Channel(△I_{OUT})	I_{OUT}=400uA		±2		%
	I_{OUT}=200uA		±3		
Input Reference Voltage(VREF)		1.1	1.22	1.28	V
DVDD33 Supply Current			20		mA
AVDD33 Supply Current	I_{OUT}=400uA		8.4		mA
	I_{OUT}=200uA		4.2		
LED_PV Supply Current (DAC[5:0]=6'b111111)	I_{OUT}=400uA		91		mA
	I_{OUT}=200uA		46		

3.7.3. Pixel Floorplan of LED Block

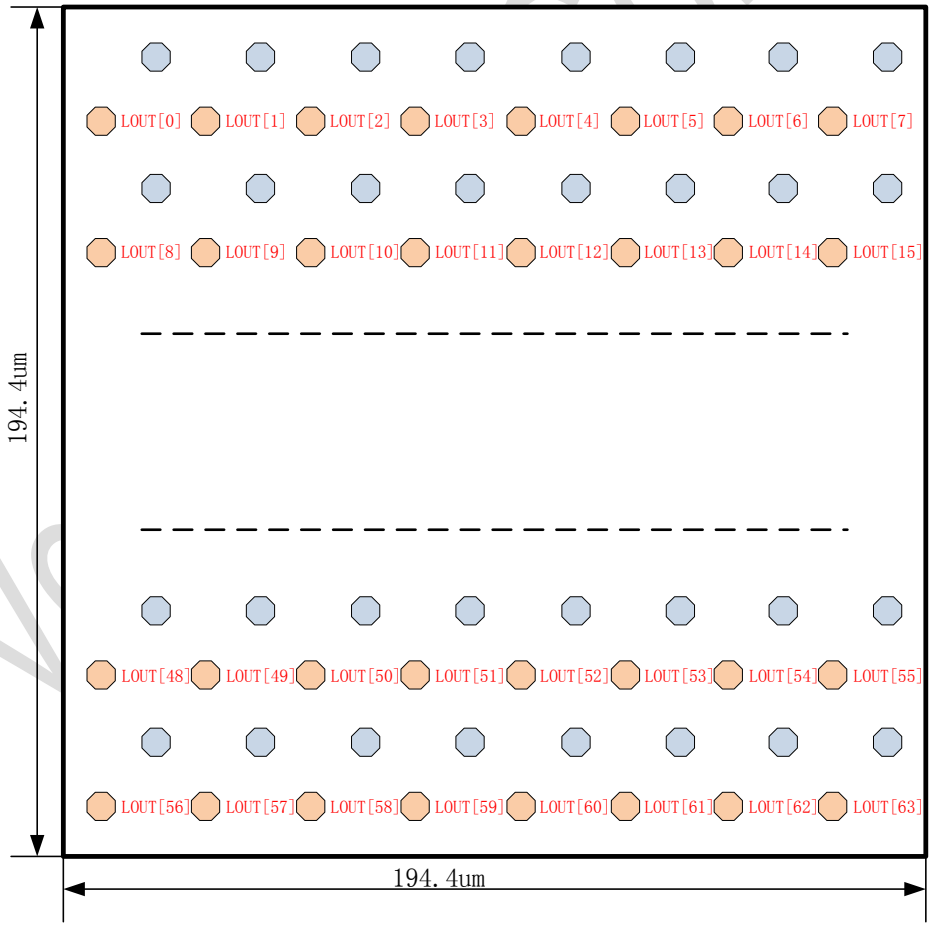


Fig. 6 Pixel Floorplan of LED Block

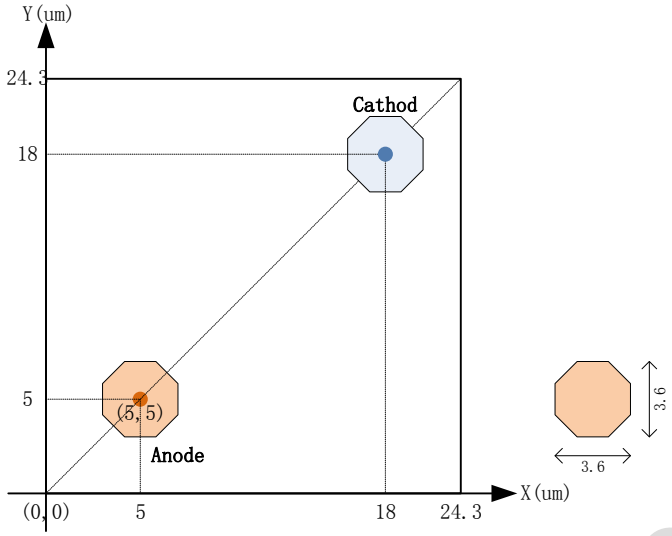


Fig. 7 Pad Opening of Pixel Cell

3.8. Power ON Reset (POR)

The chip has an internal POR circuit, the power on reset (POR) generates system reset signal (RESET and RESETN) when 1.2V power (POR_VDD) rises to a specific level, i.e., Vtr.

3.8.1. Feature

- Supply voltage: 1.2v
- Quiescent current: <5uA
- Operating junction temperature: - 40°C ~ +25°C ~ +125°C

3.8.2. Electrical Specifications

Table. 18 POR Electrical Specifications

Characteristics	Sym	Min	Typ	Max	Unit	Condition
Power Supply	VDD	1.08	1.2	1.32	V	
Reset Trigger Level	Vtr	0.48	0.8	1.00	V	VDD Slew Rate: 1.2v/10us
Reset Delay Time	Tdelay	20	70	200	us	
Quiescent Current	IDD		3	5	uA	POR_EN='0'
PD Current	IPD		50	1000	nA	POR_EN='1'

3.9. Temperature Detector (TSHUT)

The chip integrates a Temperature Detector, it detects chip temperature with on chip PNP. (The chip temperature is not the same as the circumstance temperature.) When the temperature exceeds the threshold, this IP will output a high active signal.

3.9.1. Feature

- **Detection thresholds:** the up-threshold +125℃
- **Thermal hysteresis:** about 50℃
- **Typical current consumption:** 100uA
- **Power down current:** 0.1uA

3.9.2. Electrical Characteristics

Table. 19 TSHUT Electrical Characteristics

Characteristics	Sym	Min	Typ.	Max	Unit	Conditions
Power supply	AVDD	2.97	3.3	3.63	V	
Power supply	DVDD	1.08	1.2	1.32	V	
Supply current	I_{AVDD}		100		uA	Standby Mode
			0.1			Shutdown Mode
	I_{DVDD}		1		uA	Standby Mode
			0.1			Shutdown Mode
Threshold variation			±18		℃	
Threshold adjust step			10		℃	
Thermal hysteresis			50		℃	
Startup and detect time	t		2		ms	

4. References

[1] MicroLED 驱动芯片设计需求书
[2] S11V33_LVDSRX_04
[3] S13V33_PLL_07_1G
[4] S13V33_POR_01_1P2V
[5] S11V33_TSHUT_01
[6] VS_ MicroLED Driver Matrix Spec