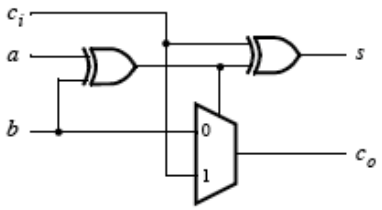
ECE3270 Digital System Design
Lab 2: OpenCL Libraries

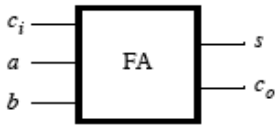
Homework Overview: The purpose of this homework is to ensure each student can successfully use OpenCL and familiarize themselves with the concept of Libraries for OpenCL.

Part I

You are to design a 16-bit ripple carry adder in VHDL. You will design the Full Adder as a behavioral circuit and then use this as a component to generate the Ripple Carry Adder. A 4-bit example is shown in Part d) of the figure below. Using a generate statement will make the process much easier, and a generic will allow you to test a smaller design for verification before building the full 16-bit adder.



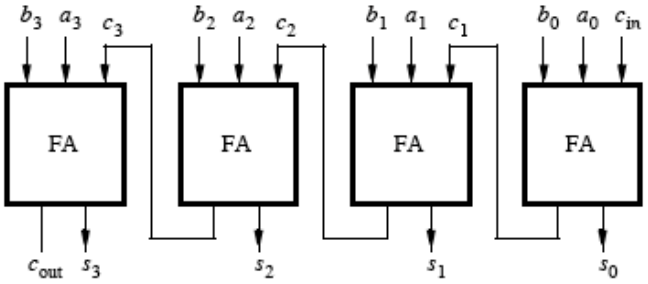
a) Full adder circuit



b) Full adder symbol

b	a	c_i	c_o	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

c) Full adder truth table



d) Four-bit ripple-carry adder circuit

After designing this circuit, write a testbench to verify functionality. You will submit this testbench with your code.

Part II

Create a new entity and instantiate a component of your Ripple Adder within it. Include all signals necessary for OpenCL Libraries and set them as required. Follow the OpenCL compilation and Usage Instructions guide to run and test your circuit. OpenCL will send the data to your adder and save all the results. It will then give you human readable output for each test input. View the README.txt in the tarball for sample output and verify this matches your program execution.

You will be required to write a full report using the LaTeX template. Include images showing signals updating correctly using the testbench. Submit all of your *.vhd and *.vht files to the assign server as assignment 2.