ECE 3270 Project Report Grading Guide and Instructions

DEMO (40Points): Follow instructions for demo date and time. Come prepared to demo and NOT work on your code!

CODE: Submit your VHDL-code, including testbench (as attached files named **xxxx.vhd or xxxx.vht**, where **xxxx** is Lab1a.vhd, Lab1b.vhd, TB1a.vht, TB1b.vht, etc.) to Email = ece_assign@clemson.edu. Use as subject header **ECE3270-1,#X user=*userid*** where ***userid*** is your Clemson user ID and **X** is the lab number. **Code is due by 11.59pm on the day of the demo**.

LAB REPORT: Submit via Turnitin according to the schedule in the assignment.

Project Report Discussion: 20 points

See discussion that follows on how to prepare a lab report.

Simulation: 30 points

These are the simulation results included in your Project Report (i.e. your test strategy, test coverage, analysis, timing diagrams, etc.)

Simulation test case coverage and documentation: 20 points possible

above average	20 points
average	15 points
below overage	10 points
minimal	5 points

Results: 10 points

Expect correlation with truth tables, state diagrams, and analysis in the report discussion… include **NOTES on the simulation graphs** that illustrate that the waveform is the correct output - that you actually checked the results rather than just handing in whatever output you obtained.

Incomplete annotation	-5 points
Lack of verification of results	-10 points

Partial credit given where appropriate

Instructions for Preparing Laboratory Reports

1. Your lab report should consist of the following:

   a) Cover Sheet
   b) Abstract
   c) Body of the Report (in appropriately named sections)
   d) References
   e) Appendices (multipage timing diagrams, etc.)

2. **Cover Sheet**: The cover sheet should follow the format similar to the sample cover sheet that is attached.

3. **Abstract**: The abstract is a brief (50-150 words) summary of your report. The project goals, major results, and/or conclusions should be stated in the abstract. The abstract should occupy a single page with the centered title, "ABSTRACT".

4. **Body of the Report**: The body of the report should begin with an INTRODUCTION and end with a CONCLUSIONS section that includes “lessons learned”. The remainder of the report should be divided into several named sections as appropriate. You should have sections titled according to what is described in that section, e.g. “Design of a 4-bit Comparator Circuit”, “Test of a 4-bit Comparator Circuit”, etc. Note: You should never have a section titled “Body of the Report”.

Include block diagrams, circuit diagrams, state diagrams, truth tables, Boolean equations, etc. as appropriate (i.e. what you used to develop and explain your design) complete with discussion of these figures as appropriate to the project (you may choose to put figures in an appendix as discussed below). At a minimum, the report discussion should include theory of operation, testing strategy, etc. If things are not working correctly, also include a discussion describing what you think is wrong and your strategy for correcting.

5. **References**: As appropriate, include a list of reference material used in your design development and preparing your report (i.e. your book, internet sources, conference/journal papers, etc.). References should be listed in the order they were cited in the report and should be in standard IEEE format (see the *IEEE Information for Authors* document on the course website). The *Preparation of Papers for IEEE TRANSACTIONS and JOURNALS* document on the course website also provides good examples. The references should occupy one or more separate pages with the centered title "REFERENCES". **References that do not follow these conventions will be graded as completely incorrect**.

6. **Appendices**: Diagrams, programs, tabular data, etc. may be included as appendices or may be contained within the body of the report. Any data that spans more than one page should be included in an appendix. Construct multiple, titled and lettered appendices as appropriate, e.g. Appendix A – VHDL Code Segments for a 4-bit Comparator, Appendix B – Timing diagram for a 4-bit up/down counter, etc.

7. **Figures**: Figures should be legible and have an appropriate figure number and caption. Logic diagrams and timing diagrams may be screen captured and imported as figures where appropriate. Logic and/or timing diagrams may appear in landscape mode to enhance readability. All information in logic diagrams and timing diagrams should be labeled appropriately. The *IEEE Information for Authors* document in the Labs folder of the blackboard website is the source for describing proper formatting and referencing of figures (do not put a figure in your report that is not properly referenced and described in the text). **Figures that do not follow these conventions or are unreadable will be graded as completely incorrect**.

8. **VHDL Source Code**: All VHDL source code must follow coding conventions presented and

discussed in class. **Code that does not follow these conventions will be graded as completely incorrect**. All code must be submitted to the Assign server as previously described. Do NOT include your entire code in your report but you may use code segments to describe implementation and operation where appropriate.

9. **Timing diagrams**: Remember, timing diagrams are meant to convey information to your reader about the functionality of a given design. Related signals should be grouped together to enhance readability. For example, **clock** and **clock related** signals should be grouped together and placed at the top of the timing diagram. Controls signals should also be grouped together with the data signals they control. Timing diagrams should be sized so that it is easy to read appropriate information from the timing diagram. Long timing diagrams should be split into multiple figures as appropriate. Annotations should be added to these diagrams to indicate important test vectors, modes of operation, etc. **Timing diagrams that do not follow these conventions or are unreadable will be graded as completely incorrect**.

10. All pages are to be numbered with the exception of the cover sheet and abstract page.

11. All reports must be typed and submitted via Turnitin.

13. All reports should be free of grammatical and typographical errors. Use an appropriate word processor with spell and grammar check capabilities.

14. All reports are to be 1.5-spaced with appropriate margins (one inch on all sides).

<Title of the Lab>

Lab Report for ECE327
Digital Systems Design

Submitted by

<Name>

Department of Electrical & Computer Engineering
Clemson University

<Date>