

$\therefore$  256 opcodes as maximum.

(b) PC : 17 bits      IR = 15 bits or 32 bits  
 MAR : 17 bits      AC = 32 bits  
 MDR : 32 bits

2.

(a) AND (There's already another operand in AC)

• Fetch

- i)  $MAR \leftarrow PC$
- ii)  $MDR \leftarrow M[MAR], PC \leftarrow PC + 1$
- iii)  $IR \leftarrow MDR(opcode), MAR \leftarrow MDR(address)$

• execute

- i)  $MDR \leftarrow M[MAR]$
- ii)  $AC \leftarrow AC \wedge MDR$

(b) ISZ

• Fetch

- i)  $MAR \leftarrow PC$
- ii)  $MDR \leftarrow M[MAR], PC \leftarrow PC + 1$
- iii)  $IR \leftarrow MDR(opcode), MAR \leftarrow MDR(address)$

• Execute

- i)  $MDR \leftarrow M[MAR]$
- ii)  $AC \leftarrow MDR$
- iii)  $AC \leftarrow AC + 1$ , If  $(Z=1)$  then  $PC \leftarrow PC + 1$

(c) DCA (There's already another operand in AC)

• Fetch

- i)  $MAR \leftarrow PC$
- ii)  $MDR \leftarrow M[MAR], PC \leftarrow PC + 1$
- iii)  $IR \leftarrow MDR(opcode), MAR \leftarrow MDR(address)$

• Execute

- i)  $MDR \leftarrow AC$
- ii)  $M[MAR] \leftarrow MDR, AC \leftarrow 0$

(d) SMS

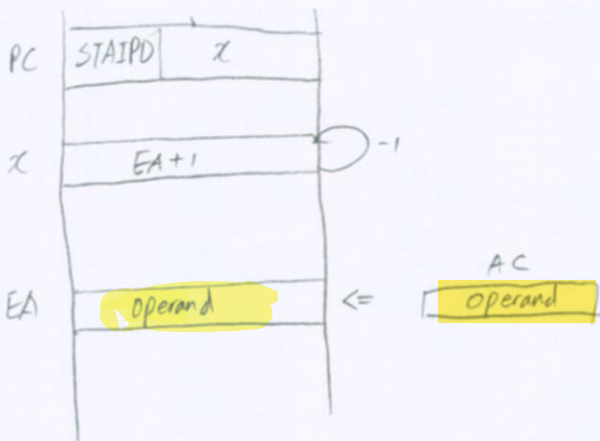
• Fetch

- i)  $MAR \leftarrow PC$
- ii)  $MDR \leftarrow M[MAR], PC \leftarrow PC + 1$
- iii)  $IR \leftarrow MDR(opcode), MAR \leftarrow MDR(address)$

• Execute

- i)  $MDR \leftarrow PC$
- ii)  $M[MAR] \leftarrow MDR, PC \leftarrow MAR$
- iii)  $PC \leftarrow PC + 1$

3.



i)  $TEMP \leftarrow AC, MDR \leftarrow MEMAR]$

ii)  $AC \leftarrow MDR$

iii)  $AC \leftarrow AC - 1, TEMP \leftarrow TEMP$

iv)  $MDR \leftarrow AC$

v)  $MEMAR \leftarrow MDR, MAR \leftarrow MDR$

vi)  $MDR \leftarrow TEMP$

vii)  $MEMAR \leftarrow MDR$

4.

i) MOV R1, R24

R0 01

R1 02

R2 1B

R3 07

R4 01

X 0106

Y 0102

SREG -----  $\frac{0}{N} \frac{0}{Z} \frac{0}{C}$

ii) LD R4, Y+

R0 01

R1 05

R2 1B

R3 07

R4 EC

X 0106

Y 0103

SREG -----  $\frac{1}{N} \frac{0}{Z} \frac{0}{C}$

0100, 01

0101, BE

0102, 35

0103, EC = 0b(1110 1100)

0104, 48

0105, 2D

0106, 04

0107, 02

N Flag

iii) LDI R4, 33

R0 01

R1 05

R2 1B

R3 07

R4 21

X 0106

Y 0102

SREG -----  $\frac{0}{N} \frac{0}{Z} \frac{0}{C}$

iv) MUL R2, R3

R0 BD

R1 00

R2 1B

R3 07

R4 01

X 0106

Y 0102

SREG -----  $\frac{0}{N} \frac{0}{Z} \frac{1}{C}$

v) ROL R3

R0 01

R1 05

R2 1B

R3 0F

R4 01

X 0106

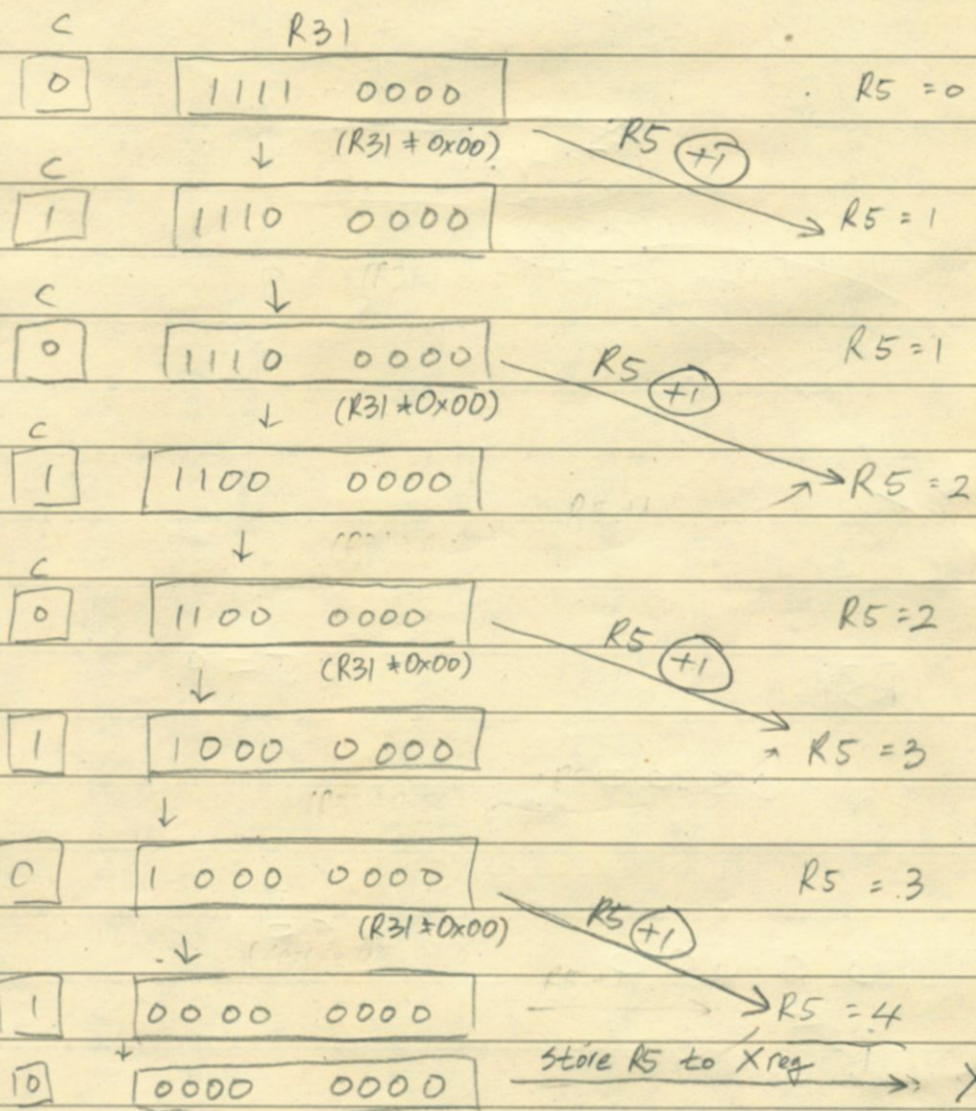
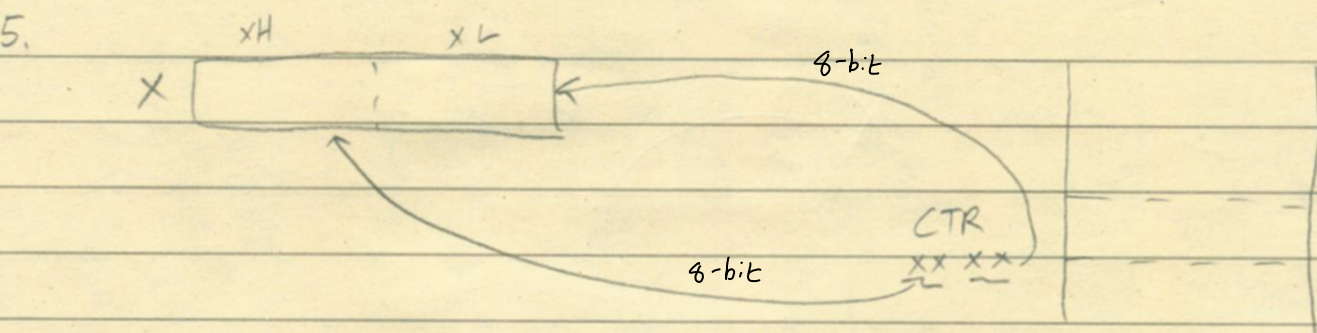
Y 0102

SREG -----  $\frac{0}{N} \frac{0}{Z} \frac{0}{C}$

( $\because 1B \times 07 = 00BD$ )  
 $\begin{matrix} \downarrow & \downarrow \\ R1 & R0 \end{matrix}$

0000 0111  $\xrightarrow{C}$   $\therefore SREG = FF$   
 $\downarrow$   
 $\begin{matrix} \text{S} & \text{S} \\ \text{0} & \text{0} \end{matrix} 0000 1111 \Rightarrow \begin{matrix} \text{S} & \text{S} \\ \text{0} & \text{0} \end{matrix} 0F$





Program counts number of bit '1's in the R31 register. By rotating bits to left and clearing carry, it keeps incrementing R5 until there is no bit '1' in R31 register. Thus, it iterates the number of bit '1' in register. By storing R5 to X register, it changes the value of location CTR.

The value of location CTR = 0x0004.