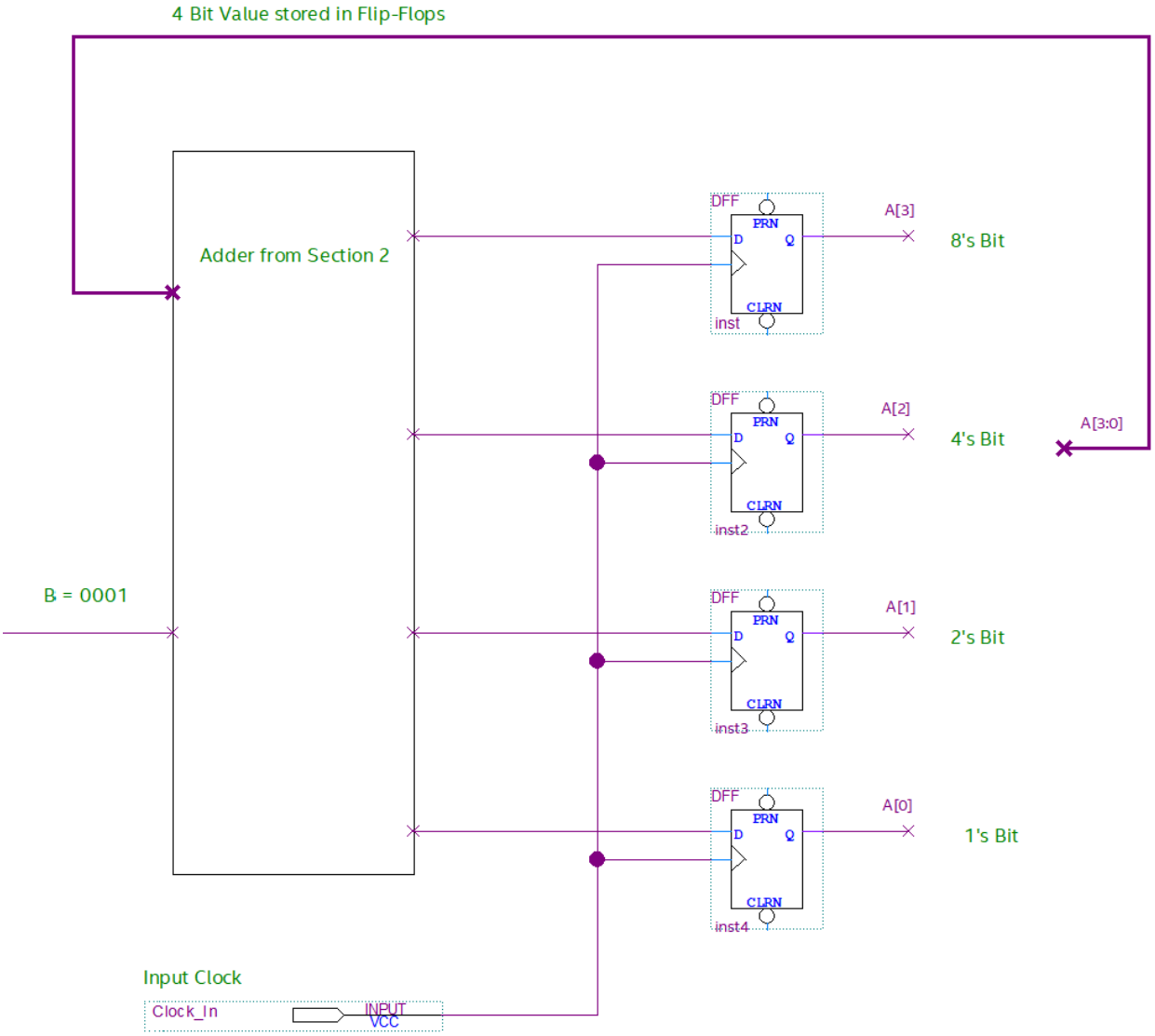
Lab 4 Prelab

Lab 4 will use D Flip-Flops and adders to make a counter. A 4-bit example is shown below. Note that this could use the adder developed in section 2. The output of each flip-flop is connected to a 4-bit bus which connects to the first input of the adder. The second input is connected to 1, which would be 0001 for a 4-bit adder. Each rising edge of the clock will load the sum output by the adder into the flip-flops.



Questions

1. Given an input clock signal at 10 MHz, what frequency would A[0] alternate? What frequency would A[1] alternate?

   A[0] will alternate 5MHz.
   A[1] will alternate 2.5MHz.

2. What do the PRN and CLRN inputs do on the D Flip-Flops in Quartus? Refer to this link for more information: https://www.intel.com/content/www/us/en/programmable/quartushelp/13.0/mergedProjects/hdl/prim/prim_file_dff.htm

   PRN and CLRN inputs turn on or off the D Flip-Flops in Quartus when there is no clock value. The reason is that in the table, when there were no clock values and only PRN and CLRN inputs, the outputs of the D outputs were depending on PRN and CLRN inputs, but when there were clock values including the change with stable PRN and CLRN inputs (H), the outputs were depending on the clock values.

3. How many bits would a counter need to be to make the MSB of the counter alternate at almost 1/1000th of the input clock speed?

$$N\ bit\ \Rightarrow \frac{10MHz}{2^N}$$

$$\frac{10MHz}{2^N} = \frac{1}{1000} * 10MHz$$

$2^N = 10^3\ \Rightarrow N = \log_2 10^3 = 3\log_2 10 = 9.9657840$

Therefore, a counter needs 10-bits to make the MSB of the counter alternate at almost 1/1000 th of the input clock speed.