1. HDL source (System Verilog file)

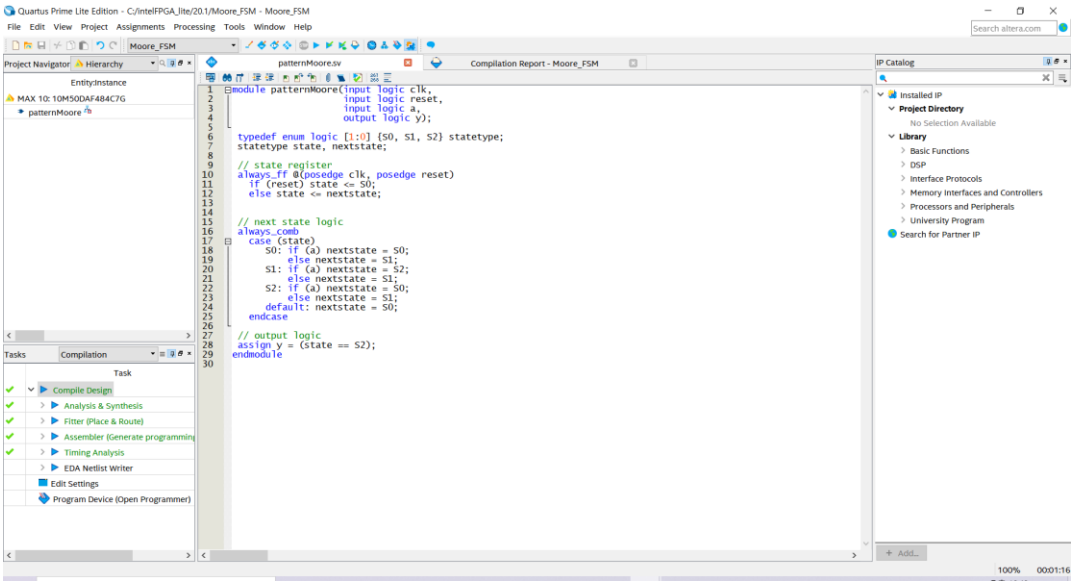
```
module patternMoore(input logic clk,
                    input logic reset,
                    input logic a,
                    output logic y);

  typedef enum logic [1:0] {S0, S1, S2} statetype;
  statetype state, nextstate;

  // state register
  always_ff @(posedge clk, posedge reset)
    if (reset) state <= S0;
    else state <= nextstate;


  // next state logic
  always_comb
    case (state)
       S0: if (a) nextstate = S0;
           else nextstate = S1;
       S1: if (a) nextstate = S2;
           else nextstate = S1;
       S2: if (a) nextstate = S0;
           else nextstate = S1;
       default: nextstate = S0;
    endcase

  // output logic
  assign y = (state == S2);
endmodule
```



(The System Verilog source is compiled successfully.)

2. Interface definitions

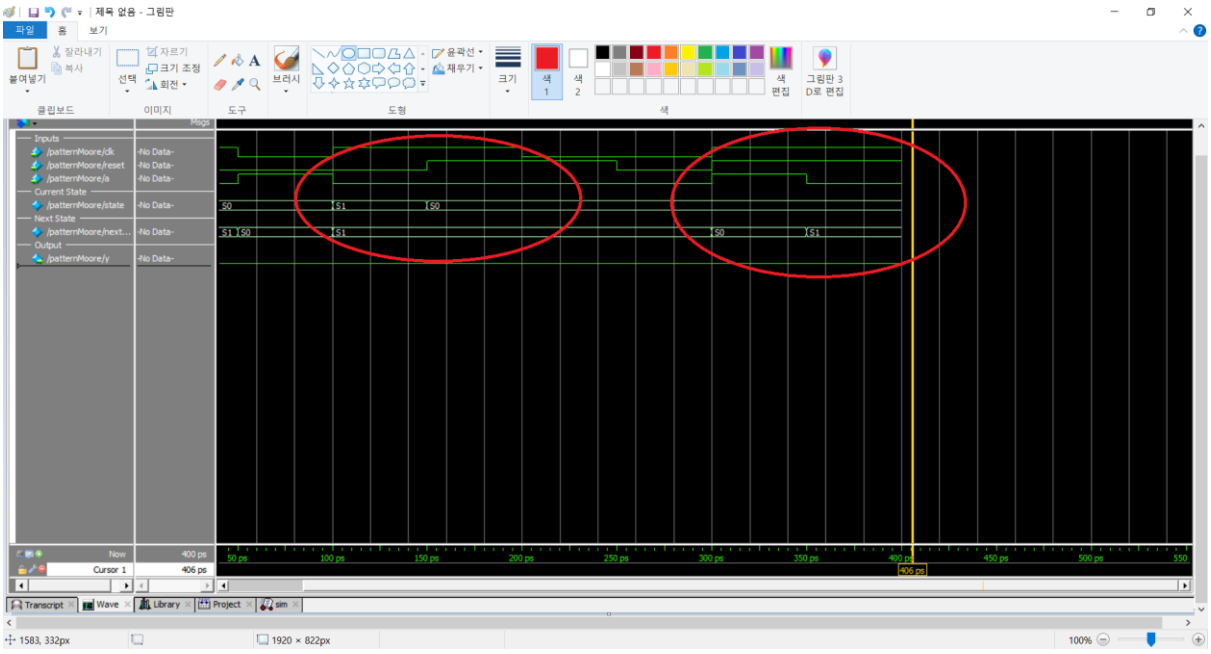
<Expected inputs and results>

Current State	Input (a)	CLK	Reset	Next State	Output
S0	0	0	0	S1	0
S0	1	0	0	S0	0
S0	0	1	0	S1	0
S0	1	1	1	S0	0
S0	0	0	1	S0	0
S0	1	0	0	S0	0

3. List of the script

```
VSIM 2> add wave *
VSIM 3> force clk 1 @ 0
VSIM 4> force clk 0 @ 50
VSIM 5> force clk 1 @ 100
VSIM 6> force clk 0 @ 200
VSIM 7> force clk 0 @ 300
VSIM 8> force a @ 0
# Invalid binary digit: @.
# ** UI-Msg: (vsim-4011) Invalid force value: @ 0.
#
VSIM 9> force a 0 @ 0
VSIM 10> force a 1 @ 50
VSIM 11> force a 0 @ 100
VSIM 12> force a @ 150
# Invalid binary digit: @.
# ** UI-Msg: (vsim-4011) Invalid force value: @ 150.
#
VSIM 13> force a 0 @ 250
VSIM 14> force a 0 @ 300
VSIM 15> force reset 0 @ 0
VSIM 16> force reset 1 @ 150
VSIM 17> force reset 0 @ 250
VSIM 18> force reset 0 @ 300
VSIM 19> run 300
VSIM 20> force clk 1 @ 300
VSIM 21> force a 1 @ 300
VSIM 22> force reset 1 @ 300
VSIM 23> run 50
VSIM 24> force clk 1 @ 350
VSIM 25> force a 0 @ 350
VSIM 26> force reset 1 @ 350
VSIM 27> run 50
```

4. Simulation Output



5. System Validation Summary

   In the prediction of the left red circle, when the value of reset is 0 and the value of a is 1with current state S1, the next will be S1. However, in the simulation, as the value of reset changes to 1, the actual next state was S0.

   In the prediction of the right red circle, when the value of the reset is 1 and the value of a is 0 with current state 0, the next state will be S0. However, in the simulation, the next state was S1.

   Thus, the prediction was proved wrong through the simulation.