1. $(111.111)_2$

$= 1\cdot2^2 + 1\cdot2 + 1\cdot2^0 + 1\cdot2^{-1} + 1\cdot2^{-2} + 1\cdot2^{-3}$

$= 4 + 2 + 1 + 0.5 + 0.25 + 0.125 = 7 + 0.875 = 7.875$

$\therefore (111.111)_2 = (7.875)_{10}$

2. $(14.6)_{16} = 1\cdot16^1 + 4\cdot16^0 + 6\cdot16^{-1}$

$= 16 + 4 + \frac{6}{16} = 16 + 4 + \frac{3}{8} = 20 + 3\cdot0.125 = 20 + 0.375$

$= 20.375$

$\therefore (14.6)_{16} = (20.375)_{10}$

3. $(11)_{16} = 1\cdot16^1 + 1\cdot16^0 = 1\cdot2^4 + 0\cdot2^3 + 0\cdot2^2 + 0\cdot2^1 + 1\cdot2^0$

$= (10001)_2$

$\therefore (11)_{16} = (10001)_2$

4. $(1011\,1010\,1101)_2 = (\underbrace{1011}_{(i)}\ \underbrace{1010}_{(ii)}\ \underbrace{1101}_{(iii)})_2$

(i) $1011_2 = 11_{10} = B_{16}$

(ii) $1010_2 = 10_{10} = A_{16}$

(iii) $1101_2 = 13_{10} = D_{16}$

$\therefore (1011\,1010\,1101)_2 = (BAD)_{16}$

5. $(19.25)_{10} = 1\cdot2^4 + 0\cdot2^3 + 0\cdot2^2 + 1\cdot2^1 + 1\cdot2^0 + 0\cdot2^{-1} + 1\cdot2^{-2}$

$\Rightarrow 10011.01_2 \times 2^0 = 1.001101 \times 2^4$

- Singn : 0
- Biased Exponent : $4 + 127 = 131 = 128 + 2 + 1 = 10000011_2$
- Fraction : 001 1010 0000 0000 0000 0000

$\therefore$ Sign : 0

$\therefore$ Biased Exponent : 1000 0011

Fraction : 001 1010 0000 0000 0000 0000

6.

Decimal	Octal	Hexadecimal
7322	333	ABAD
+ 1933	+ 257	− ABA
9255	612	0F3

7. $(11111100)_2$

$$\begin{array}{r} 00000011 \\ +\ 00000001 \\ \hline 00000100 \end{array}$$

$\therefore$ 2's complement operation on $(11111100)_2 = 00000100$

8. 1's complement : Swap 0s and 1s (i.e. $0 \Rightarrow 1$ or $1 \Rightarrow 0$)

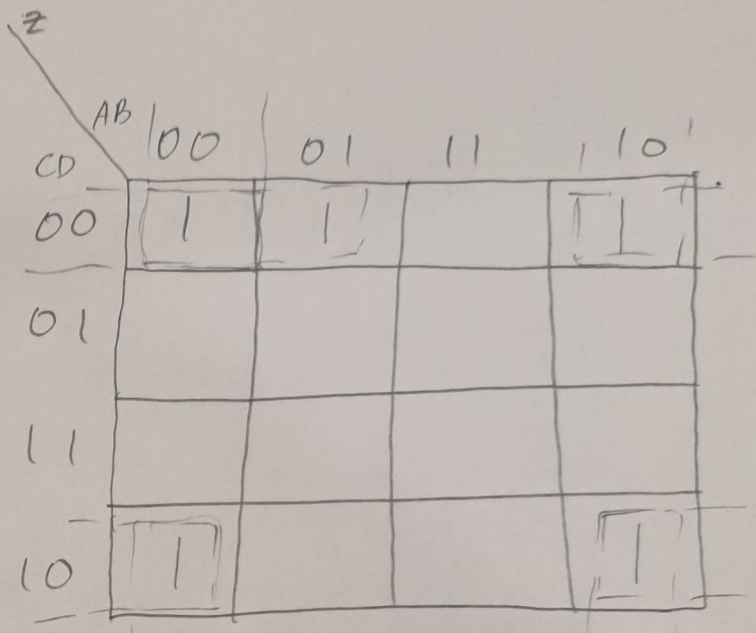
$$(11111100)_2 \xrightarrow{\text{1's complement}} (00000011)_2$$

$\therefore (00000011)_2$

$Z(A,B,C,D) = \sum 0, 2, 4, 8, 10$

A	B	C	D	Z
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

<k-map>



i) $\bar{A}B\bar{C}\bar{D} + \bar{A}BC\bar{D} = \bar{A}B\bar{D}$

ii) $\bar{A}B\bar{C}\bar{D} + AB\bar{C}\bar{D} = B\bar{C}\bar{D}$

iii) $\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} = \bar{A}\bar{B}\bar{D}$

iv) $\bar{A}\bar{B}C\bar{D} + AB\bar{C}\bar{D} = \bar{B}C\bar{D}$

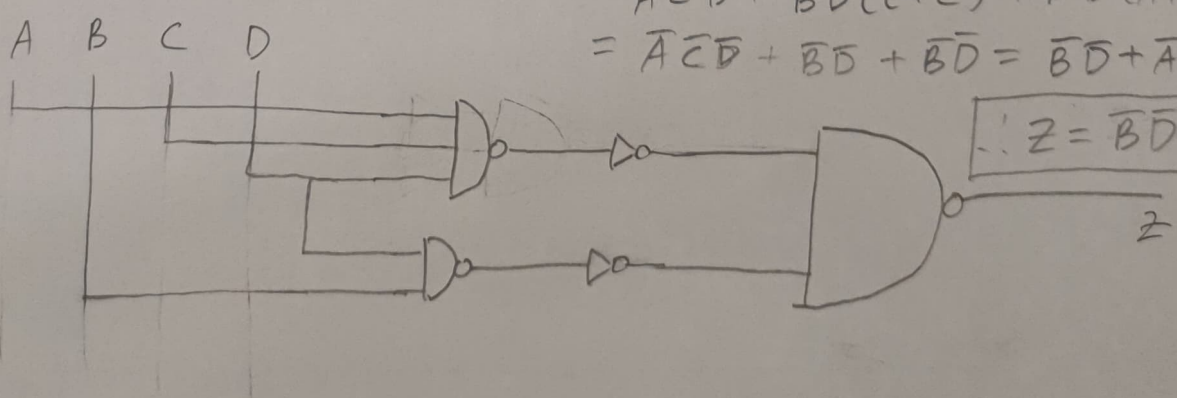
v) $A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D} = A\bar{B}\bar{D}$

$\therefore Z = \bar{A}\bar{C}\bar{D} + \bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{D} + \bar{B}C\bar{D} + A\bar{B}\bar{D}$

$= \bar{A}\bar{C}\bar{D} + \bar{B}\bar{D}(C+\bar{C}) + \bar{B}\bar{D}(A+\bar{A})$

$= \bar{A}\bar{C}\bar{D} + \bar{B}\bar{D} + \bar{B}\bar{D} = \bar{B}\bar{D} + \bar{A}\bar{C}\bar{D}$

$\therefore Z = \bar{B}\bar{D} + \bar{A}\bar{C}\bar{D}$



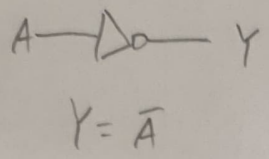
2 x 2-input NAND + 2x NOT Gate + 1 x 3input - NAND Gate

$= 2\times4 + 2\times2 + 1\times6 = 8+4+6 = 18$

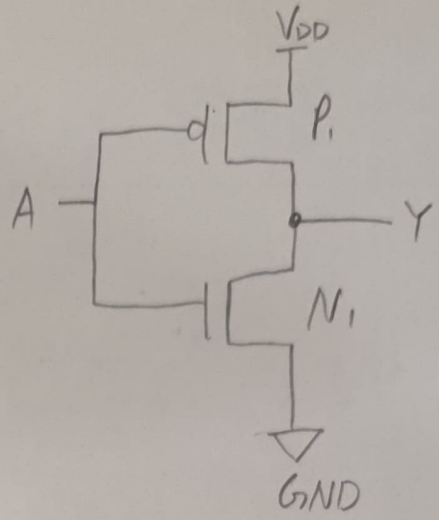
$\therefore$ 18 transistors

[CMOS]

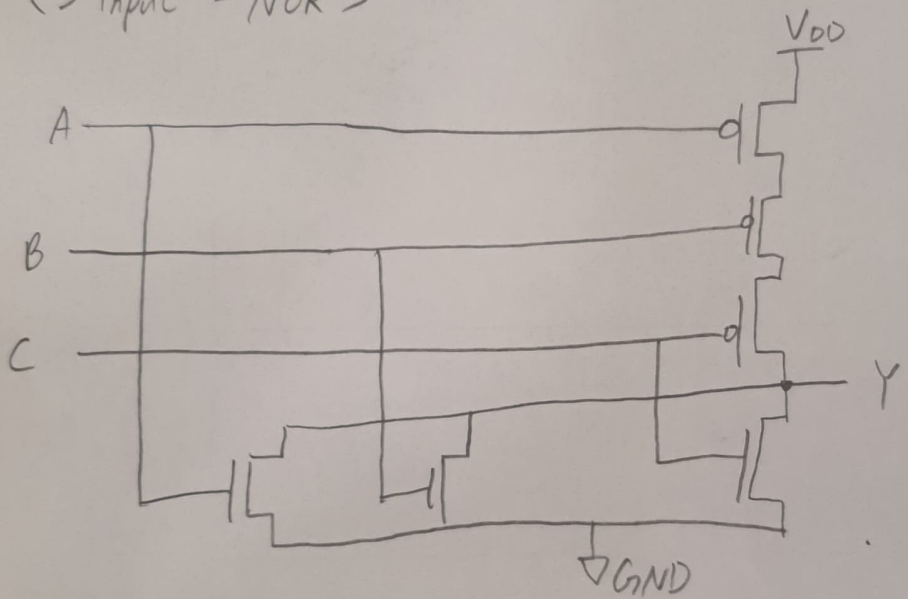
<NOT>



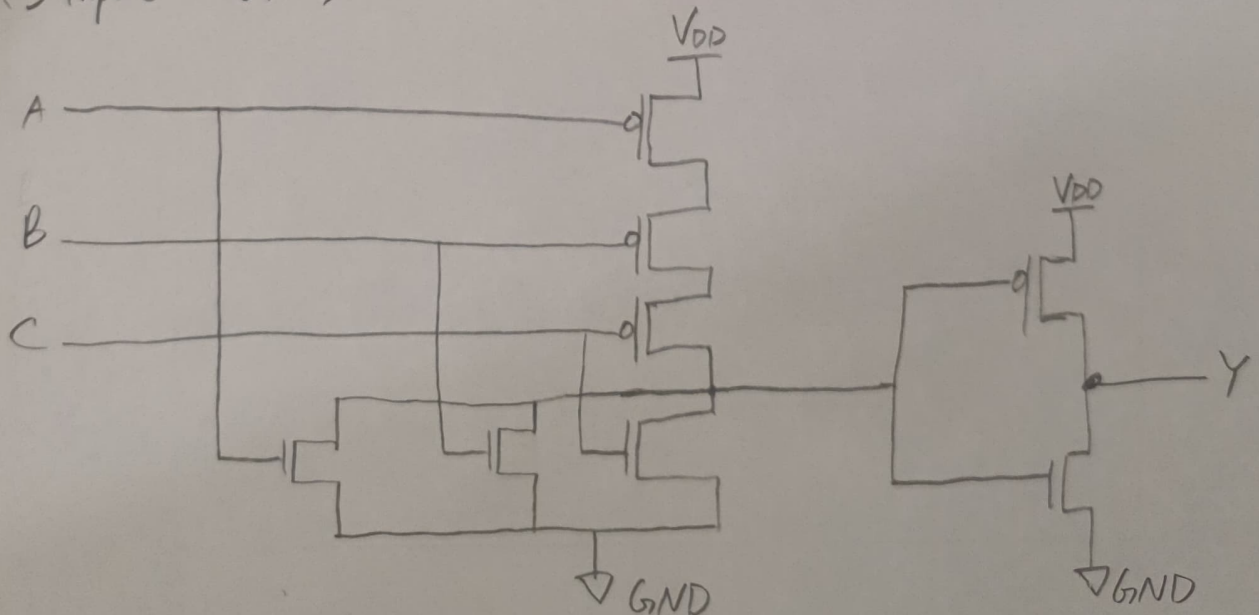
$Y = \bar{A}$



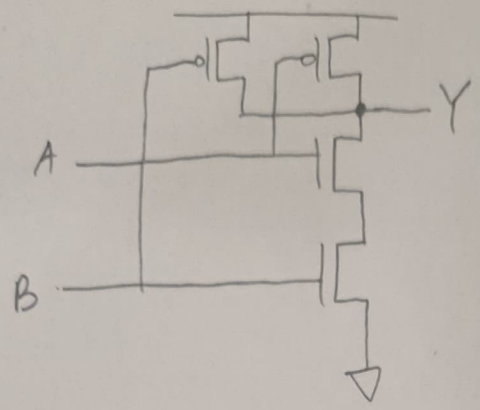
<3 input - NOR>



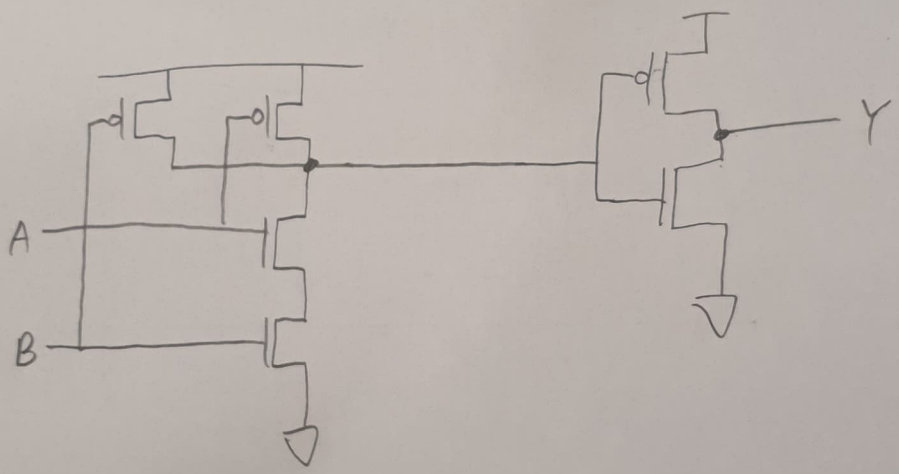
<3 input - OR>



<2-input NAND>



<2 -input AND>



<Sequential Logic Timing>

1.

Setup Time Constraint : $T_c \geq t_{pcq} + t_{pd} + t_{setup}$

$T_c = 200ps$, $t_{setup} = 90ps$, $t_{pcq} = 75ps$.

In the pipeline, there are four of Routing delay and delays by three of LUT.

So, entire t_{pd} is $4 \times 10ps + 3 \times 15ps = 85ps$.

$200ps \geq 75ps + 85ps + 90ps \Rightarrow 200ps \geq 250ps$.

This doesn't make sense!

Thus, through these reasons, if the clock period is 200ps, there is a setup time violation.

2.

Hold Time Constraint : $t_{hold} < t_{ccq} + t_{cd}$

$t_{hold} = 60ps$, $t_{ccq} = 15ps$.

The short path is the entire pipeline of digital logic.

The entire t_{cd} is $3 \times 5ps + 4 \times 5ps = 35ps$ because there are 3 LUTs and 4 Routing delays in pipeline.

$60ps < 15ps + 35ps \Rightarrow 60ps < 50ps$. This doesn't make sense!

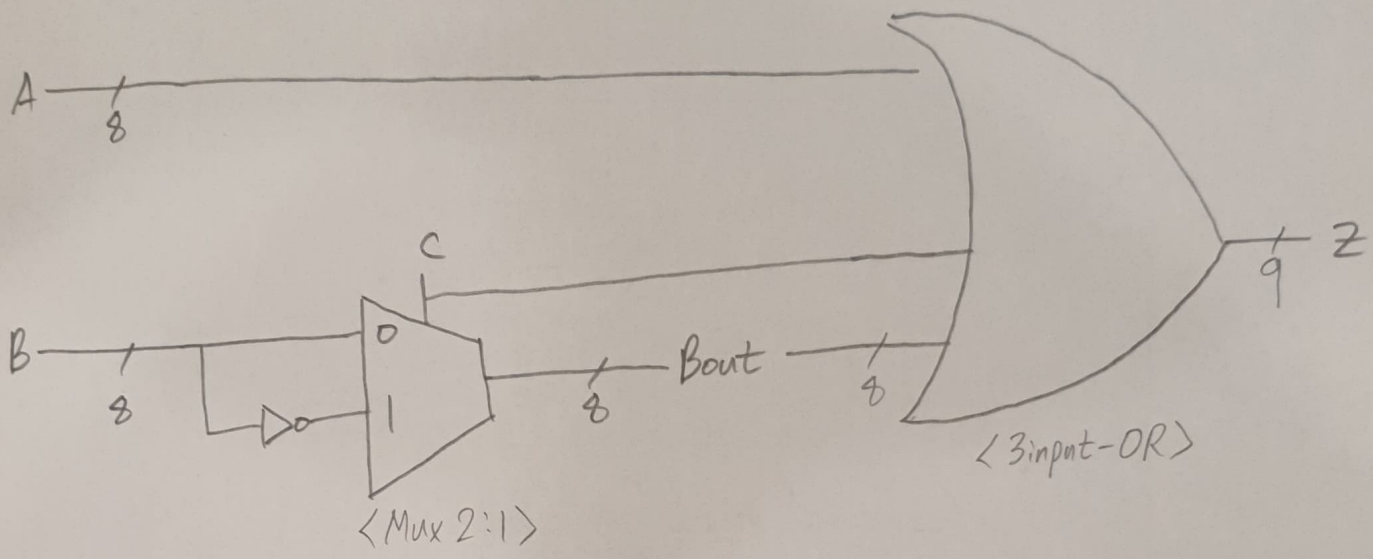
Thus, through these reasons, if the clock period is 400ps, there is a hold time violation.

3. Setup violation can be fixed by increasing the clock period, by redesigning the combinational logic to have a shorter propagation delay, or using synchronizer.

4. Hold violation can be fixed by adding more buffers the short path of the combinational logic to increase entire contamination delay.

5. The acronym LUT represents lookup table which enables to perform combinational logic in FPGA.

<Mystery Block>



<PLA>

$X(A,B,C) = \sum 0,4,6,7 = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + AB\bar{C} + ABC$

$Y(A,B,C) = \sum 0,2,3,4 = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C}$

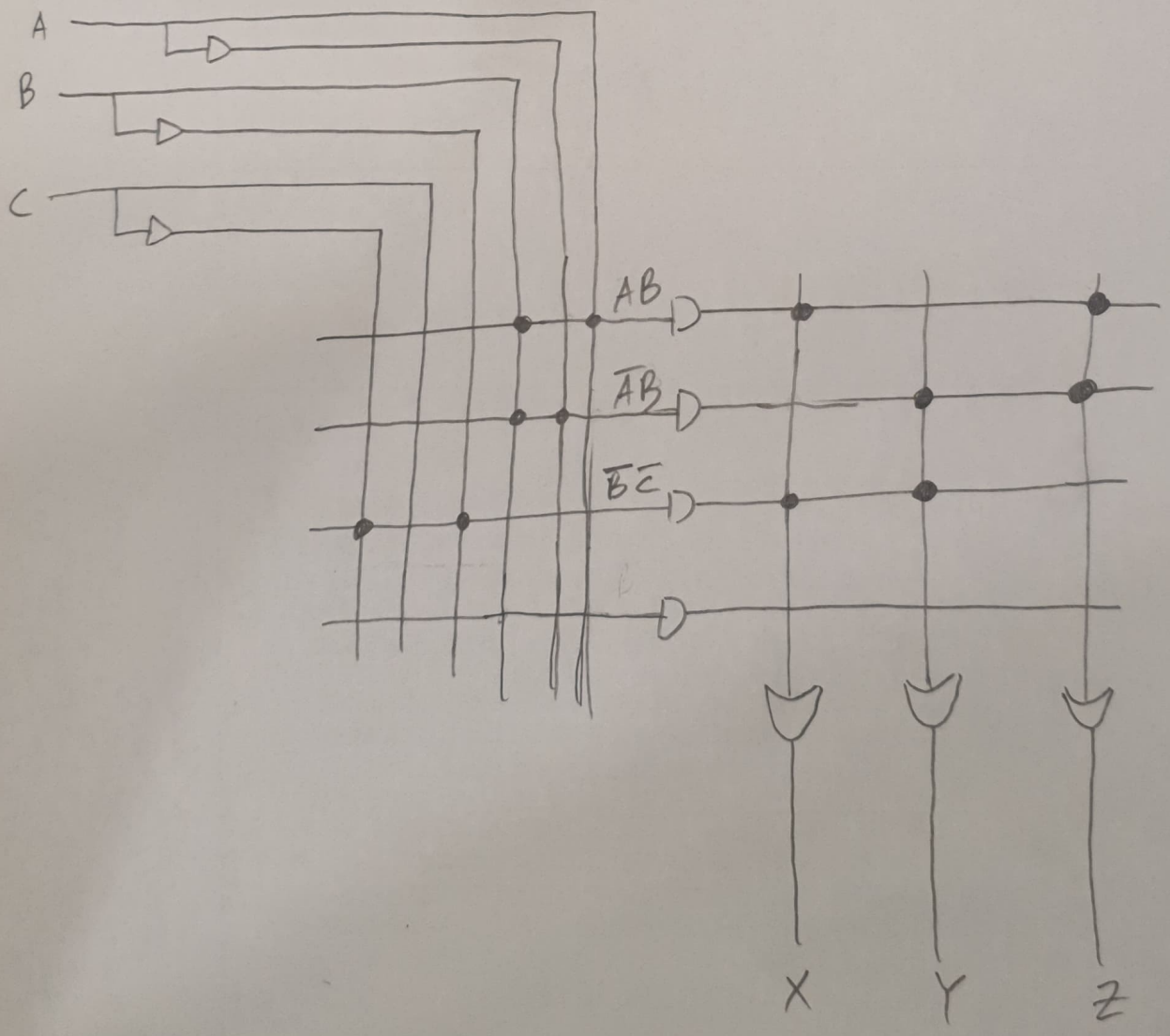
$Z(A,B,C) = \sum 2,3,6,7 = \bar{A}B\bar{C} + \bar{A}BC + AB\bar{C} + ABC$

$\Rightarrow X(A,B,C) = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + AB\bar{C} + ABC = \bar{B}\bar{C} + AB$

$Y(A,B,C) = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C}$

$= \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC = \bar{B}\bar{C} + \bar{A}B$

$Z(A,B,C) = \bar{A}B\bar{C} + \bar{A}BC + AB\bar{C} + ABC = \bar{A}B + AB = (\bar{A}+A)B = B$



<State Machines>

1. 2 bits of memory are used in this state machine.

2. Let current state and next state of upper D Flip-Flop in the schematic be S_0, S_0'

   Let current state and next state of lower D Flip-Flop in the schematic be S_1, S_1'.

   ∴ current state : S_0, S_1 , next state : S_0', S_1',
   Input : Din

$$S_0' = Din\,\overline{S_0}\,\overline{S_1} + \overline{Din}\,\overline{S_0}\,S_1 + Din\,S_0S_1 + \overline{Din}\,S_0\,\overline{S_1}$$
$$S_1' = \overline{S_1}$$

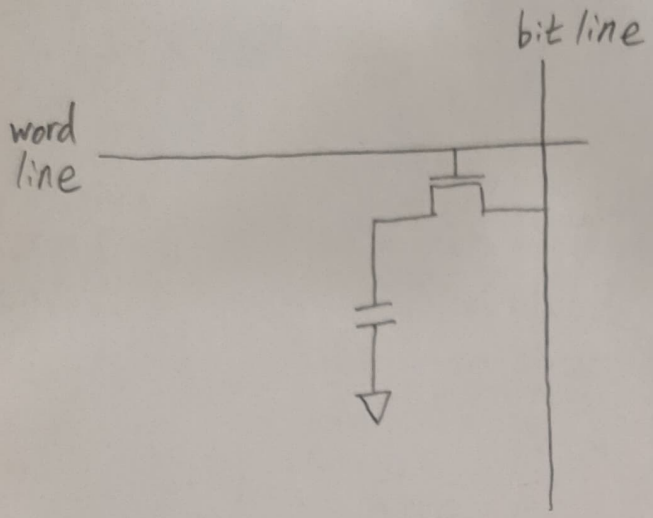
3.
1) $Q_0 = S_1$
2) $Q_1 = S_0$
3) $A = \overline{S_0}\,\overline{S_1}$
4) $B = \overline{S_0}\,S_1$
5) $C = S_0\,\overline{S_1}$
6) $D = S_0S_1$

4. The output of this state machine is only depending on the current state; S_0 and S_1.

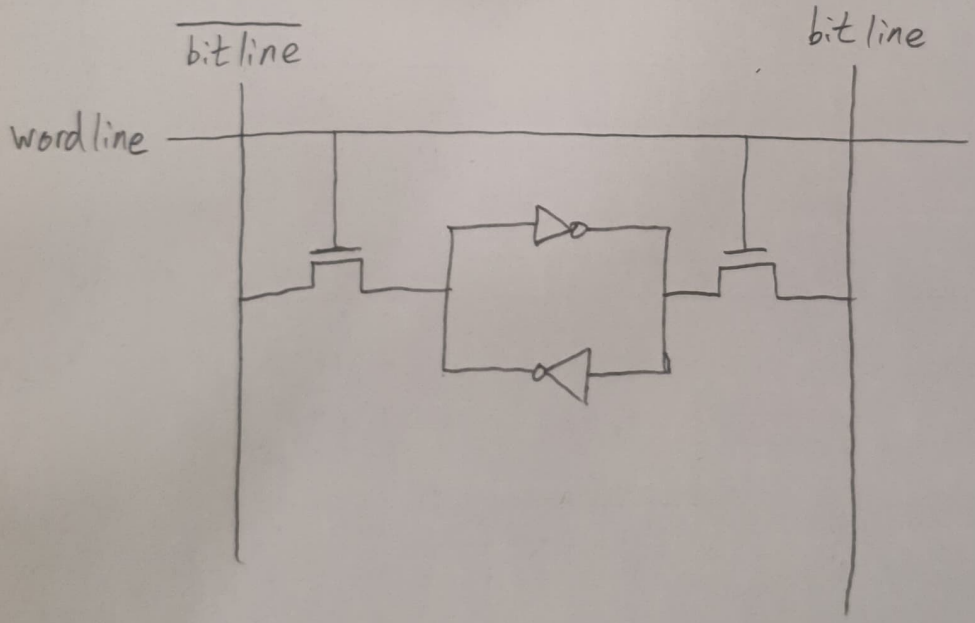
Therefore, this state machine is a Moore State Machine.

<Memory>

1. DRAM



2. SRAM



<Adders>

1. Size Table

	8bits	16 bits	32 bits	64bits
Ripple Carry	40	80	160	320
Prefix Adder	68	160	304	704

2. Time Table

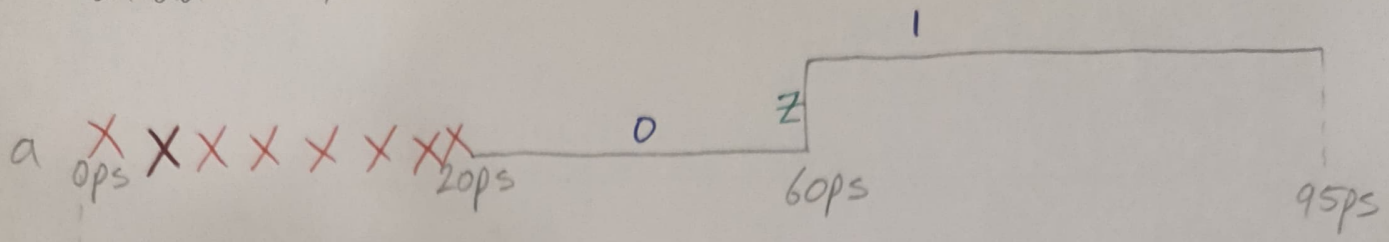
$t_{ripple} = N t_{FA}$

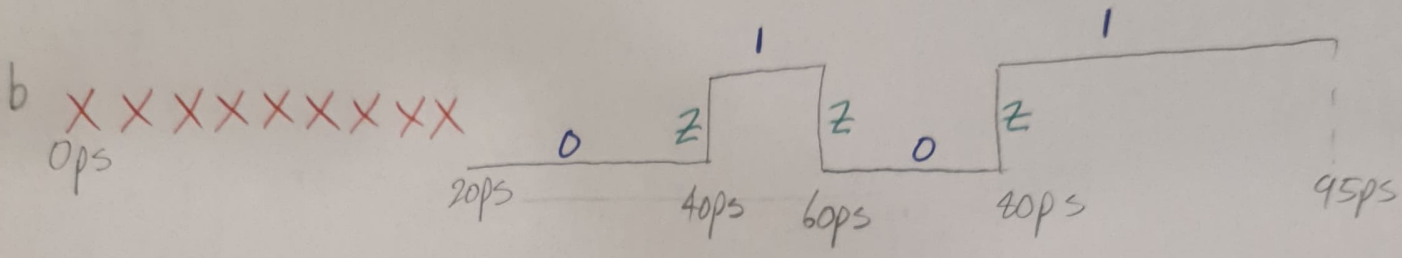
$t_{PA} = t_{pg} + \log_2 N(t_{pg\_prefix}) + t_{XOR}$

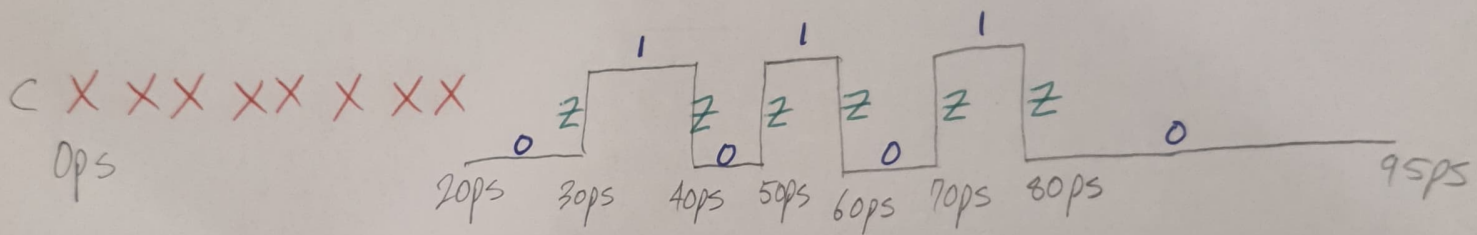
($t_{FA} = 500ps$, $t_{pg} = 100ps$, $t_{XOR} = 100ps$, $t_{pg\_prefix} = 200ps$)

	8bits	16bits	32bits	64bits
Ripple Carry	4000	8000	16000	32000
Prefix Adder	800	1000	1200	1400

<Validation>


a
0ps
20ps
60ps
95ps
1
Z
0


b
0ps
20ps
40ps
60ps
80ps
95ps
1
Z
0


c
0ps
20ps
30ps
40ps
50ps
60ps
70ps
80ps
95ps
1
Z
0