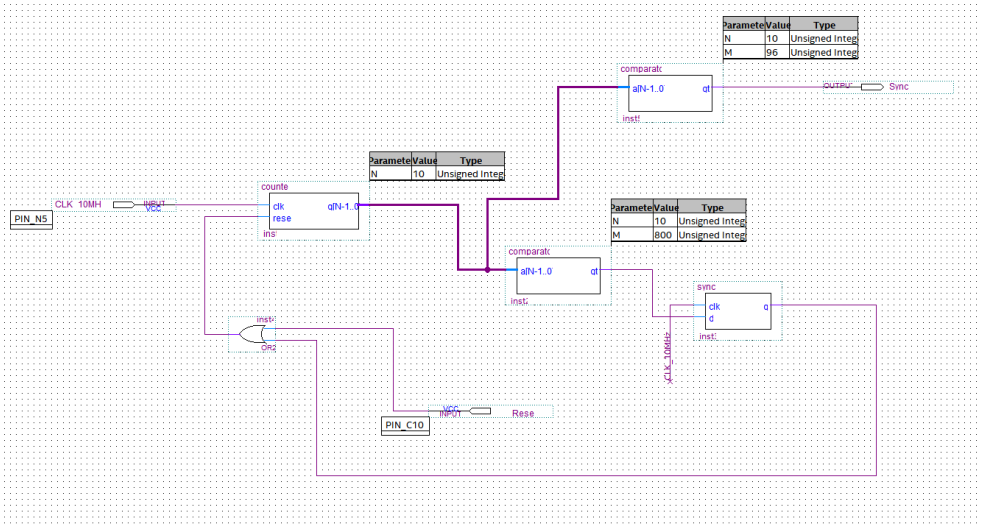
Create and simulate a module that generates a signal that is logic LOW for 96 continuous cycles of an arbitrary clock, and Logic HIGH for 704 continuous cycles of the same clock.

This makes for a total of 800 cycles per period.

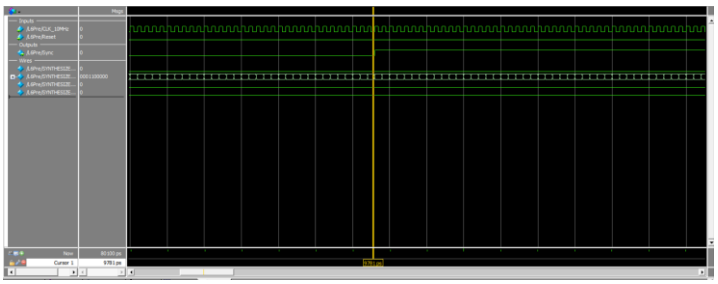
Pg 37 of the DE10-Lite manual has information about the timing of this signal.

Submit a screenshot of the module you created and it's Modelsim simulation.

<Module created>



<Modelsim Simulation>



```
# Reading pref.tcl
# Loading project ECE272L6Pre
# Compile of comparator.sv was successful.
# Compile of counter.sv was successful.
# Compile of L6Pre.v was successful.
# Compile of parser.sv was successful.
# Compile of sevenseg.sv was successful.
# Compile of sync.sv was successful.
# 6 compiles, 0 failed with no errors.
ModelSim> vsim -gui work.comparator work.counter work.L6Pre work.parser work.sevenseg work.sync
VSIM 2> add wave *
add wave -position end sim:/L6Pre/*
force -freeze sim:/L6Pre/CLK_10MHz 1 0, 0 {50 ps} -r 100
VSIM 5> force Reset 1
VSIM 6> run 100
VSIM 7> force Reset 0
VSIM 8> run 80000

VSIM 9>
```

(Note: The clock period is 100ps.**)**