# RICHARD LOURETTE

**Principal Payload Architect | Principal Embedded Computing Systems Design Engineer**

📧 rlourette@gmail.com | 📱 585.953.5309 | 📍 Fairport, New York | Remote Ready
🔒 **U.S. Citizen | Previously held DoD Top Secret/SCI Clearance**

## PROFESSIONAL SUMMARY

Principal Payload Architect and Embedded Computing Systems Design Engineer with 30+ years of experience developing high-reliability aerospace computing systems and spacecraft payload architectures. Expert in FPGA/SoC architecture, high-performance embedded computing, radiation-hardened embedded systems, and real-time software development for mission-critical applications. Proven track record delivering spacecraft payload systems, GPS-III satellite test equipment, and distributed high-performance processing architectures for defense and aerospace programs. Deep expertise in payload system integration, hardware-software co-design, system requirements decomposition, and multi-disciplinary embedded systems architecture.

**Core Competencies:** Payload Architecture | High-Performance Embedded Computing | Computer Architecture | Software Architecture | FPGA/SoC Design | Fault-Tolerant Systems | Radiation-Hardened Systems | Real-Time Embedded Software | Aerospace Computing | System Requirements Analysis | Hardware-Software Integration

## TECHNICAL EXPERTISE

**Computing Architectures:** High-Performance Embedded Computing, FPGA/SoC Design, ARM Cortex-A/M/R, TI ARM A9, Heterogeneous CPU/FPGA Systems, VPX Computing Clusters
**Embedded Platforms:** Radiation-Hardened MCUs, Bare Metal Programming, RTEMs RTOS, FreeRTOS, Embedded Linux
**Communication Interfaces:** SpaceWire, SpaceFibre, PCIe, DDR Memory Systems, High-Speed Downlinks, UART, RS-422/RS-485, Ethernet, I2C, SPI, CAN Bus
**Programming Languages:** C/C++ (30+ years), Python, Assembly Language, VHDL/Verilog
**Development Tools:** FPGA Architecture Definition, GCC Toolchain, JTAG Debuggers, Oscilloscopes, Logic Analyzers, Protocol Analyzers, Spectrum Analyzers
**Aerospace Standards:** NASA Core Flight System (cFS), CCSDS C&DH, DO-178C, Space-Qualified Development, Radiation Mitigation Techniques, Fault-Tolerant Design
**System Design:** Payload Architecture, Software Architecture, Requirements Decomposition, Architecture Definition, Trade Studies, Hardware-in-the-Loop Testing

## PROFESSIONAL EXPERIENCE

### RL TECH SOLUTIONS LLC | President & Chief Technology Officer

**October 2022 – Present | Rochester, NY**

**D3 Engineering/L3Harris Aerospace – Chief Engineer Consultant***October 2022 – December 2023*

* **Spacecraft Payload Architecture:** Architected complex spacecraft payload systems integrating 5 radiation-hardened MCUs via SpaceWire/SpaceFibre communication for distributed high-performance embedded computing applications
* **High-Performance Embedded Computing:** Designed heterogeneous CPU/FPGA computing architectures running NASA Core Flight System (cFS) framework on RTEMs RTOS for onboard processing
* **CCSDS C&DH Systems:** Implemented CCSDS Command & Data Handling protocols and high-speed downlink architectures for spacecraft payload data processing
* **Software Architecture:** Implemented microservices architecture with fault-tolerant design principles for enhanced reliability and maintainability in space environments
* **Requirements Analysis:** Decomposed high-level satellite system requirements into detailed hardware, software, and firmware specifications
* **Radiation Hardening:** Implemented error correction codes, redundancy schemes, and radiation mitigation techniques for space-qualified embedded systems
* **Business Impact:** Contributed to winning $50M+ aerospace contract through technical architecture presentation and system design including multi-Terrabyte data recorder architecture for mission data management

**Topcon Positioning Systems – Senior Embedded Software Consultant***October 2023 – April 2025*

* **Embedded Computing Systems:** Architected high-performance Linux C++ subsystems for GNSS receivers using embedded ARM A9 TI processors
* **Memory Systems:** Optimized DDR memory interfaces and high-speed data processing for resource-constrained embedded devices
* **Performance Analysis:** Achieved 40% performance improvement through systematic CPU profiling and bandwidth optimization

### PANASONIC INDUSTRIAL IOT DIVISION | Engineering Group Manager

**February 2021 – October 2022 | Rochester, NY**

* **Multi-Disciplinary Leadership:** Managed cross-functional teams spanning RF Engineering, FPGA design, antenna development, and embedded firmware
* **System Architecture:** Directed development of industrial IoT computing platforms with integrated communication interfaces
* **Communication Protocols:** Resolved critical RF protocol issues for 2000+ device enterprise deployment
* **Test Methodology:** Transformed manual testing processes to automated frameworks, reducing test cycles from weeks to 3 days

### L3HARRIS GEOSPATIAL SYSTEMS | Chief Scientist/Principal Investigator

**May 2002 – September 2015 | Rochester, NY**

* **GPS-III Program:** Served as lead architect for GPS-III satellite program test equipment, defining system requirements and FPGA-based hardware architecture
* **High-Performance Embedded Computing:** Principal Investigator for onboard payload processing electronics for Wide Area Airborne Surveillance (WAAS) systems
* **VPX Supercomputing:** Led development of 7-slot high-altitude VPX supercomputing cluster for Advanced Geospatial Processing applications
* **Space Payload Systems:** Architected electronic payload systems for visual and infrared sensor platforms with radiation-hardened components
* **Algorithm Development:** Developed advanced wavefront correction algorithms using Python for space-based optical systems

### TOKENIZE INC. | Vice President of Engineering

**September 2015 – February 2021 | Rochester, NY**

* **Ultra-Low Power Design:** Designed embedded electronics meeting strict battery life requirements for wearable applications
* **Hardware-Software Integration:** Collaborated with hardware teams on power optimization and communication interface design
* **System Validation:** Led hardware bring-up activities using embedded test software, oscilloscopes, logic analyzers, spectrum analyzers, and lab instrumentation

### EASTMAN KODAK COMPANY | Chief Firmware Architect

**1995 – 2002 | Rochester, NY**

* **Embedded Architecture:** Led international firmware development teams for hybrid consumer digital camera products
* **Communication Protocols:** Co-architected USB device drivers and PIMA 15740 application layer protocol implementation
* **Memory Systems:** Designed application frameworks for memory-constrained embedded systems
* **Real-Time Processing:** Developed real-time image processing algorithms and calibration systems for laser marking engines

## KEY ACHIEVEMENTS

### Aerospace & Defense Systems

* **Spacecraft Payload Architecture:** Designed distributed satellite payload processing systems with radiation-hardened MCUs
* **Contract Success:** Contributed to winning $50M+ aerospace contract through technical leadership
* **GPS-III Program:** Led system architecture for satellite test equipment using FPGA-based designs
* **High-Performance Computing:** Developed VPX supercomputing clusters for high-altitude aerospace applications

### System Performance & Innovation

* **Performance Optimization:** Achieved 40% performance improvements through systematic architecture analysis
* **Software Architecture:** Designed scalable, fault-tolerant software architectures for mission-critical aerospace applications
* **Process Innovation:** Reduced testing cycles from weeks to days through automated methodologies
* **Technology Leadership:** Led adoption of emerging computing architectures across multiple aerospace programs
* **Patent Portfolio:** 20+ issued US patents in embedded systems, signal processing, and computer architecture

### Team Leadership & Collaboration

* **Multi-Disciplinary Teams:** Successfully managed 13+ engineers across firmware, hardware, FPGA, and RF disciplines
* **Requirements Management:** Led decomposition of complex system requirements into actionable hardware/software specifications
* **Technical Reviews:** Conducted architecture reviews and design validation for mission-critical aerospace systems

## EDUCATION

**Bachelor of Science in Electrical Engineering**
University of Dayton | Dayton, Ohio

## SECURITY CLEARANCES

* **Previously held DoD Top Secret Clearance with SCI Access**
* **Completed Single Scope Background Investigation (SSBI)**
* **Available for security clearance reinstatement**
* **U.S. Citizen**

## ADDITIONAL QUALIFICATIONS

* **Aerospace Experience:** 20+ years in space systems, satellite programs, payload architecture, CCSDS C&DH systems, and defense applications
* **FPGA System Architecture:** Extensive experience architecting FPGA-based systems including Rad Tolerant Versal for space applications, with team leadership for implementation
* **Radiation Hardening:** Deep knowledge of space-qualified components and radiation mitigation techniques
* **System Integration:** Proven success in hardware-software integration and multi-disciplinary system design
* **High-Performance Computing:** Expertise in VPX computing clusters and distributed processing architectures
* **Space Communications:** Experience with CCSDS standards, high-speed downlinks, and spacecraft data handling systems
* **Remote Collaboration:** 5+ years of successful remote work with distributed aerospace development teams