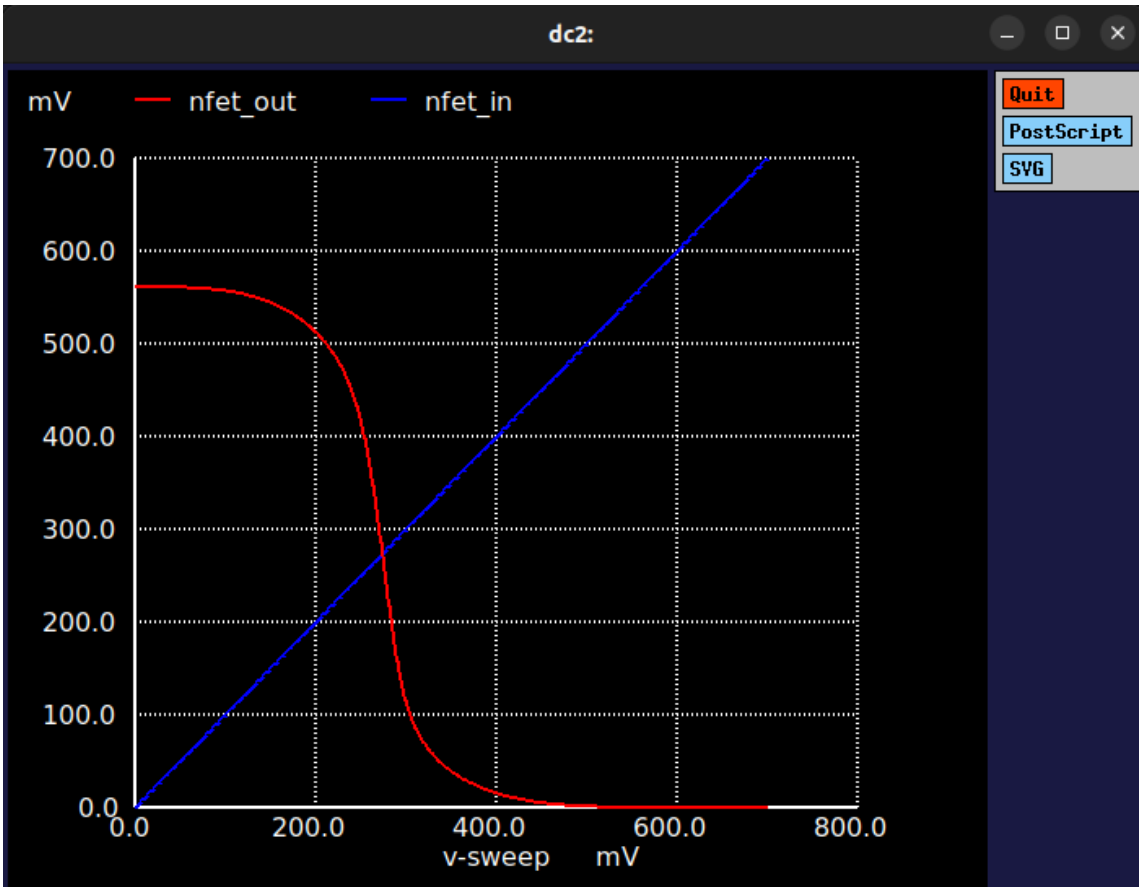
Module 2 Assignment

7nm FinFET Device and Inverter Characteristics

-> For my username (rlvsk) the ASCII sum in V is 0.562.

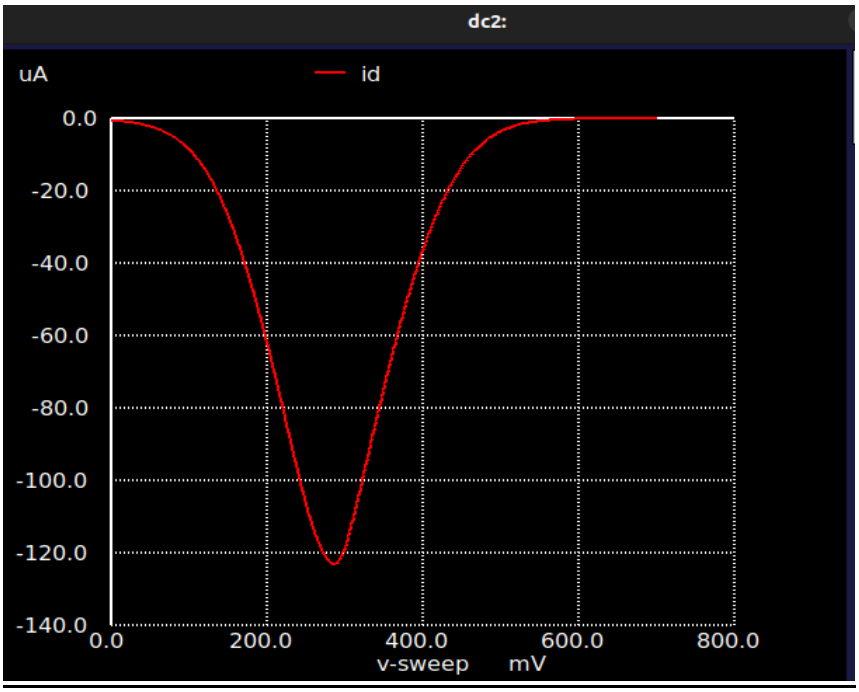
-> So I have taken the voltage of V2 as 0.562 V.

1. VTC Curve

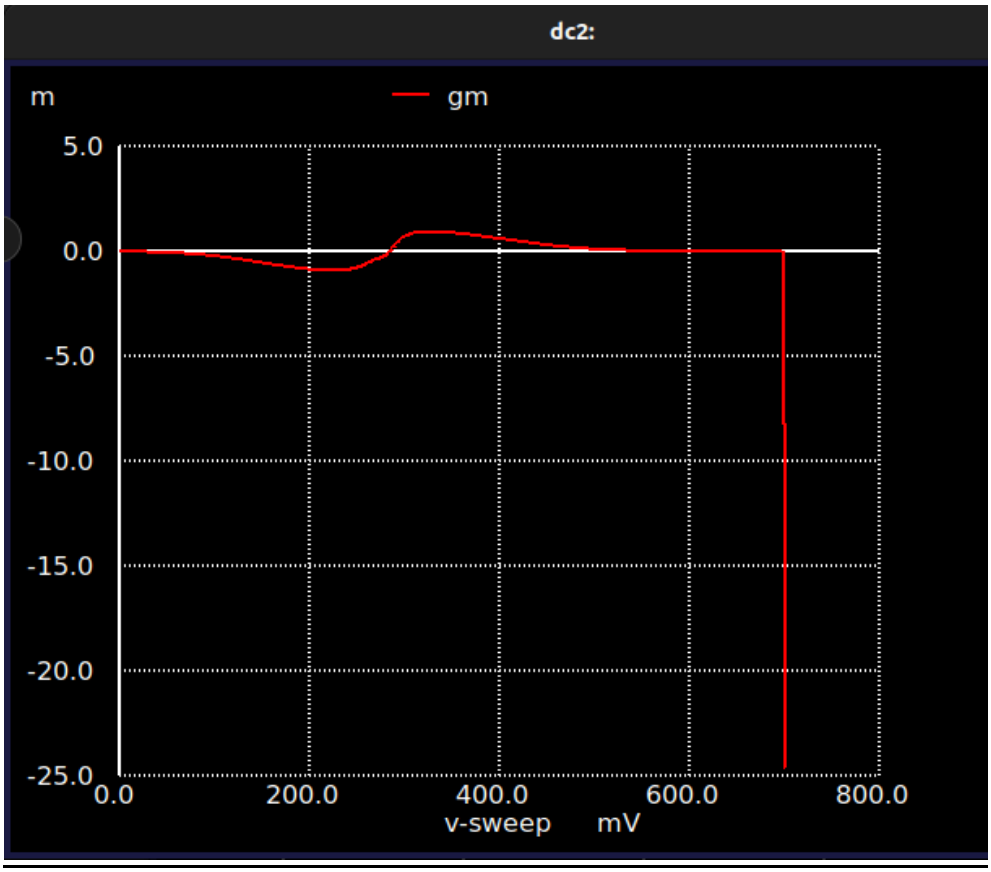


- **This curve shows the relation between the input and output voltage of the inverter.**
- **Vth – is the point where both the curves intersect.**
- **Vth = 0.273 V**

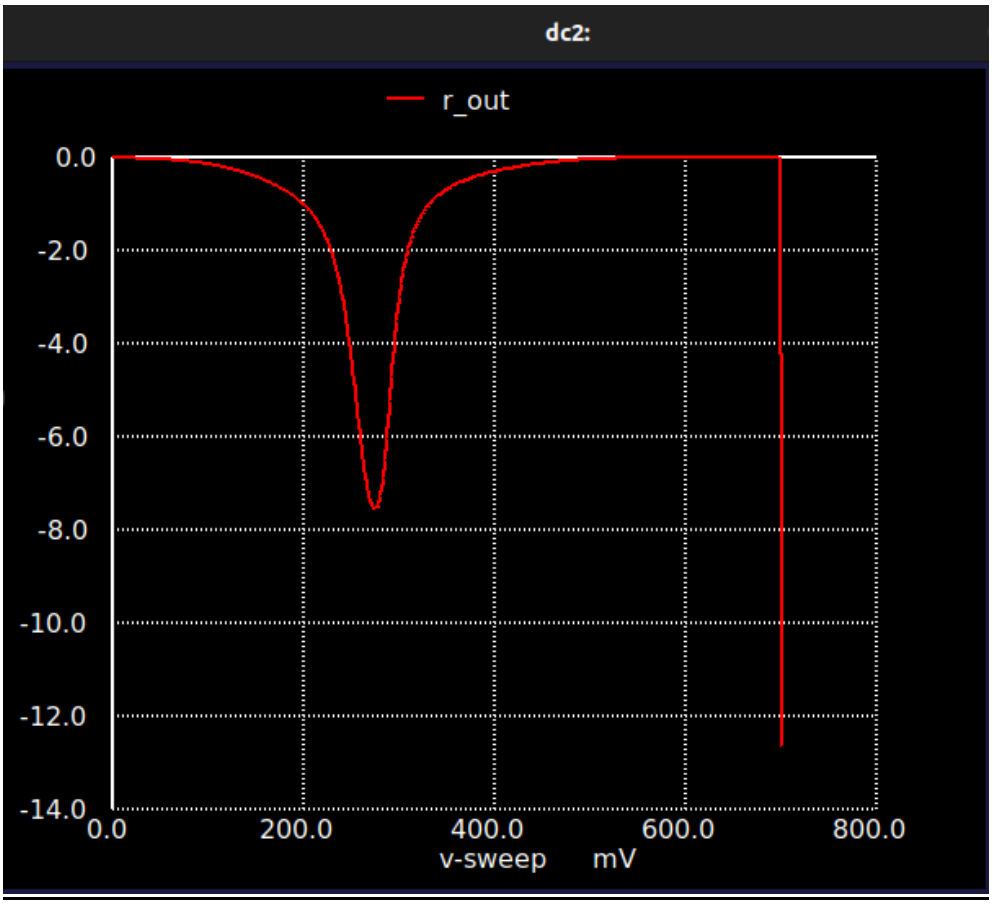
2. Drain Current (Id) = 123.083uA



3. Transconductance (gm)



4. Output Resistance (r_out)



5. Max Gain, Noise Margin & Transconductance

```
No. of Data Rows : 701
v_th                =  2.735608e-01
max_gain            =  7.542514e+00 at=  2.760000e-01
vil                 =  2.755041e-01
voh                 =  2.589595e-01
vih                 =  2.774596e-01
vol                 =  2.442102e-01
v_th = 2.735608e-01
max_gain = 7.542514e+00
vil = 2.755041e-01
voh = 2.589595e-01
vih = 2.774596e-01
vol = 2.442102e-01
nmh = -1.85001e-02
nml = 3.129390e-02
gm_max              =  9.319728e-04 at=  3.270000e-01
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
```

6. Power Consumption and Propagation Delay

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Initial Transient Solution
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Node                                   Voltage
----                                   -------
nfet_out                              0.561735
nfet_in                                      0
vdd                                      0.562
v2#branch                          -5.37516e-07
v1#branch                           7.70734e-12

 Reference value :  0.00000e+00
No. of Data Rows : 120
tpr                =  2.500000e-11
tpf                =  2.443827e-11
id_pwr             =  -6.96304e-16 from=  2.00000e-11 to=  6.00000e-11
tpr = 2.500000e-11
tpf = 2.443827e-11
tp = 2.471913e-11
id_pwr = -6.96304e-16
pwr = -3.91323e-16
power = 9.783070e-06
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver
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7. Frequency

```
Initial Transient Solution
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Node                                   Voltage
----                                   -------
nfet_out                              0.561735
nfet_in                                      0
vdd                                      0.562
v2#branch                          -5.37516e-07
v1#branch                           7.70734e-12


No. of Data Rows : 71
tr                 =  2.080000e-11
tf                 =  2.318204e-11
t_delay = 4.398204e-11
f = 2.273655e+10
```

Characteristic Table:

S.No	W/L (PMOS)	W/L (NMOS)	Vth (V)	Id (uA)	P (W)	tpd (ps)	Av	f (Hz)
1	2.00	2.00	0.2735608	123.083	9.78307E-06	2.47191E-11	7.572514	22736550000
2	1.00	1.85	0.2454671	82.35	6.70E-06	2.45E-11	7.730707	2.28E+10
3	1.85	1	0.3020096	80	6.71E-06	2.50E-11	7.494735	2.26E+10

Observations:

Effect of Increasing NMOS width

- **Strengthens the channel conduction, leading to larger discharge current.**
- **Output node pulls down quicker, resulting in shorter falling delay.**
- **Switching occurs sooner as the effective threshold voltage moves slightly lower.**

Effect of Increasing PMOS wodth

- **Improves the ability to charge the output node, causing higher charging current.**
- **Output rises faster, giving smaller rising delay.**
- **Devices switches later as the threshold point shifts upwards.**
- **Overall power usage becomes greater due to increases current flow.**

Balances PMOS and NMOS Sizing

- **Pull-up and pull-down paths show similar driving capability.**
- **The inverter toggles close to half of the supply voltage (VDD/2).**
- **Rise and fall delays become almost equal.**
- **Provides a good compromise between performance and power efficiency.**