K7 heaven

Can AMD really bite into Intel's massive market share? The company's new chip, the Athlon, might have the teeth for it, writes Ian Robson.

AMD renamed its eagerly awaited seventh-generation K7 processor at the end of June: it's now called the Athlon. Much has been made of the Athlon's new architecture, specifically the new x87 co-processor, with pre-release comparisons claiming overall speed increases of almost 40 percent over equally clocked Pentium IIIs.

Efforts to improve system performances have been focused on multimedia processing for some time now, with optimising instruction sets and the beginnings of architectural changes with the Pentium-class processors. Never before has the hardware solution been so radically improved as with the Athlon.

These processors are first destined for high-end PCs, taking over from the K6-III and with initial clock frequencies of 500, 550 and 600MHz. Once Athlon's presence is established, AMD plans to invade Intel's most successful market areas, from the Celeron-soaked Value PCs right up to the Pentium III Xeon server market.

History has shown that faster processors consume more power. This in turn generates a copious amount of heat that requires extensive cooling techniques. One method to combat this is to reduce the distances electrons have to travel between the processor's transistors. With GigaFlops of data transferred as electrons, this equates to lower power consumption and lower core voltage requirements, resulting in less heat.

▼AMD logo aside, the K7 looks just like a Pentium II

As with the current Pentium III CPUs, initial Athlon releases will be based on a 0.25 micron production process . Both Intel and AMD plan to produce 0.18 micron desktop releases in the second half of 1999, although AMD is likely to be the first with its 750MHz Athlon release.

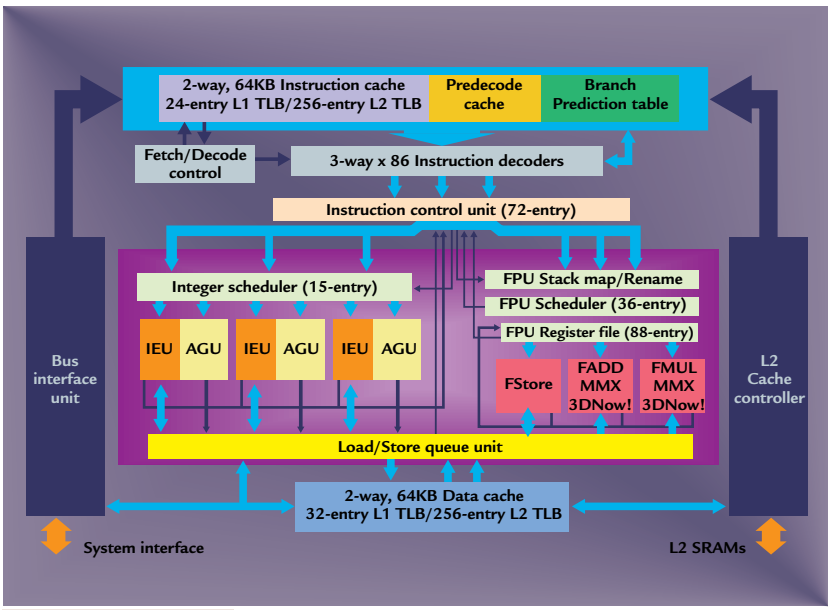
All Athlons will include the enhanced 3DNow! (with the addition of 19 integer instructions) Single Instruction Multiple Data (SIMD) instruction sets. SIMD carries out repetitive tasks such as adding, multiplying, subtracting and loading by using a single instruction to process multiple data packets, while at the same time advancing graphics throughput and processing.

Key parts of the Athlon are already etched at 0.12 micron, with AMD's fabrication plant in Dresden preparing for the next innovation — the production of 0.1 micron production processors. However, AMD wasn't satisfied with mere clock frequency increases, and decided to redesign key processor components to alleviate the pressure on the core processor with far more efficient pre-processing of data.

Also, the interface between the processor and the system bus has been redesigned to accommodate increases in required data bandwidths, ensuring that the processor's newly acquired skills are kept busy.

The processor

Externally, the Athlon is virtually identical to the Pentium II Single Edge Contact package, making it easy to create the same form factor parts and boards. This allowed for a subsequent faster time-to-market. However, rather than using Intel's Slot 1 P6 bus protocol, GTL+, the Athlon uses Digital's Alpha bus protocol EV6. Known as Slot A, the new design will feature different pin-outs and electrical signals from Intel's Slot 1 line.



▲ **Inside the Athlon. The three floating point units make it unlike any other x86 CPU**

Processor cache enhancements begin with the on-chip Level 1 capacity doubled from the K6-III's 64Kb to 128Kb, split equally between two-way accessed data cache and instruction cache giving the CPU rapid access to a generous store of the most frequently used data.

The prefetching functionality of the Level 1 cache is working with data-hungry SIMD instruction types like 3DNow!, or Streaming SIMD Extensions (SSE) for the Pentium III. Prefetching 120 (or more) instructions may occur before the data needs one, and the increased cache capacities reduce Level 1 cache misses. In other words, there is more room to store the prefetched data and instructions.

It can also be said that the increased Level 1 cache combats a previous AMD failing in that 3DNow! registers (8 x 64-bit) are two times smaller than the SSE registers (8 x 128-bit), requiring many more data loads to and from the registers: this is where a larger Level 1 cache can assist. The instruction cache presents its pre-decoded information via a 2048-entry branch prediction table.

Level 2 cache using normal as well as Double Data Rate SRAMs will range from 512Kb one-third core-speed for the consumer market, to 8Mb back-side (full core speed) for the server market. A 'programmable' 64-bit Level 2 cache controller will determine the speed and capacity support, although AMD will lock this at the manufacturing stage.

If the EV6 bus can supply the Athlon's Level 1 and 2 cache with enough data, the bandwidth problem will pass on to the processor's decode and dispatch logic. Here, AMD has taken two major steps.

Instead of taming those wild CISC instructions into well-behaved RISC-like instructions, three parallel instruction decoders break down the x86 (or IA-32) instructions into slightly more complex macro-ops. These are then sent via one of two decoding pipelines, the DirectPath and the VectorPath.

Both x87 data paths are fully pipelined for double precision compared to only one x87 data path available to the Pentium III, which is not fully pipelined. By optimising the data format to an improved hardware, more efficient number crunching will result in lower processing-cycle counts. So, end-users will see noticeable speed increases to any execution dependent on co-processing, which in this day and age is just about everything.

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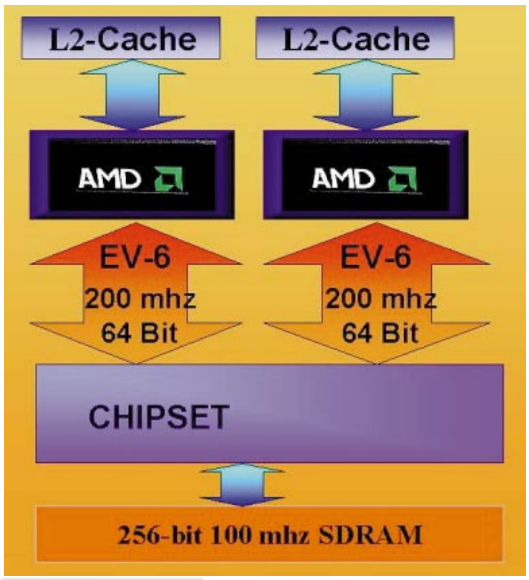
Three Superscalar, Out-of-Order Integer Pipelines start the DirectPath with common x86 instructions from 1-15 bytes in length, put through the Integer Scheduler for decoding in one of three x87 Integer Execution Units (IEUs) and the Address Generation Units (AGUs).

The VectorPath decodes uncommon, complex x86 instructions via three fully pipelined Floating Point Units (FPUs), one for additions and subtractions (FADD MMX 3DNow!),

another for multiplication and complex operations (FMUL MMX 3DNow!), and another for loading and special instructions (FStore) such as MMX and trigonometric calculations. The Pentium III has only two FPUs, one of which is only partially pipelined, so a multiplication must be immediately followed by an addition in order to reach its peak performance.

With the Althon operating each FPU independently, and in parallel, a theoretical maximum throughput should be roughly twice that of an equally clocked Pentium III. In fact, for x87 instruction, double precision dictates that a PIII cycles the instruction through the pipe twice, meaning that the Athlon has four times the peak execution rate.

The macro-ops are heavily buffered throughout the decode, reservation and dispatch (Load/Store Queue unit) process to avoid stalls. One thing that differentiates the Athlon from essentially any other x86 processor is its deep buffers, that help sustain the bandwidth needed to uncover all the work that's available in auto-decode.



▲Adding a second processor to the EV6 bus doesn't degrade the throughput of the first processor

This departure from P6 core architecture, specifically the FPUs, allows for new application optimisation, hopefully through a simple CPU patch, although this could be difficult. The Athlon maintains the x86 instruction microcode backward-compatibility, but current compilers will only create machine code that looks for two FPUs since, until now, no x86 processors had more.

The supporting architecture

Initial core logic will consist of AMD's AGP4x-supporting 'Irongate' Northbridge, with VIA, ALi and SiS variations to follow. However, full optimisation of AGP4x 1.1Gb/sec maximum bandwidth can't be realised with standard PC100 SDRAM's maximum 800Mb/sec bandwidth, and PC133 SDRAM still falls short at 1.06Gb/sec. The same limitations apply to current Pentium III systems, although when front-side bus speeds increase to 133MHz in September, it's likely that Intel will opt for RAMBUS memory architecture.

RAMBUS will run at very high frequencies, up to 800MHz, but a small 16-bit bus means that bandwidth, although sufficient, is limited to a maximum of 1.6Gb/sec. This will be sufficient support for optimised use of Intel's AGP4x-enhanced Camino 820 chipset.

Althon's core logic will initially be designed to support the mass-marketed PC100 memory, but will soon feature support for RDRAM modules on a RAMBUS architecture. However, RDRAM has very high latencies: it wastes a lot of clock cycles while the memory prepares itself for an access.

Another likely solution is DDR-SDRAM (Double Data Rate Access Memory). Working at only100MHz, DDR-SDRAM delivers data at the rising and the falling edge of the clock, so the memory bus performs as if running at 200MHz, similar in principal to AGP2x. It can therefore offer the same 1.6Gb/sec bandwidth as RAMBUS but with lower latencies, and using PC133 will increase this to 2.1Gb/sec.

Athlon's more aggressive superscalar design puts heavy demands on bus bandwidth. Thus AMD uses a 200MHz Alpha EV6-compatible system bus interface — also used by the Alpha 21264 CPU — licensed from DEC, now majority owned by Samsung and partially by Compaq.

The EV6-bus is not the bus connected to the memory but, in fact, just a fat pipe connected to the chipset. The chipset has different pipes to all the other buses, including main memory, PCI, and AGP. In an Intel Slot 1 system, the same local I/O bus must handle the I/O requests of the CPU, main memory, AGP, and PCI bus. But an Althon system has its own private pipe to the chipset.

Now AMD can offer different memory solutions by changing the supporting chipset. Apart from impressive single processor performance, its point to point (PTP) topology offers scalable multiprocessing. PTP means that each processor gets its own dedicated connection to the rest of the bus, removing the performance bottlenecks associated with x86 multiprocessor configurations. Adding a second CPU to an EV6 system doesn't degrade throughput to the first CPU, as it uses an independent connection.

Besides increasing performance, this type of interconnect also increases the overall scalability of a system and the speed at which its bus can operate. Sixteen processor configurations are possible, compared to the maximum four-CPU configuration with the Pentium III Xeon.

However, even though each processor gets a dedicated connection to the chipset, it shares a system bus from the chipset to main memory.

AMD's vision to be a serious rival to Intel could be a reality with the K7. Claims of performance improvements over equally clocked Pentium III processors may even be reserved on AMD's part, with our initial tests blowing Intel out of the water.

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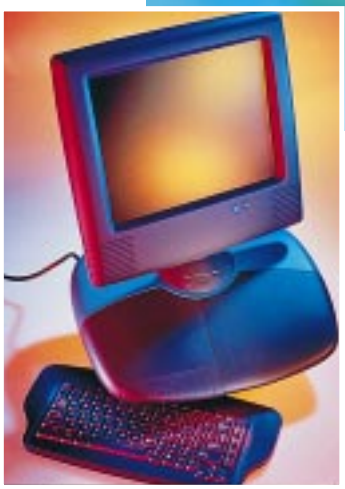
Intel **futures**

CAN INTEL'S SUCCESS STORY GO ON INTO THE NEXT MILLENNIUM, ASKS JOHN WEBSTER.



◂▲CONCEPT PCS FROM INTEL'S RESEARCH & DEVELOPMENT LAB

Only a decade ago, the thought of a computer microchip manufacturer transforming its product into a status symbol to rival such leading international brand names as Coca-Cola and Nike would have been laughable. And yet hardly a day goes by that Intel's brilliant Intel Inside marketing campaign doesn't appear on our television screens, or scream at us from computer and even glossy magazines. And it's a fiendishly clever campaign, to boot.

It's this mixture of marketing nous, coupled with brilliant business alliances with the likes of Microsoft — hence the name WinTel — and sharp technology, that has enabled Intel to reap rewards beyond the wildest dreams of King Midas; even if the corporation has had to pay out billions in marketing and R&D costs for the privilege.

Intel's competitors can only look on and weep. They must have a heart attack every time the market research statistics roll in: today Intel makes 90 percent of the planet's PC microprocessors. The corporation is now worth a staggering $115 billion, which makes it even more valuable than IBM. In 1997 Intel declared $5.1 billion in annual profits, and transformed itself into the seventh most profitable company in the world. Its revenues for the last financial year were, we've just discovered, a crushing $27,375 million.

But as we enter a new millennium, can this spectacular growth last? Already, new kids on the block are encroaching upon Intel's microprocessor monopoly market [*see pp122-124*].

I asked company hot-shot Sean Maloney about the competition. Sean is a Senior Vice President of Intel Corporation and Director of the Sales and Marketing Group: is he worried by upstarts like Cyrix and AMD? 'Intel's questioning nature continually projects and plans for living in a competitive world, and that means planning for the worst,' says Sean. 'I get very uncomfortable if people start assuming that the competition isn't going to execute. My colleagues and I always assume the nightmare doomsday scenario — that the competition will hit every single milestone — and then we plan accordingly.'

As a Sales and Marketing Director, does he see the split between budget processors and genuine workstations, and the opportunities that will open up as a result? 'We wish, and indeed, need, to embrace every market,' says Sean emphatically. 'We see budget processors as a big opportunity, one which can be developed alongside your typical workstations. Intel won't allow itself to be fettered in its approach to one or the other. So we have people in the company energetically pursuing both markets.'

But what is Intel going to do in response to Athlon, formerly known as K7? 'As I've indicated, we always keep up with the competition, and as far as K7 is concerned we'll just have to improve the power of our microprocessors that are required by businesses and consumers and are desirable. We're confident we have the answers.

'You'll be interested to hear that we're just about to roll out a whole new 64-bit architecture, and there are some big-time announcements in the offing concerning the desktop arena as well. The competition ought to be concerned because

Chipping in

we have some truly wonderful product lines just around the corner. You'll have to watch this space to find out what they are!'

In the meantime, would Intel ever bring its release dates forward or drop prices to take the wind out of its competitor's sails? Sean looks a little askance at such a pragmatic if cut-throat suggestion. 'We wouldn't drop prices in order to take the wind, as you say. We might drop prices to win business in a competitive situation. As regards bringing forward release dates, we might well consider doing so; but not as a knee-jerk reaction: we'd be concerned not to compromise quality.'

▲ Intel senior vice-president Sean Maloney: Ready to take on the competition

With AMD developing the 3DNow! instructions, isn't the market going to get split, with developers having to develop multiple versions of the same product, which they would rather not do? 'It's really not up to the developer to decide how big the base is going to be,' says Sean. 'We believe we have unparalleled Research & Development in microprocessors. We're making them better and better, and we think the developers will go our way.'

The subject of the internet is clearly very close to Sean's heart. He needs little prompting to divulge Intel's policy as encouraging small businesses to take e-commerce more seriously. 'Intel goes along to events like Internet World and tells people what we're doing. We don't want to be patronising because these are big challenges for small businesses, but there again, we know that many businesses are already implementing our new ideas. More than anything else, what we are into as a company is sharing our experiences.'

Intel has a big drive on at the moment to encourage the benefits of networking, one of which is based on, according to Sean, 'common-sense. We're hopefully going to reach our goals in this arena by reducing the cost of, and striving for greater simplicity, in networking products. Whether in the home or in the very small business, users need to understand the benefits of networking in sharing a printer, files or an internet connection. Intel is working on exciting home networking technologies such as wireless and phone-line networking, which amply demonstrates that we recognise the key need of this group of users for a "no new wires" approach.'

The challenge of networking is something that Intel as a corporation clearly takes very seriously indeed. So much so that the company has started up its very own Network Communications Group. Current and future product developments will be designated to match up with the requirements of the various user segments which fall into the broad market bands of home, small business, small to medium enterprise, and enterprise/carrier.

'In the small business, the initial challenge is to simply get connected. Evidence from the United States suggests small businesses that take advantage of networking technology are more productive than those that simply rely on standalone PCs. Europe, and especially the UK, needs to catch up.

'So in order to provide networking solutions that are easy to install and manage, Intel developed the InBusiness line specifically with the small business in mind. And it's a nifty piece of technology, if I say so myself,' he says, smiling broadly. 'For example, based on market research, InBusiness hubs and switches feature our on/off switches — not something that an IT manager in a large corporation would find useful, but the ability to turn off equipment before leaving is important in many small offices. It's no longer a case of one size fits all.'

One of the most important 'building blocks' for the next generation of computers is Intel's Easy PC Initiative. Developed jointly with Microsoft, the initiative focuses on delivering PCs that are simple to set up, easy to expand, instantly available, smaller and quieter. According to Sean, 'Easy PC has benefits for everyone. It will help reach first-time PC consumers overcoming usability barriers, while making peripherals and software easier to install. PC users will have a more rewarding and productive out-of-the-box experience, and, correspondingly, the costs of PC ownership and support will be reduced.'

And if the Easy PC initiative still cannot persuade your more techno-illiterate friends and relations to get computer-savvy and enter the 21st century, then you could always do to them what happens to Homer Simpson in the latest Intel ad. Homer undergoes surgery to replace the world's most inferior brain with an Intel processor. Now, I wonder if that's what Intel has really got up its sleeve for us all? ❐