CELL ONE **The development of a fast, small-scale memory cell could mean doom for DRAM.**

Cell of the century

A recent joint announcement by Hitachi Semiconductors and the Cavendish Laboratory at Cambridge University could mean an end to hard-disk crashes. It could also mean an end to hard disks and other forms of rotating storage. Phase-state Low Electron (hole)-number Drive Memory, or PLEDM, is a high-density memory technology promising multi-gigabit memory chips that could not only revolutionise conventional Dynamic RAM (DRAM) but also supersede Flash Memory and hence conventional storage media as well.

Scientists at Hitachi and Cambridge University have developed a new type of cell structure to overcome DRAM's difficulty in building in smaller geometries: the new PLEDM cell replaces the capacitor with a second, 'stacked' transistor to make a 'gain cell' in a smaller area: a memory cell that amplifies a small storage charge. Current through the vertical transistor charges the gate of the larger transistor, creating a cell the size of a single transistor but with both storage and signal gain. This configuration should allow a chip to store twice as much data in the same area as a DRAM built using the same process technology.

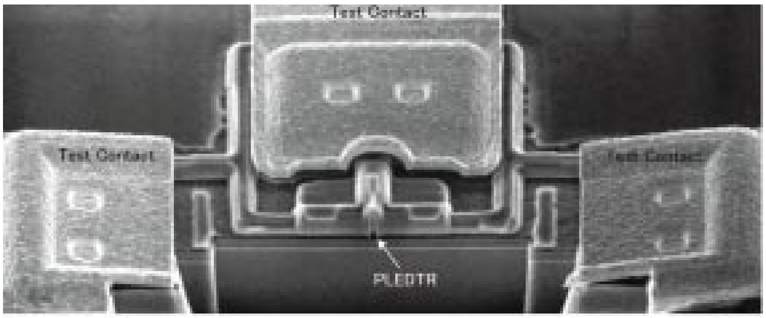
The key to the PLEDM cell lies in the unique characteristics of the upper transistor. This device, resembling an MOS transistor, is constructed vertically, with the source on top and drain on the bottom. The polysilicon gate is a layer wrapped around the outside of the device.

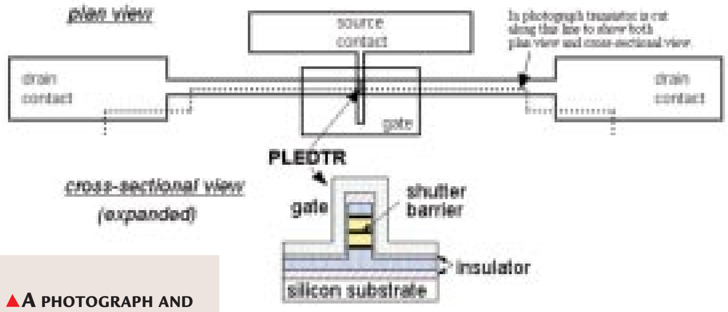
PLEDM could be used as a hard-disk substitute, enabling large quantities of CHEAP, FAST, NON-VOLATILE STORAGE to be used in pocket devices

But the most unusual features are three barriers running across its channel region: the source barrier, shutter barrier and drain barrier, which block conventional current flow.

The potential at these barriers can be modulated by the side gate on the transistor. When the side gate lowers the potential at the middle, or shutter, barrier, a small tunnelling current flows through the device. This current is sufficient to quickly charge the gate of the larger MOS transistor on which the vertical device sits.

When the shutter barrier is on, it takes just one microamp to charge up the gate of the MOSFET, taking a nanosecond. When off, the barrier is tight and ensures long refresh times.





▲A PHOTOGRAPH AND FUNCTIONAL DIAGRAM OF THE PLEDM CELL

The researchers have said that only about 1000 electrons are involved in determining if current would flow through the large transistor. Simulations of a PLEDM cell built in a 0.2-micron silicon process show a read/write time of less than 10ns and refresh times of longer than one-tenth of a second.

PLEDM technology offers an ideal combination of lower power and faster read and write cycle times than DRAM, as well as scalability beyond the levels at which DRAM cells become problematic, and fabrication with existing tools and techniques. Unlike conventional RAMs, in which it becomes harder to store enough charge in the capacitor as the size of the cell decreases, the PLEDM cell is scalable and its performance should actually increase with smaller sizes.

PLEDM is fast, low power, and, says Hitachi, could be developed to retain memory even with the power switched off. This would allow it to be used as a hard-disk substitute, enabling large quantities of cheap, fast, non-volatile storage to be used in pocket devices.

Hitachi's European arm and the Cavendish Laboratory at Cambridge University hope to produce memory chips using the technology within a year and have it on the market in five.

ROGER GANN

CELL TWO **The QCA cell is a novel chip technology set to break all speed and size barriers.**

Quantum leap

Time is running out for silicon chips as we know them. Although rapid advances in manufacturing technology are bringing us smaller, faster, cheaper and more densely-packed chips, there's a fundamental physical limit looming. When we hit it, reckoned to be around 2020 or so, we'll need to turn to a quite different technology if computers are to continue to grow in speed and shrink in size. Recent research results are pointing to a novel computer technology that needs almost no power, operates at speeds we can only dream about today, and is incredibly small.

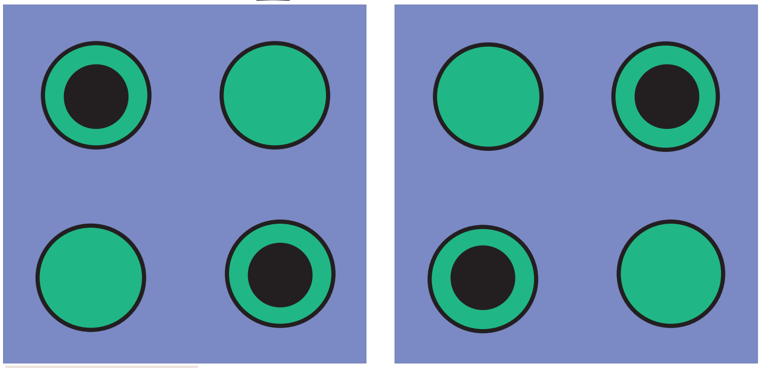
The new approach is dauntingly named quantum cellular automata, QCA for short, and it's implemented on a semiconductor chip using gallium arsenide technology. QCA's basic component is a cell which contains four quantum dots, arranged in a square pattern.

A quantum dot is a kind of artificial atom that provides a comfortable spot for a passing electron to rest in. During manufacture, two free electrons are inserted into the cell. The electrons can move around within the cell, but can't escape from it. Because they repel each other, the electrons try to get as far apart as possible, and end up sitting on diagonally-opposed quantum dots.

This leads to two possible configurations for the cell, as shown above. The quantum dots are the open circles, and the electrons the black dots. The two configurations can be used to stand for a binary 0 (left), and a 1 (right). Effectively, each cell is a memory element holding one bit. Incredibly, you can actually see an image of electrons in a quantum dot, at <www.belllabs.com/new/gallery/einaqd.html.

Something interesting happens when you place these cells very close together. Suppose we give the first cell on the left a tiny electrical nudge to set it to encode a 1, with its electrons sitting on the top-right and bottom-left dots. Although the electrons can't leave the first cell, their charges are felt by the electrons in the next cell along, which are repelled to its top-right and bottom-left dots. So, the second cell is now also a binary 1. As more cells are lined up, the same thing happens, like a collapsing line of dominos.

What you effectively get is a wire, where the state of the last cell in the wire is a copy of the state of the first cell. In this case, a 1 has been transmitted down the wire, but in contrast to a conventional wire, no current has actually flowed. You can experiment with a nice Java animation of this effect on Craig Lent's QCA pages at www.nd.edu/~qcahome.



▲1970s KITCHEN TILES? NO. TWO CONFIGURATIONS OF A QCA CELL, REPRESENTING A BINARY 0 (LEFT) AND 1 (RIGHT)

Taking the principle further, groups of cells in arrays and other configurations can be used to perform the basic logic functions of AND, OR and NOT. And crucially, logic elements can be interconnected using the current-less QCA wires. Recent work at Indiana's Notre Dame University has demonstrated that this really does work.

What makes QCA so exciting is that it operates on an incredibly tiny scale, allowing vast numbers of logic elements to be crammed into chips. Because only miniscule power is needed to prod a cell into an initial 0/1 state, after which the domino effect performs the computation with almost no power dissipation, QCA chips will run cool.

A QCA-based notebook PC MIGHT RUN FOREVER on a single tiny battery, although lugging around enough liquid helium to keep it cool might be awkward

For now, QCA exists only in research laboratories. There are many unsolved practical problems, not least of which is the slightly annoying constraint that current systems only work at temperatures just above absolute zero. A QCA-based notebook PC might run forever on a single tiny battery, although lugging around enough liquid helium to keep it cold enough might prove awkward. But researchers are optimistic that room-temperature QCA will eventually be possible, and then we'll have some seriously cool hardware. And by 2020, we might even have some seriously cool software.

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